24-port 10/100M + 2-port Gigabit Smart Switch Controller

Features

- Provides 24 SS-SMII, 2 RGMII, 2 1000Base-X SERDES and one MII
- Built-in 2.75Mb RAM
- Support packet length up to 1536 Bytes
- Store & forward, share memory, non-blocking architecture
- Supports flow control
  - 802.3x in full duplex
  - Collision/carrier_sense based backpressure in half duplex
- Provides up to 4K MAC address entries
  - CRC/ direct hashing algorithm
  - Programmable aging timer (55s~15.7hr) error < 4 %
  - Configurable MAC address table
  - Optional MAC address learning
- Supports porting mirroring function (Tx, Rx, Tx&Rx)
- Supports IGMP snooping function
  - Version 1 and Version 2
- Supports flexible 3 trunking groups
  - (Port 0 ~ port 3, port 4~ port 7, Gigabit port 1 ~ port 2)
  - Load balance based on (physiccal port, Destinationn MAC Address, Source MAC Address, Destination MAC Address/Source MAC Address)
- Link failure recovery
- Supports VLAN
  - Port based VLAN
  - Tag based VLAN
  - Add/ remove/ modify tag based on VID or physical port
- Support Class of Service
  - Port based CoS
  - 802.1Q priority tag based
  - IP TOS/DSCP based (IPv4/IPv6)
  - TCP/UDP port based
  - 2 level of priority per port
  - WRR/ First-Come-First-serve/ Srict priority
- Broadcast storm control support
  - Broadcast rate control per port
  - Block broadcast packet that does not belong to ARP or IP packet forwarded to CPU port
- Supports port security
  - MAC address based
  - IP address based
  - TCP/UDP port based
- Supports Bandwidth control with/without flow control
  - 480 configurable levels for p0~p23 and MII port (from 32kbps to 63.75 Mbps)
  - 508 configurable levels for RGMII port (from 32kbps to 510 Mbps)
- Supports 5 port state for Spanning Tree protocol
  - Blocking/ listening/ learning/ forwarding/ disabled
  - Forward BPDU to CPU port
- Captures the specific packet and forward it to CPU port
  - BPDU, LACP, 802.1x, GMRP, GVRP, ARP
    ICMP, IGMP, TCP, UDP, OSPF
  - Packets with specific TCP/UDP port number
- PHY address setting for CPU, Giga 1 and Giga2 port
- Operating mode configuration
  - Pin initial setting
  - 2 wire serial interface for EEPROM
  - 2 wire serial interface for register setting
- Status counters for each port
  - RX/TX packet count
  - CRC error packet count
  - Dropped packet count
  - Collision count
- Programmable serial driving LED functions
- Only one 25MHz crystal is needed
- Optional 25Mhz, 50Mhz clock output
- Adjustable IO voltage (3.3/2.5v MII, 3.3/1.8v SS-SMII, 2.7V~1.9V RGMII)
- Built-in 2.5v and 1.9 regulator
- 144 pin EPAD. Lead-free package

General Description

The IP1826D is a non-blocking, store-and-forward architecture switch controller, which supports 24-port SS-SMII, 2-port RGMII/ SERDES, and one-port MII for a 24+2G smart switch application. With two built-in SERDES transceiver, the IP1826D provides a very cost-effective solution for a 24+2 Gigabit fiber without external Gigabit Ethernet transceivers.
Note: In the following paragraphs, 24-port SS-SMII is referred to as port 0 ~ port 23, 2-port RGMII as port 24 (or Giga 1)and port 25 (or Giga 2) and MII port as port 26. These ports are named as P0 ~ P26 in abbreviation. The PHY address for P0 ~ P23 are “8~31” respectively. The PHY addresses “1” and “2” correspond to P24 and P25 respectively.

The IP1826D embeds a 2.75Mb SSRAM for the use of packet buffer and 4K MAC address table. It provides a 2-wire CPU interface, which allows the designer to access to the register. The system configuration can be downloaded from EEPROM upon reset. The serial LED informations is provided through a 2-wire LED interface, simplifing the PCB layout task for LED display. With the external logic devices, the IP1826D can show the status of link, speed, duplex and activity.

In addition to the fundamental function such as the flow control, the broadcast storm control and the programmable MAC address aging time, the IP1826D also supports many advanced features which allow the designer to implement the smart switch features. The IGMP (Internet Group Management Protocol) snooping provides a method to build a multicast link without complicated CPU code. The designer can also use the 2 levels of priority queue to support the real-time streaming application. Supporting both port_based and tag_based VLAN, the IP1826D can partition the network traffic by programming the VLAN table. Furthermore the IP1826D supports both non-VID related tag based VLAN and VID related tag based VLAN. The access control based on the MAC layer, the IP layer and TCP/UDP layer provides a method for the designer to implment the Class of Service and the network security.

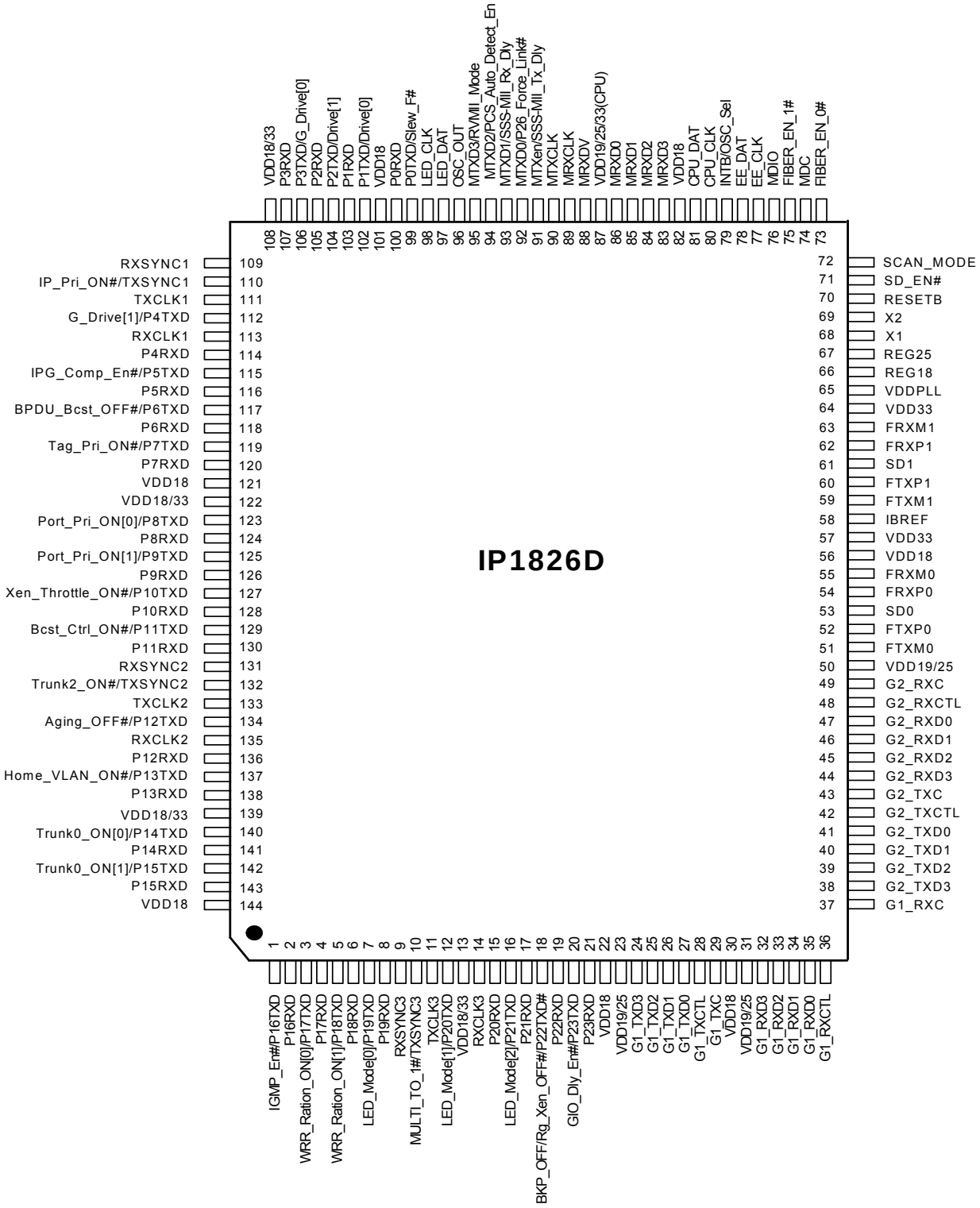
An 8051 CPU based web controller can easily support the web management. With the web management function, designers can remotely configure and monitor IP1826D smart switches through browsers, such as Microsoft Internet Explorer or Chrome and no program installation is required for the smart switch management.

Table of Contents

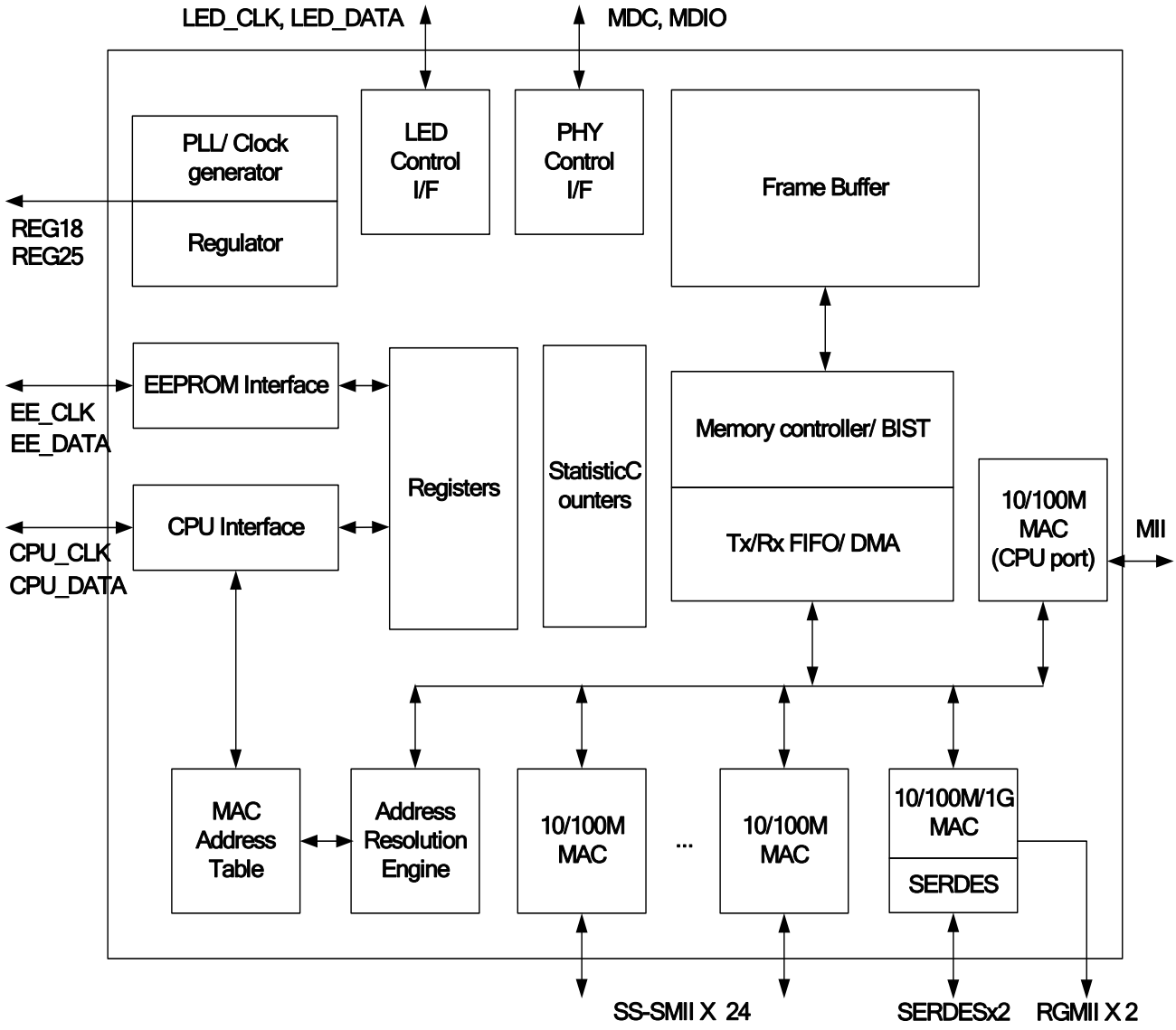
Revision History

Revision #	Change Description
IP1826D-DS-R01	Initial release.
IP1826D-DS-R02	1. Modify SS-SMII、MII & RGMII $V_{IL}$and V_{IH} threshold to DC characteristics 2. Modify register 0x40H description
IP1826D-DS-R03	Modify the default value of register：0xEC and 0xEF
IP1826D-DS-R03.1	Modify MDC signal description: connect a 300ohm bead (page 11)

1 Pin Diagram



2 Block Diagram



3 Pin description

Type	Description
P	Power or ground
I; O	I: Input pin; O:Output pin
IL	Input latched upon reset

Type	Description
PD	PD: Pulled down with internal resistor
PU	PU: Pulled up with internal resistor
I/O	Bi-direction Input/Output

Pin No.	Label	Type	Description
SS-SMII			
99 102,104 106,112 115,117 119,123 125,127 129,134 137,140 142,1 3, 5 7,12 16,18 20	P0TXD, P1TXD, P2TXD, P3TXD, P4TXD, P5TXD, P6TXD, P7TXD, P8TXD, P9TXD, P10TXD, P11TXD, P12TXD, P13TXD, P14TXD, P15TXD, P16TXD, P17TXD, P18TXD, P19TXD, P20TXD, P21TXD, P22TXD, P23TXD	O	SS-SMII transmits data output for port 0 to port 23.
110 132 10	TXSYNC1, TXSYNC2, TXSYNC3	O	SS-SMII synchronization output for transmit data
111 133 11	TXCLK1, TXCLK2, TXCLK3	O	SS-SMII transmit clock output

100 103,105 107,114 116,118 120,124 126,128 130,136 138,141 143,2 4,6 8,15 17,19 21	P0RXD, P1RXD, P2RXD, P3RXD, P4RXD, P5RXD, P6RXD, P7RXD, P8RXD, P9RXD, P10RXD, P11RXD, P12RXD, P13RXD, P14RXD, P15RXD, P16RXD, P17RXD, P18RXD, P19RXD, P20RXD, P21RXD, P22RXD, P23RXD	I	SS-SMII receive data input
109 131 9	RXSYNC1, RXSYNC2, RXSYNC3	I	SS-SMII receive synchronization input
113 135 14	RXCLK1, RXCLK2, RXCLK3	I	SS-SMII receive clock input

Pin description (continued)

Pin No.	Label	Type	Description
RGMII			
24,25 26,27 38,39 40,41	G1_TXD3, G1_TXD2, G1_TXD1, G1_TXD0, G2_TXD3, G2_TXD2, G2_TXD1, G2_TXD0	O	RGMII Transmit Data When it works in 10BASE-T or 100BASE-TX mode, TXD[3:0] present the transmit data at the rising edge of TXC, and when it works in 1000BASE-T mode, TXD[3:0] present the low nibble of transmit data byte at the rising edge of TXC, and present the high nibble of transmit data byte at the falling edge of TXC.
28 42	G1_TXCTL, G2_TXCTL	O	RGMII Transmit Control A GMII-like signal “TX_EN” is presented on the rising edge of TXC and a GMII-like signal “TX_ER” is derived by logical operation of the value of TXCTL at the falling edge of TXC, with the latched value of TX_EN, per RGMII specification.
29 43	G1_TXC, G2_TXC	O	RGMII Transmit Clock It is a 125Mhz clock in 1000BASE-T mode, 25 MHz clock in 100BASE-TX mode, or a 2.5 MHz clock in 10BASE-T mode. IP1001 uses the clock to sample TX_CTL and TXD[3:0].
32,33 34,35 44,45 46,47	G1_RXD3, G1_RXD2, G1_RXD1, G1_RXD0, G2_RXD3, G2_RXD2, G2_RXD1, G2_RXD0	I	RGMII Receive Data When the PHY works in 10BASE-T or 100BASE-TX mode, RXD[3:0] latch the receive data at the rising edge of RXC, and when it works in 1000BASE-T mode, RXD[3:0] latch the low nibble of receive data byte at the rising edge of RXC, and present the high nibble of transmit data byte at the falling edge of RXC.
36 48	G1_RXCTL, G2_RXCTL	I	RGMII Receive Control A GMII-like signal “RXCTL” is presented on the rising edge of RXC and a GMII-like signal “RX_ER” is derived by logical operation of the value of RXCTL at the falling edge of RXC, with the latched value of RX_DV, per RGMII specification.
37 49	G1_RXC, G2_RXC	I	RGMII Receive Clock. It is a 125 MHz, 25MHz, or 2.5MHz reference clock from a Gigabit PHY working in 1000BASE-T, 100BASE-TX, or 10BASE-T.

Pin description (continued)

Pin No.	Label	Type	Description
MII/Reverse MII. MII mode: this port acts as a MAC. Reverse MII port: this port acts a PHY.			
91	MTXEN/MRXDV	O	MII mode(MAC mode): transmit enable Rsverse MII mode(PHY mode): receive data valid.
95,94,93,92	MTXD[3:0]/MRXD[3:0]	O	MII mode(MAC mode): transmit data Rsverse MII mode(PHY mode): receive data.
88	MRXDV/MTXEN	I	MII mode(MAC mode): receive data valid Rsverse MII mode(PHY mode): transmit enable.
83,84,85,86	MRXD[3:0]/MTXD[3:0]	I	MII mode(MAC mode): receive data Rsverse MII mode(PHY mode): transmit data
90	MTXCLK	I/O	MII transmit clock. Input for normal (MAC mode) MII. Output for reverse (PHY mode) MII
89	MRXCLK	I/O	MII receive clock. Input for normal (MAC mode) MII. Output for reverse (PHY mode) MII.
SMI			
74	MDC	O	Clock for serial management bus. It's recommended to connect a 300ohm bead close to the IP1826D and add a 30pf capacitor to ground for noise filtering.
76	MDIO	I/O	I/O data for serial management bus. It's recommended to add a 1.5K pull up resistor connecting to VDD and a 30pf capacitor connecting to ground.
EEPROM			
77	EE_CLK	O, PU	Serial EEPROM clock output
78	EE_DATA	I/O,PU	Serial EEPROM data

Pin description (continued)

Pin No.	Label	Type	Description
CPU			
80	CPU_CLK	I, PU	Serial CPU access clock input.
81	CPU_DAT	I/O, PU	Serial CPU data
LED			
98	LED_CLK	PU	This pin drives periodical pulse to the serial to parallel latch for the LED display.
97	LED_DAT	PU	This pin drives data pattern to the serial to parallel latch for the LED display.
Miscellaneous			
68	X1	I	Crystal/ Oscillator 25MHz input. The frequency tolerance is + - 50PPM.
69	X2	O	Crystal output.
70	RESETB	I	System reset (low active). Should be kept at “low” for at least 10 microseconds.
79	INTB	O, PU	Interrupt output. Active low. Please refer to register F7h and F8h for more detailed information.
66	REG19	O	1.9V regulator control. This pin can be connected to the base of the PNP transistor to generate the 1.9V power.
67	REG25	O	2.5V regulator control. This pin can be connected to the base of the PNP transistor to generate the 2.5V power.
72	SCAN_MODE	I, PD	Leave this pin unconnected during normal operation.
96	OSC_OUT	O	A 25Mhz/ 50 Mhz clock output
Power & Ground			
22,30, 56,82,101, 121,144	VDD19	P	1.9V power for Core circuit
65	VDDPLL	P	1.9V power for PLL circuit
13,108,122,139	VDD19/33	P	3.3/1.9V power for I/O PAD of SS-SMII port
23,31,50	VDD19/25	P	2.5/1.9V power for I/O PAD of RGMII port
87	VDD19/25/33 (CPU)	P	3.3/2.5/1.9V power for I/O PAD of MII port It is recommended to use 2.5 or 1.9V if other VDD power is 1.9V.
57,64	VDD33	P	3.3V power for analog circuit
--	GND		Exposed PAD (E-PAD (Thermal PAD) is Analog and Digital ground.

Pin description (continued)

Pin No.	Label	Type	Description
Power On setting. These pins' state will be latched upon reset			
129	BCST_CTRL_ON#	IL, PU	Enable the broadcast storm control 1: Disable (Default); 0: Enable The setting can be updated by writing register 42h~43h.
134	AGING_OFF#	IL, PU	Disable the MAC address table aging function 1: Enable aging (Default); 0: Disable aging The setting can be updated with register 40h[1].
142 140	TRUNK0_ON[1], TRUNK0_ON[0]	IL, PU	The trunk group 0 setting: Trunk0_ON[1:0] 00: port 0, 1, 2, 3 trunk-grouped 01: port 0, 1, 2 trunk-grouped 10: port 0, 1, trunk-grouped 11: no trunk (Default) The setting can be updated with register 4Ch.
132	TRUNK2_ON#	IL, PU	The trunk group 2 setting: 1: no trunk (Default); 0: port 24 and port 25 trunk-grouped The setting can be updated with register 4Eh.
137	HOME_VLAN_ON#	IL, PU	Home VLAN setting enable Port 0 ~ Port23 are all individual VLAN shared with 2 RGMII and MII ports. For example, Port 0, port 24 ~ port 26 form a VLAN group, etc. 1: Disabled (Default); 0: Enabled The setting can be updated with register 80h~B5h.
1	IGMP_EN#	IL, PU	IGMP snooping. 1: Disable (Default); 0: Enable The setting can be updated with register C0h[1].
117	BPDU_BCST_OFF#	IL, PU	Filter the packet with MAC destination address 01-80-c2-00-00-04 ~01-80-c2-00-00-0F 1: Broadcast (Default); 0: Filter This pin is valid only if pin 20 GIO_DLY_EN# is set to 1.
20	GIO_DLY_EN#	IL, PU	RGMII I/O delay pin setting enable 1: Disable (default); 0: Enable This pin is used to select the modes of pin 3, 127, 18, 119, 117 and 110.
10	MULTI_TO_1 #	IL, PU	When set to "0", the switch controller will adjust the queue management to fit the multi-clients to one server application. 1: Disable (default); 0: Enable
94	PCS_AUTO_DETECT_EN	IL, PD	Port 25 and 26 TP/ fiber auto switching 1: Enable; 0: Disable (Default) When the function is turned on, IP1826D enables SERDES or RGMII of port 25(26) depending on the link status of SERDES. If the SERDES link status of port 25(26) is off, IP1826D recognizes port 25(26) as a TP port; otherwise IP1826D recognizes port 25(26) as a fiber port. The details are illustrated in the following table. The setting can be updated with register FFh[7].

16, 12, 7	LED_Mode[2] LED_Mode[1] LED_Mode[0]	IL, PU	Please refer to LED Display Mode.
95	RVMII_MODE	IL, PD	Reverse MII mode 1: Reverse MII (IP1826D works as a PHY) 0: Normal MII (IP1826D works as a MAC)
18	RG_XEN_OFF# /BKP_OFF#	IL, PU	Disable the flow control/back pressure of all ports 1: Turn on (Default); 0: Turn off This pin is valid only if pin 20 GIO_DLY_EN# is set to 1. Can be updated with register D9h[13].
3, 127	TXC_DELAY[1] TXC_DELAY[0]	IL, PU	RGMII TXC output delay added 00: delay 3ns; 01: delay 2ns; 10: delay 1ns; 11: no delay These pins are valid only if pin 20 GIO_DLY_EN# is set to 0. Can be updated with register F9.
18	TXC_REV	IL, PU	Reverse TXC 0: reverse; 1: normal This pin is valid only if pin 20 GIO_DLY_EN# is set to 0. Can be updated by setting register F9.
119, 117	RXC_DELAY[1] RXC_DELAY[0]	IL, PU	RGMII RXC input delay added 00: delay 3ns; 01: delay 2ns; 10: delay 1ns; 11: no delay These pins are valid only if pin 20 GIO_DLY_EN# is set to 0. Can be updated by setting register F9.
110	RXC_REV	IL, PU	Reverse RXC 0: reverse; 1: normal This pin is valid only if pin 20 GIO_DLY_EN# is set to 0. Can be updated by setting register F9.
91	SS-SMII_Tx_Dl y	IL, PD	SS-SMII Tx delay 4ns 1:Enable; 0:Disable (Default)
127	XEN_THROTTL E_ON#	IL, PU	Auto turn off the flow control, when the flow control and the priority is enabled. 1: Disable auto turn off function (Default) 0: Enable auto turn off function This pin is valid only if pin 20 GIO_DLY_EN# is set to 1.
73	FIBER_EN_0#	IL, PU	Port 24 RGMII/SERDES selection (force mode) 1: RGMII (Default); 0: SERDES When PCS_AUTO_DETECT_EN is disabled, this pin is used to configure port 24 to be TP or fiber manually. It must be left open to disable force mode, if PCS_AUTO_DETECT_EN is enabled. The setting can be updated with register FFh[5].
75	FIBER_EN_1#	IL, PU	Port 25 RGMII/SERDES selection (force mode) 1: RGMII (Default); 0: SERDES When PCS_AUTO_DETECT_EN is disabled, this pin is used to configure port 25 to be TP or fiber manually. It must be left open to disable force mode, if PCS_AUTO_DETECT_EN is enabled. The setting can be updated with register FFh[6].
71	SD_EN#	IL, PU	SD detect mode of port 24 (SD1) and 25 (SD2) 1: Low active (GBIC/ Default); 0: high active The setting can be updated with register FFh[8].

92	P26_FORCE_LINK#	IL, PD	Port 26 (MII) forced link on 1: Enable; 0: Disable (Default) The setting can be updated with register D9h[13].
115	IPG_COMP_EN#	IL, PU	Transmit IPG compensation (+80ppm). 1: Disable (Default); 0: Enable The setting can be updated with register 01h[0].
125 123	PORT_PRI_ON[1], PORT_PRI_ON[0]	IL, PU	Enable port base high priority function 11: Disabled (default) 10: Set port 0~3 as high priority port 01: Set port 24, 25 (RGMII port) as high priority port 00: Set port 26 (CPU port) as high priority port The setting can be updated with register 22h~23h.
119	TAG_PRI_ON#	IL, PU	Enable 802.1Q TAG priority function of all ports 1: Disable (Default); 0: Enable This pin is valid only if pin 20 GIO_DLY_EN# is set to 1. The setting can be updated with register 24h~25h.
110	IP_PRI_ON#	IL, PU	Enable IP TOS/DS priority function of all ports 1: Disable (Default); 0: Enable This pin is valid only if pin 20 GIO_DLY_EN# is set to 1. The setting can be updated with register 26h~27h.
5 3	WRR_RATIO_ON[1], WRR_RATIO_ON[0]	IL, PU	The high priority to low priority ratio of the packet number for the weighted round robin mode. 11: First in first out (Default) 10: 2 to1; 01: 4 to 1; 00: 8 to 1 These pins are valid only if pin 20 GIO_DLY_EN# is set to 1. The setting can be updated with register 3Dh.
104 102	DRIVE[1], DRIVE[0]	IL, PU	Driving current selection for 3SMII and MII, port 0~23 and port 26 00: 2 mA; 01: 12 mA; 10: 8 mA; 11: 4 mA (Default) The setting can be updated with register FAh[9:8].
112 106	G_DRIVE[1], G_DRIVE[0]	IL, PU	Driving current selection for RGMII, port 24~25 00: 4 mA; 01: 2 mA; 10: 12 mA; 11: 8 mA (Default) The setting can be updated with register F9h[13:12].
99	SLEW_F#	IL, PU	Output pad slew rate setting for RGMII, SS-SMII and MII. 1: Normal (Default); 0: Fast The setting can be updated with register FAh[14].
93	SS-SMII_Rx_Dly	IL, PD	SS-SMII Rx delay 4ns 1:Enable; 0:Disable (Default)
79	OSC_SEL	IL, PU	OSC Clock selection of pin OSC_OUT. 1:25MHz; 0:50MHz

Gigabit Port COMBO Configuration

Note: X means "don't care" **Fiber port**	**SDx voltage**	**PCS_AUTO_ DETECT_EN**	**FIBER_EN_x#**	**SD_EN#**	**Active I/F**	**TP/FX Auto Change**
Link on	0v	1	NC	1	SERDES (Min GBIC/ GBIC)	Yes
Link off	3.3v	1	NC	1	RGMII (TP is active if fiber port is link off.)	Yes
Link on	3.3v	1	NC	0	SERDES 1X9 or 2x5(SFF)	Yes
Link off	0v	1	NC	0	RGMII (TP is active if fiber port is link off.)	Yes
Link on	0v	0	0	1	SERDES (Min GBIC/ GBIC)	No
Link off	3.3v	0	0	1		No
Link on	3.3v	0	0	0	SERDES 1X9 or 2x5(SFF)	No
Link off	0v	0	0	0		No
X	X	0	1	X	RGMII	No

Pin description (continued)

Pin No.	Label	Type	Description
Gigabit SerDes port			
51	FTXM0	O	SERDES TXM. There is an internal 100 ohms resistor between FTXM0 and FTXP0.
52	FTXP0	O	SERDES TXP
53	SD0	I	Signal detect The input threshold voltage is around 1.6v. It is recommended to use a fiber MAU, which supports TTL level SD signal.
54	FRXP0	I	SERDES RXP. There is an internal 100 ohms resistor between FRXM0 and FRXP0.
55	FRXM0	I	SERDES RXM
58	IBREF		This pin must be connected to analog ground through a 6.19k resister.
59	FTXM1	O	SERDES TXM. There is an internal 100 ohms resistor between FTXM1 and FTXP1.
60	FTXP1	O	SERDES TXP
61	SD1	I	Signal detect The input threshold voltage is around 1.6v. It is recommended to use a fiber MAU, which supports TTL level SD signal.
62	FRXP1	I	SERDES RXP. There is an internal 100 ohms resistor between FRXM1 and FRXP1.
63	FRXM1	I	SERDES RXM

Note:

1. All the trapped pins are latched upon reset and are pulled down or pulled up by a 50K resistor inside the chip.
2. The designer can connect a 4.7K ohms resistor to set these pins to “1” or “0” to change the default state.
3. The content of an EEPROM will override the pin setting.

4 Functional Description

4.1 Switch Engine and Queue Management

4.1.1 Packet forwarding

IP1826D utilizes the “store & forward” method to handle packet transfer. IP1826D begins to forward a packet to a destination port after the entire packet is received. A received packet will be forwarded to the destination port only if it is error free; otherwise, it will be discarded.

4.1.1.1 Address learning and hashing

Related registers	40[1:0], 44h~46h

IP1826D can handle up to 4096 MAC address entries. And it provides two kinds of hash method to maintain the MAC address table; one is the direct mapping and the other is the CRC algorithm. When the direct mapping method is selected, register 40h[0] set to “1”, IP1826D recognizes the least significant 12 bits of the MAC address. When the CRC algorithm is used, register 40h[0] set to “0”, IP1826D uses 48-bit MAC address to hash.

The address learning function for each port can be either enabled or disabled by setting the corresponding bit in registers 45h and 46h.

Packets with the following conditions will not be stored in MAC address table.

- Erroneous packet
- 802.3x pause packet
- 802.1D Reserved Group packet
- Multicast source MAC address

4.1.1.2 Aging

Address aging

Related registers	40h[1], 44h[9:0]

IP1826D supports programmable aging time to meet various system requirement, ranging from 55.3 sec to 56627sec ±3.8%. The designer can program aging time by writing register 44h[9:0]. The address aging function can be disabled by programming register 40h[1].

Packet aging

Related registers	3Dh[15], 3Dh[13:8]

IP1826D supports packet aging (out queue aging). If a packet stays in IP1826D longer than out queue aging time defined in register 3Dh[13:8], IP1826D will drop the packet to improve the efficiency of packet buffer. The packet aging function can be enabled by programming register 3Dh[15].

4.1.1.3 802.1D packet forwarding

Related registers	01h[1], 02h[1]

Besides the erroneous packet and the IEEE802.3x pause packet, 802.1D Reserved Group packet with MAC address from 01-80-c2-00-00-04 to 01-80-c2-00-00-0F can be optionally dropped by setting register 01h[1]. A packet with MAC address equal 01-80-c2-00-00-00 can be forwarded to CPU or be dropped according to the setting in register 02h[1]. A packet with MAC address equal 01-80-c2-00-00-03 can be forwarded to CPU or be dropped according to the setting in register 02h[2].

4.1.1.4 Inter frame gap compensation

Related registers	01h[0]

IP1826D supports an option to transmit a packet with IPG changed from 96 bits to 88 bits after a period of transmission to compensate the data accumulation due to TX clock frequency difference between local machine and link partner. This function can be turned on by writing “1” to register 01h[0].

4.1.2 Flow Control

IP1826D supports two kinds of flow control mechanisms, backpressure for half duplex operation and IEEE 802.3x for full duplex operation.

4.1.2.1 IEEE802.3x

Related registers	D2h~D3h, D4h~D5h

When operating in full duplex mode, IP1826D supports IEEE802.3x flow control, both symmetric pause and asymmetric pasue function. Each port’s flow control function can be enabled individually by programming register D2h~D5h. When the packets in buffer reach the threshold, IP1826D generates a “Xoff” pause packet immediately or right after the current packet has been transmitted. When receiving a pause packet, the link partner stops transmission for a period of time defined in the pause packet. This prevents the buffer of IP1826D from overrun. When the packets in buffer lower than threshold, IP1826D generates a “Xon” pause packet to notify the link partner the receive buffer is available.

4.1.2.2 Backpressure

Related registers	D6h~D7h, 01h[2], 01h[3]

When operating in half duplex mode, the IP1826D supports backpressure flow control. Each port’s backpressure function can be enabled individually by programming register D6h~D7h. When the packets in buffer reach the threshold, IP1826D generates a jam pattern to back off the link partner. IP1826D supports the collision based and carrier-based backpressure. When the collision based backpressure is enabled, register 01h[2] set to “0”, IP1826D generates a jam pattern only when the link partner is transmitting data and the receive buffer in IP1826D is not available. When detecting a collision on line, the link partner stops transmission until a back off time expires. When the carrier based backpressure is enabled, register 01h[2] set to “1”, IP1826D transmits null packets continuously to prevent link partner’s transmission when the buffer is not available.

To prevent the packet loss due to excessive collision caused by backpressure mechanism, designer can clear bit 3 of register 01h to disable the drop function due to 16 consecutive collisions defined in IEEE802.3.

4.1.2.3 Flow control off for high priority packet

Related registers	01h[6]

To prevent the flow control function from blocking the high priority traffic, each port of IP1826D can turn off flow control function for a period of time automatically when receiving a high priority packet. This function can be enabled by writing register 01h[6].

4.1.3 Bandwidth Control (Egress/Ingress rate control)

Related registers	03h~1Dh, 01h[5]

IP1826D implements a sophisticated data rate control mechanism, which is very useful for the bandwidth-limited network. By controlling both the ingress and the egress data rate, IP1826D provides a variety of bandwidth configurations. It limits the maximum byte counts, by which a port can send or receive in a period of time. If the transmit byte counts or receive byte counts of a port reaches a pre-defined threshold, it will stop transmitting or receiving data.

Each port's egress/ingress data rate can be programmed individually. The maximum rate of port0~port 23 are defined in register 03h~1Ah. The maximum rate of port 24, port 25 and port 26 are defined in register 1Bh~1Dh. The high byte of the registers defines the receive rate and low byte defines transmission rate. Register 01h[5] defines the high /low throttle value using in bandwidth control function. It is noted that once the rate is set, it is independent of the status of link speed and flow control. The detailed configuration is shown in the following table.

Maximum output rate (transmit rate)

	Port 0~23	Port 26	Port 24, 25
	Register 03h~1Ah	Register 1Dh	Register 1Bh~1Ch
Link speed	10/100 Mbps		10/100/1000 Mbps
01h[5]=0	Bit [7:0] * 4K Byte/s		Bit [7:0] * 4K Byte/s.
01h[5]=1	Bit [7:0] * 32K Byte/s		Bit [7:0] * 256K Byte/s

Maximum input rate (receive rate)

	Port 0~23	Port 26	Port 24, 25
	Register 03h~1Ah	Register 1Dh	Register 1Bh~1Ch
Link speed	10/100 Mbps		10/100/1000 Mbps
01h[5]=0	Bit [15:8] * 4K Byte/s		Bit [15:8] * 4K Byte/s
01h[5]=1	Bit [15:8] * 32K Byte/s		Bit [15:8] * 256K Byte/s

Note: The 0x00 rate value denotes the maximum speed.

4.1.4 Broadcast Storm Control

Related registers	42h~43h, 44h[15:10]

To prevent the broadcast storm, the IP1826D implement a broadcast storm control mechanism. When this function is enabled, a port begins to drop the incoming broadcast packets if the received broadcast packet

counts reach the threshold defined in register 44h[15:10]. Each port's broadcast storm protection function can be enabled individually by programming register 42h~43h.

4.1.5 Block broadcast packet flooding to CPU port

Related registers	40h[4], F2h[0]

IP1826D supports an option to block broadcast packets flooding to CPU port. To enable the function, designer has to assign port 26 as a CPU port by programming register F2h[0], and then turn on the function by programming register 40h[4].

4.1.6 SS-SMII, RGMII and MII/Reverse MII

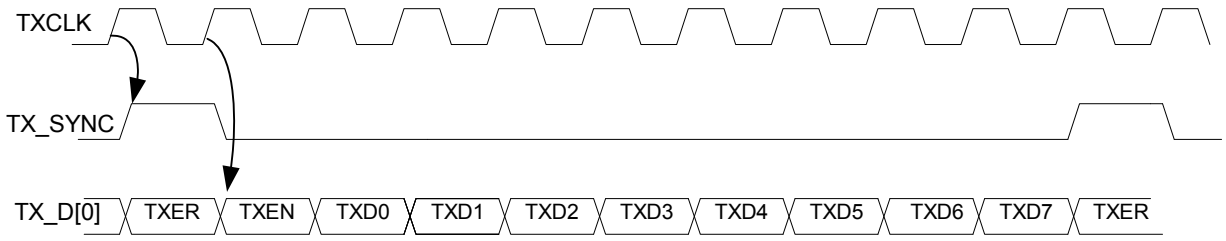
4.1.6.1 SS-SMII

Related registers	FAh

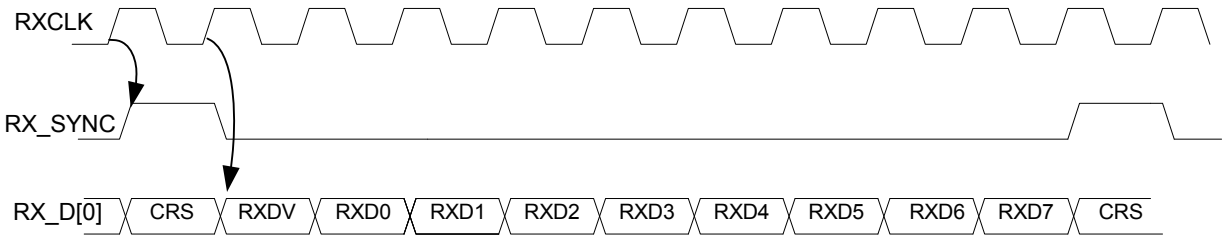
IP1826D sends out data on TX_D at the rising edge of TXCLK and uses TX_SYNC to indicate the start of a 10-bit frame. By recognizing the high pulse of the TX_SYNC, a PHY can capture the correct data stream. A PHY sends out data on RX_D at the rising edge of RXCLK and uses RX_SYNC to indicate the start of a 10-bit frame. By recognizing the high pulse of the RX_SYNC, IP1826D samples the correct data at the rising edge of RXCLK.

Accompanied by the high pulse of TX_SYNC, the TXEN, TX_ER and 8-bit TX data are present on the TX_D pin. For the RX part of SS-SMII, the CRS, RXDV, and 8-bit RX data are present on the RX_D pin.

To fit the timing requirement, the delay on TXCLK and RXCLK can be adjusted by programming register FAh. The driving current can be adjusted by pin DRIVR[1:0] and register FAh.

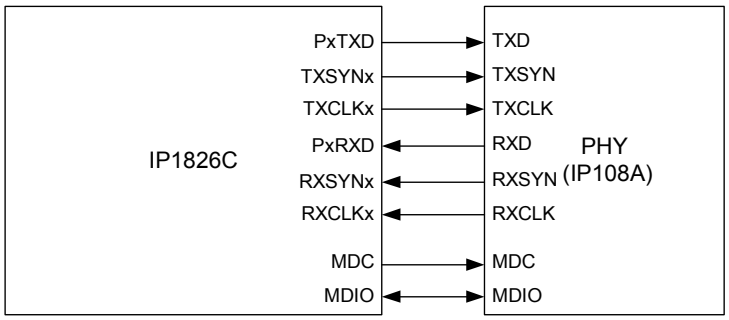


Transmit SS-SMII



Receive SS-SMII

SS-SMII



4.1.6.2 RGMII

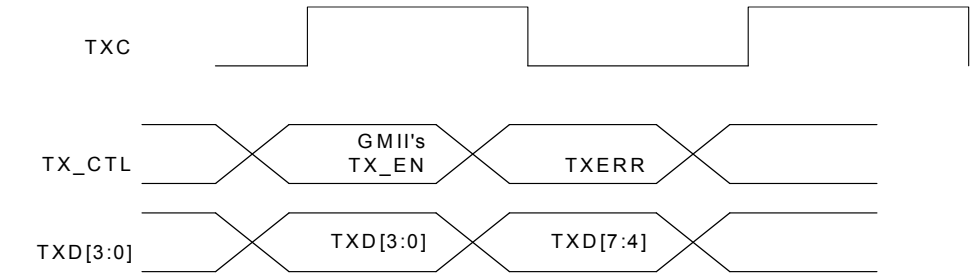
Related registers	F9h

IP1826D sends out data TXD[3:0] and control signal TX_CTL at the rising and falling edge of TXC. Two GMII like signals TX_EN and TXERR are embedded in the TX_CTL. GMII like information TXD[7:0] is embedded in the TXD[3:0]. By recognizing the decoded TX_EN, TXD[7:0] and TXERR, a PHY can capture the correct data stream.

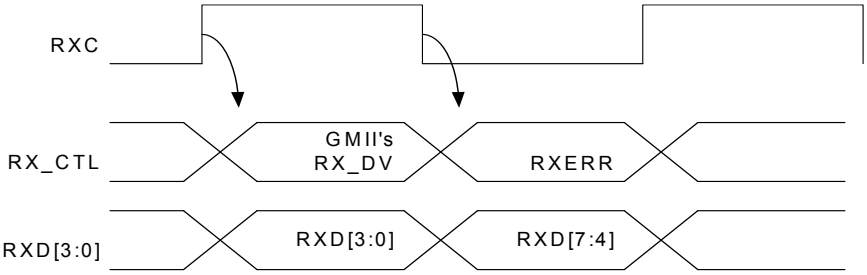
A PHY sends out data RXD[3:0] and control signal RX_CTL at the rising and falling edge of RXC. Two GMII like signals RX_DV and RXERR are embedded in the RX_CTL. GMII like information RXD[7:0] is embedded in the RXD[3:0]. By recognizing the decoded RX_DV, RXD[7:0] and RXERR, IP1826D can capture the correct data stream. IP1826D samples the correct data at the rising edge of RXCLK.

To fit the timing requirement, the delay on TXC and RXC can be adjusted by programming register F9h. The driving current can be adjusted by pin G_DRIVR[1:0] and register F9h.

RGMII

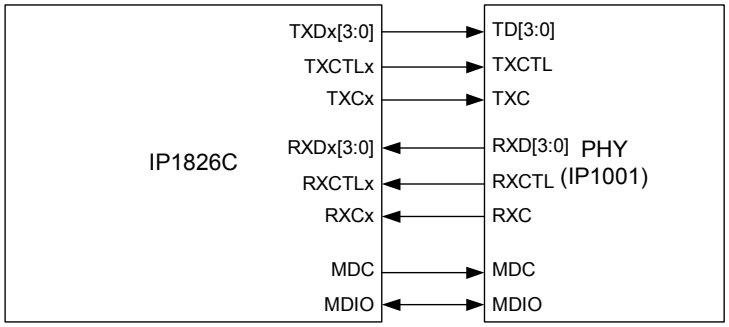


TXERR = GMII's TX_EN (XOR) GMII's TX_ER



RXERR = GMII's RX_DV (XOR) GMII's RX_ER

RGMII



4.1.6.3 MII/Reverse MII

Related registers	FAh[7:6]

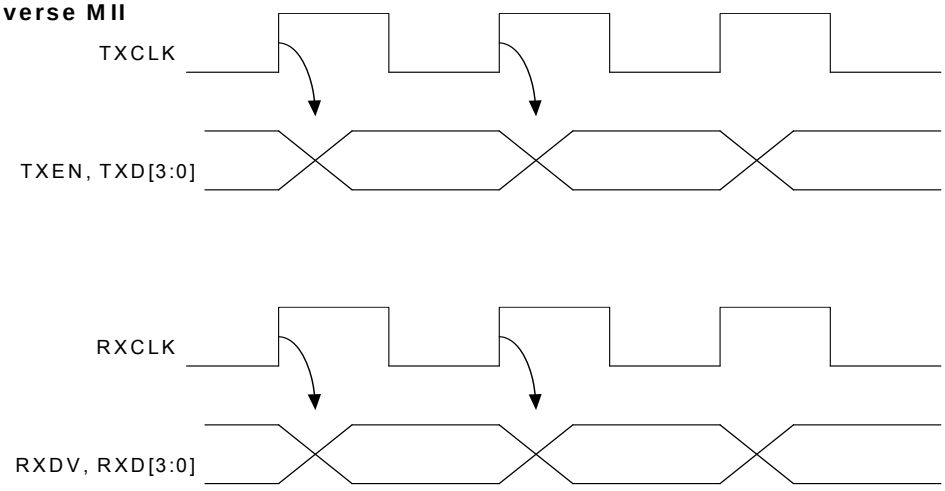
When set to reverse MII mode(PHY mode), IP1826D sends out data RXDV and RXD[3:0] at the rising and falling edge of RXCLK. By recognizing the RXDV and RXD[3:0], an external CPU can capture the correct data stream.

An external CPU sends out data through TXD[3:0] and control signal TXEN at the rising edge of TXCLK. By recognizing the TXEN, TXD[7:0], IP1826D can capture the correct data stream. IP1826D samples the correct data at the rising edge of TXCLK.

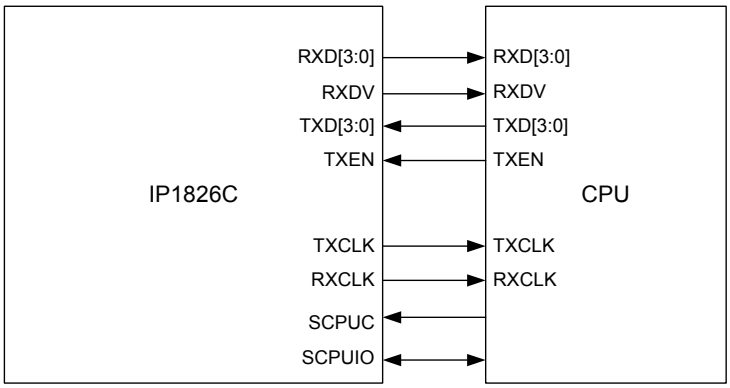
Both TXCLK and RXCLK are sent out by IP1826D. To fit the timing requirement, the delay on TXCLK and RXCLK can be adjusted by programming register FAh[6:7].

Note: If the designer set IP1826D to MII mode(MAC mode), the pin function will be swapped between Tx part and Rx part. Please refer to the pin description.

MII/Reverse MII



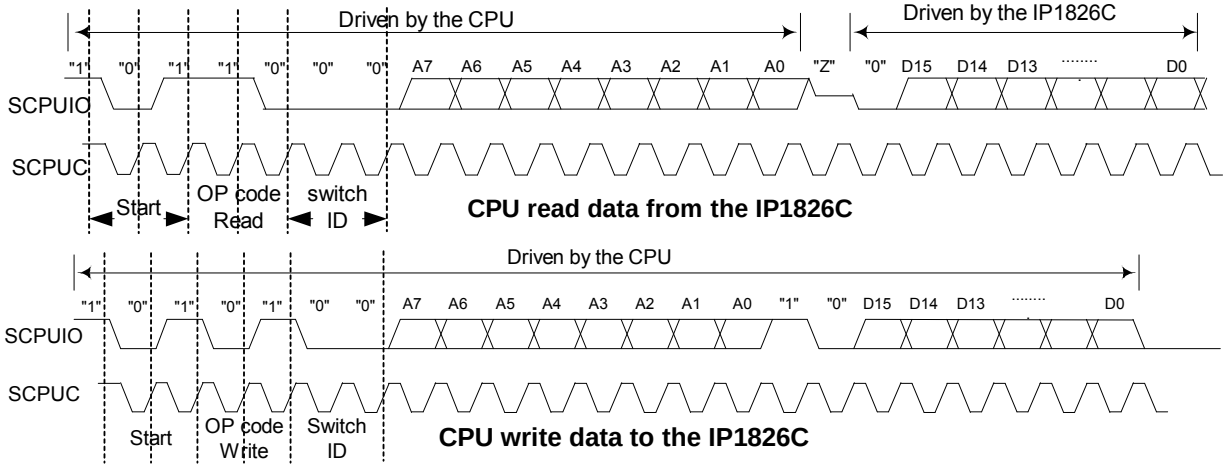
IP1826C acts as PHY



4.1.7 CPU interface

There is no need to program the register of the IP1826D for the generic application. However it's probably necessary to program the internal register to fit some special applications. The interface between the IP1826D and the CPU is a serial bus, which comprises a clock and an I/O signal. Like the access cycle of the serial management interface, the serial interface comprises the switch ID, the read/write command, the address and the data. The access cycle is depicted as below.

The access cycle is much like the access cycle of MDC, MDIO. Care should be taken that the switch ID is 2-bit wide rather than 5-bit wide.



4.1.8 Configure the port properties

Related registers	CBh~D7h, DEh~E7h

The designer can configure the property of each port through CPU Interface. The property of each port can be configured individually. The designer can set the auto-negotiation, speed, duplex, pause, and backpressure function by writing register CBh~D7h. Besides updating the property of IP1826D, it also updates the property of the corresponding PHY through SMI.

The designer can get the status of a port by reading register DEh~E7h. The registers provide the status of Asyn pause function, syn pause function, duplex, speed and link of each port.

4.1.9 Force link

Related registers	D9h

IP1826D supports force link function for port 24~ 26. Port 24~ 26 can be configured individually by programming D9h[13:11]. This function is useful when IP1826D is connected to a PHY, which doesn't support SMI. In this case, IP1826D can't get the link status and will not forward/receive a packet through this port. Force link function will keep this port active regardless of the link status.

4.1.10 Read / write address table (LUT)

Related registers	C5h~C8h

Designer can access IP1826D's MAC address table, ranging from 0 to 4095. To write an entry to the MAC address table, designer has to fill the 46-bit data to register C6h~C8h and then specify the address of the entry and issues a write command by programming register C5h. To read an entry from MAC address table, designer has to specify the address of the entry and issues a read command by programming register C5h. The entry can be read from register C6h~C8h. It is note that the bit 14 and 15 of register C8h is invalid, because of entry is 46-bit wide.

Because IP1826D builds and accesses the MAC address table with the address derived with hashing algorithm, designer has to calculate the address of an entry in the same way before accessing the table. That is, if direct hashing is selected, the address of an entry is the 12 LSB of a MAC address. If CRC hashing is selected, the address of an entry is the 12 LSB of CRC calculation result of a MAC address.

4.1.11 Read / write PHY registers

Related registers	DAh~DBh

The designer can access the register of a PHY connected to IP1826D through CPU I/F. To read a register of PHY, the designer has to specify the address of the PHY, address of the MII register, read command by programming register DAh. The content of the register can be read from register DBh. To write a register of PHY, designer has to specify the address of the PHY, address of the MII register, write command, and written data by programming register DAh~DBh.

The associated PHY addresses from port 0 to port 23 are 8~31. The PHY addresses of port 24, port 25 and port 26 are programmable and they are defined in register DCh (PHY address: 0~7).

4.1.12 Read / write EEPROM

Related registers	FBh~FCh

The designer can access the EEPROM through CPU I/F. To read one byte from EEPROM, the designer has to specify the byte address, device address, read command by programming register FBh. The data can be read from register FCh. To write one byte to EEPROM through CPU I/F, designer has to specify the byte address, device address, write command and written data by programming register FBh~FCh.

4.1.13 EEPROM interface

IP1826D supports EEPROM I/F to access 24C04/08/16. After detecting the rising edge of reset input, the IP1826D will start to read the content of EEPROM (acting like an EEPROM master). Being an EEPROM master, the IP1826D downloads the content of EEPROM only if the first two bytes in EEPROM are “1826h”.

The mapping relationship between the IP1826D registers and the EEPROM address are depicted as the following table.

EEPROM address	EEPROM content	IP1826D’s Register
00h	18h	XX
01h	26h	XX
02h	Expected value	01h[15:8]
03h	Expected value	01h[7:0]
04h	Expected value	02h[15:8]
05h	Expected value	02h[7:0]
•••••• ••••••	•••••• ••••••	•••••• ••••••
1FEh	Expected value	FFh[15:8]
1FFh	Expected value	FFh[7:0]

Note:

1. The EEPROM ID should be set to “3’b000”; i.e. A2=0; A1=0; A0=0
2. IP1826D downloads the content of the EEPROM ranging from address 00h to 1F1h; i.e. the register beyond this range is not recognized by IP1826D.
3. The ID for IP1826D recognition should be set at address 00h and address 01h as shown in the table.

4.1.14 Statistic counters

Related registers	01[10:9], 38h~3Ah, 3Bh~3Ch

IP1826D provides 54 statistic counters, two counters for one port. These counters are enabled if register 01h[10] is set to 1. The designer can select the function of counters to be RX packet count, TX packet count, collision count, or CRC error count by programming register 01h[9] and register 3Bh~3Ch. Each bit of register 3Bh~3Ch is corresponding to one port individually as shown in the following table.

	The function of counters of a port	
01h[9], one bit of 3Bh ~ 3Ch	Counter 2	Counter 1
0,0	Receive packet count	Transmit packet count
0,1	Transmit packet count	Collision count
1,0	Receive packet count	Drop packet count (MAC)
1,1	Receive packet count	CRC error packet count

To read the content of a counter, designer has to specify the address of counter in register 38h[5:0] and issue read command by setting register 38h[8]. Then, designer reads the content of the counter by reading register 39h and 3Ah. The address of counter of each port is shown in the following table.

Address of counter (38h[5:0])	Location of counter
0	Port 0 counter 1
1	Port 0 counter 2
2	Port 1 counter 1
3	Port 1 counter 2
……..	……..
……..	……..
46	Port 23 counter 1
47	Port 23 counter 2
48	Port 26 counter 1
49	Port 26 counter 2
50	Port 24 counter 1
51	Port 24 counter 2
52	Port 25 counter 1
53	Port 25 counter 2

4.1.15 Interrupt

Related registers	F7h~F8h

IP1826D provides one interrupt pin to indicate status change. When one of the following conditions happen, IP1826D will asserts the interrupt pins if the function is enabled.

1. A CPU R/W SMI command is completed
2. A CPU R/W EEPROM command is completed
3. Link status changes on PHY of any port
4. Auto-negotiation next page received on port 25 and 26 in fiber mode.
5. TP/fiber mode change on port 25 and 26.

An interrupt function can be enabled by programming the corresponding bit of register F7h, the interrupt mask register. The designer can read register F8h to identify the interrupt source. The polarity of interrupt pin can be configured by writing register F7h[15].

4.1.16 LED Display Mode

Related registers	DDh

The bit stream is output sequentially through LED_DAT and LED_CLK and its sequence starts from port 25 to port 0,. In the other word, Port 0 LED status is present on the latest LED bit, as shown in the table. To store the serial LED stream, a serial-to-parallel shift register should be used.

There are 2 dsiplay groups can be confgiured for LED display.

- **LED Dispaly Mode –Group 1**

If register DDh[9] is set to “0”, the slow blinking display mode will be present on those port running in half duplex mode or 10Mbps link speed. See the following tabled for the details.

Display Sequence

Register DDh[9]=0		
Pin Setting LED_Mode [2:0]	**Register Setting DDh[2:0]**	**LED Display Sequence. (1), (2) ..... indicate the bit stream sequence shifted from LED_DAT.**
111	000	(1) P25 Link/Act/Dupx; (2) P25 Speed, …….(Last one) P0 Speed.
110	001	(1) P25 Dupx/Col; (2) P25 Link/Act; (3) P25 Speed; ….(Last one) P0 Speed
101	010	(1) P25 Link/Act; (2) P25 Speed 1; (3) P25 Speed 0; ….(Last one) P0 Speed 0
100	011	Reserved.
011	100	(1) P25 Flow Ctrl; (2) P25 Link/Act/Dupx; (3) P25 Speed 1; (4) P25 Speed 0; ….. (Last one) P0 Speed 0
010	101	(1) P25 Dupx/Col; (2) P25 Link/Act; (3) P25 Speed1; (4) P25 Speed0; …..(Last one) P0 Speed0

001	110	(1) P25 Flow Ctrl; (2) P25 Dupx/Col; (3) P25 Link/Act; (4) P25 Speed; …..(Last one) P0 Speed
000	111	(1) P25 Tx; (2) P25 Rx; (3) P25 Link/Act; (4) Speed; …..(Last one)Speed; …..(Last one) P0 Speed

LED Display Behaviour: Register DDh[9]=0

LED mode selection. There are 4 LED display states, as shown below.
●: Light. ○: Inactive. ✳: Blinking slowly @ 4S cycle. ✱:Blinking fast @98 mS cycle.

LED_Mode: Pin Setting= 111 or DDh[2:0]=000. (2 LEDs)

LED Name	LED Function
Speed	(1)P0 ~P23. ●: Link at 100Mbps. ✳: Link at 10Mbps. (2)P24 ~P25. If register DDh[12]=0 ●: Link at Giga bps. ✳: Link at 100Mbps. ○: Link at 10Mbps. If regsiter DDh12]=1 ●: Link at Giga bps; ○: Link at 100Mbps/Link at 10Mbps.
Link/Act/Duplex	●: Link in full duplex mode and no activity ✱: Tx/Rx Activity ongoing. ✳: Link in half duplex mode and no activity ○: Link down

LED_Mode: Pin Setting= 110 or DDh[2:0]=001. (3 LEDs)

LED Name	LED Function
Speed	(1)P0 ~P23. ●: Link at 100Mbps. ✳: Link at 10Mbps. (2)P24 ~P25. ●: Link at Giga bps. ✳: Link at 100Mbps. ○: Link at 10Mbps.
Link/Act	●: Link and no activity ✱: Tx/Rx Activity ongoing.
Duplex/Col	●: Link in full duplex mode ○: Link in half duplex mode and no collision ✱: Collision

LED_Mode: Pin Setting= 101 or DDh[2:0]=010. (1 bicolor / 1 mono)

LED Name	LED Function
Speed[1:0]	(1)P0 ~P23. 10: Link at 100Mbps. 01: Link at 10Mbps; 11: no link. (2)P24 ~P25. 10: Link at Giga bps/100Mbps. 01: Link at 10Mbps; 11: no link.
Link/Act/Duplex	●: Link in full duplex mode and no activity ✱: Tx/Rx Activity ongoing. ✳: Link in half duplex mode and no activity ○: Link down

LED_Mode: : Pin Setting= 100 or DDh[2:0]=011.
Reserved

LED_Mode: **Pin Setting= 011 or DDh[2:0]=100.** (1 bicolor / 2 mono)

LED Name	LED Function
Speed[1:0]	(1)P0 ~P23. 10: Link at 100Mbps. 01: Link at 10Mbps; 11: no link. (2)P24 ~P25. 10: Link at Giga bps. 01: Link at 100Mbps; 11: Link at 10Mbps or no link.
Link/Act/Duplex	●: Link in full duplex mode and no activity ✱: Tx/Rx Activity ongoing. ✳: Link in half duplex mode and no activity ○: Link down
Flow control	✱: Receive pause frame ○: No pause frame

LED_Mode: Pin Setting= 010 or DDh[2:0]=101. (1 bicolor / 2 mono)

LED Name	LED Function
Speed[1:0]	(1)P0 ~P23. 10: Link at 100Mbps. 01: Link at 10Mbps; 11: no link. (2)P24 ~P25. 10: Link at Giga bps. 01: Link at 100Mbps; 11: Link at 10Mbps or no link.
Link/Act	●: Link and no activity ✱: Tx/Rx Activity ongoing.
Duplex/Collision	●: Link in full duplex mode ○: Link in half duplex mode and no collision ✱: Collision

LED_Mode: **Pin Setting= 001 or DDh[2:0]=110.** (4 LEDs)

LED Name	LED Function
Speed	(1)P0 ~P23. ●: Link at 100Mbps. ✳: Link at 10Mbps. (2)P24 ~P25. ●: Link at Giga bps. ✳: Link at 100Mbps. ○: Link at 10Mbps.
Link/Act	●: Link and no activity ✱: Tx/Rx Activity ongoing.
Duplex/Col	●: Link in full duplex mode ○: Link in half duplex mode and no collision ✱: Collision
Flow control	✱: Receive pause frame ○: No pause frame

LED_Mode: **Pin Setting= 000 or DDh[2:0]=111.** (4 LEDs)

LED Name	LED Function
Speed	(1)P0 ~P23. ●: Link at 100Mbps. ✳: Link at 10Mbps. (2)P24 ~P25. ●: Link at Giga bps. ✳: Link at 100Mbps. ○: Link at 10Mbps.
Link/Act	●: Link and no activity ✱: Tx/Rx Activity ongoing.
Tx	✱: Tx ongoing
Rx	✱: Rx ongoing

- **LED Dispaly Mode –Group 2**

If register DDh[9] is set to "1", only the fast blinking display mode will be present on those port.

Register DDh[9]=1		
Pin Setting LED_Mode [2:0]	**Register Setting DDh[2:0]**	**LED Display Sequence. (1), (2) ..... indicate the bit stream sequence shifted from LED_DAT.**
111	000	(1) P25 Speed, (2) P25 Link/Act; …….(Last one) P0 Link/Act.
110	001	(1) P25 Dupx/Col; (2) P25 Link/Act; (3) P25 Speed; ….(Last one) P0 Speed
101	010	(1) P25 Dupx/Col; (2) P25 Link/Act/Speed0;; (3) P25 Link/Act/Speed1; ….(Last one) P0 Link/Act/Speed1;

LED Display Behaviour : Register DDh[9]=1

LED mode selection. There are 3 LED display states, as shown below.
●: Light. ○: Inactive. ✱:Blinking fast @98 mS cycle.

LED_Mode: Pin Setting= 111 or DDh[2:0]=000.

LED Name	LED Function
Speed	(1)P0 ~P23. ●: Link at 100Mbps. ○: Link at 10Mbps. (2)P24 ~P25. ●: Link at Giga bps/100Mbps. ○: Link at 10Mbps.
Link/Act	●: Link in full duplex mode and no activity ✱: Activity ongoing. ○: Link down

LED_Mode: Pin Setting= 110 or DDh[2:0]=001. (3 LEDs)

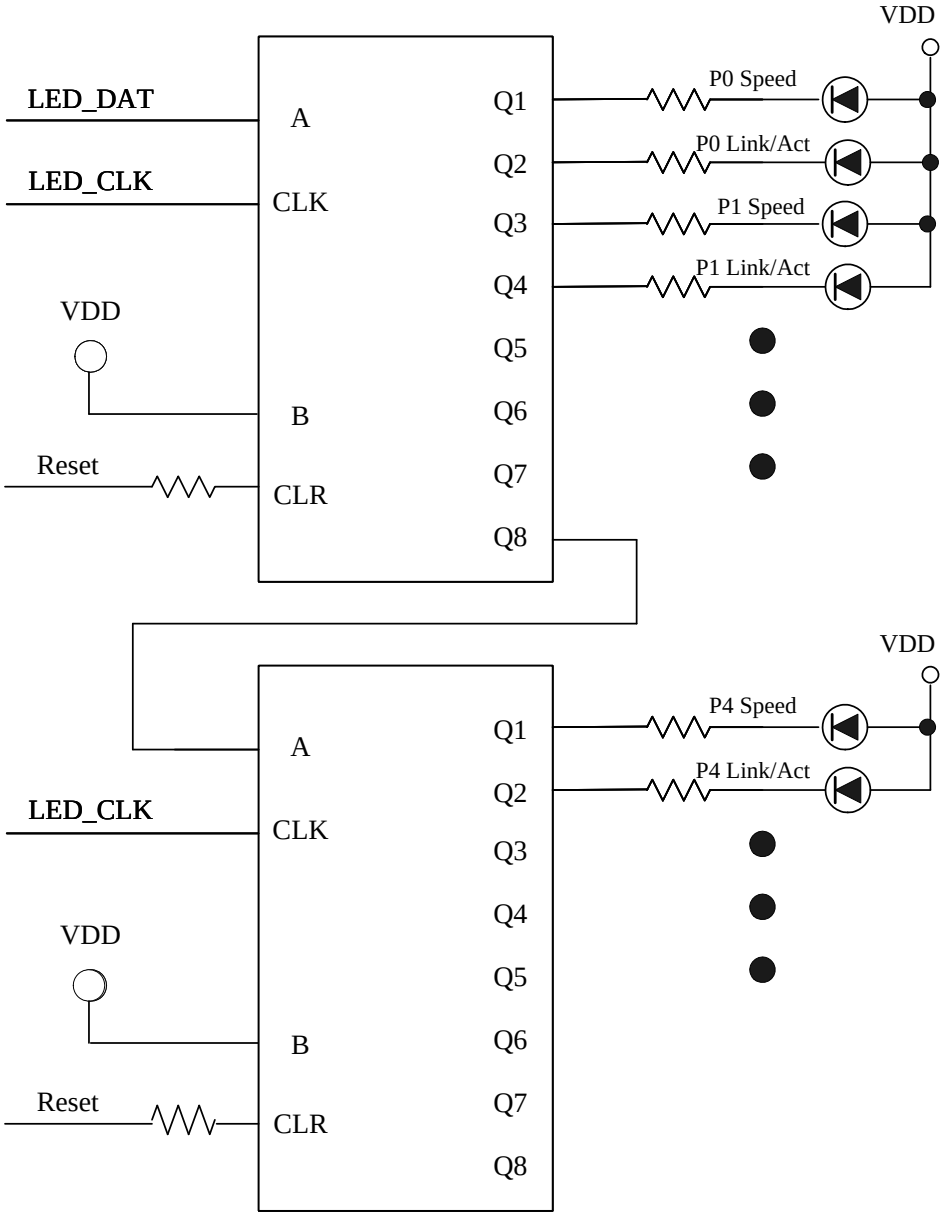
LED Name	LED Function
Speed	(1)P0 ~P23. ●: Link at 100Mbps. ○: Link at 10Mbps. (2)P24 ~P25. ●: Link at Giga bps/ Link at 100Mbps. ○: Link at 10Mbps.
Link/Act	●: Link and no activity ✱: Tx/Rx Activity ongoing.
Duplex/Col	●: Link in full duplex mode ○: Link in half duplex mode and no collision ✱: Collision

LED_Mode: Pin Setting= 101 or DDh[2:0]=010. (1 bicolor / 1 mono)

LED Name	LED Function
Link/Act/ Speed[1:0]	(1)P0 ~P23. 10: Link at 100Mbps. 01: Link at 10Mbps; 11: no link. (2)P24 ~P25. 10: Link at Giga bps. 01: Link at 100Mbps; 11: Link at 10Mbps or no link.
Col/Duplex	●: Link in full duplex mode ✱: Collision ○: Half duplex

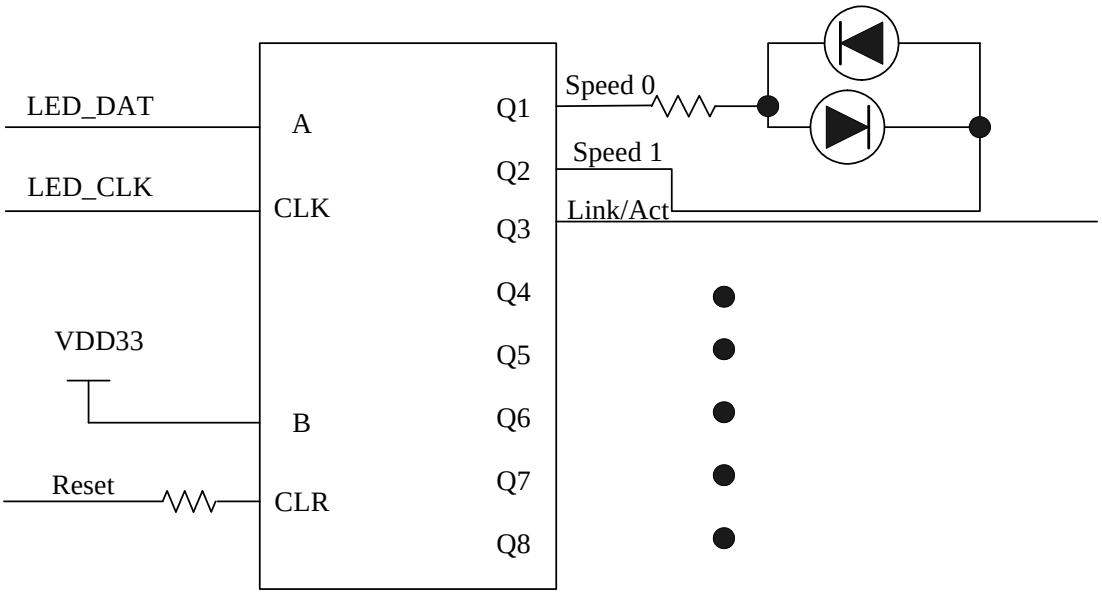
4.1.16.1 Mono Color LED Display

An example for 2 LED display mode is shown below.



2 LED Mode Display Sequence

4.1.16.2 Bi-color and Mono-Color Combination LED Display



Speed[1:0]	LED indication for SS-SMII	LED indication for RGMII port
00	None	10Mbps
01	10Mbps	100Mbps
10	100Mbps	1000Mbps

4.1.17 Group MAC Address Handling Method

The IP1826D provides 2 handling methods for group MAC address by configuring register 1[11]. If register 1[11] is set to "1", the packet with group address ranging from 01 80 C2 00 00 04 to 01 80 C2 00 00 0D will be dropped; otherwise it will be either broadcasted to other ports or dropped, depending on register 1[1] setting. The follwing table shows the handling methods for these group MAC addresses.

Register Setting / Group MAC Address	Register 01h[11]=0		Register 01h[11]=1	
	Register 1[1]=0	Register 1[1]=1	Register 1[1]=0	Register 1[1]=1
01 80 C2 00 00 00 (BPDU)	Drop if register 2[1] =0;	Broadcast	Drop if register 2[1] =0;	Broadcast
	Forward to CPU if register 2[1]=1;		Forward to CPU if register 2[1]=1;	
01 80 C2 00 00 02 (LACP)	Drop if register 2[3]=0			
	Forward to CPU if register 2[3]=1			
01 80 C2 00 00 03 (802.1X)	Drop if register 2[2]=0	Broadcast	Drop if register 2[2]=0	Broadcast

	Forward to CPU if register 2[2]=0		Forward to CPU if register 2[2]=0	
01 80 C2 00 00 04 ~ 01 80 C2 00 00 0D	Drop	Broadcast	Drop	Drop
01 80 C2 00 00 0E (LLDP)	Drop if register 1[12]=0	Broadcast if register 1[12]=0	Drop if register 1[12]=0	Broadcast if register 1[12]=0
	Forward to CPU if register 1[12]=1			
01 80 C2 00 00 20 (GMRP) & 01 80 C2 00 00 21 (GVRP)	Broadcast if register 2[4]=0			Drop
	Forward to CPU if register 2[4]=1			
Other Group Address	Drop	Drop	Drop	Drop

4.2 VLAN

IP1826D supports port based VLAN and tag based VLAN as the function described below.

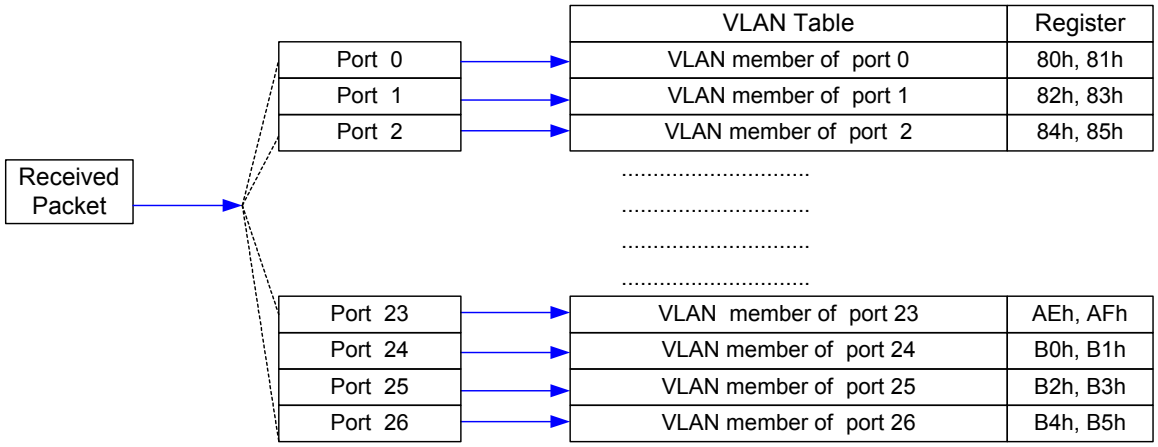
4.2.1 Port based VLAN

Related registers	80h~B5h, 40h[6]

The port based VLAN can be enabled by writing 0 to register 40h bit 6. Each port uses two registers to describe its port based VLAN configuration. Each port based LAN entry defines the broadcast domain of the ingress port and consists of 2 registers. The overall number of port based VLAN groups that the IP1826D can support is 27, defined in registers ranging from 80h to B5h.

Take the following example for the detailed description. The data coming from port 0 will be forwarded to the corresponding port configured as “1” in register 80h and 81h. Register 80h[0] corresponsds to port 0 and register 81h[10] corresponds to port 26. “For example, if register 81h and 80h are written with “000F” and “000F”, the broadcast packet coming from port 0 can only be forwarded to port 16~19 and port 1~3 only. Similarly, the forwarding rule for the data incoming from port 1 will refer to the register 82h and 83h. The forwarding rule for the data incoming from port 26 will refer to the register B4h and B5h.

Note: The port ID is counted from 0 to 26.

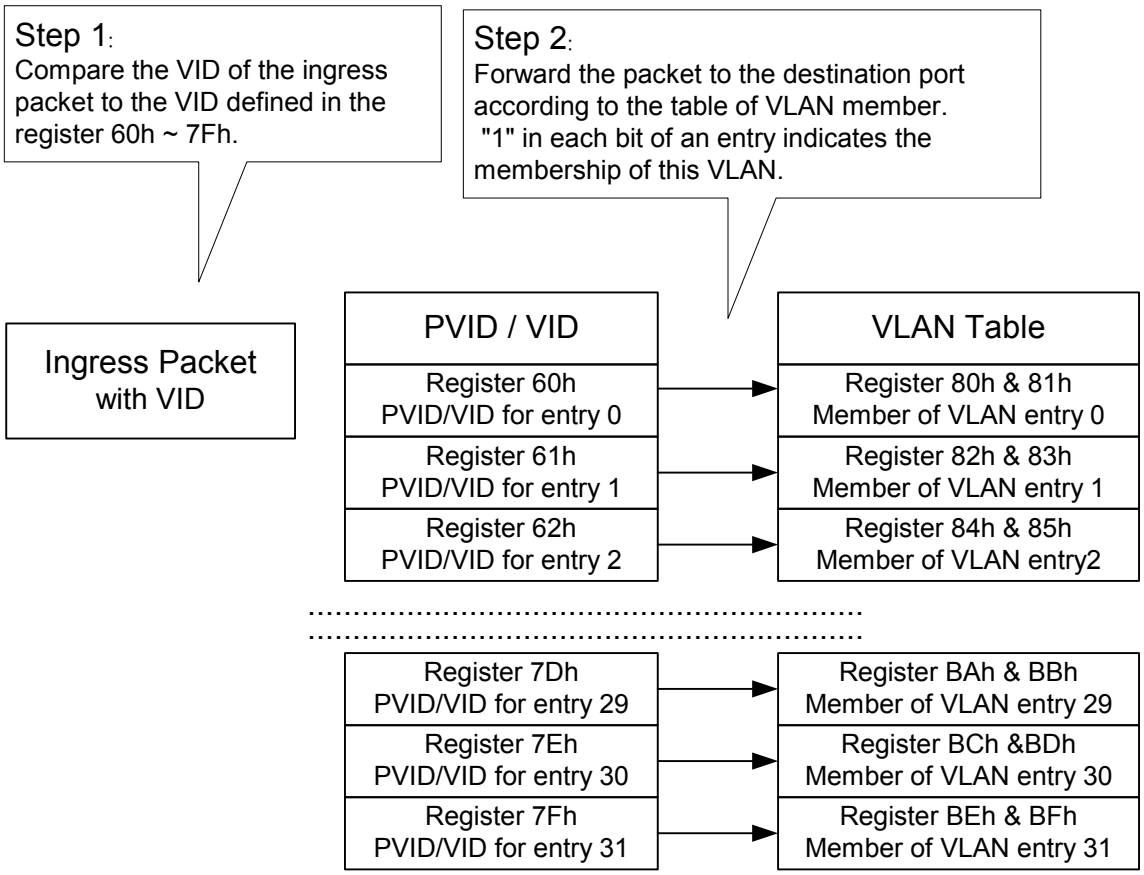


4.2.2 Tag based VLAN

Related registers	80h~BFh, 60h~7Fh, 53h~5Bh, 40h[6]

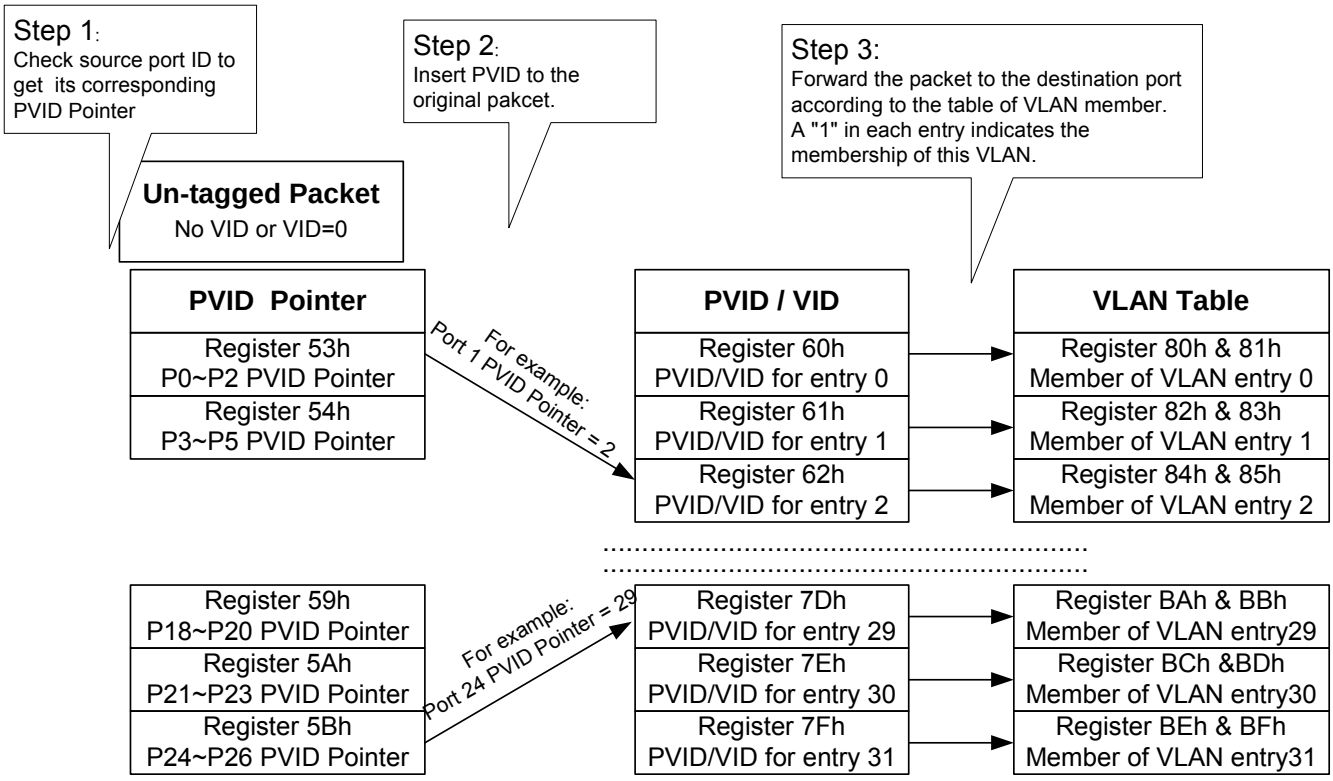
The IP1826D provides a tag based VLAN table with 32 entries; i.e. VID table entry 0~31. To activate the tag based VLLAN function, the designer should define 32 groups for the VLAN table, configure 32 PVID/VID defined in register 60h~7Fh and then enable tag based VLAN by setting register 40h[6] to “1”.

As the figure shown below, when a tagged packet is received, the IP1826D compares the tag in the packet with the one defined in the VID table. If it does not match, the IP1826D drops the packet. If it matches any entry of the VID table, the IP1826D forwards the packet to the VLAN member of the corresponding VLAN group. A “1” in each entry of VLAN table indicates the membership of this VLAN.



Handling a Tagged Packet

When an un-tagged packet is received, the IP1826D searches for the PVID pointer defined in register ranging from 53h to 5Bh and then get the correct PVID defined in registers ranging from 60h to 7Fh. This PVID will be inserted to the received packet and then it will be forwarded to the destination port according to the VLAN membership correponding to this PVID. The following figure depicts the details of this procedure.



Handling an Un-tagged Packet

4.2.3 Add/ Remove/ Modify VLAN tag

Related registers	5Ch~5Dh, 5Eh~5Fh, 60h~7Fh

There are 2 tagging/untagging methods for the egress packet, named as non-VID based mode and VID based mode. If register 40h[13] is set to “0”, the IP1826D can add/remove tag according to the register setting of register 5Ch to 5Fh, which is called non-VID based tagging/untagging mode. If register 40h[13] is set to “1”, the IP1826D will remove/add tag by inspecting the VID and its corresposnding tag handling method defined in register 80H to BFH, which is called VID-based tagging/untagging mode.

The various packet formats with/without a tag are showm below.

A packet without tag

DA	SA	data	CRC

A packet with VLAN tag

DA	SA	8100	VID	data	CRC

A packet with special tag and VLAN tag

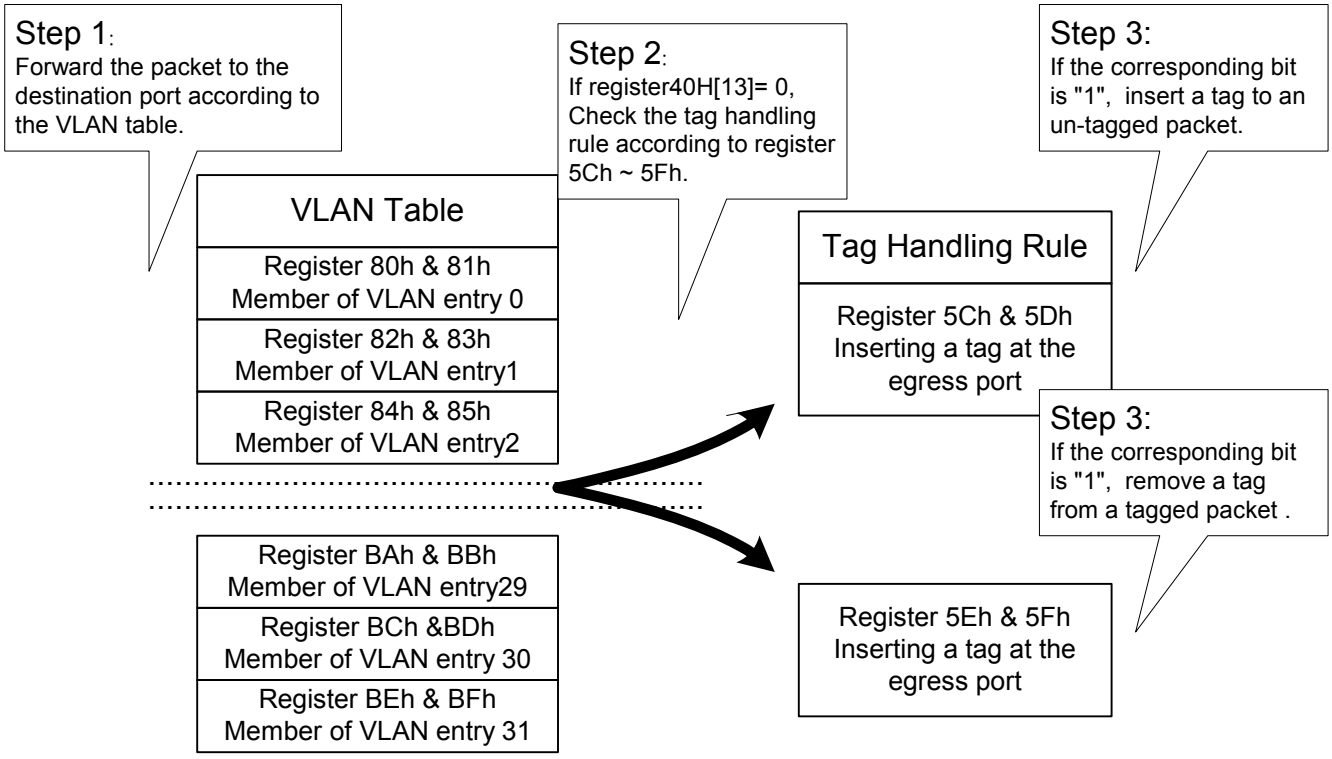
DA	SA	9126	Port Info.	8100	VID	data	CRC

- **Non-VID Based Tag Handling Method**

The non-VID based tag handling method is enabled by setting register 40h[13] to “0” and 40h[6] to ”1”. The IP1826D can change an un-tagged packet to a tagged packet by inserting EtherType ”8100h” and the VLAN tag. On the contrary, the IP1826D can also remove a tag from a tagged packet. When an un-tagged packet reaches the ingress port, the IP1826D will inspect the PVID pointer defined in register ranging from 53h to 5Bh and assign a corresponding PVID to the packet. The IP1826D forwards the packet to the member port according to the VLAN table defined in register ranging from 80h to BFh. Before sending the packet to the egress port, the IP1826D will check the tag handling rule defined in registers 5Ch to 5Fh. Adding tag at the egress port is enabled if the corresponding bit in register 5Ch and 5Dh is set to “1”. Removing a tag from a packet is enabled if the corresponding bit in register 5Eh and 5Fh is set to “1”.

Adding a tag or removing a tag at the egress port is performed simulatneously. If the received packet at the ingress port is an un-tagged type, the IP1826D will check the adding tag rule. On the contrary, if the received packet at the ingress port is a tagged type, the IP1826D will check the removing tag rule.

The operation is illustrated as follows.



Handling a Packet Without the Reference to VID

The behaviour for add/removing the tag is illustrated as the following table.

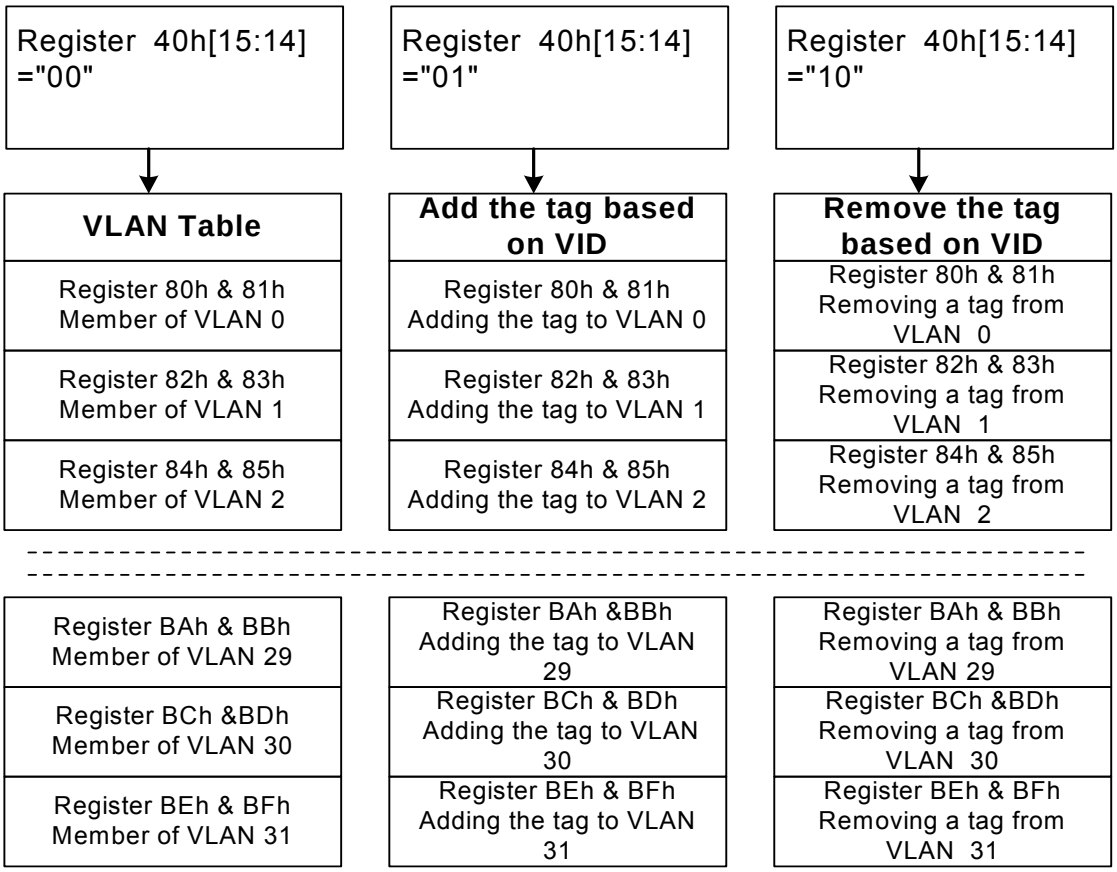
Received packet	**Register 40h[13] =0 & 40h[6] =1; Non-VID based Tag Handling Method**	
	Removing a Tag	**Adding a Tag**
	The corresponding bit of register 5Eh and register 5Fh is set to "1".	The corresponding bit of register 5Ch and register 5Dh is set to "1".
Untagged	Forward the ingress packet without modification	1. Insert EtherType "8100h" and VLAN tag. The VID value is defined in the register 60h~7Fh. 2. Calculate new CRC
Priority-tagged (VLAN ID=0)	1. Strip EtherType "8100h" and VLAN tag 2. Calculate new CRC	1. Keep priority field. 3. Replace the VID field with the PVID of the source port. The PVID value is defined in the register 60h~7Fh. 3. Calculate new CRC
VLAN-tagged	1. Strip EtherType "8100h" and VLAN tag 2. Calculate new CRC	Forward the packet without modification

❑ VID Based Tag Handling Method

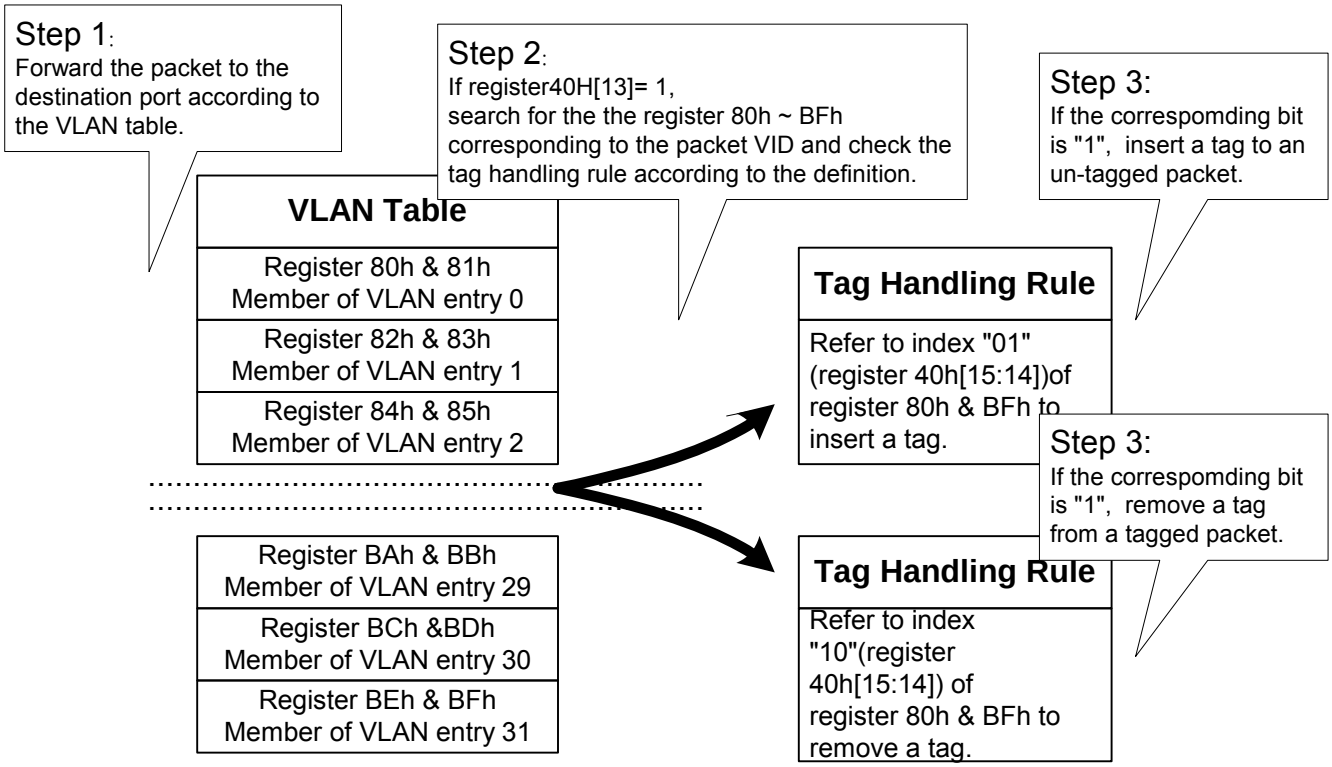
The VID based tag handling method is enabled by setting register 40h[13] to “1” and 40h[6] to ”1”. The IP1826D can change an un-tagged packet to a tagged packet by inserting EtherType ”8100h” and VLAN tag. When an un-tagged packet reaches the ingress port, the IP1826D will inspect the PVID pointer defined in register 53h to 5Bh and assign a corresponding PVID to the packet. The IP1826D forwards the packet to the member port according to the VLAN table defined in register ranging from 80h to BFh. At the egress port, the IP1826D will check the tag handling rule defined in registers ranging from 80h to BFh. Please note that there are 3 categories of registers defined in the range of 80h to BFh. Ranging from 80h to BFh, IP1826D contains 32 VLAN entries in total and every 2 registers correspond to 1 VLAN entry. Before accessing to these registers, the designer should configure register 40h[15:14] to “00”, “01” or “10” to set the index of these registers.

Adding a tag or removing a tag at the egress port is performed simulatneously. If the received packet at the ingress port is an un-tagged type, the IP1826D will check the adding tag rule. On the contrary, if the received packet at the ingress port is a tagged type, the IP1826D will check the removing tag rule.

The operation is illustrated as follows.



3 Blocks of Registers Defined in Register 80h to BFh



Handling a Packet with the Reference to VID

The behaviour for add/removing the tag is illustrated as the following table.

Received packet	**Register 40H[13] =1; Register 40h[6] =1; Tag based VLAN with the reference to VID**	
	Removing a Tag	**Adding a Tag**
	Index defined in regsiter 40[15:14]=”10”. The corresponding bit of register 80h ~ BFh is set to “1”.	Index defined in regsiter 40[15:14]=”01”. The corresponding bit of register 80h ~ BFh is set to “1”.
Untagged	Forward the ingress packet without modification	1. Check the PVID and compare the corresponding tag handling method defined in registers 80H ~ BFH. 2. If the egress port is defined as adding a tag, insert “8100h” and the PVID defined in the register 60H~7FH. 3. Calculate new CRC.

Priority-tagged (VLAN ID=0)	1. Check the PVID and compare the corresponding tag handling method defined in registers 80H ~ BFH. 2. If the egress port is defined as removing a tag, remove tag according to the definition of register 80H ~ BFH. 3. Calculate new CRC	1. Keep priority field. 2. Check the PVID and compare the corresponding tag handling method defined in registers 80h ~ BFh. 3. If the egress port is defined as adding a tag, replace the VID field with the PVID defined in registers 60h ~7Fh. 4. Calculate new CRC
VLAN-tagged	1. Check the VID and compare the corresponding tag handling method defined in registers 80H ~ BFH. 2. If the egress port is defined as removing a tag, remove tag according to the definition of register 80H ~ BFH. 3. Calculate new CRC	Forward the packet without modification

4.2.4 VLAN Striding

Related registers	40h[7]

In normal case, a packet is not allowed to be forwarded across a VLAN. That is, if the destination port does not belong to the same VLAN, the packet is dropped. IP1826D provides a VLAN option to allow uni-cast packets to stride across a VLAN. This function is enabled by set bit 7 of register 40h.

4.2.5 VLAN up-link

Related registers	40h[8], 4Ah~4Bh

In normal operation, if the destination and source are located in different VLANs, the packets will be dropped. IP1826D supports an option to forward the packets filtered by this condition to up-link ports if register 40h bit 8 is set to “1”. The up-link ports are defined in register 4Ah and 4Bh.

4.3 Class of Service

4.3.1 Output Queue scheduling with priority

Related registers	01h[6], 3Dh

IP1826D implements two levels of priority queues, high priority and low priority. The priority for each packet is based on the following schemes:

1. Physical port
2. 802.1Q VLAN tag
3. IP TOS/DS
4. TCP/UDP port number

Each incoming packet is mapped to either a high priority queue or a low priority queue. When no CoS function is enabled, the first-in/ first-out forwarding method is used. The weight function, for the ratio of high/low priority, is defined in register 3Dh.

When multiple CoS schemes are enabled, the data packet is treated as the high priority as long as any one of four CoS schemes is mapped to “high”. IP1826D guarantees the priority of traffic in spite of whether the flow control function is on or off.

Take the following example for the detailed explanation.

If a port is set as a low priority port, when it receives a packet embedding a VLAN tag with high priority and embedding IP DS field with low priority, this packet will be forwarded as a high priority packet. In the other words, the priority of a packet would be set to high if any of three CoS schemes is interpreted as the high priority.

IP1826D provides an option to pause flow control function to prevent the extra delay for a high priority packet. A port’s flow control function is disabled for 1.5s automatically when it receives a high priority packet. This function can be enabled by writing “1” to register 01h[6].

4.3.2 Port based CoS

Related registers	22h~23h

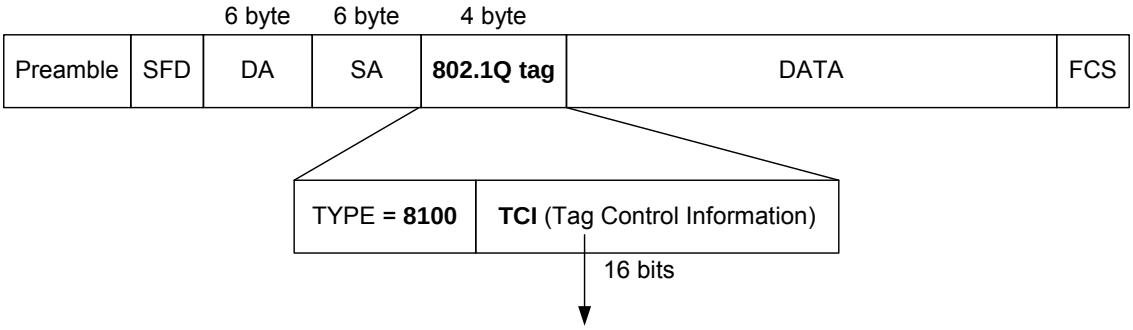
The port-based priority only concerns the physical port location in a switch. A packet received by a high priority port is handled as a high priority packet. Each port of IP1826D can be configured as a high priority port individually by programming register 22h and 23h. For example, the bit 0 of register 22h corresponds to port 0 and the bit 0 of register 23h corresponds to port 16.

4.3.3 802.1Q priority tag based CoS

Related registers	24h~25h

When the CoS for 802.1Q VLAN tag is enabled, the IP1826D will examine the 3 bits of priority field carried by a VLAN tag and map it to the corresponding priority. A packet with priority field ranging from 0 to 3 will be treated as a low priority packet, and will be stored in low priority queue. A packet with priority field ranging from 4 to 7 will be treated as a high priority packet, and will be stored in high priority queue. The CoS function of each port can be enabled individually by programming register 24h and 25h. For example, the bit 0 of register 24h corresponds to port 0 and the bit 0 of register 25h corresponds to port 16.

802.1Q priority tag based CoS



Bit[15:13]: Priority
IP1826 uses these bits to define priority.
Low priority: 000~011
High priority: 100~111

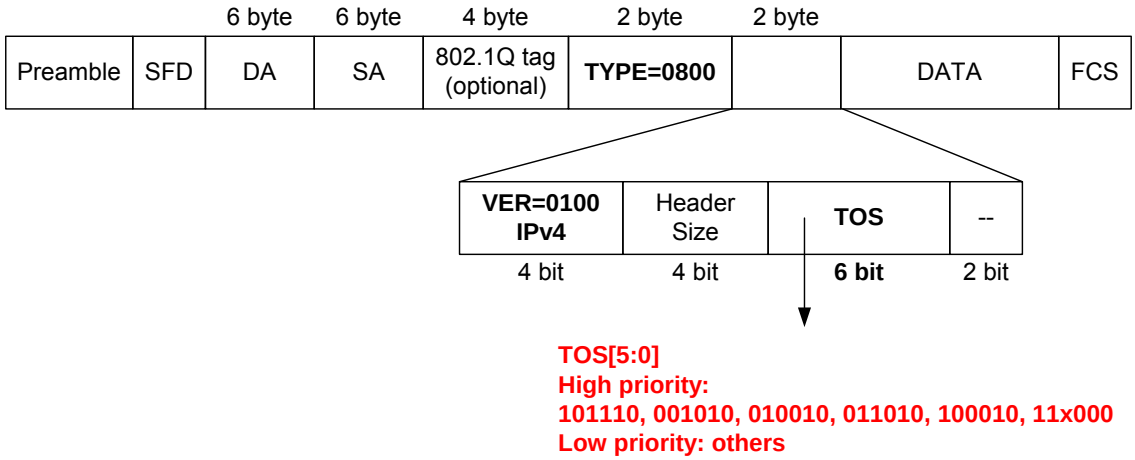
Bit 12: Canonical Format Indicator (CFI)
Bit[11~0]: VLAN ID.

4.3.4 IP TOS based CoS

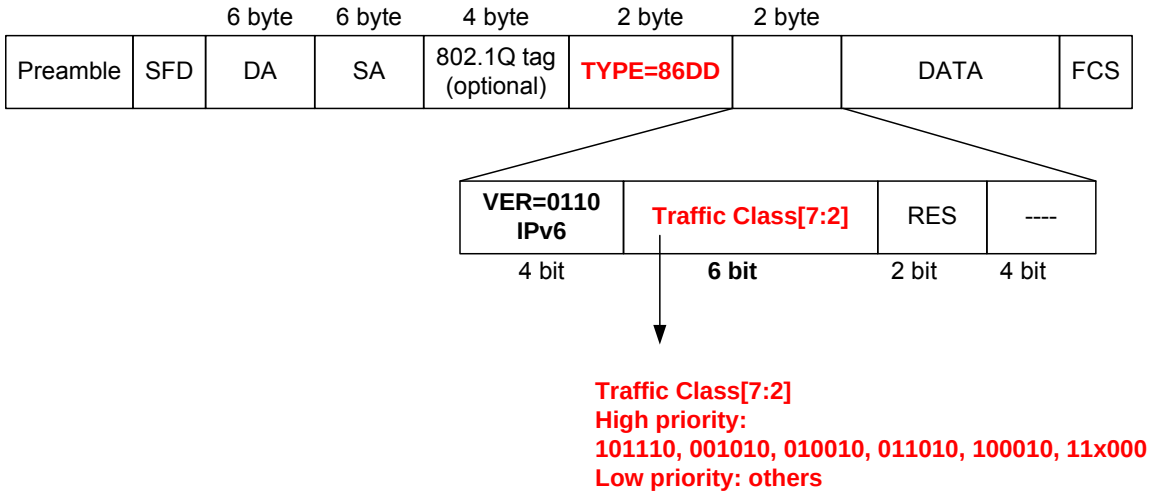
Related registers	26h~27h

IP1826D provides the IP layer CoS function by recognizing the priority octet and mapping it to the corresponding priority. For an IPv4 packet, it is embedded in the TOS (type of Service) Octet. For an IPv6 data packet, the Traffic Class Octet is used to differentiate the Class of Service. When this function is enabled, the IP1826D will automatically recognize the IP version and capture the either the TOS field (IPv4) or Traffic Class field (IPv6).

IPv4 frame format



IPv6 frame format



The IP TOS/DS priority function of each port can be enabled individually by programming register 26h and 27h. For example, the bit 0 of register 26h corresponds to port 0 and the bit 0 of register 27h corresponds to port 16.

4.3.5 TCP/UDP port number based CoS

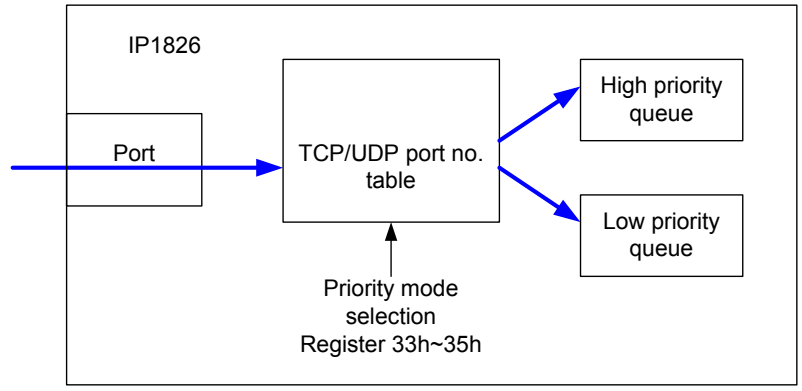
Related registers	33h~35h, 2Dh~32h, 01h[8]

When the CoS based on TCP/UDP port number function is enabled, IP1826D will examine the TCP/UDP destination port number in a packet to decide its priority.

Designer can define the priority of protocols, based on TCP/UDP port number, by programming register 33h~35h. A packet with TCP/UDP port number matched that listed in register 33h~35h will be treated as a high/ low priority packet according to the corresponding setting in the registers. For example, a packet with TCP/UDP port number equal to 20 or 21 (FTP) will be handled as a high priority packet if register 33h[1:0] is set to “11”. A packet with TCP/UDP port number equal to 20 or 21 (FTP) will be handled as a low priority packet if register 33h[1:0] is set to “10”. The priority of the TCP/UDP port number will override the priority of the user-defined port number if the priority of FTP (20, 21) is set to low and the priority of the port number (1~21) is set to high for user-defined setting, the priority of port number (20,21) will be treated as low priority rather than high priority.

A packet with TCP/UDP port number matched the user-defined port number in register 2Fh~32h will be treated as a high/ low priority packet according to the setting in the register 35h[15:8]. For example, a packet with TCP/UDP port number matched the one defined in the register 2Fh will be handled as a high priority packet if register 35h[9:8] is set to “11”. IP1826D will not check the bits of user -defined port number if the corresponding bit in register 2Dh and 2Eh is written with “0”. For example, if the bit 8 of register 2Dh is “1”, the bit 0 of the port number defined in register 30h will not be checked.
Note: The user-defined port should not cover the well-know port specified in Reg33h~Reg35h.

In addition to the priority classification, a packet matching the defined TCP/UDP port number can be either dropped or forwarded to CPU, depending on the register0x01[7].
Note: When port 24 or port 25 works at Gigabit speed, the packet incoming to these ports cannot be forwarded to CPU port.



A packet with TCP/UDP port number defined as low priority in register 33h~35h will be treated as a low priority packet if register 01h[8] is set to “1”; regardless port based/ tag based/ IP based priority setting. That is, it overwrites other settings.

Register 33h

bit	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
Protocol	POP3	HTTP_0,1	TFTP	DNS	SMTP	TELNET	SSH	FTP
definition	00: TCP/UDP port number based Cos function disabled 11: high priority 10: low priority							

Register 34h

bit	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
Protocol	XP_RDP	MSN	HTTPS	SNMP_0,1	IMAP_0,1	NETBIOS0,1,2	SNTP	NEWS
definition	00: TCP/UDP port number based Cos function disabled 11: high priority 10: low priority							

Register 35h

bit	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
Protocol	user define port no. D in register 32h	user define port no. C in register 31h	user define port no. B in register 30h	user define port no. A in register 2Fh	BOOTP/DHCP	YAHOO	ICQ	QQ_0,1
definition	00: TCP/UDP port number based Cos function disabled 11: high priority 10: low priority							

4.4 Capture Ethernet protocol frame & IP packet to CPU port

IP1826D recognize the following type of packets by examing the field listed in the following table.

	DA	Type	Protocol no. In IP Header	Port no. In UDP header	Note
In-band management	1826's MAC address	--	--	--	Global setting
BPDU	01-80-C2-00-00-**00**	--	--	--	Global setting
LACP	01-80-C2-00-00-**02**	--	--	--	Global setting
802.1x	01-80-C2-00-00-**03**	--	--	--	Per port setting
GVRP, GMRP	01-80-C2-00-00-**20~21**	--	--	--	Global setting
OSPF	--	0800	89	--	Global setting
ARP	--	0806	--	--	Global setting
ICMP	--	0800	01	--	Global setting
IGMP	01-00-5E-XX-XX-XX	0800	02	--	Global setting
TCP	--	0800	06	--	Global setting
UDP	--	0800	17	--	Global setting

Note:
1. "--" means don't care.
2. Pause frame is not forwarded to CPU.

4.4.1 In-band management frame

Related registers	02h[0], F2h[0], 28h~2Ah

IP1826D has a default MAC address 00-90-c3-00-00-01. If an incoming packet with DA equal to IP1826D's MAC address will be dropped if register 02h[0] is set to "0" or forwarded to CPU port if register 02h[0] is set to "1" and register F2h[0] is set to "1". IP1826D's MAC address can be updated by programming register 28h~2Ah.

4.4.2 ARP, 802.1x

Related registers	02h[2], 2Bh and 2Ch, 02h[5]

A port only forwards ARP and 802.1x EAPOL frames and drops other packets if the corresponding bit in register 2Bh and 2Ch is set to "1" and 02h[2] is set "1", too. A port resumes to normal operation if the corresponding bits are cleared. Please refer to section 4.5.2 802.1x port based security for more detail information.

Besides forwading ARP to its destination port, IP1826D can forward an ARP to CPU port if register 02h[5] is set to "1'.

4.4.3 BPDU, LACP, GVRP, GMRP

Related registers	02h[4:3], 02h[1], 01h[2], F2h[0]

IP1826D recognizes an incoming BPDU, LACP, GVRP and GMRP packet and decides to forward it to CPU only or drop it according to the setting in register 02h[1], 01h[2] and 02h[4:3]. Register F2h[0] defines port 26 to be CPU port.

Bit		02h[4]		02h[3]		02h[2]		02h[1]	
Protocol		GVRP, GMRP		LACP		01-80-C2-00-00-03		BPDU 01-80-C2-00-00-00	
01h[1]	F2h[1]	0	1	0	1	0	1	0	1
0	0	Broadcast	Drop	Drop	Drop	Drop	Drop	Drop	Drop
	1		To CPU only		To CPU only		To CPU only		To CPU only
1	0		Drop		Drop	Broadcast	Drop	Broadcast	
	1		To CPU only		To CPU only		To CPU only		

4.4.4 ICMP, TCP, UDP, OSPF

Related registers	02h[13:6], F2h[0]

IP1826D recognizes an incoming ICMP, TCP, UDP, and OSPF packet and decides to either forward it to CPU or drop it, according to the setting in register 02h[13:6]. Register F2h[0] defines port 26 to be CPU port.

Register 02h

bit	13:12	11:10	9:8	7:6
Protocol	OSPF	UDP	TCP	ICMP
definition	00: Send to its destination port. 01: Send to CPU port and its destination port. 10: Send to CPU port only. 11: drop			

4.4.5 The other IPv4 protocols

IP1826D handles the other IPv4 protocols not mentioned above according to the setting of 02h[15:14].

bit	02h[15:14]
Protocol	Other prorocols of IPv4
definition	00: Send to its destination port. 01: Send to CPU port and its destination port. 10: Send to CPU port only. 11: drop

4.4.6 Block broadcast frame to CPU port

All broadcast frames will be inhibited to forwarded to CPU port if register 40h[4] is set to “1”. When this function is enabled, IPv4 can be still forwarded to CPU port, if register 40h[5] is set to “1”.

4.5 Security

4.5.1 MAC address based Security

Related registers	45h~46h, 49h[1:0]

IP1826D supports MAC address based security function if register 49h[1] is written with “0”. When the function is enabled, IP1826D drops the packet with a SA not found in the address table. This function is valid only if the address learning function is disabled by programming register 45h and 46h.

IP1826D provides an option to forward the un-known SA packets to CPU when the function is enabled. An un-known SA packet is forwarded to CPU, if bit 0 of register 49h is cleared.

4.5.2 802.1x port based security

Related registers	2Bh, 2Ch, 02h[2]

IP1826D supports 802.1x based security function. If the function is enabled, IP1826D only forwards 802.1x EAPOL packets (DA=01 80 C2 00 00 03 or switch’s mac address which defined in 28~2Ah and packet type=88 8E) to CPU port and drops other types of packets. ARP packets are not affected by the function and are forwarded according to their destination address. This function can be enabled for each port individually by programming register 2Bh and 2Ch. Designer has to write “1” to register 02h[2] to instruct IP1826D to forward EAPOL packets to CPU. If register 02h[2] is written with ‘0”, all EAPOL packets will be dropped.

4.5.3 IP address based Security

Related registers	41h

IP1826D supports IP address based security function by examining the IP address and source port of an incoming packet. Designer can instruct IP1826D to check source IP address or destination IP address by programming register 41h[3] and select one of the 4 matching modes by programming register 41h[1:0] as shown in the following table. This function is enabled if register 41h[7] is set to 1.

For example, if register 41h[3:0] is written with 4'b1101, mode 2 is selected. A packet will be dropped by IP1826D if its destination IP doesn't match.

To perform IP security, designer has to fulfill the IP entries, which contains the source port and IP information. There are two ways to decide the location of an IP entry, hashing result and source port.

If hashing result method is selected, register 41h[2] set to "0", IP1826D uses the hashing result of the 32-bit IP address as the address of the entry. If register 41h[3] is set to '1', IP1826D uses the hashing result of the destination IP of a packet as the address of the entry. If register 41h[3] is set to '0', IP1826D uses the hashing result of the source IP of a packet as the address of the entry.

If source port method is selected, register 41h[2] set to "1", IP1826D uses the source port as the address of the entry. For example, port 0 is corresponding to "000" and port 3 is corresponding to "003", etc. The IP entry should be configured as a static address by writing the aging field with "1111". Please refer to section 4.1.10 for the detail description of accessing the address table.

Mode	41h[1:0]	Checking items			The address of an IP entry	
		41h[3]=X	41h[3]=0	41h[3]= 1		
		Source port	Source IP	Destination IP	41h[2]= 1	41h[2]= 0
1	00	X	0	0	Source port	IP address hashing result
2	01	X	1	1		
3	10	1	1	1		
4	11	0	1	1		

Note: 1: match, 0:un-match, X: don't care

IP1826D supports an option to shift the location of IP entry. If register 41h[6] is set to "1", IP1826D will add the address of an entry derived from the algorithm mention above by 1~3 according to the setting of register 41h[5:4] to prevent entry collision in IP address table.

4.5.4 TCP/UDP port based Security

Related registers	33h~35h, 01h[7]

IP1826D supports TCP/UDP port based security function by examining the port number in an incoming packet. Designer can enable the function by programming register 33h~35h.

When the function is enabled, a packet with TCP/UDP port number matched that listed in register 33h~35h will be dropped or forwarded to CPU port according to registers 01h[7]. For example, a packet with TCP/UDP port number equal to 20 or 21 (FTP) will be dropped if register 33h[1:0] is set to "01" and register 01h[7] is set to "0". A packet with TCP/UDP port number equal to 25 (SMTP) will be forwarded to CPU if register 33h[7:6] is set to "01" and register 01h[7] is set to "1".

Register 33h

bit	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
Protocol	POP3	HTTP_0,1	TFTP	DNS	SMTP	TELNET	SSH	FTP
definition	00: TCP/UDP port number based security function disabled 01: drop (if 01h[7]=0)/ forward to CPU (if 01h[7]=1)							

Register 34h

bit	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
Protocol	XP_RDP	MSN	HTTPS	SNMP_0,1	IMAP_0,1	NETBIOS0,1,2	SNTP	NEWS
definition	00: TCP/UDP port number based security function disabled 01: drop (if 01h[7]=0)/ forward to CPU (if 01h[7]=1)							

Register 35h

bit	15:14	13:12	11:10	9:8	7:6	5:4	3:2	1:0
Protocol	user define port no. D in register 32h	user define port no. C in register 31h	user define port no. B in register 30h	user define port no. A in register 2Fh	BOOTP/DHCP	YAHOO	ICQ	QQ_0,1
definition	00: TCP/UDP port number based security function disabled 01: drop (if 01h[7]=0)/ forward to CPU (if 01h[7]=1)							

4.6 WAN port filtering

Related registers	F4h~F5h, 36h~37h, 2Dh~32h

IP1826D supports a function to enable/disable a WAN port to send out packets with specific TCP/UDP port number. Each port can be configured to be a WAN port individually by programming register F4h and F5h. When the function is enabled, IP1826D forwards or drops a packet with TCP/UDP port number, defined in register 36h and 37h, to WAN port, defined in register F4h and F5h, according to the setting of 37h[8].

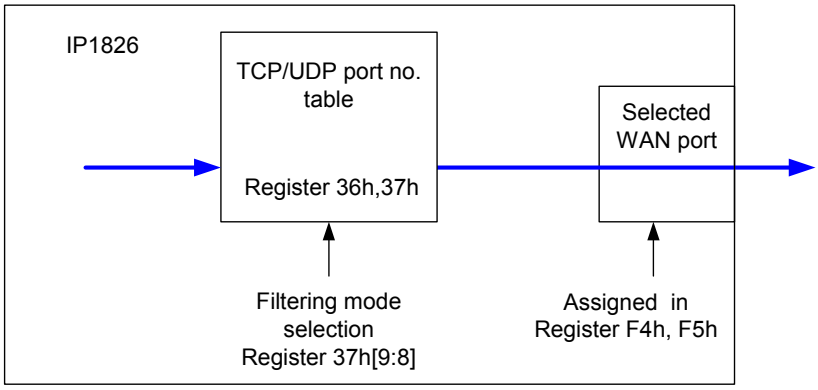
If designer defined TCP/UDP port number is selected, 37h[7:4], IP1826D handles packets according to the TCP/UDP port number defined in register 2Fh~32h.

For example, a packet with destination TCP/UDP port number matched the one defined in the register 2Fh will be dropped by a filtering port, if register 37h bit 8 and bit 4 are set to “01”. A packet with destination TCP/UDP port number matched the one defined in the register 32h will be sent by a filtering port, if register 37h[8:7] are set to “11”. The network administrator is recommended to set this secure WAN at the physical port near the server side.

IP1826D only checks the bits in destination TCP/UDP port number of which corresponding mask bits in register 2Dh~2Eh are set.

In addition to the TCP/UDP port defined in Reg36h and Reg37h, the user-defined TCP/UDP port, which is described in Reg2Fh~Reg32h, can be applied to this rule, expanding the TCP/UDP security.

Note: The user-defined TCP/UDP port should not cover the protocol defined in Reg36h and Reg37h.



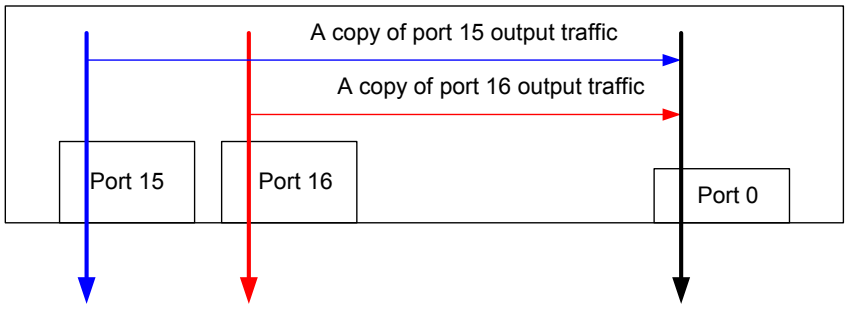
4.7 Port Mirroring

Related registers	40h[10:9], 4Fh~52h

In some circumstances, the network administrator requires to monitor the network status. The port mirroring function helps the network administrator diagnose the network.

A port mirroring function is accomplished by assigning monitored ports (source ports), snooping ports (destination ports) and snooping method. IP1826D will copy the traffic of monitored ports to all snooping ports. That is, the snooped packets for all snooping ports are the same. The IP1826D supports three kinds of mirroring methods: the ingress, the egress and ingress plus egress. It is defined in register 40h[10:9]. Registers 4Fh and 50h define the ports to be monitored (mirroring source). Register 51h and 52h specifies the ports to snoop (mirroring destination).

For example, if designer wants to monitor the output traffic of port 15 and port 16 from port 0 as shown in the following figure. He has to write “01” to register 40[10:9] to choose monitor method to be output traffic, write 8000h and 0001h to register 4Fh and 50h to select port 15 and 16 to be monitored ports, write 0001h and 0000h to register 51h and 52h to select port 0 as a monitoring port. IP1826D will copy the traffic out of port 15 and port 16 to port 0.

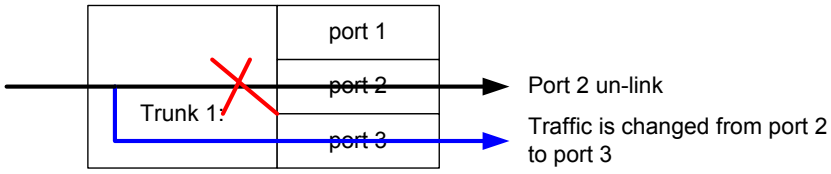


4.8 Trunk Channel

Related registers	40[3:2], 4Ch~4Eh

4.8.1 Trunk channel behavior

IP1826D supports 3 trunk channels consisting of port 0~3, port 4~7 and port 24~25. Each trunk channel may comprise 2 to 4 ports. Designer can configure the trunk channel individually by writing non-zero values to the corresponding bits of a port in the register 4Ch~4Eh. A trunk channel works as if a “big” port with multiple times of bandwidth. If the destination port of a packet is un-link, IP1826D forwards the packet to the other port of the trunk.

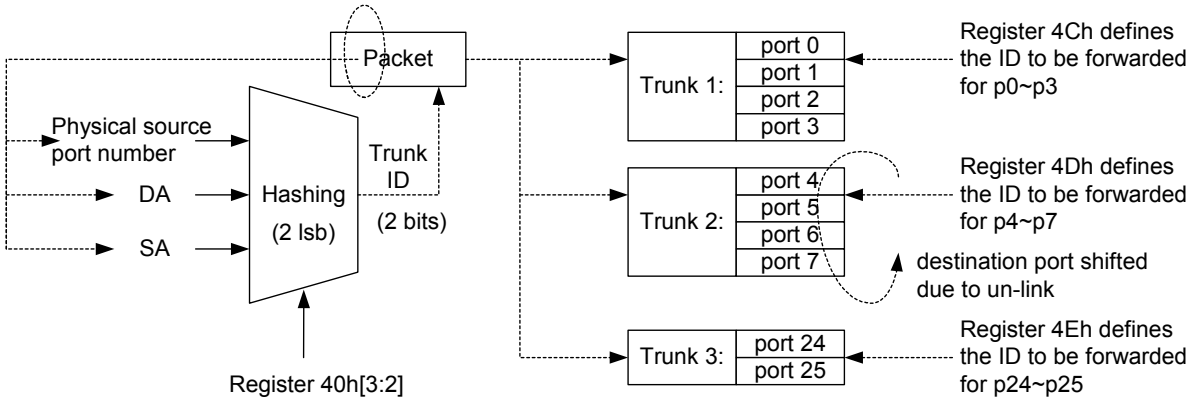


4.8.2 Load balance

To fully utilize the bandwidth in a trunk channel, IP1826D supports load balance function. A physical port of a trunk forwards a packet only if the trunk ID of the packet matches the ID setting of the port. That is, when a packet is forwarded to a port in a trunk, its destination port is according to trunk ID. The trunk ID of each trunk port is defined in register 4Ch~4Eh. For example, if register 4Ch[3:0] is written with 0001, only the packet with ID equal to 0 will be forwarded by port 0. If register 4Ch[7:4] is written with 0010, only the packet with ID equal to 1 will be forwarded by port 1.

IP1826D performs a hashing algorithm to calculate a 2-bit trunk ID of a packet. It is used to select one of the trunk ports to forward packets. Designer can select the hashing algorithm to be based on physical port number, DA, SA, or DA&SA by programming registers 40h[3:2].

If the destination port of a trunk is un-link, the packet will be forward the port shifted by 2. If the port is un-link, too, the packet will be forward the port shifted by 3. For example, if port 1 is un-link, its packet will be forwarded to port3. If port 3 is un-link, too, the packet will be forwarded to port 0.

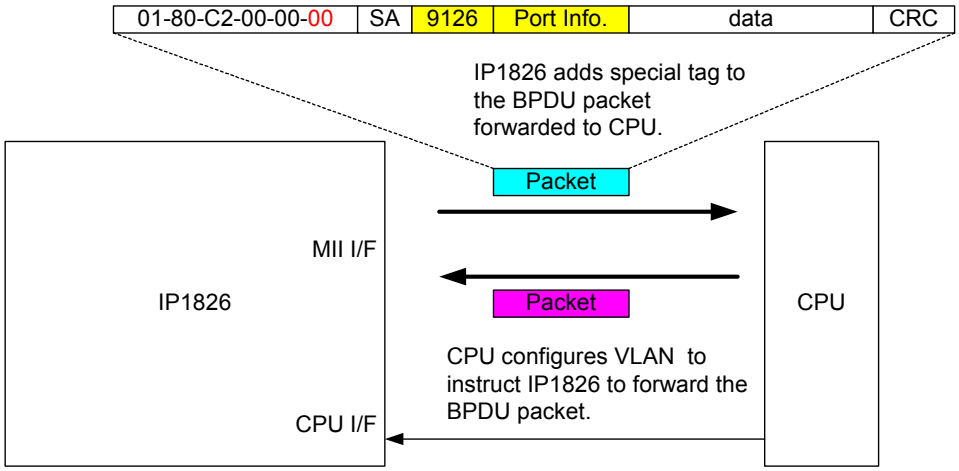


4.9 Spanning tree (receiving/ learning/ forwarding enable/disable)

4.9.1 BPDU packet forwarding

Related registers	02h[1], F2h[1:0], 60h~7Fh, C3h~C4h

IP1826D supports spanning tree function with the following features:
1. Detect BPDU frames by examining multicast address (01-80-c2-00-00-00).
2. Forward BPDU packets to CPU through port 26 and add special tag for source port information. The function is enabled by writing “1” to register 02h[1], “0” to register 01h[1] and “11” to register F2h[1:0].
3. Forward BPDU packets from CPU according to the VLAN Configuration.



4.9.2 Port states

Related registers	1Eh~1Fh, D8h~D9h, 45h~46h, 47h~48h

To support IEEE802.1D spanning tree protocol, each port of IP1826D supports five states defined in IEEE802.1D by providing four functions on each port as shown in the following table. Port 0~25 of IP1826D can be configured in one of the five spanning tree states individually by programming register 1Eh~1Fh, D8h~D9h, 45h~46h, 47h~48h to enable/disable receiving, transmission, learning and BPDU receiving function.

	The corresponding bit for setting of port 15~port 0	The corresponding bit for setting of port 26~port 16	Description
Packet receiving	Register 1Eh, bit15 ~ bit0	Register 1Fh, bit10 ~ bit0	1: Enable receiving; 0: Receive no packets
Packet transmission	Register D8h, bit15 ~ bit0	Register D9h, bit10 ~ bit0	1: Enable transmission; 0: Transmit no packets
MAC address learning	Register 45h, bit15 ~ bit0	Register 46h, bit10 ~ bit0	1: Enable; 0: Disable

Packet forwarding	Register 47h, bit15 ~ bit0	Register 48h, bit10 ~ bit0	1: Receive & Forward packets; 0: Forward no packets except BPDU.

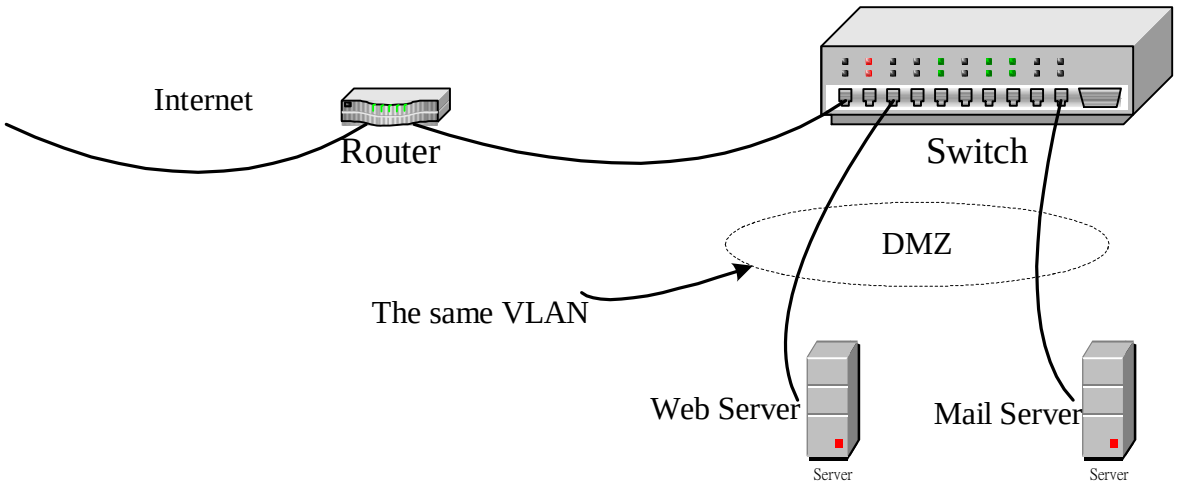
States In 802.1D	Corresponding function (register) supported by IP1826D								
	1Eh~1Fh		D8h~D9h		45h~46h		47h~48h		
	Receive	Bit value	Transmit	Bit value	Learning	Bit value	Fwd BPDU	Fwd packet	Bit value
Disabled	X	0	X	0	X	0	X	X	0
Blocking	O	1	X	0	X	0	X	X	0
Listening	O	1	O	1	X	0	O	X	0
Learning	O	1	O	1	O	1	O	X	0
Forwarding	O	1	O	1	O	1	O	O	1

Note1: O: enabled, X: disabled

4.10 Port Excluding

If a port is set to be “excluded”, it will not allowed to forward data to the other port which is also “excluded”. This function is useful for preventing the server from the hacker’s intrusion. Take the following figure for example. In the normal application, the web server and the mail server are located in a DMZ and probably in the same VLAN. Imagine a worse scenario about the network security. If either server is compromised by an intrusion, it’s probably that the hacker will source an attack from that server. By enabling the port excluding function of both ports, both mail servers and web server are not allowed to communicate each other, preventing the attack sourced by the other.

Setting VLAN to both servers can also accomplish this goal, but it requires to set more complicated VLAN table. By configuring port excluding function, the network is more secure and the maintenance is easier.



4.11 IGMP Snooping

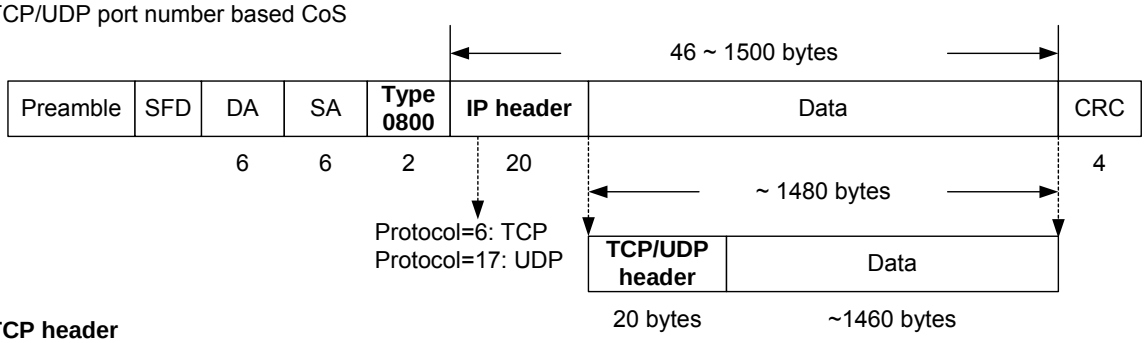
Related registers	C0h

For a switch without IGMP snooping, a multicast packet is forwarded to all ports, that is, it is treated as a broadcast packet. With IGMP snooping, a multicast packet of a group is only forwarded to ports that are members of that group. IGMP (Internet Group Management Protocol) is used to establish membership in a Multicast group. It significantly reduces multicast traffic in a switch.

4.12 Frame format

4.12.1 Frame format of TCP/UDP header

TCP/UDP port number based CoS



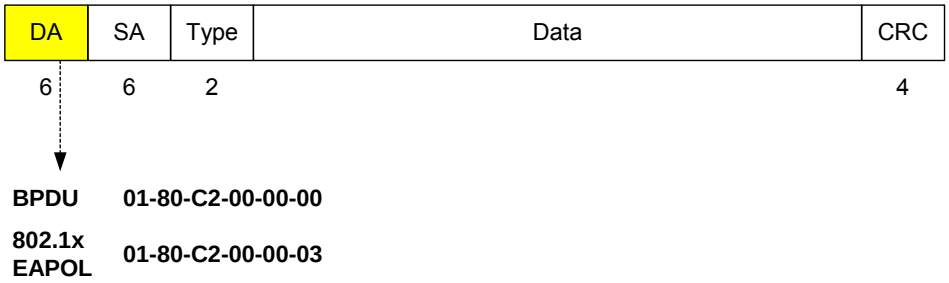
TCP header

0	8	16	24	31
Source port			**Destination port**	
Sequence number				
Acknowledge number				
HLEN	Reserved	UGR ACK PSH RST SYN FIN	Window	
Check Sum of TCP header (16)			Urgent pointer	
Options				Padding

UDP header

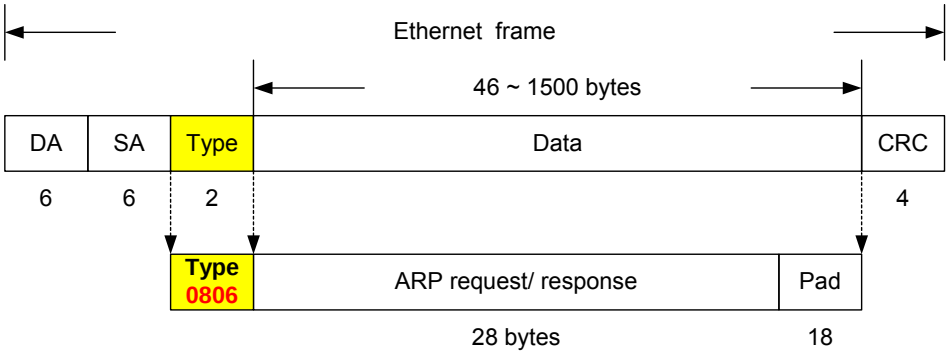
0	8	16	24	31
Source port			**Destination port**	
Length			Check Sum of UDP header	

4.12.2 Frame format of BPDU and 802.1x

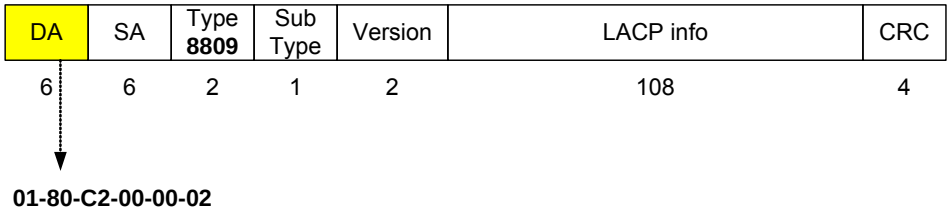


4.12.3 Frame format of ARP, LACP, GVRP, GMRP

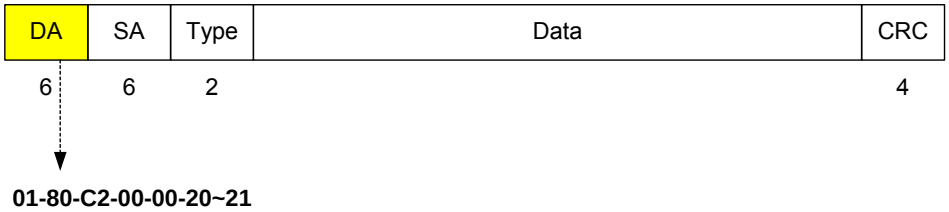
ARP



LACP

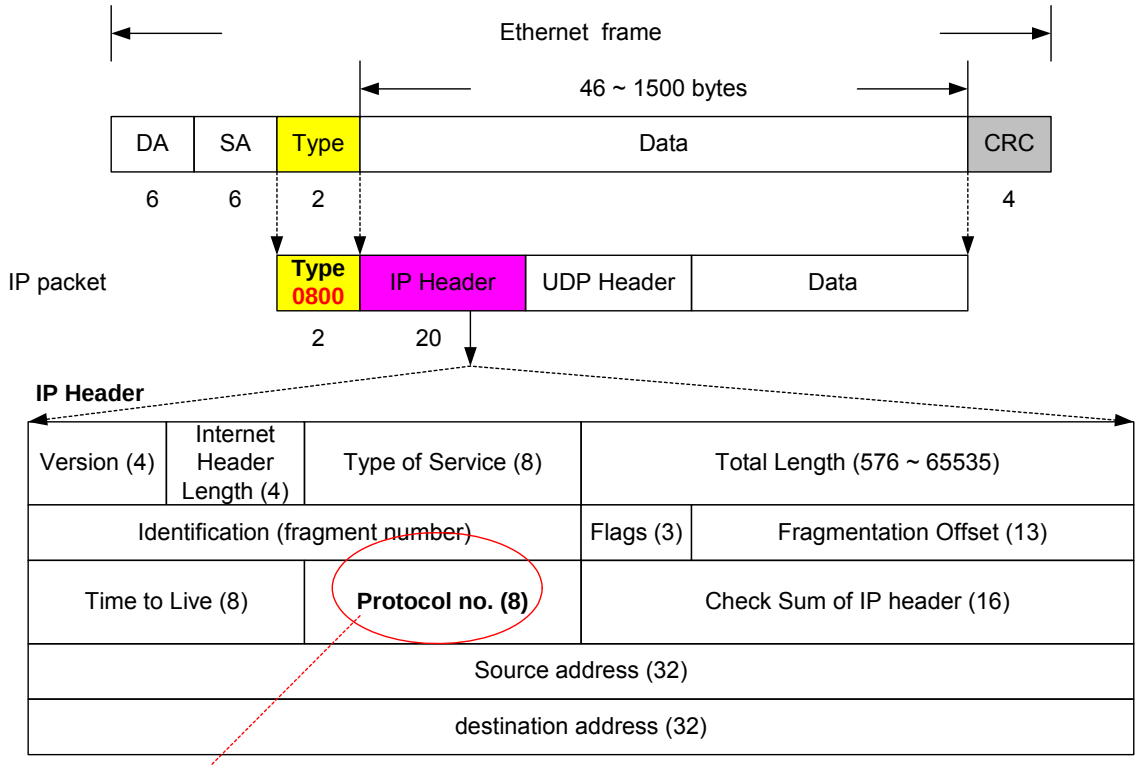


GVRP, GMRP



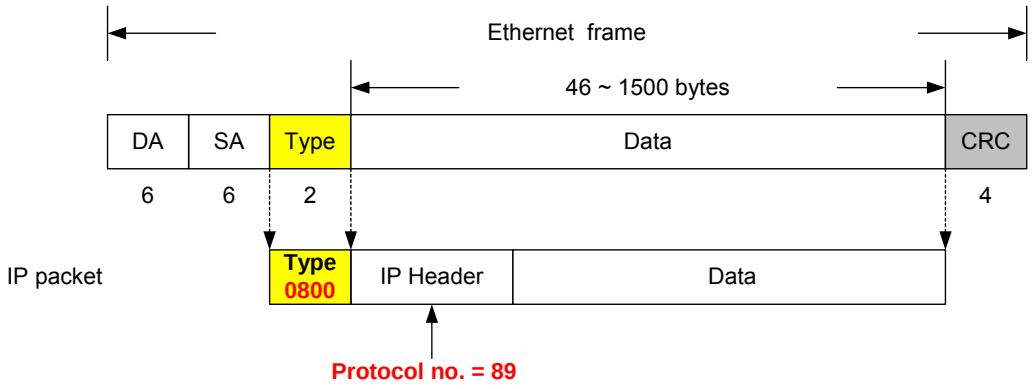
4.12.4 Frame format of ICMP, IGMP, TCP, UDP, OSPF

ICMP, IGMP, TCP, UDP



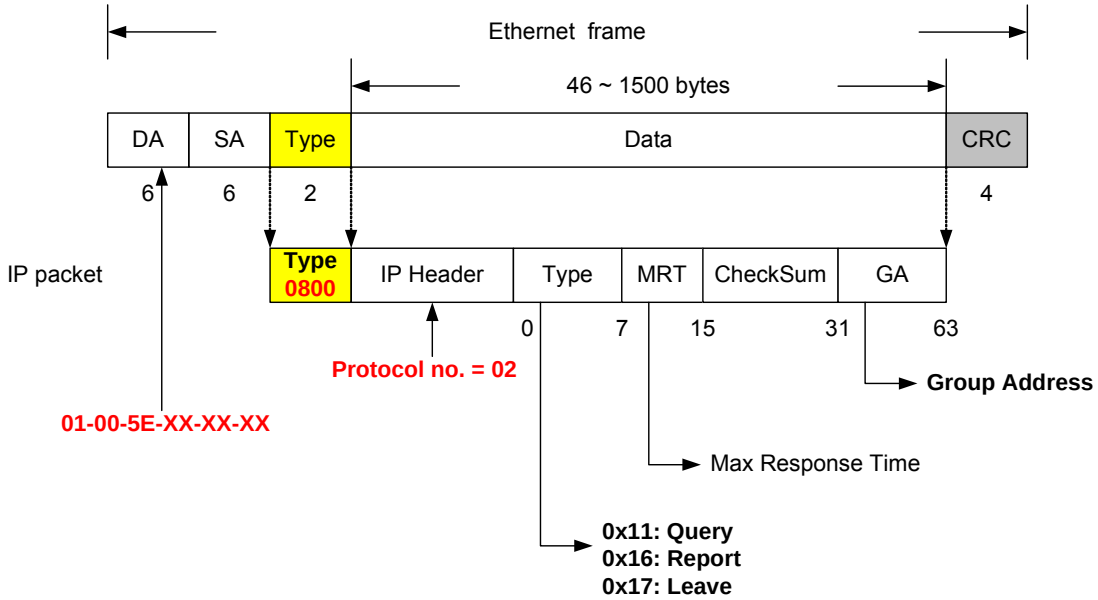
Protocol no.	Name
1	ICMP (Internet Control Message Protocol)
2	IGMP (Internet Group Management Protocol)
6	TCP (transmission Control Protocol)
17	UDP (User Datagram Protocol)

OSPF (Open Shortest Path First)



4.12.5 Frame format of IGMP

IGMP version 2 frame format



5 Register Map

In the followong table, R, W and R/W denote “Read”, “ Write” and “Read or Write” respectively.

5.1 MAC Control Register (00h~3Ah)

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
01H	02H 03H	General MAC operation behavior Bit[0] : IPG compensation 0: Disable; 1: Enable Bit[1] : broadcast all control packets whose destination MAC address equals to 01-80-C2-00-00-04 ~ 01-80-C2-00-00-0F. For control packet with DA 01-80-C2-00-00-00, please refer to register 02h[1]. 0: Disable; 1: Enable Bit[2] : Back pressure method 0: Collision base; 1: Carrier Sense base Bit[3] : Collision 16 times drop 0: Disable; 1: Enable Bit[4] : Collision back off 0: Disable; 1: Enable Bit[5] : High/Low bandwidth throttle selection 0: 32 kbps/ unit for (p0 ~ p25, CPU port) 1: 256 kbps/ unit for (p0~p23, CPU port) 2048 kbps/ unit for (p24, p25) Please refer to register 03h~1Dh for more detailed information. Bit[6] : Auto turn off flow control function if priority queue defined in register 22h~27h, 33h ~ 35h is enabled. 0: Disable; 1: Enable Bit[7] : TCP/UDP destination port number based priority. 0: Drop packet; 1: Forward to CPU-port. This setting is invalid for port 24 and port 25 when they are working in Gigabit mode. This bit affects register 33h, 34h and 35h. Bit[8] : TCP/UDP port number based packet to low priority. 0: Disable; 1: Enable A packet with TCP/UDP port number defined as low priority in register 33h~35h will be treated as a low priority packet; regardless of port based/ tag based/ IP based priority setting, meaning that it overwrites other settings. Bit[9] : Port statistic counter method Please refer to register 39h for more detailed information.	R/W	11'h12

<table>
<tr><th>Reg Addr.</th><th>ROM Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td></td><td></td><td>Bit[10] : Port statistic counter enable
0: Disable; 1: Enable

Bit[11]: Reserved Multicast Address handling. This bit defines the handling method for the destination MAC address “0180C2xxxxxx”.
0: Handling method 0; 1: Handling method 1.

Bit[12]: LLDP handling method.
0: Drop; 1: Forward to CPU port</td><td></td><td></td></tr>
<tr><td>02H</td><td>04H
05H</td><td>Ethernet protocol frames capture
Bit[0] : In-band management
1: Forward the packet to CPU port, if its destination MAC address (DA) equals switch’s MAC address.
0: Drop the packet, if its DA equals switch’s MAC address
IP1826D’s MAC address is defined in register 28h, 29h and 2Ah.

Bit[1] : Spanning tree (This bit is valid only if 01h[1] is set to 0)
0: Drop; 1: Forward to CPU port
This bit also defines the way in which the switch handle packet with DA 0x0180c2000000.

Bit[2] : 802.1x protocol enable
0: Drop; 1: Forward to CPU port
This bit is effective only if the corresponding bit of register 2Bh and register 2Bh is set to “1”.
<table>
<tr><td>02h[2]</td><td>2Bh & 2Ch</td><td>The method for handling EAPOL packet</td></tr>
<tr><td>1</td><td>1</td><td>Forward to CPU only</td></tr>
<tr><td>0</td><td>1</td><td>Drop</td></tr>
<tr><td>0</td><td>0</td><td>Broadcast</td></tr>
</table>
Please refer to the description of register 2Bh and register 2Ch.

Bit[3] : LACP
0: Drop; 1: Send to port 26 (CPU) only

Bit[4] : GxRP
0: Broadcast; 1: Send to port 26 (CPU) only

Bit[5] : ARP
0: Forward according to DA; 1: Forward to DA and CPU port

IP packet capture
Bit[7:6] : ICMP
Bit[9:8] : TCP
Bit[11:10] : UDP</td><td>R/W</td><td>16'd1</td></tr>
</table>

<table>
<tr><th>Reg Addr.</th><th>ROM Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td></td><td></td><td>Bit[13:12] : OSPF
Bit[15:14] : IPv4 Other protocol,
00: Forward a packet according to its DA.
01: Not only forward the packet according to its DA, but also forward a packet to port 26 (CPU).
10: Forward packets to port 26 (CPU) only;
11: Drop</td><td></td><td></td></tr>
<tr><td>03H-1AH</td><td>06H – 35H</td><td>Egress/Ingress Rate control for port 0~port 23

Port 0 Egress/Ingress Rate. 0x00 denotes full speed.
<table>
<tr><td>01h.5</td><td>Egress Rate</td><td>Ingress Rate</td></tr>
<tr><td>0</td><td>03h[7:0] x 32 kbps</td><td>03h[15:8] x 32 kbps</td></tr>
<tr><td>1</td><td>03h[7:0] x 256 kbps.</td><td>03h[15:8] x 256 kbps</td></tr>
</table>
Register 03h~1Ah correspond to port 0~23.</td><td>R/W</td><td>16'h0000</td></tr>
<tr><td>1BH-1CH</td><td>36H – 39H</td><td>Egress/Ingress Rate control for port 24 ~ 25.

Port 24, Port 25 Egress/Ingress Rate. 0x00 denotes full speed.
<table>
<tr><td>1Bh[7:0]</td><td>01h.5</td><td>Egress Rate</td><td>Ingress Rate</td></tr>
<tr><td>Value=1~255</td><td>0</td><td>1Bh[7:0] x 32 kbps</td><td>1Bh[15:8] x 32 kbps</td></tr>
<tr><td>Value=1~255</td><td>1</td><td>1Bh[7:0] x 2048 kbps</td><td>1Bh[15:8] x 2048 kbps</td></tr>
</table></td><td>R/W</td><td>16'h0000</td></tr>
<tr><td>1DH</td><td>3AH – 3BH</td><td>Egress/Ingress Rate control for port 26 (CPU port). 0x00 denotes full speed.

Port 26 Egress/Ingress Rate
<table>
<tr><td>01h.5</td><td>Egress Rate</td><td>Ingress Rate</td></tr>
<tr><td>0</td><td>03h[7:0] x 32 kbps</td><td>03h[15:8] x 32 kbps</td></tr>
<tr><td>1</td><td>03h[7:0] x 256 kbps</td><td>03h[15:8] x 256 kbps</td></tr>
</table></td><td>R/W</td><td>16'h0000</td></tr>
<tr><td>1EH</td><td>3CH 3DH</td><td>Port receive enable for port15~port0, 1 bit per port
Bit[15:0] : 0: Disable; 1: Enable</td><td>R/W</td><td>16'hffff</td></tr>
<tr><td>1FH</td><td>3EH 3FH</td><td>Port receive enable for port26~pot16, 1 bit per port
Bit[10:0] : 0: Disable; 1: Enable</td><td>R/W</td><td>11'h7ff</td></tr>
<tr><td>20H</td><td>40H 41H</td><td>Reserved. Keep the default setting.</td><td>R/W</td><td>16'hffff (SC)</td></tr>
<tr><td>21H</td><td>42H</td><td>Reserved. Keep the default setting.</td><td>R/W</td><td>11'hffff</td></tr>
</table>

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
	43H			(SC)
22H	44H 45H	Port base priority enable for port15~port0, 1 bit per port Bit[15:0] : 0: Disable; 1: Enable	R/W	16'h0000
23H	46H 47H	Port base priority enable for port26~port16, 1 bit per port Bit[10:0] : 0: Disable; 1: Enable	R/W	11'h0
24H	48H 49H	VLAN Tag base priority enable for port15~port0, 1 bit per port Bit[15:0] : 0: Disable; 1: Enable	R/W	16'h0
25H	4AH 4BH	VLAN Tag base priority enable for port26~port16, 1 bit per port Bit[10:0] : 0: Disable; 1:Enable	R/W	11'h0
26H	4CH 4DH	IP CoS base priority enable for port15~port0, 1 bit per port Bit[15:0] : 0: Disable; 1: Enable	R/W	16'h0
27H	4EH 4FH	IP CoS base priority enable for port26~port16, 1 bit per port Bit[10:0] : 0: Disable; 1: Enable	R/W	11'h0
28H	50H 51H	Switch's MAC address[15:0]	R/W	16'h0001
29H	52H 53H	Switch's MAC address[31:16]	R/W	16'hc300
2AH	54H 55H	Switch's MAC address[47:32]	R/W	16'h0090
2BH	56H 57H	Port 802.1x port locking (port 0 ~ port 15) Bit[15:0]: 0: Normal operation (Disable port lock) 1: Enable port locking. (ARP & 802.1x EAPOL packet will be forwarded to port 26). Please refer to register 02h[2].	R/W	16'd0
2CH	58H 59H	Port 802.1x port locking (port16 ~ port 25) Bit[9:0]: 0: Normal operation (Disable port-locking) 1: Enable port locking (ARP & 802.1x EAPOL packet will be forwarded to port 26). Please refer to register 02h[2].	R/W	10'd0
2DH	5AH 5BH	Designer-defined TCP/UDP port number mask Bit[15:8] : mask for bit[7:0] of TCP/UDP port numer B defined in register 30H. Bit[7:0] : mask for bit[7:0] of TCP/UDP port number A defined in register 2FH. 0: the corresponding TCP/UDP port number bit will be checked 1: the corresponding TCP/UDP port number bit will not be checked	R/W	16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
2EH	5CH 5DH	Designer-defined TCP/UDP port number mask Bit[15:8] : mask for bit[7:0] of TCP/UDP port number D defined in register 32H. Bit[7:0] : mask for bit[7:0] of TCP/UDP port number C defined in register 31H. 0: the corresponding TCP/UDP port number bit will be checked 1: the corresponding TCP/UDP port number bit will not be checked	R/W	16'h0000
2FH	5EH 5FH	Designer-defined TCP/UDP port number A	R/W	16'h0000
30H	60H 61H	Designer-defined TCP/UDP port number B	R/W	16'h0000
31H	62H 63H	Designer-defined TCP/UDP port number C	R/W	16'h0000
32H	64H 65H	Designer-defined TCP/UDP port number D	R/W	16'h0000
33H	66H 67H	TCP/UDP port number based priority setting: Bit[1:0] : FTP (20,21) Bit[3:2] : SSH (22) Bit[5:4] : TELNET (23) Bit[7:6] : SMTP (25) Bit[9:8] : DNS (53) Bit[11:10] :TFTP (69) Bit[13:12] :HTTP_0,1 (80, 8080) Bit[15:14] :POP3 (110) Please refer to register 01h bit 7 for the setting of “01”: drop/forward to CPU. 00: Disable 01: Drop /Forward to CPU 10: Low priority 11: High priority	R/W	16'h0000
34H	68H 69H	TCP/UDP port number based priority setting: Bit[1:0] : NEWS (119) Bit[3:2] : SNTP (123) Bit[5:4] : NETBIOS0,1,2 (137,138,139) Bit[7:6] : IMAP_0,1 (143,220) Bit[9:8] : SNMP_0,1 (161,162) Bit[11:10] :HTTPS (443) Bit[13:12] : Port number 1863 Bit[15:14] :XP_RDP (3389) Please refer to register 01h bit 7 for the setting of “01”: drop/forward to CPU. 00: Disable 01: Drop /Forward to CPU 10: Low priority 11: High priority	R/W	16’h0000

Reg Addr.	ROM Addr.	Register Description		R/W	Default value
35H	6AH 6BH	TCP/UDP port number based priority setting: Bit[1:0] : Port number 4000,8000 Bit[3:2] : Port number 5190 Bit[5:4] : Port number 5050 Bit[7:6] : BOOTP/DHCP (67,68) Bit[9:8] : TCP/UDP port defined in register 2FH. Bit[11:10] : TCP/UDP port defined in register 30H. Bit[13:12] : TCP/UDP port defined in register 31H. Bit[15:14] : TCP/UDP port defined in register 32H. Please refer to register 2Fh~ 32h for the setting of Bit[15:8]. Please refer to register 01h bit 7 for the setting of “01” drop/forward to CPU.	00: Disable 01: Drop /Forward to CPU 10: Low priority 11: High priority	R/W	16’h0000

<table>
<tr><th>Reg Addr.</th><th>ROM Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td>36H</td><td>6CH
6DH</td><td>TCP/UDP port number based filter select:

<table>
<tr><td>Bit[0]</td><td>FTP</td><td>0: Don't care the protocol,
1: Select the protocol (forward or drop.
Please refer to register 37h[8])</td></tr>
<tr><td>Bit[1]</td><td>SSH</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[2]</td><td>TELNET</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[3]</td><td>SMTP</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[4]</td><td>DNS</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[5]</td><td>TFTP</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[6]</td><td>HTTP_0,1</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[7]</td><td>POP3</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[8]</td><td>NEWS</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[9]</td><td>SNTP</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[10]</td><td>NETBIOS0, 1, 2</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[11]</td><td>IMAP_0,1</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[12]</td><td>SNMP_0,1</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[13]</td><td>HTTPS</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[14]</td><td>Port number 1863</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[15]</td><td>XP_RDP</td><td>0: Don't care, 1: Select</td></tr>
</table>
</td><td>R/W</td><td>16'h0000</td></tr>
</table>

<table>
<tr><th>Reg Addr.</th><th>ROM Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td>37H</td><td>6EH
6FH</td><td>TCP/UDP port number based filter select:
<table>
<tr><td>Bit[0]</td><td>Port number 4000, 8000</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[1]</td><td>Port number 5190</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[2]</td><td>Port number 5050</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[3]</td><td>BOOP/DHCP</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[4]</td><td>Designer-defnied TCP/UDP port A</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[5]</td><td>Designer-defnied TCP/UDP port B</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[6]</td><td>Designer-defined TCP/UDP port C</td><td>0: Don't care, 1: Select</td></tr>
<tr><td>Bit[7]</td><td>Designer-defined TCP/UDP port D</td><td>0: Don't care, 1: Select</td></tr>
</table>
Bit[8]: filtering mode
0: negative list. Drops the protocol selected in Reg 36H [15:0] and Reg 37H[7:0] and forwards the other protocol.
1: positive list. Forwards the protocol selected in Reg 36H [15:0] and Reg 37H[7:0] and drops the other protocol.
It is valid only if 37h[9] is set to 1.

Bit[9]: filter function
1: Enable (Configurations in register 36h and 37h take effect)
0: Disable (Register settings of 36h and 37h are all disabled)
(Bit[9:8]: Ref to offset address 0xF4h, 0xF5h)</td><td>R/W</td><td>10'h0000</td></tr>
</table>

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
38H	70H 71H	CPU Read statistic counter command [5:0]: statistic counter read address [6]: statistic counter data updating stop 0: update; 1: stop updating [7]: statistic counter 0: Keep the original value; 1: Clear [8]: command enable for read & reset 0: Disable; 1: Enable	W/ [8] SC	9'h000
39H	72H 73H	CPU Read high 16 bits statistic counter data	R	16'h0000
3AH	74H 75H	CPU Read low 16 bits statistic counter data	R	16'h0000

5.2 Queue Control Register (3Bh~3Fh)

<table>
<tr><th>Reg Addr.</th><th>ROM Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td>3BH</td><td>76H
77H</td><td>Port statistic counter selection (port 0 ~ port 15)
Register 01h[9]= (Port statistic counter method)

<table>
<tr><td></td><td colspan="2">The functions of counters</td></tr>
<tr><td>01h[9], 3Bh[x]</td><td>Counter 2</td><td>Counter 1</td></tr>
<tr><td>0,0</td><td>Receive packet count</td><td>Transmit packet count</td></tr>
<tr><td>0,1</td><td>Transmit packet count</td><td>Collision count</td></tr>
<tr><td>1,0</td><td>Receive packet count</td><td>Drop packet count (MAC)</td></tr>
<tr><td>1,1</td><td>Receive packet count</td><td>CRC error packet count</td></tr>
</table>

<table>
<tr><td>38h[5:0] counter address</td><td>Counter to be accessed</td></tr>
<tr><td>6’b000000 (0)</td><td>Port 0 counter 1</td></tr>
<tr><td>6’b000001 (1)</td><td>Port 0 counter 2</td></tr>
<tr><td>6’b000010 (2)</td><td>Port 1 counter 1</td></tr>
<tr><td>6’b000011 (3)</td><td>Port 1 counter 2</td></tr>
<tr><td>…….</td><td>…….</td></tr>
<tr><td>6’b101110 (46)</td><td>Port 23 counter 1</td></tr>
<tr><td>6’b101111 (47)</td><td>Port 23 counter 2</td></tr>
<tr><td>6’b110000 (48)</td><td>Port 26 counter 1</td></tr>
<tr><td>6’b110001(49)</td><td>Port 26 counter 2</td></tr>
<tr><td>6’b110010 (50)</td><td>Port 24 counter 1</td></tr>
<tr><td>6’b110011 (51)</td><td>Port 24 counter 2</td></tr>
<tr><td>6’b110100 (52)</td><td>Port 25 counter 1</td></tr>
<tr><td>6’b110101(53)</td><td>Port 25 counter 2</td></tr>
</table>
</td><td>R/W</td><td>16'h0000</td></tr>
<tr><td>3CH</td><td>78H
79H</td><td>Port statistic counter selection (port 16 ~ port 26)</td><td>R/W</td><td>11'h0000</td></tr>
</table>

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
3DH	7AH 7BH	Out queue schedule mode / weight selection Bit[1:0]: Schedule mode 00: First-in First-out 01: Strict Priority. If this mode is enabled, IP1826D will forward all packets in high priority queue before forwarding low priority queue. 10: Weight-and-roundrobin. If this mode is enabled, IP1826D will forward the packet count defined in Bit[4:2] and then the packet count defined in Bit[7:5]. The procedure is repeated alternatively. 11: undefined Bit[4:2] : Low priority queue weight number when in WRR mode Bit[7:5] : High priority queue weight number when in WRR mode Bit[13:8] : Out queue aging time = (1~2) x value of Bit[13:8]x 100 ms Bit[14] : Reserved Bit[15] : Out queue aging 0: Disable 1: Enable	R/W	16'h0000
3EH	7CH 7DH	Reserved. Keep the default setting.	R/W	16'h8168
3FH	7EH 7FH	Reserved. Keep the default setting.	R/W	16'h8187

5.3 Address Resolution Logic Register (40h~E8h)

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
40H	80H 81H	MAC address entry operation Bit[0] : Hash algorithm selection 0: Based on CRC algorithm. The calculation result points to the table address. 1: Based on direct mapping. The lowest 12-bit of MAC address points to the table address. Bit[1] : Address table aging function 0: Enable; 1: Disable Bit[3:2] : Trunk hash algorithm selection 2'b00: The least significant 2 bits of the source port ID plus 2. **Note:** The source port ID is counted from 0 to 25. 2'b01: The least significant 2 bits of the source MAC address. 2'b10: The least significant 2 bits of the destination MAC address. 2'b11: The logic operation result of SA (least significant 2 bits) XOR DA (least significant 2 bits). Bit[4]: Block broadcast frames to CPU port 0: Forward; 1: Block Bit[5]: Forward all broadcast IPv4 packet to CPU when blocking broadcast frame to CPU (40h[5])=1). 0: Block; 1: Forward Bit[6]: VLAN type 0: port base VLAN; 1: 802.1Q tag based VLAN Bit[7]: uni-cast packet stride across VLAN 0: Disable; 1: Enable Bit[8]: Forward the packet to VLAN uplink port 0: Disable; 1: Enable The uplink ports are defined in register 4Ah and 4Bh. Bit[10:9]: Prot mirroring method 00: Disable; 01: egress; 10: ingress; 11: egress / ingress Bit[11]: The CPU port can forward the packet to the destination port according to the special tag. 0: Disable this function; 1: Enable this function. Bit[12]: The CPU port can forward this packet to the destination port regardless of the VLAN function and port-trunking. This function works only if Register 40h[11] is set to “1”. 0: Disable this function; 1: Enable this function (This function only dispose of CPU sends packets to specific ports.)	R/W	11'h00

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
		Bit[13]: Tag handling Method for adding tag/removing tag if tag based VLAN is selected. 0: Based on physical port. Adding tag or removing tag is decided by register 5Ch ~5Fh ; 1: Based on VID and physical port. Adding tag or remove tag is decided by registers 80h ~ BFh. Bit[15:14]: Tag handling method and VLAN member These two bits defines the index of registers 80h ~ BFh. Please refer to the description of registers 80h ~ BFh.		

<table>
<tr><th>Reg Addr.</th><th>ROM Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td>41H</td><td>82H
83H</td><td>Source/Destination IP address security setting

Bit[1:0]: IP address filter mode configuration
The switch engine compares IP address of the incoming packet with the content of LUT and decides whether or not to forward.
<table>
<tr><th>Filerting
Bit[1:0]</th><th>IP address</th><th>Source port</th><th>Rules</th></tr>
<tr><td>00</td><td>Mismatch</td><td>Don’t care</td><td>Forward</td></tr>
<tr><td>01</td><td>Match</td><td>Don’t care</td><td>Forward</td></tr>
<tr><td>10</td><td>Match</td><td>Match</td><td>Forward</td></tr>
<tr><td>11</td><td>Match</td><td>Mismatch</td><td>Forward</td></tr>
</table>
Bit[2] : IP address filtering type
0: the IP address in LUT will base on hashing result. 32 bits IP address should match exactly.
1: the IP address in LUT will base on the source port.
For example, Packets from port 0 will be compared with IP address in LUT address 12'h0. Packets from port 1 will be compared with IP address in LUT address 12'h1. Packets from port 2 will be compared with IP address in LUT address 12'h2,
……
Packets from port 25will be compared with IP address in LUT address 12'h1A
In this mode, only the incoming packet with IP address [31:8] will be compared with the LUT and IP address [7:0] will be masked
Bit[3] : Source/ Destination IP selection
0: Source IP; 1: Destination IP
Bit[5:4]: To avoid the LUT address collision, an offset is added to the LUT address after the calculation of hashing algorithm.
00: none; 01: add 1; 10: add 2; 11: add 3
Bit[6] : Enable IP address shifting in LUT
0: Do not shift 1:Shift

Bit[7] : IP address filter function enable
0: Disable; 1: Enable</td><td>R/W</td><td>8'h00</td></tr>
</table>

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
42H	84H 85H	Broadcast storm control setting (p15 ~ p0) Bit[15:0]: broadcast storm control 1: Enable; 0: Disable	R/W	16'h0000
43H	86H 87H	Broadcast storm control setting (p26 ~ p16) Bit[15:0]: broadcast storm control 1: Enable; 0: Disable	R/W	11'h0000
44H	88H 89H	Aging timer and broadcast storm threshold setting Bit[9:0] : Aging timer, the aging time is about : (mg_aging_time + 1) x 55.3 sec. 3.8% Bit[15:10] : Broadcast storm control threshold The number of broadcast frames allowed in one period 1000M : 50 us 100M : 500 us 10M : 5 ms	R/W	16'hFC05
45H	8AH 8BH	Enable Source MAC address learning function port 15 ~ port 0 Bit[15:0] : 0: Disable learning 1: Enable learning	R/W	16'hffff
46H	8CH 8DH	Enable Source MAC address learning function port 26 ~ port 16 Bit[10:0] : 0: Disable learning 1: Enable learning	R/W	11'h7ff
47H	8EH 8FH	Enable data packets handling for port15~port0 Bit[15:0] : 0: Disable data packet receiving / forwarding, except control packets such as BPDU. 1: Enable data packet receiving / forwarding	R/W	16'hffff
48H	90H 91H	Enable data packets handling for port26~port16 Bit[10:0] : 0: Disable data packet receiving / forwarding, except control packets such as BPDU. 1: Enable data packet receiving / forwarding	R/W	11'h7ff
49H	92H 93H	Security configuration Bit[0]: unknown SA packet to CPU port 0: forward; 1: not forward Bit[1]: forward unknown SA packet if source address learning function is disable 0: Drop the unknown SA packet 1: forward the unknown SA packet	R/W	2'b10

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
4AH	94H 95H	VLAN uplink function support Bit[15:0] : uplink port configuration 0: normal port 1: uplink port Please refer to register 40h bit 8 for more detail information.	R/W	16'h00
4BH	96H 97H	VLAN uplink function support Bit[10:0] : uplink port configuration 0: normal port 1: uplink port	R/W	11'h00
4CH	98H 99H	Trunk group setting P00 ~ p03 are the same trunk group and can be any combination. bit [3:0] : trunk configuration for port 0 4'b0000: the port is not in the trunk 4'bxxx1: pass the packet with ID = 0 4'bxx1x: pass the packet with ID = 1 4'bx1xx: pass the packet with ID = 2 4'b1xxx: pass the packet with ID = 3 Bit[7:4] : trunk configuration for port 01 Bit[11:8] : trunk configuration for port 02 Bit[15:12] : trunk configuration for port 03 ID is the trunk hashing result using the algorithm selected by register 40h[3:2]. Note: In a trunk group, the configuration should be ORed to 4'b1111 and no more than one port has the same configuration bit	R/W	16'h00
4DH	9AH 9BH	Trunk group setting P04 ~ p07 are the same trunk group and can be any combination. bit [3:0] : trunk configuration for port 4 4'b0000: the port is not in the trunk 4'bxxx1: pass the packet with ID = 0 4'bxx1x: pass the packet with ID = 1 4'bx1xx: pass the packet with ID = 2 4'b1xxx: pass the packet with ID = 3 Bit[7:4] : trunk configuration for port 05 Bit[11:8] : trunk configuration for port 06 Bit[15:12] : trunk configuration for port 07 Note: In a trunk group, the configuration should be ORed to 4'b1111 and no more than one port has the same configuration bit	R/W	16'h00

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
4EH	9CH 9DH	Trunk group 2 (p25, p24) setting Port 24 ~port 25 are the same trunk group Bit[3:0] : trunk configuration for port 24 Bit[7:4] : trunk configuration for port 25 **Note:** In a trunk group, the configuration should be Oared to 4'b1111 and no more than one port has the same configuration bit	R/W	8'h00
4FH	9EH 9FH	Port mirroring function configuration bit [15:0] : mirrored(source) port configuration. Port 15~port 0 0: This port is not mirrored 1: This port is mirrored	R/W	16'h00
50H	A0H A1H	Port mirroring function configuration bit [10:0] : mirrored(source) port configuration. Port 26~port 16 0: This port is not mirrored 1: This port is mirrored	R/W	11'h00
51H	A2H A3H	Port mirroring function configuration bit [15:0] : the mirroring(destination) port. Port 15~port 0	R/W	16'h00
52H	A4H A5H	Port mirroring function configuration bit [10:0] : the mirroring(destination) port. Port 26~port 16	R/W	11'h00
53H	A6H A7H	PVID pointer setting for p0 ~ p2 bit [4:0] : PVID configuration for port 0 bit [9:5] : PVID configuration for port 1 bit [14:10] : PVID configuration for port 2	R/W	15'h0820
54H	A8H A9H	PVID pointer setting for p3~ p5 bit [4:0] : PVID configuration for port 3 bit [9:5] : PVID configuration for port 4 bit [14:10] : PVID configuration for port 5	R/W	16'h1483
55H	AAH ABH	PVID pointer setting for p6 ~ p8 bit [4:0] : PVID configuration for port 6 bit [9:5] : PVID configuration for port 7 bit [14:10] : PVID configuration for port 8	R/W	16'h20E6
56H	ACH ADH	PVID pointer setting for p9 ~ p11 bit [4:0] : PVID configuration for port 9 bit [9:5] : PVID configuration for port 10 bit [14:10] : PVID configuration for port 11	R/W	16'h2D49
57H	AEH AFH	PVID pointer setting for p12~ p14 bit [4:0] : PVID configuration for port 12 bit [9:5] : PVID configuration for port 13 bit [14:10] : PVID configuration for port 14	R/W	16'h39AC

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
58H	B0H B1H	PVID pointer setting for p15~ p17 bit [4:0] : PVID configuration for port 15 bit [9:5] : PVID configuration for port 16 bit [14:10] : PVID configuration for port 17	R/W	16'h460F
59H	B2H B3H	PVID pointer setting for p18 ~ p20 bit [4:0] : PVID configuration for port 18 bit [9:5] : PVID configuration for port 19 bit [14:10] : PVID configuration for port 20	R/W	16'h5272
5AH	B4H B5H	PVID pointer setting for p21 ~ p23 bit [4:0] : PVID configuration for port 21 bit [9:5] : PVID configuration for port 22 bit [14:10] : PVID configuration for port 23	R/W	16'h5ED5
5BH	B6H B7H	PVID pointer setting for p24 ~ p26 bit [4:0] : PVID configuration for port 24 bit [9:5] : PVID configuration for port 25 bit [14:10] : PVID configuration for port 26	R/W	16'h6B38
5CH	B8H B9H	VLAN output port add tag bit [15:0] : output packet add tag port 15~port 0 0: Disable; 1: add VLAN tag to output packet	R/W	16h0000
5DH	BAH BBH	VLAN output port add tag bit [10:0] : output packet add tag port 26~port 16 0: Disable; 1: add VLAN tag to output packet	R/W	11h0000
5EH	BCH BDH	VLAN output port remove tag bit [15:0] : output packet remove tag port 15~port 0 0: Disable; 1: remove VLAN tag of output packet	R/W	16h0000
5FH	BEH BFH	VLAN output port remove tag bit [10:0] : output packet remove tag port 26~port 16 0: Disable; 1: remove VLAN tag of output packet	R/W	13h0000
60H~ 7AH	C0H F5H	VID configuration for VLAN table entry 0 ~ 26 bit [11:0] : VID configuration	R/W	12'h001~ 1B
7BH~ 7FH	F6H FFH	VID configuration for VLAN table entry 27 ~ 31 bit [11:0] : VID configuration	R/W	12'h000

<table>
<tr><th>Reg Addr.</th><th>ROM Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td>80H</td><td>100H
101H</td><td>This register contains 3 functions. Before accessing to these 3 different registers block, the designer should define the index of these regisetrs by setting register 40h[15:14] to “00”, “01” or “10”, The default values upon reset for these 3 blocks are different.

<table>
<tr><td>Register 40H[15:14]</td><td>2’b00</td></tr>
<tr><td>Description</td><td>Port based or 802.1Q tag based VLAN member for VLAN entry 0. Bit 0 corresponds to port 0. Bit 15 corresponds to port 15 and so forth.

0: Non-member of VLAN entry 0.
1: The member of VLAN entry 0.

If a packet contains a VID identical to the VID of entry 0, it will be forwarded to the destination port as the definition of VLAN table. If there is no match for VID, the IP1826D drops this packet.</td></tr>
</table>

<table>
<tr><td>Register 40H[15:14]</td><td>2’b01(Adding tag)</td><td>2’b10(Removing tag)</td></tr>
<tr><td>Description</td><td>0: Keep the original ingress packet
1: Add the tag to the ingress packet.</td><td>0: Keep the original ingress packet.

1: Remove the tag from the ingress packet.</td></tr>
<tr><td></td><td colspan="2">This register defines the 802.1Q tag handling method for VLAN entry 0.
Bit 0 corresponds to port 0. Bit 15 corresponds to port 15 and so forth. For each destination port, adding a tag to a packet is effective under the following conditions.
(a) The ingress packet contains no tag.
(b) The ingress packet contains a VID “0”.
In both cases the PVID of the ingress port is inserted to the ingress packet, and then the packet is forwarded to the destination port. The PVID/VID will be kept only if “adding tag” function of the corresponding port is set to “1”.
If the ingress packet contains a VID, the “adding tag” function has no effect. .

At the egress port, the tag will be removed, if the “removing tag” function of the corresponding port is set to”1”.</td></tr>
</table>
</td><td>R/W</td><td>16’hFFFF for VLAN member table.

16’h0 for tagging/ untagging function</td></tr>
</table>

<table>
<tr><th>Reg Addr.</th><th>ROM Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td>81H</td><td>102H
103H</td><td>This register contains 3 functions. Before accessing to these 3 different registers block, the designer should define the index of these regisetrs by setting register 40h[15:14] to “00”, “01” or “10”,

<table>
<tr><td>Register 40H[15:14]</td><td>2’b00</td></tr>
<tr><td>Description</td><td>Port based or 802.1Q tag based VLAN member for VLAN entry 0. Bit 0 corresponds to port 16. Bit 10 corresponds to port 26 and so forth.

0: Non-member of VLAN entry 0.
1: The member of VLAN entry 0.

If a packet contains a VID identical to the VID of entry 0, it will be forwarded to the destination port as the definition of VLAN table. If there is no match for VID, the IP1826D drops this packet.</td></tr>
</table>

<table>
<tr><td>Register 40H[15:14]</td><td>2’b01(adding tag)</td><td>2’b10(removing tag)</td></tr>
<tr><td>Description</td><td>0: Keep the original ingress packet.

1: Add the tag to the ingress packet.</td><td>0: Keep the original ingress packet.

1: Remove the tag from the ingress packet.</td></tr>
<tr><td colspan="2">This register defines the 802.1Q tag handling method for VLAN entry 0.
Bit 0 corresponds to port 16. Bit 10 corresponds to port 26 and so forth. For each port, adding a tag to a packet is effective under the following conditions.
(a) The ingress packet contains no tag.
(b) The ingress packet contains a VID “0”.
In both cases the PVID of the ingress port is inserted to the ingress packet, and then the packet is forwarded to the destination port. The PVID/VID will be kept only if “adding tag” function of the corresponding port is set to “1”.
If the ingress packet contains a VID, the “adding tag” function has no effect. .

At the egress port, the tag will be removed, if the “removing tag” function of the corresponding port is set to”1”.</td></tr>
</table>
</td><td>R/W</td><td>11’h7FF for VLAN member table.

11’h0 for tagging/ untagging function</td></tr>
</table>

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
82H ~ B5H	104H ~ 16BH	Similar to register 80H and register 81H, the function of these registers corresponds to tag/port based VLAN entry 1 ~ tag/port based VLAN entry 26. Two reg6isters correspond to one VLAN entry.	R/W	16'hFFFF or 11'h7FF for VLAN member table. 16'h0 or 11'h7FF0 for tagging/ untagging function

<table>
<tr><th>Reg Addr.</th><th>ROM Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td>B6H</td><td>16CH
~
16DH</td><td>This register contains 3 functions. Before accessing to these 3 different registers block, the designer should define the index of these regiseters by setting register 40h[15:14] to “00”, “01” or “10”,

<table>
<tr><td>Register 40H[15:14]</td><td>2’b00</td></tr>
<tr><td>Description</td><td>802.1Q tag based VLAN member for VLAN entry 27. Bit 0 corresponds to port 0. Bit 15 corresponds to port 15 and so forth.

0: Non-member of VLAN entry 27.
1: The member of VLAN entry 27.

If a packet contains a VID identical to the VID of entry 27, it will be forwarded to the destination port as the definition of VLAN table. If there is no match for VID, the IP1826D drops this packet.</td></tr>
</table>

<table>
<tr><td>Register 40H[15:14]</td><td>2’b01(adding tag)</td><td>2’b10(removing tag)</td></tr>
<tr><td>Description</td><td>0: Keep the original ingress packet.

1: Add the tag to the ingress packet.</td><td>0: Keep the original ingress packet.

1: Remove the tag from the ingress packet.</td></tr>
<tr><td colspan="3">This register defines the 802.1Q tag handling method for VLAN entry 27.
Bit 0 corresponds to port 0. Bit 15 corresponds to port 15 and so forth.

For each port, adding a tag to a packet is effective under the following conditions.
(a) The ingress packet contains no tag.
(b) The ingress packet contains a VID “0”.
In both cases the PVID of the ingress port is inserted to the ingress packet, and then the packet is forwarded to the destination port. The PVID/VID will be kept only if “adding tag” function of the corresponding port is set to “1”.
If the ingress packet contains a VID, the “adding tag” function has no effect. .

At the egress port, the tag will be removed, if the “removing tag” function of the corresponding port is set to”1”.</td></tr>
</table>
</td><td>R/W</td><td>16’hFFFF for VLAN member table.

16’h0 for tagging/ untagging function</td></tr>
</table>

<table>
<tr><th>Reg Addr.</th><th>ROM Addr.</th><th>Register Description</th><th>R/W</th><th>Default value</th></tr>
<tr><td>B7H</td><td>16EH
~
16FH</td><td>This register contains 3 functions. Before accessing to these 3 different registers block, the designer should define the index of these registers by setting register 40h[15:14] to “00”, “01” or “10”,

<table>
<tr><td>Register 40H[15:14]</td><td>2’b00</td></tr>
<tr><td>Description</td><td>802.1Q tag based VLAN member for VLAN entry 27. Bit 0 corresponds to port 16. Bit 10 corresponds to port 26 and so forth.
0: Non-member of VLAN entry 27.
1: The member of VLAN entry 27.

If a packet contains a VID identical to the VID of entry 27, it will be forwarded to the destination port as the definition of VLAN table. If there is no match for VID, the IP1826D drops this packet.</td></tr>
</table>

<table>
<tr><td>Register 40H[15:14]</td><td>2’b01(adding tag)</td><td>2’b10(removing tag)</td></tr>
<tr><td>Description</td><td>0: Keep the original ingress packet.

1: Add the tag to the ingress packet.</td><td>0: Keep the original ingress packet.

1: Remove the tag from the ingress packet.</td></tr>
<tr><td colspan="3">This register defines the 802.1Q tag handling method for VLAN entry 27.
Bit 0 corresponds to port 16. Bit 10 corresponds to port 26 and so forth.

For each port, adding a tag to a packet is effective under the following conditions.
(a) The ingress packet contains no tag.
(b) The ingress packet contains a VID “0”.
In both cases the PVID of the ingress port is inserted to the ingress packet, and then the packet is forwarded to the destination port. The PVID/VID will be kept only if “adding tag” function of the corresponding port is set to “1”.
If the ingress packet contains a VID, the “adding tag” function has no effect. .

At the egress port, the tag will be removed, if the “removing tag” function of the corresponding port is set to”1”.</td></tr>
</table>
</td><td>R/W</td><td>11’h7FF for VLAN member table.

11’h0 for tagging/ untagging function</td></tr>
</table>

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
B8H ~ BFH	170H ~ 17FH	Similar to register B6H and register B7H, the function of these registers corresponds to tag based VLAN entry 28 ~ tag based VLAN entry 31. Two registers correspond to one VLAN entry.	R/W	16'hFFFF or 11'h7FF for VLAN member table 16'h0 or 11'h0 for tagging/ untagging function

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
C0H	180H 181H	IGMP snooping function configuration Bit[0] : Enable IGMP snooping function 0: Disable; 1: Enable Bit[1]: Multicast group table is built by CPU(Report/Leave packet is forwarded to CPU). 1: Build group table by CPU; 0: Build group table by hardware; Bit[2]: packets with DA= 01:00:5E:00:00:XX 1: forwarded to group member if group table is valid / broadcast if group table is invalid 0: Broadcast Bit[3]: Report packet is also forwarded to IGMP host port (if bit 0 is set to “1” and bit 1 is set to “0”) 1: forwarded to host port and IGMP router ports; 0: forwarded to router ports only Bit[4]: Leave packet will be forwarded to IGMP router ports. (if bit 0 is set to “1” and bit 1 is set to “0”) 1: Forwarded to router ports; 0: Do not forward leave packet. Bit[5]: Router port list configured by CPU only 1: Configured by CPU only; 0: Configured by both hardware and CPU. Bit[6]: This function is used in hardware based IGMP snooping. 1: Ignore leave message; 0: Remove the corresponding port from the group table according to the leave message. Bit[7]: forward Multicast packets (Destination MAC address is Multicast MAC address & not IGMP packet) to CPU 1: Enable; 0:Disable. Bit[8]: Query packet will be forwarded to CPU when the group table is built by CPU. 1: Forwarded to CPU; 0: Broadcast. Bit[9]: Report packet will only be forwarded to CPU when the group table is built by CPU. 1: Forwarded to CPU; 0: Forwarded to CPU and router Port. Bit[10]: Keep this bit at “0”. **Note:** The multicast address mentioned above is in the range 01:00:5E:00:00:00 to 01:00:5E:00:07:FF:FF	R/W	11'h000
C1H	182H 183H	IGMP router port selection. Each bit corresponds to one port. Bit[0] corresponds to port 0 and bit[15] to port 15. 1: This port is selected as IGMP router port. 0: This port is a normal port.	R/W	16'h00

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
C2H	184H 185H	IGMP router port selection. Each bit corresponds to one port. Bit[0] corresponds to port 16. 1: This port is selected as IGMP router port. 0: This port is a normal port.	R/W	11'h00
C3H	186H 187H	CPU sends packets to specific ports, port 15~ port 0 Bit[15:0] : 0: packet from CPU will not send to this port 1: packet from CPU will send to this port	R/W	16'h00
C4H	188H 189H	CPU sends packets to specific ports, port 25~ port 16 Bit[9:0] : 0: packet from CPU will not forwarded to this port 1: packet from CPU will be forwarded to this port Bit[10] : 0: Destination ports of packet from CPU are forwarded according to LUT 1: Destination ports of packet from CPU are determined by register C3h and C4h[9:0] **Note:** Do not use this function in the following cases. Use VLAN instead. (a) Forward a BPDU to a specified port. (b) Forward a LACP to a specified port.	R/W	11'h00
C5H	18AH 18BH	CPU read/write address table configuration bit [11:0] : the address table address bit [12] : read/write configuration 0: read; 1: write bit [13] : the register C6H, C7H and C8H data indicator 0: C6, C7 and C8 contain the read back data 1: C6, C7 and C8 contain the data that will be written to into address table bit [14] : Enable command 0: Disable; 1: Enable the function of read/write address table. bit [15] : command complete	R/W	16'h0000
C6H	18CH 18DH	CPU read/write address table data[15:0] If the command is read, it stores the bit 15~0 of read back data. If the command is write, it contains the bit 15~0 of written data.	R/W	16'h0000
C7H	18EH 18FH	CPU read/write address table data[31:16] If the command is read, it stores the bit 31~16 of read back data. If the command is write, it contains the bit 31~16 of written data.	R/W	16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
C8H	190H 191H	CPU read/write address table data[45:32] If the command is read, it stores the bit 45~32 of read back data. If the command is write, it contains the bit 45~32 of written data.	R/W	14'h0000
C9H	192H 193H	Port excluding (port15~port0) Bit[15:0] 0:this port is a normal port 1:this port is an excluded port	R/W	16'h0000
CAH	194H 195H	Port excluding(port26~port16) Bit[9:0] 0:this port is a normal port; 1:this port is an excluded port Bit[10]: Reserved. Keep the default setting. Bit[11]: Port excluding function 0:disable; 1:enable	R/W	12'h000
CBH	196H 197H	Auto negotiation Configuration Bit [15:0]: auto negotiation for port 15~ port 0 0: Disable auto negotiation; 1: Enable auto negotiation	R/W	16'hffff
CCH	198H 199H	Auto negotiation configuration Bit [10:0]: auto negotiation for port 26~ port 16 0: Disable auto negotiation; 1: Enable auto negotiation Bit [11]: reserved (This register doesn't set the AN configuration of Giga fiber ports)	R/W	12'h7ff
CDH	19AH 19BH	Speed setting for 100/10 Mbps, port 15~ port 0, 1 bit/port Bit [15:0]: 0: 10 Mbps; 1: 100 Mbps	R/W	16'hffff
CEH	19CH 19DH	Speed setting for 100/10 Mbps, port 26~ port 16, 1 bit/port Bit [10:0]: 0: 10 Mbps; 1: 100 Mbps	R/W	11'h7ff
CFH	19EH 19FH	Speed setting for 1000 Mbps for port 24, port 25 Bit[1:0] : 0: Disable 1000 Mbps ability; 1: Enable 1000 Mbps ability	R/W	2'h3
D0H	1A0H 1A1H	Duplex setting for Port 0 ~ Port 15, 1bit/port bit [15:0] : 0: half duplex; 1: full duplex	R/W	16'hffff
D1H	1A2H 1A3H	Duplex setting for Port 16 ~ Port 26, 1bit/port bit [10:0] : 0: half duplex; 1: full duplex	R/W	11'h7ff
D2H	1A4H 1A5H	Pause setting for Port 0 ~ Port 15, 1bit/port bit [15:0] : 0: Disable pause; 1: Enable pause	R/W	16'hffff

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
D3H	1A6H 1A7H	Pause setting for Port 16 ~ Port 26, 1bit/port bit [10:0] : 0: Disable pause capability; 1: Enable pause capability (This register doesn't set the Pause configuration of Giagbit fiber ports)	R/W	11'h7fff
D4H	1A8H 1A9H	Asymmetric pause setting for Port 0 ~ Port 15, 1bit/port bit [15:0]: 0: Disable asymmetric pause; 1: Enable asymmetric pause	R/W	16'hffff
D5H	1AAH 1BBH	Asymmetric pause setting for Port 16 ~ Port 26, 1bit/port bit [10:0]: 0: Disable asymmetric pause; 1: Enable asymmetric pause (This register doesn't set the Asyn Pause configuration of Gigabit fiber ports)	R/W	11'h7ff
D6H	1ACH 1ADH	Backpressure setting for Port 0 ~ Port 15, 1bit/port bit [15:0]: 0: backpressure function disable; 1: backpressure function enable	R/W	16'hffff
D7H	1AEH 1AFH	Backpressure setting for Port 16 ~ Port 26, 1bit/port bit [10:0]: 0: disable backpressure function e; 1: enable backpressure function	R/W	11'h7ff
D8H	1B0H 1B1H	Transmit setting for Port 0 ~ Port 15, 1bit/port bit [15:0] : 0: disable transmit; 1: enable transmit	R/W	16'hffff
D9H	1B2H 1B3H	Transmit setting for Port 16~ Port 26 1bit/port bit [10:0] : 0: Disable Tx; 1: Enable Tx Bit[13:11]: Force link setting Bit[11]: Force link setting (Port 24) 0: Disable; 1: Enable Bit[12]: Force link setting (Port 25) 0: Disable; 1: Enable Bit[13]: Force link setting (Port 26) 0: Disable; 1: Enable	R/W	14'h7ff

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
DAH	1B4H 1B5H	CPU read/write PHY register command bit [4:0] : PHY ID bit [9:5] : MII register address bit [11:10] : reserved bit [12] : the read/write PCS register command trigger 0: idle or command complete; 1: start command bit [13] : 0: command not complete; 1: command complete bit [14] : 0: read operation; 1: write operation bit [15] : the read/write PHY register command trigger 0: idle or command complete; 1: start command	R/W	16'h0000
DBH	1B6H 1B7H	CPU read/write PHY register command data bit [15:0] : in read command - the read back data in write command - data to be written to PHY	R/W	16'h0000
DCH	1B8H 1B9H	PHY address setting [2:0]: PHY address for port 24(00xxx) [5:3]: PHY address for port 25(00xxx) [8:6]: PHY address for port 26(00xxx) Port 0~7 correspond to the PHY address “01xxx”. Port 8~15 correspond to the PHY address “10xxx”. Port 16~23 correspond to the PHY address “11xxx”.	R/W	9'hd1

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
DDH	1BAH 1BBH	LED setting Bit[2:0] : Switch LED operation mode selection Please refer to LED display mode. Bit[6:3] : LED blinking period 49 ms x n (n= 1,2,3,4) for link/act/col/TX/RX/flow 500 ms x m(m= 1,2,3,4) for speed, duplex Bit[8]: LED test mode. Keep this bit at “0” for normal operation. 1:Enable; 0:Disable; Bit[9]: LED display mode 0: Group1; 1: Group2 Bit[10]:Keep this bit at “0” for normal operation. Bit[11]: LED_CLK clock selection 0: 625K hz; 1: 1.25Mhz Bit[12]: Supress the slow blinking display. This bit is only effective when the display is 2-bit stream mode and Bit[9] is set to “0”. 0: Keep the original display mode. 1: Supress the slow blinking display. Bit[13]: Skip Gigabit TP port status for P24 and P25. 0: Display Gigait TP port and 1000Base-X fiber status. 1: Display 1000Base-X fiber status only. The corresponding bit of the shift register output will be set to “0”. Bit[14]: keep this bit at “0” for normal operation.	R/W	9'h00

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
DEH	1BCH 1BDH	The port status of port 2, 1 and port 0, 5 bit/port bit [4:0] : port 0 status bit [9:5] : port 1 status bit [14:10] : port 2 status The meaning of these bits: {asymmetric pause, flow_ctrl, duplex,speed, link}. Flow_ctrl includes backpressure in half duplex. **Asymmetric pause** 1: Enable asymmetric pause; 0: Disable asymmetric pause **Flow_ctrl** 1: Enable flow control; 0: Disable flow control. **Duplex** 1: Full duplex; 0: Half duplex. **speed** 1: 100 Mbps; 0: 10 Mbps **Link** 1: Link up; 0: Link down	R	16'h0000
DFH	1BEH 1BFH	The port status of port 5, 4 and port 3, 5 bit/port bit [4:0] : port 3 status bit [9:5] : port 4 status bit [14:10] : port 5 status The meaning of these bits: {asymmetric pause, flow_ctrl, duplex,speed, link}. Flow_ctrl includes backpressure in half duplex. The defination for each bit is the same as that of Register DEH.	R	16'h0000
E0H~ E5	1C0H ~1CB H	The port status of port 6 ~ port 23, 5 bit/port bit [4:0] : port 21 status bit [9:5] : port 22 status bit [14:10] : port 23 status The meaning of these bits: {asymmetric pause, flow_ctrl, duplex,speed, link}. Flow_ctrl includes backpressure in half duplex. The defination for each bit is the same as that of Register DEH.	R	16'h0000

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
E6H	1CCH 1CDH	The port status of port 24, 25, 6 bit/port bit [5:0] : port 24 status bit [11:6] : port 25 status The meaning of these bits: {asymmetric pause, flow_ctrl, duplex,speed, link}. Flow_ctrl includes backpressure in half duplex. **Asymmetric pause** 1: Enable asymmetric pause; 0: Disable asymmetric pause **Flow_ctrl** 1: Enable flow control; 0: Disable flow control. **Duplex** 1: Full duplex; 0: Half duplex. **speed** 1x: Gigabit; 01: 100 Mbps; 00: 10 Mbps **Link** 1: Link up; 0: Link down	R	12'h000
E7H	1CEH 1CFH	The port status of port 26, 5 bit/port bit [4:0] : port 26 status The meaning of these bits: {asymmetric pause, flow_ctrl, duplex,speed, link}. Flow_ctrl includes backpressure in half duplex. The defination for each bit is the same as that of Register E6H.	R	5'h00
E8H	1D0H 1D1H	Reserved. Keep the default setting.	R	10'h1CC

5.4 Buffer Management Control Register (E9h~EFh)

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
E9H	1D2H 1D3H	Reserved. Keep the default setting.	R/W	7'd15
EAH	1D4H 1D5H	Reserved. Keep the default setting.	R/W	7'h34
EBH	1D6H 1D7H	Reserved. Keep the default setting.	R/W	7'h22
ECH	1D8H 1D9H	Reserved. Keep the default setting.	R/W	7'h0F
EDH	1DAH 1DBH	Reserved. Keep the default setting.	R/W	13'h3AC
EEH	1DCH 1DDH	Reserved. Keep the default setting.	R/W	7'h24
EFH	1DEH 1DFH	Reserved. Keep the default setting.	R/W	7'h4D

5.5 Miscellaneous Control Register (F0h~FAh)

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
F0H	1E0~ 1E1	Reserved. Keep the default setting	R/W	5'd0(SC)
F1H	1E2 1E3	Reserved. Keep the default setting.	R/W	16'h001f
F2H	1E4 1E5	CPU mode setting Bit[0]: port 26 linked to CPU 0: Disable 1: Enable Bit[1]: Special tag for packet that is forwarded to CPU port 0: Disable 1: Enable, Insert a special tag to the received packet.(16'h9126 + 16' bit source port) The lowest 5 bits of 16-bit special tag is used to indicate source port number. Bit[2]: CPU interface 0: MII mode; 1: Reverse MII mode Bit[3]: clock out selection 0: 25 Mhz 1: 50 Mhz Bit[15]: reserved	R/W	4'd0
F3H	1E6 1E7	Special TAG Type/Len setting Bit[15:0]: special tag type/length item	R/W	16'h9126
F4H	1E8 1E9	TCP/UDP port filter setting Bit[15:0]: P00 ~ P15 port filter 1: filter function of the corresponding port is enabled 0: filter function of the corresponding port is disabled This register is valid only if bit 35h.15 is set to "1". This register and register 37h[15:6] define TCP/UDP port filter function. Bit 37h.14 is valid only if register 37h bit 15 is set to "1".	R/W	16'd0
F5H	1EA 1EB	TCP/UDP port filter setting Bit[10:0]: P16 ~ P26 port filter This register is valid only if register 35h bit15 is set to "1".	R/W	16'h0
F6H	1EC 1ED	Reserved. Keep the default setting.		9'h0

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
F7H	1EE 1EF	Interrupt signal setting (0 : Do not mask; 1: Enable interrupt mask bits[0]~Bit[7]) Bit[0] : mask for CPU r/w SMI command complete Bit[1] : mask for PHY link status notification Bit[3] : mask for CPU r/w EPROM command complete Bit[4] : mask for P24 next page received in fiber mode Bit[5] : mask for P25 next page received in fiber mode Bit[6] : mask for P24 TP/Fiber mode status change notification Bit[7] : mask for P25 TP/Fiber mode status change notification Bit[14:8]: reserved Bit[15] : Interrupt pin active mode (0: low active 1: high active) **Note:** Interrupt signal that is triggered by any event will be asserted until this register(0xF0) is read.	W	16'h2
F8H	1F0 1F1	Interrupt signal setting Bit[0] : Interrupt of CPU r/w SMI command complete (R/SC) 0: not complete; 1: completed Bit[1] : PHY link status change notification (R/SC) 0: status not change; 1: status changed Bit[3] : Interrupt of CPU r/w EPROM command complete (R/SC) 0: not complete; 1: completed Bit[4] : P24 fiber page received notification (R/SC) 0: not received; 1: received fiber page Bit[5] : P25 fiber page received notification (R/SC) 0: not received; 1: received fiber page Bit[6] : p24 TP/Fiber mode change notification (R/SC) 0: mode not changed; 1: mode changed Bit[7] : p25 TP/Fiber mode change notification (R/SC) 0: mode not changed; 1: mode changed	R/W	16'h2

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
F9H	1F2 1F3	RGMII Interface signal Delay setting Bit[1:0]: port 24 Rx clock delay 00 : no delay; 01 : 1 ns delay; 10 : 2 ns delay; 11 : 3 ns delay Bit[2] : Port 24 Rx clock reverse 0: normal 1: reverse Bit[4:3] : Port 24 Tx clock delay 00 : no delay; 01 : 1 ns delay; 10 : 2 ns delay; 11 : 3 ns delay Bit[5] : port 24 Tx clock reverse 0: normal 1: reverse Bit[7:6] : Port 25 Rx clock delay Bit[8] : Port 25 Rx clock reverse. 0: normal; 1: reverse Bit[10:9] : Port 25 Tx clock delay Bit[11] : Port 25 Tx clock reverse. 0: normal; 1: reverse Bit[13:12]: Port24/25 TX driving current 00 : 8 mA; 01 : 12 mA; 10 : 2 mA; 11 : 4 mA Bit[14]: Port 24 MII interface select 0: RGMII interface 1: MII interface Bit[15]: Port 25 MII interface select 0: RGMII interface 1: MII interface	R/W	16'h1EBA

FAH	1F4 1F5	MII/SS-SMII Interface signal Delay setting Bit[0]: Port 0 ~ Port 7 SS-SMII RX Clock delay 0 : no delay 1 : delay 4 ns; Bit[1]: Port 0 ~ Port 7 SS-SMII TX Clock delay 0 : no delay 1 : delay 4 ns; Bit[2]: Port 8 ~ Port 15 SS-SMII RX Clock delay 0 : no delay 1 : delay 4 ns; Bit[3]: Port 8 ~ Port 15 SS-SMII TX Clock delay 0 : no delay 1 : delay 4 ns; Bit[4]: Port 16 ~ Port 23 SS-SMII RX Clock delay 0 : no delay 1 : delay 4 ns; Bit[5]: Port 16 ~ Port 23 SS-SMII TX Clock delay 0 : no delay 1 : delay 4 ns; Bit[6]: CPU MII RX Clock delay 0 : no delay 1 : delay half period; Bit[7]: CPU MII TX Clock delay 0 : no delay 1 : delay half period; Bit[9:8] : Port 0 ~ Port 23, CPU port TX driving current 00 : 4 mA 01 : 8 mA 10 : 12 mA 11 : 2 mA Bit[10] : Port 0 ~ Port 7 SS-SMII RX SYNC delay 0 : no delay 1 : delay 4 ns Bit[11] : Port 8 ~ Port 15 SS-SMII RX SYNC delay 0 : no delay 1 : delay 4 ns Bit[12] : Port 16 ~ Port 23 SS-SMII RX SYNC delay 0 : no delay 1 : delay 4 ns Bit[14] : Slew Rate 0: Normal 1: Fast	R/W	16'h4100

5.6 SerDes Function Setting (FBh~FFh)

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
FBH	1F6 1F7	CPU read/write EEPROM command bit [7:0] : Byte Address bit [10:8] : Device Address bit [12:11] : reserved bit [13] : 0 : command not complete 1 : command complete bit [14] : 0 : read operation 1 : write operation bit [15] : the read/write command trigger 0 : idle or command complete 1 : start command	R/W	16'h000
FCH	1F8 1F9	CPU read/write EEPROM command data bit [7:0] : in read command - the read back data in write command - data to be written to EEPROM	R/W	8'h0000
FDH	1FA 1FB	It should be written with BE02h for SerDes setting.	R/W	16'hBE02
FEH	1FC 1FD	It should be written with BE02h for SerDes setting.	R/W	16'hBE02

Reg Addr.	ROM Addr.	Register Description	R/W	Default value
FFH	1FE 1FF	PCS setting for P24, P25. Set this register to “16’h3681” for 2-port GBIC +1000Base-T combo interface. Bit[7:0]: Set this register to 8’h81 for combo auto-detection mode. Set this register to 8’h”01 for 1000Base-T only. Bit[8]: Signal detect(SD) active mode 0: Low active (GBIC type) 1: High active Bit[10:9]: port 24 PCS receive clock delay 00 : no delay; 01: 1 ns delay; 10: 2 ns delay; 11: 3 ns delay Bit[11] : port 24 PCS receive clock phase 0: in phase; 1: reverse phase Bit[13:12]: port 25 PCS receive clock delay 00: no delay; 01: 1 ns delay; 10: 2 ns delay; 11: 3 ns delay Bit[14] : port 25 PCS receive clock reverse 0: in phase; 1: reverse phase	R/W	16’h3681

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Permanent device damage may occur if Absolute Maximum Ratings are applied. Functional operation should be restricted to the conditions as specified in the following section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

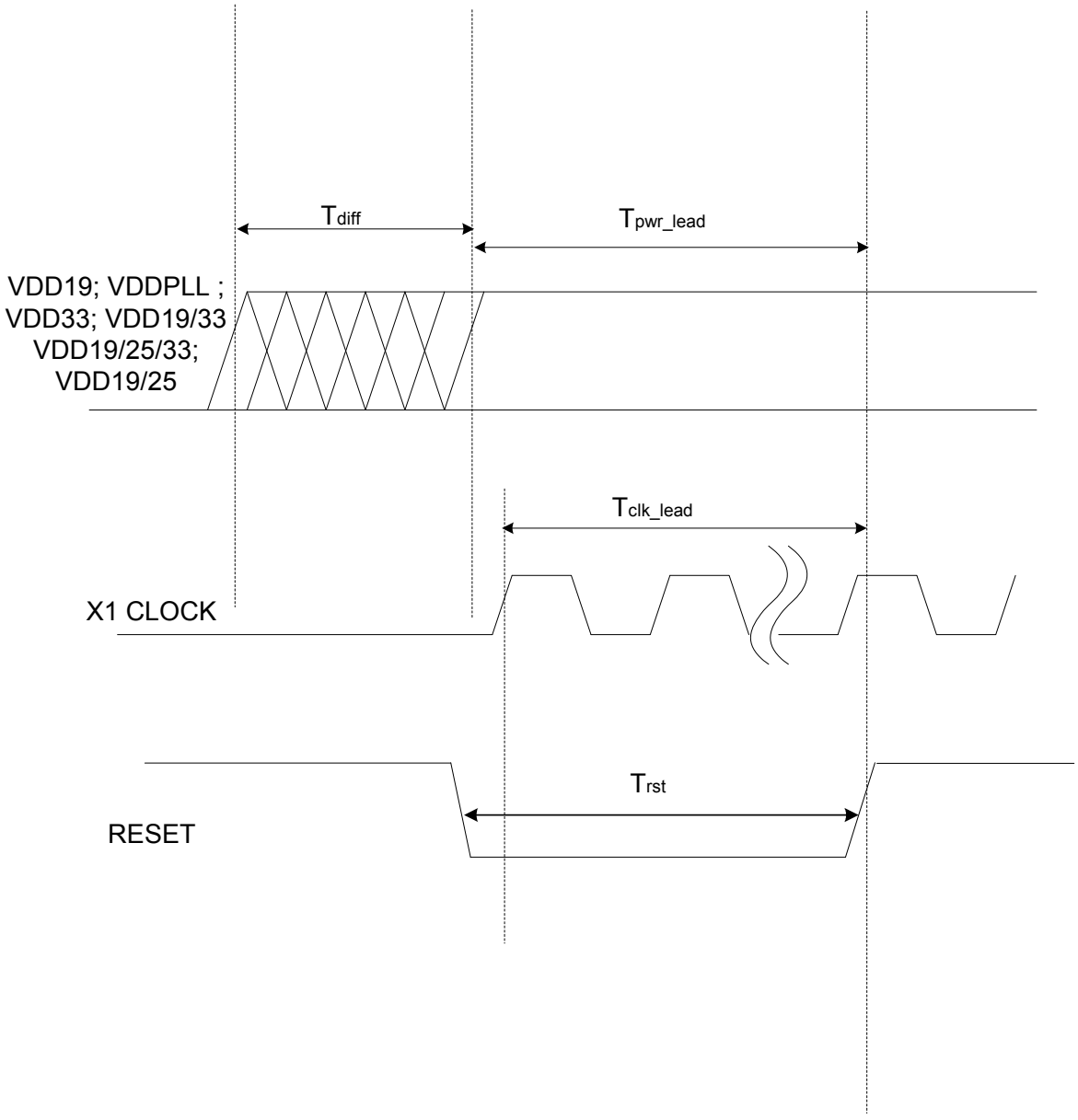
PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	I/O	$V_{DDI/O}$	– 0.5	+3.6V	V
	Core	V_{DDCore}	– 0.5	+2.3V	V
Input Voltage		V_I	– 0.5	$V_{DDI/O}$	V
Output Voltage		V_O	– 0.5	$V_{DDI/O}$	V
Storage Temperature		T_{STG}	-65	+150	°C
Operation Temperature		T_{OPT}	0	+70	°C
IC Junction Temperature				+125	°C

Note: The maximum ratings are the limit value that must never be exceeded even for short time.

6.2 AC Characteristics

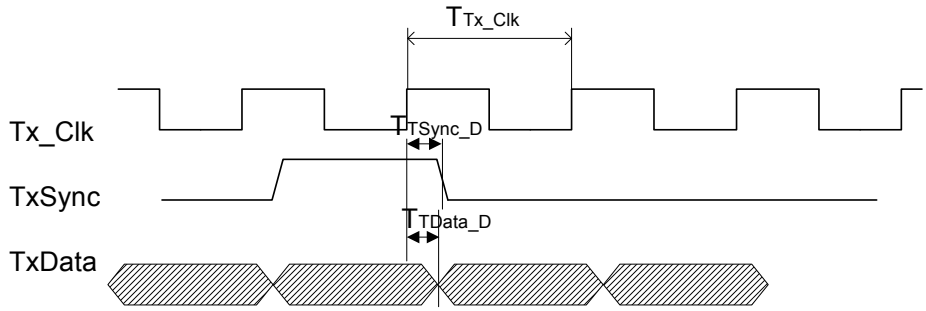
6.2.1 Reset, Clock and Power Source

Symbol	Description	Min.	Typ.	Max.	Unit
T_{clk_lead}	X1 clock valid before reset released	10	-	-	ms
T_{rst}	Reset period	10	-	-	ms
T_{diff}	Time difference among power sources			30	ms
T_{pwr_lead}	All power source ready before reset released	11			ms



SS-SMII Transmit Timing (data driving current @8 mA , clock driving current @12 mA)

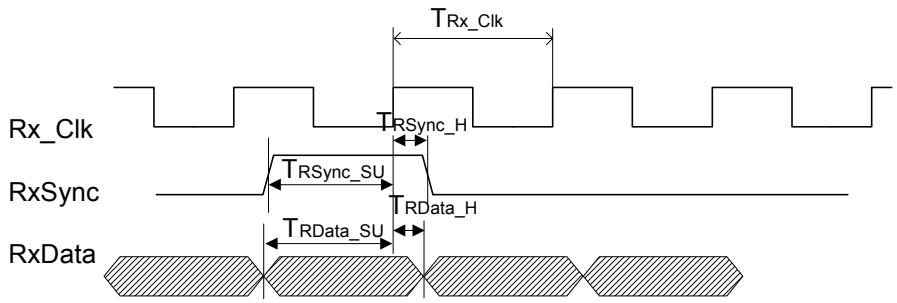
Symbol	Description	Min.	Typ.	Max.	Unit
T_{Tx_Clk}	Transmit clock cycle time	-	8	-	ns
T_{TSync_D}	Tx_Clk rising edge to TX_Sync output delay	0.5		3.9	ns
T_{TData_D}	Tx_Clk rising edge to TXD output delay	0.8	-	5.2	ns



SS-SMII Transmit

SS-SMII Receive Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rx_Clk}	Receive clock cycle time	-	8	-	ns
T_{RSync_SU}	Rx_Sync Set up time	1.8			ns
T_{Rsync_H}	Rx_Sync Hold time	0	-		ns
T_{Rdata_SU}	RxData Set up time	2.2			ns
T_{RData_H}	RxData Hold time	0	-		ns

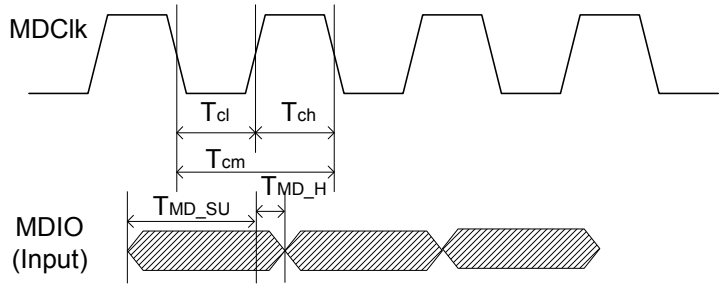


SS-SMII Receive

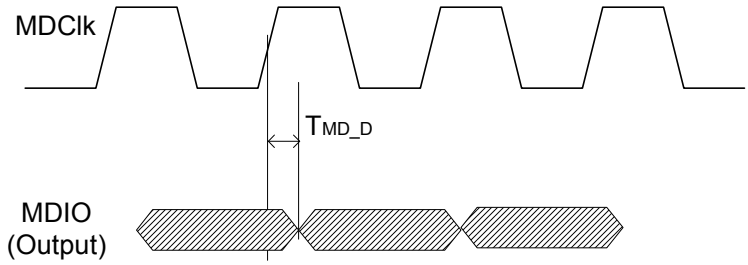
PHY Management (MDIO) Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDCK High Time	-	200	-	ns
T_{cl}	MDCK Low Time	-	200	-	ns
T_{cm}	MDCK cycle time	-	400	-	ns
T_{MD_SU}	MDIO set up time	10	-		ns

T_{MD_H}	MDIO hold time	10	-	-	ns
T_{MD_D}	MDIO output delay time	200	-	210	ns



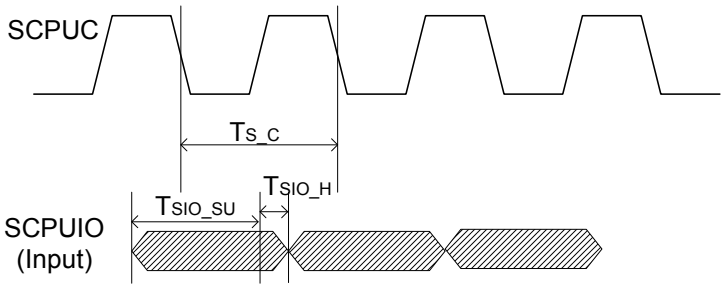
MDIO Input Cycle



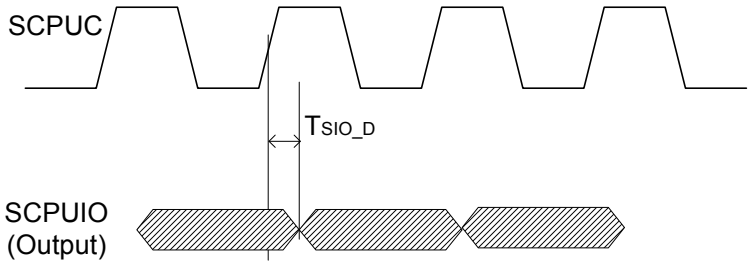
MDIO Output Cicle

CPU Serial Bus Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{S_C}	SCPUC cycle time	400		-	ns
T_{SIO_SU}	Serial I/O set up time	10	-		ns
T_{SIO_H}	Serial I/O hold time	10	-	-	ns
T_{SIO_D}	Serial I/O output delay time		-	20	ns



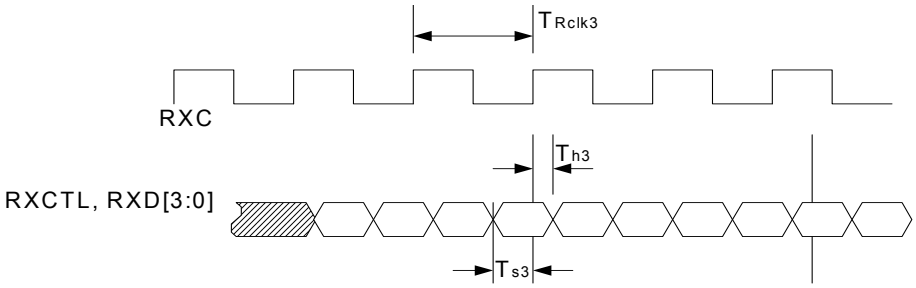
Serial I/O Input Cycle



Serial I/O Output Cycle

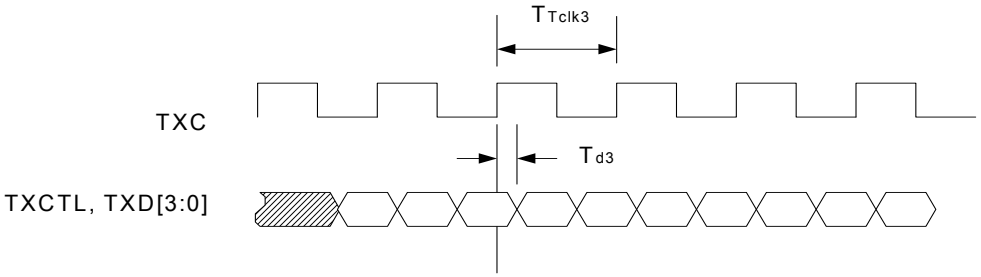
RGMII Rx Part Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rclk3}	Period of transmit clock in giaga mode	-	8	-	ns
T_{Rclk3}	Period of transmit clock in 100M mode	-	40	-	ns
T_{Rclk3}	Period of transmit clock in 10M mode	-	400	-	ns
T_{s3}	RXCTL, RXD to RXC setup time (no clock delay added)	1			ns
	(RGMII Rx delay setting = 010)	-0.95			
T_{h3}	RXCTL, TXD to TXC hold time (no clock delay added)	1.3			ns
	(clock delay setting = 010)	-0.95			



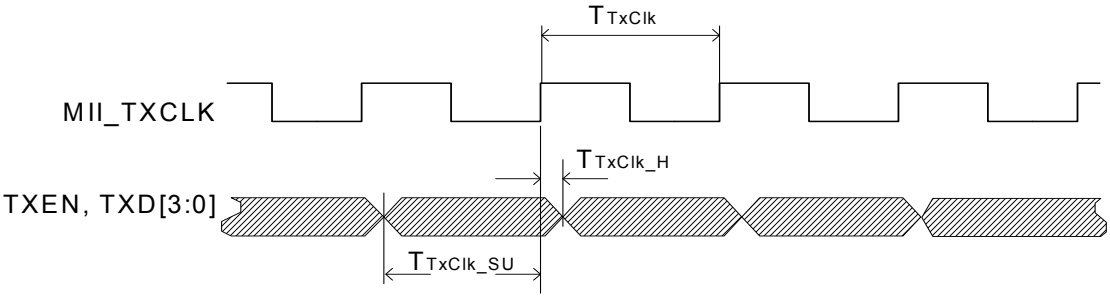
RGMII Tx Part Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Rclk3}	Period of receive clock in giga mode	-	8	-	ns
T_{Rclk3}	Period of receive clock in 100M mode	-	40	-	ns
T_{Rclk3}	Period of receive clock in 10M mode	-	400	-	ns
T_{d3}	TXCTL, TXD output delay from TXC edge (no clock delay added)	1.7		3.5	ns
	(clock delay setting = 111)	1.1		2.7	



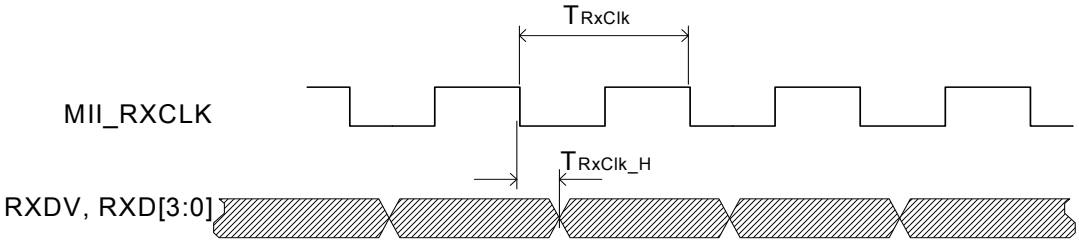
MII Transmit Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{TxClk}	Transmit clock period 100Mbps MII	-	40	-	ns
T_{TxClk}	Transmit clock period 10Mbps MII	-	400	-	ns
T_{TxClk_SU}	TXEN, TXD to MII_TXCLK setup time	2	-	-	ns
T_{TxClk_H}	TXEN, TXD to MII_TXCLK hold time	0.5	-	-	ns



MII Receive Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{RxClk}	Receive clock period 100Mbps MII	-	40	-	ns
T_{RxClk}	Receive clock period 10Mbps MII	-	400	-	ns
T_{RxClk_D}	MII_RXCLK falling edge to RXDV, RXD	1	-	4	ns



6.3 DC Characteristics

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Output low voltage		V_{OL}			0.4	V
Output high voltage		V_{OH}	1.75V for 1.9V I/O supply voltage; 3V for 3.3V I/O supply voltage;			V
VDD33 supply current						
VDD19 supply current						
VDDPLL supply current						
VDD33 supply voltage				1.9 or 3.3		V
VDD19 supply voltage			1.85	1.92	2.0	V
VDDPLL supply voltage			1.85	1.92	2.0	V
RESET Threshold voltage			$0.7*V_{CC}$		$0.85*V_{CC}$	V
X1 Input Low Voltage (1.9V operation)		X1 V_{IL}			0.6	V
X1 Input High Voltage (1.9V operation)		X1 V_{IH}	1.5			V
Pull-down resistor		R_{PD}	51		127	KΩ
Theremal resistor(Junction to ambient) @2 layer PCB; Air flow: 0ft/sec.		Θ_{JA}		40.5		℃/W
Theremal resistor(Junction to ambient) @4 layer PCB; Air flow: 0ft/sec.		Θ_{JA}		19.3		℃/W
SS-SMII						
Input Low to High	VDDIO =1.95V	V_{IH}	1.26		---	V
Input High to Low		V_{IL}	---		0.79	V
Input Low to High	VDDIO =3.3V	V_{IH}	1.99		---	V
Input High to Low		V_{IL}	---		1.41	V
RGMII						
Input Low to High	VDDIO =1.95V	V_{IH}	1.26		---	V
Input High to Low		V_{IL}	---		0.79	V
Input Low to High	VDDIO =2.5V	V_{IH}	1.56		---	V
Input High to Low		V_{IL}	---		1.05	V
MII						
Input Low to High	VDDIO =1.95V	V_{IH}	1.26		---	V
Input High to Low		V_{IL}	---		0.79	V
Input Low to High	VDDIO =2.5V	V_{IH}	1.56		---	V
Input High to Low		V_{IL}	---		1.05	V
Input Low to High	VDDIO =3.3V	V_{IH}	1.99		---	V
Input High to Low		V_{IL}	---		1.41	V

6.4 Serial Transmitter/Receiver DC characteristic

Transmitter DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_{OD}	Output Voltage Swing	300		600	mV peak
R_O	Output Impedance(single-ended)	40		140	Ωs

Receiver DC Characteristics

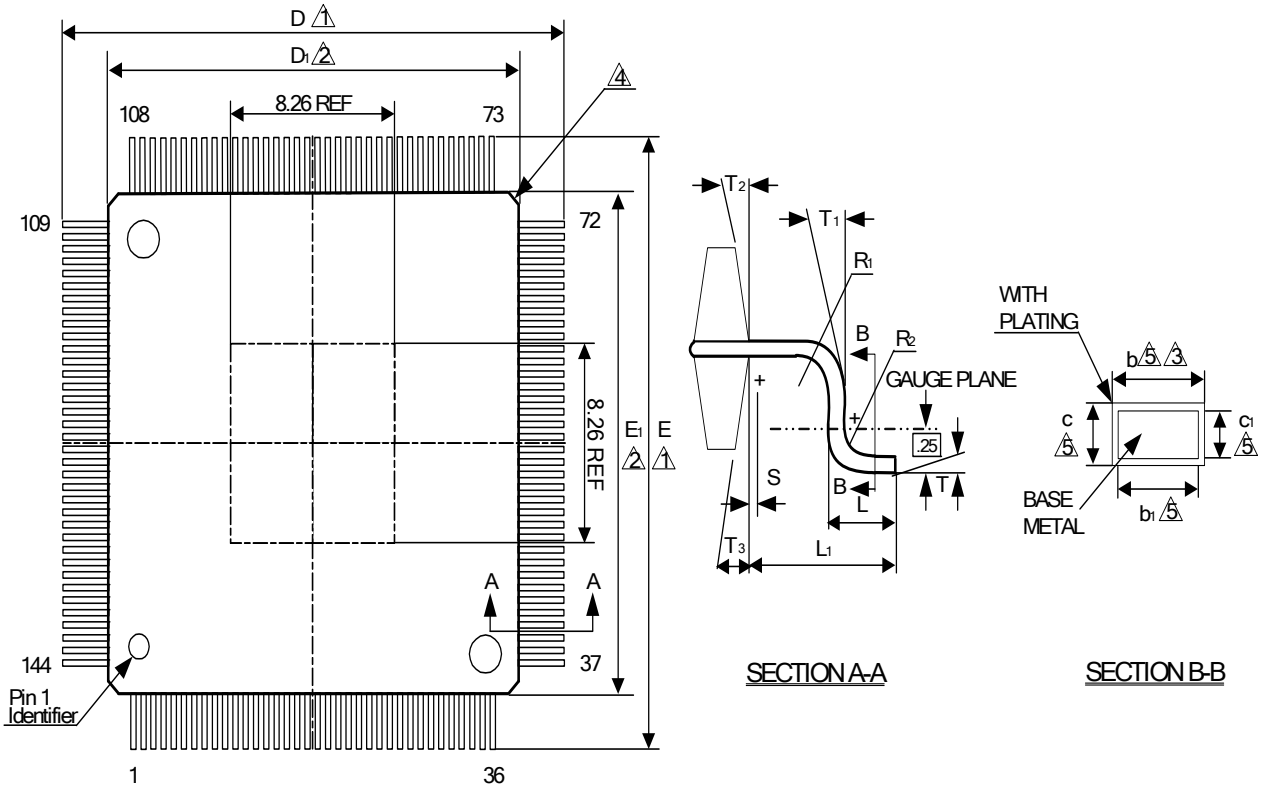
Symbol	Parameter	Min	Typ	Max	Units
V_{RCOM}	Common mode voltage(Supplied by IC itself)	1.2	1.4	1.8	V
V_{IDTH}	Input Differential Threshold	200			mV
R_{IN}	Receiver 100Ω Differential Input Impedance	80		120	Ω

7 Order Information

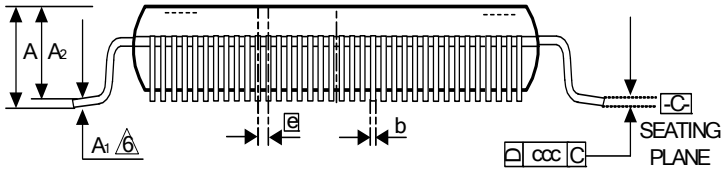
Part No.	Package	Notice
IP1826D	144-PIN EPAD	-

8 Package Detail

144 E-PAD Outline Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A1	0.05	-	-	0.002	-	-
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1		0.20 REF			0.008 REF	
c	0.12	-	0.20	0.005	-	0.008
c1		0.13 REF			0.005 REF	
D	21.85	22.00	22.15	0.860	0.866	0.872
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	21.85	22.00	22.15	0.860	0.866	0.872
E1	19.90	20.00	20.10	0.783	0.787	0.791
e		0.50 BSC			0.020 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00 REF			0.039 REF	
R1		0.15 REF			0.006 REF	
R2		0.15 REF			0.006 REF	
S		0.19 REF			0.007 REF	
T	0°	3.5°	7°	0°	3.5°	7°
T1		7° REF			7° REF	
T2		12° REF			12° REF	
T3		12° REF			12° REF	
ccc		0.08			0.003	



Note:

1 To be determined at seating plane -C- .
2 Dimensions D1 and E1 do not include mold protrusion.
D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3 Dimension b does not include dambar protrusion.
Dambar can not be located on the lower radius of the foot.
4 Exact shape of each corner is optional.
5 These dimensions apply to the flat section of the lead between 0.10mm and 0.25 mm from the lead tip.
6 A1 is defined as the distance from the seating plane to the lowest point of the Package body.
7 Controlling dimension : Millimeter.