Octal 10/100 Fast Ethernet Transceiver

Features

- Integrates eight-port 10Base-T, 100Base-TX and 100Base-FX transceivers in a single chip
- Flexible 8-port 100Base-FX configuration.
- Fully compliant with IEEE802.3/802.3u.
- Supports auto crossover function and force MDIX function.
- Supports auto-negotiation function.
- Flexible functional configuration through either pin setting or register programming
- Supports SS-SMII interfaces
- Supports BaseLine Wander (BLW) compensation
- Provides direct drive mode and serial data latch LED display mode
- Embeds DSP-based PHY Transceiver technology to improve the cable driving performance
- Adjustable current driving capabilities
- Adjustable SS-SMII interface timing
- Provides power-on LED diagnostic function
- Power supply: Selectable 3.3V/1.95V for I/O 1.95V power supply for core
- Supports Automatic Power Saving (APS) Mode
- Requires only one external clock source
- 0.18u CMOS technology
- 128 pin LQFP EPAD package
- Support Lead Free package (Please refer to the Order Information)

General description

The IP108A is a highly integrated octal PHY transceiver for 10Base-T, 100Base-TX and 100Base-FX Fast Ethernet applications. This device is implemented with advanced 0.18um CMOS process technology for low power consumption. For the high port count switch design such as 16 or 24 or 32-port, the IP108A can simplify the system design and ensure the targeted performance.

IP108A can be programmed to operate in various modes through either hardware (hardware strapping pin) or software control (registers setting via SMI). It also supports SS-SMII interface to MAC controller to reduce the pin-count.

The IP108A contains eight independent 10/100M PHY Transceiver and includes encoder, decoder, line driver, ADC, DAC, DSP and PLL circuits for each port. The IP108A enters the Automatic Power Saving Mode to lower the power consumption once the link partner is disconnected. The IP108A just needs an external OSC or crystal as the clock source, simplifying the system design. Besides the features described above, the driving capability of IP108A can be trimmed to minimize the EMI effect by the advanced slew rate control technology.

The major differences between IP108A and IP108

Unlike IP108, which supports limit combination of FX port, each port of IP108A can be configured as a TP or FX port individually. RMII is not supported in IP108A, the original RMII pins are used as LED pins.

To solve the direct mode LED problem that it needs extra TTL device to drive an active high LED when VDDIO is 1.95v, IP108A supports direct mode LED that are all active low. To achieve this target, the input setting functions on these pins are moved to non-LED pins. The differences are listed in the following table.

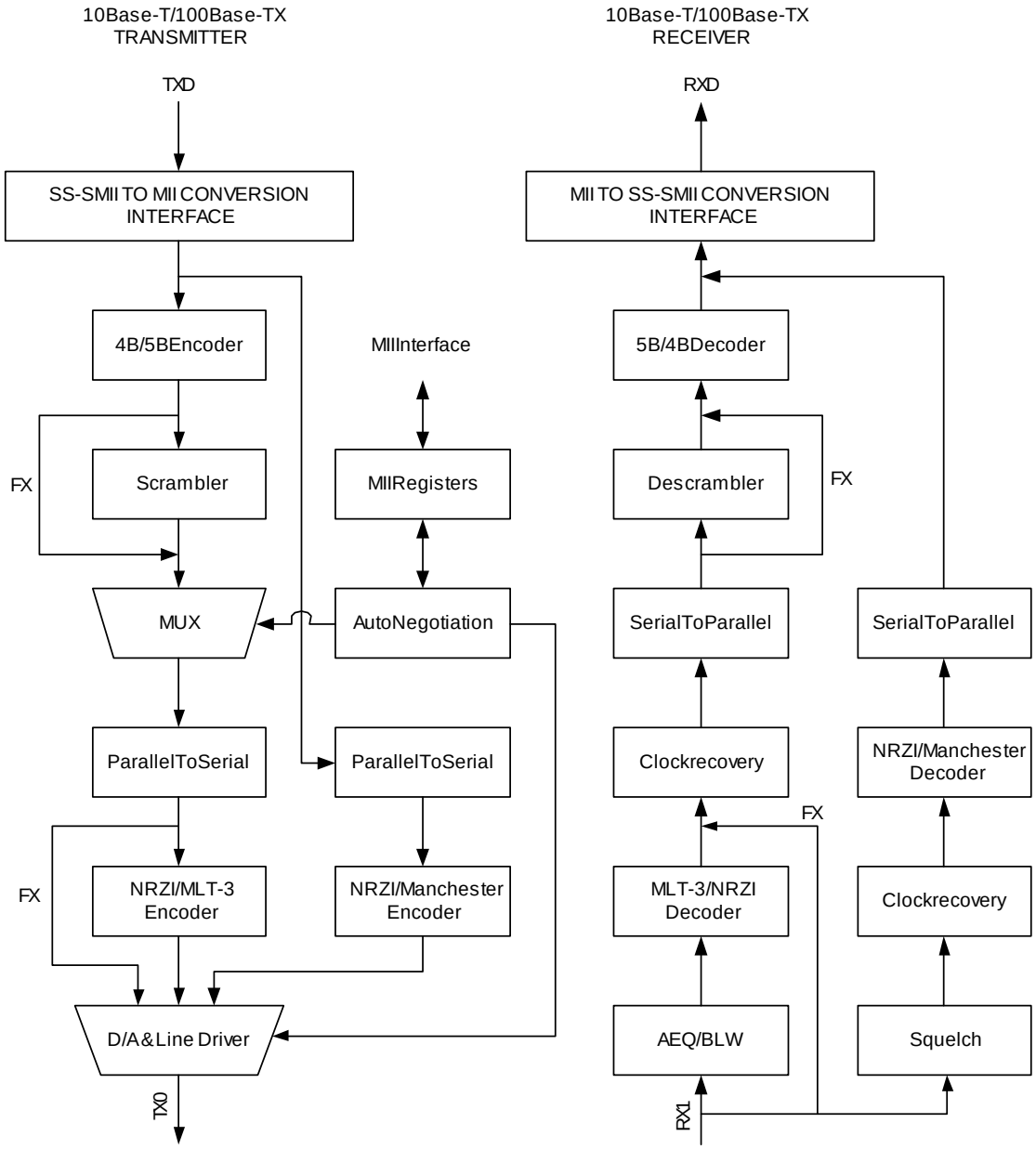
Pin No.	IPH/ IPL	IP108 / Setting function	IP108A / Setting function	
			Serial LED	Direct LED
48	↓	REFCLK	TMOD2	TMOD2
51	↑	10_PSAVE_EN	PS_MODE_SEL	--
52	↓	DRIVE[0]	RX_DRIVE[0]	RX_DRIVE[0]
53	↑	INTERFACE[0]	SS-SMII	--
59	↓	DIS_BLINK	DIS_BLINK	--
60	↓	DRIVE[1]	RX_DRIVE[1]	RX_DRIVE[1]
61	↓	INTERFACE[1]	SSCLK_EN	--
65	↑	LED_BLK_TIME	LED_BLK_TIME	--
66	↓		RX_CLK_INV	RX_CLK_INV
67	↑	TP_PAUSE	TP_PAUSE	--
73	↓	PHY_ADDR[4]	PHY_ADDR[4]	--
74	↓		LED2_COLBLK_EN	IP108A_MODE
81	↑	REPEAT_MODE	REPEAT_MODE	PHY_ADDR[4]
83	↑	PHY_ADDR[3]	PHY_ADDR[3]	--
84	↓		RX_DELAY	RX_DELAY
85	↑	FX_PAUSE	FX_PAUSE	--
92	↓	APS_DIS	FMOD_LED	PHY_ADDR[3]
93	↑	FX_DUPLEX	FX_DUPLEX	--
97	↓	CLK_INV	--	--
98	↓	RDRIVE[2]	TX_DELAY	TX_DELAY
99	↓	SEL_TXFX[1]	--	--
105	↓	MLT3_DET_EN	MLT3_DET_DIS	--
107	↓	SEL_TXFX[0]	--	--

↓: internal pull low
↑: internal pull high

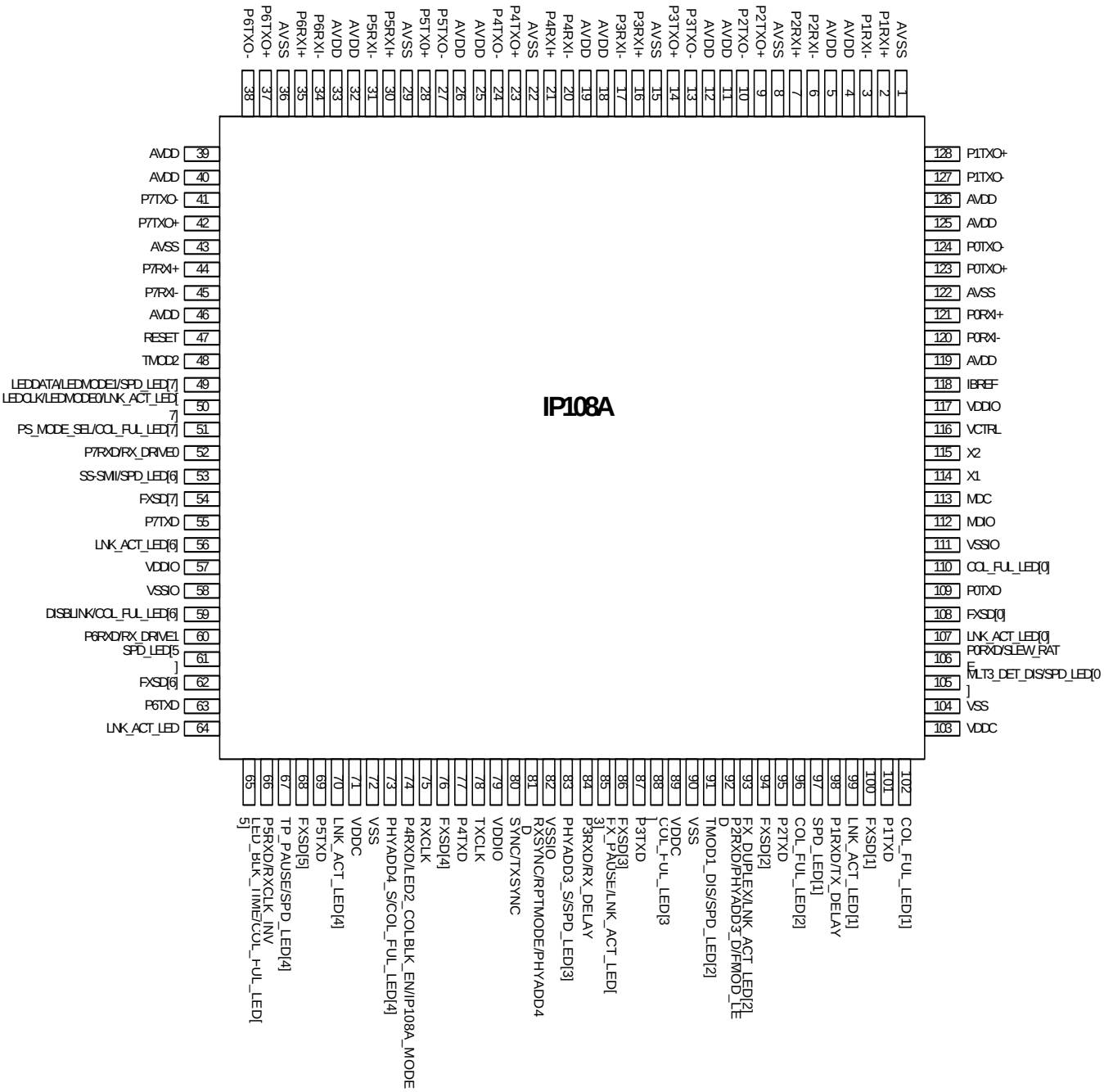
Revision History

Revision #	Change Description
IP108A-DS-R01	First Release
IP108A-DS_R02	1. Update 6.3 DC Characteristics (page44) 2. Remove SMII function description (page1,5,8,9,17,22,27,36,37,41) 3. Add SS-SMII application block diagram (page29) 4. Modify Fiber Optical application circuit resistor value (page32)
IP108A-DS_R03	1. Add power on sequence.(page 42) 2. Modify Fiber Rx common mode Voltage from AVDD*0.78 to AVDD*0.6.(page 46) 3. Add IC junction temperature description.(page 41) 4. Modify VDDIO , VDDC , AVDD supply voltage minimum value to 1.85V (Page 46) 5. Add DC Characteristics RESET Threshold and X1 Input Low/High Voltage description (Page 46) 6. Modify MDC maximum operation frequency from 25MHz to 2.5MHz for typing error (Page 14) 7. Expand VDDC,AVDD supply voltage maxima value from 2.05V to 2.1V (Page46)
IP108A-DS_R04	1. Package changed to LQFP EPAD(page1,47)

Block diagram



Pin Diagram



1. Pin Description

Type
A: analog
I: input
O: output
LI: Latch in

VDD: power source
VSS: power ground
C: core
IO: I/O pin

Pin no.	Pin name	Type	Description	Default
Power and Ground Pins				
71, 89, 103	VDDC	VDD, C	1.95V power for digital core	-
57, 79, 117,	VDDIO	VDD, IO	3.3V or 1.95V power for digital I/O.	-
4, 5, 11, 12, 18, 19, 25, 26, 32, 33, 39, 40, 46, 119, 125, 126	AVDD	VDD, A	1.95V power for analog circuit	-
72, 90, 104	VSS	VSS, D	Digital Ground	-
58, 82, 111	VSSIO	VSS, D	Digital I/O Ground	-
1, 8, 15, 22, 29, 36, 43, 122	AVSS	VSS, A	Analog Ground	-

Pin Description（continued）

Pin no.	Pin name	Type	Description	Default
SS-SMII Interface Pins				
55, 63, 69, 77, 87, 95, 101, 109,	P7TXD-P0TXD	I	In SS-SMII mode, TXD for all ports are driven by an external MAC device and are synchronous to TXCLK. In 100Mbps mode, TXD inputs 10-bit frame starting with TXSYNC to represent one byte data. TXD must repeat the frame 10 times to form one byte data when operating at 10Mbps mode.	-
52, 60, 66, 74, 84, 92, 98, 106	P7RXD-P0RXD	O	In SS-SMII mode, RXD for all ports are sent from IP108A to an external MAC deivce, and synchronous to RXCLK. In 100Mbps mode, RXD outputs 10-bit frame starting with RXSYNC to represent one byte data, RXD repeats the frame 10 times to form one byte data when operating at 10Mbps mode.	-
78	TXCLK	I	In SS-SMII mode, this pin is used as TXCLK. This pin is also used as system clock source, which is a 125MHz clock fed to IP108A.	-
75	RXCLK	O	In SS-SMII mode, this pin is used as RXCLK, which is a 125MHz clock sent out by IP108A.	-
80	TXSYNC	I	In SS-SMII mode, this pin is used as TXSYNC signal that delimit a 10-bit frame of TXD for all ports. TXSYNC should be driven by external MAC device and synchronized to TXCLK.	-
81	RXSYNC	O	In SS-SMII mode, this pin is used as RXSYNC signal that delimit a 10-bit frame of RXD for all ports. RXSYNC should be driven by IP108A and synchronized to RXCLK	-

Pin description（continued）

<table>
<tr><th>Pin no.</th><th>Pin name</th><th>Type</th><th>Description</th><th>Default</th></tr>
<tr><td colspan="5">Latched Type Input Setting Pins (The state of these pins will be latched upon power on reset)</td></tr>
<tr><td>49, 50</td><td>LEDMODE1,
LEDMODE0</td><td>LI</td><td>These pins are used to select LED display mode.
<table><tr><th>LEDMODE[1:0]</th><th>Meaning</th></tr><tr><td>00</td><td>3-bit serial stream</td></tr><tr><td>01</td><td>2-bit serial stream</td></tr><tr><td>10</td><td>3-bit bi-color serial stream</td></tr><tr><td>11</td><td>Mono color direct mode</td></tr></table>To enable LED direct mode, pin 74 should be pull high.
Please refer to section 3.3 LED mode setting for more detail information.</td><td>00</td></tr>
<tr><td>74</td><td>LED2_COLBLK_
EN</td><td>LI</td><td>LED mode 2 collision LED blinking enable
1: COL LED blinking during collision
0: COL LED not blinking during collision (default)
The above function is valid for 3-bit serial bi-color mode only (LEDMODE[1:0]=10).
To enableLED direct mode (LEDMODE[1:0]=11), this pin should be pulled high.</td><td>0</td></tr>
<tr><td>51</td><td>PS_MODE_SEL</td><td>LI</td><td>This pin is used to select the 10M power saving mode
1= 0/100 mA power saving mode
0= 40/100 mA power saving mode
This pin is invalid when pin 49,50 LEDMODE[1:0] are set to 11, direct LED mode.</td><td>1</td></tr>
<tr><td>53</td><td>SS_SMII</td><td>LI</td><td>This pin is used to select the operating mode
0= Reserved
1= SS-SMII mode
This pin is invalid when pin 49,50 LEDMODE[1:0] are set to 11, direct LED mode.</td><td>1</td></tr>
<tr><td>59</td><td>DISBLINK</td><td>LI</td><td>This pin is used to disable LED diagnostic blinking function upon power on reset
1= disable LED blinking
0= enable LED blinking
This pin is invalid when pin 49,50 LEDMODE[1:0] are set to 11, direct LED mode.</td><td>0</td></tr>
<tr><td>60,52</td><td>RX_DRIVE1,
RX_DRIVE0</td><td>LI</td><td>These 2 pins are used to control SS-SMII I/O output driving capability
Please refer to the section 3.2 I/O driving capability for more detail information.</td><td>00</td></tr>
<tr><td>65</td><td>LED_BLK_TIME</td><td>LI</td><td>This pin is used to select the LED blinking time.
1= 48ms blinking time
0= 128ms blinking time
This pin is invalid when pin 49,50 LEDMODE[1:0] are set to 11, direct LED mode.</td><td>1</td></tr>
</table>

66	RX_CLK_INV	LI	This pin is used to reverse the SS-SMII RXCLK. 1= reverse SS-SMII RXCLK 0= not reverse SS-SMII RXCLK The combination of pins 66 and 84 can adjust the SS-SMII receive timing. The detail setting of receive timing adjustment is referred to the section of “AC Characteristics”.	0

Pin description（continued）

Pin no.	Pin name	Type	Description	Default
Latched Type Input Setting Pins（continued）				
67	TP_PAUSE	LI	Flow control function for TP cable 1= enable flow control 0= disable flow control This pin is invalid when pin 49,50 LEDMODE[1:0] are set to 11, direct LED mode.	1
73, 83	PHYADD4_S PHYADD3_S	LI	PHY address 4,3 when LED works in serial mode These two pins will be latched to set the highest 2 bits of 5-bit PHY address when IP108A works in serial LED mode. These pins are invalid when pin 49,50 LEDMODE[1:0] are set to 11, direct LED mode. Please refer to the description of pin 81 PHYADD4_D and 92 PHYADD3_D for the PHY address setting in direct LED mode.	01
74	IP108A_MODE	LI	IP108A direct LED mode/ IP108 direct LED mode 1= IP108A mode, all 24 LED pins are active low. 0= IP108 compatible mode, not all LED pin are active low. The behavior is the same as IP108 for backward compatible. New design is strongly recommended to select IP108A mode in direct mode LED application, because it needs no extra TTL device to drive active high LED when VDDIO is 1.95v.	0
81	RPT_MODE / PHYADD4_D	LI	When pin 49,50 LEDMODE[1:0] not equal to 11, serial LED mode, this pin is used to set the PHYs in IP108A working in repeater mode. 1= repeater mode, no loop back during transmission. 0= not a repeater, loop back during transmission PHY address 4 when LED works in direct mode When pin 49,50 LEDMODE[1:0] are set to 11, direct LED mode. This pin is used to set the highest bit of 5-bit PHY address.	1
84	RX_DELAY	LI	This pin is used to configure the SS-SMII receive output delay 1= add SS-SMII receive output delay 0= not to add SS-SMII receive output delay The combination of pins 66 and 84 can adjust the SS-SMII receive timing. The detail setting of receive timing adjustment is referred to the section of “AC Characteristics”.	0
85	FX_PAUSE	LI	Flow control for fiber port 1= enable flow control 0= disable flow control This pin is invalid when pin 49,50 LEDMODE[1:0] are set to 11, direct LED mode.	1

Pin description（continued）

Pin no.	Pin name	Type	Description	Default
Latched Type Input Setting Pins（continued）				
91	TMOD1_DIS	LI	This pin is latched to set the operating mode upon power on reset 1= Normal mode 0= Testing mode This pin should be always pulled high for normal operation.	1
92	FMOD_LED/ PHYADD3_D	LI	When pin 49,50 LEDMODE[1:0] not equal to 11, serial LED mode, this pin is use to select the LED behavior in force mode (auto-negotiation disabled). 1= Speed/ Duplex LED on, before link up. 0= Speed/ Duplex LED off, before link up. PHY address 3 when LED works in direct mode When pin 49,50 LEDMODE[1:0] are set to 11, direct LED mode, this pin is use to set the second highest bit of 5-bit PHY address.	0
93	FX_DUPLEX	LI	This pin is used to force the operation of the duplex mode for 100Base-FX . 1= Full duplex 0= Half duplex. This pin is invalid when pin 49,50 LEDMODE[1:0] are set to 11, direct LED mode.	1
98	TX_DELAY	LI	This pin is used to configure the input delay of TXCLK 1= add input delay 4n sec to TXCLK 0= not to add delay 4n sec to TXCLK	0
106	SLEW_RATE	LI	This pin is used to select the slew rate of SS-SMII I/O pins. 0 = Normal 1 = Fast	1

Pin description（continued）

Pin no.	Pin name	Type	Description	Default
Miscellaneous Pins				
47	RESET	I	Reset is an active low signal and should be kept low for more than 1ms.	-
48	TMOD2	I	This pin is used to set IP108A to SCAN mode. 1 = SCAN mode 0 = Normal mode This pin should be always pulled low for normal operation.	0
114	X1	I	25MHz crystal or OSC input pin	-
115	X2	O	25MHz crystal output	-
Reference Pins				
118	IBREF	A	This pin must be connected to analog ground through a 6.19k ohm 1% resistor for internal circuit use.	-
116	VCTRL	O	This pin is used to control the base of a PNP transistor to generate a 1.95Volt power source for VDDC and AVDD.	-
SMI Interface Pins				
112	MDIO	I/O	A MAC device access to MII registers in IP108A through MDIO pin and MDC pin. This pin should be kept at tri-state at least 700us after the reset completes. The MDIO must be pulled high by an external 1.5K resistor.	-
113	MDC	I	This pin should be kept at tri-state at least 700us after the reset completes. The MDC is sourced by a MAC device, and runs up to 2.5MHz.	-

Pin description（continued）

Pin no.	Pin name	Type	Description	Default
Serial LED Control Pins				
49	LEDDATA	O	This pin sends out a bit stream for serial mode LED display. Its data format depends on the setting of LEDMOD[1:0].	-
50	LEDCLK	O	External TTL devices use this signal to sample LEDDATA for serial mode LED display. The LEDCLK period is 3.2 uSec +/-10%	-
Direct LED Control Pins				
107, 99, 93, 85, 70, 64, 56, 50	LINK_ACT_LED[0]~ LINK_ACT_LED[7]	O	These pins are link/active LED output for direct LED display.	-
105, 97, 91, 83, 67, 61, 53, 49	SPD_LED[0]~ SPD_LED[7]	O	These pins are speed LED output for direct LED display.	-
110, 102, 96, 88, 73, 65, 59, 51	COL_FUL_LED[0]~ COL_FUL_LED[7]	O	These pins are duplex/collision LED output for direct LED display.	-

Pin description（continued）

Pin no.	Pin name	Type	Description	Default
Media dependent pins				
108, 100, 94, 86, 76, 68, 62, 54	FXSD[0]~FXSD[7]	A, I	These are optical fiber signal detection used for 100Base-FX. These pins are also used to configure a port to be TP or FX. If the input voltage is higher than 0.8V, the corresponding port works at 100Base-FX mode. Otherwise, it works at 10Base-T or 100Base-TX. Each port can be configured individually. The FXSD threshold for fiber link status is higher than 1.72V.	-
123, 128, 9, 14, 23, 28, 37, 42	P0TXO+~P7TXO+	A, O	These are positive transmit differential pair used for 10Base-T, 100Base-TX,and 100Base-FX.	-
124, 127, 10, 13, 24, 27, 38, 41	P0TXO-~P7TXO-	A, O	These are negative transmit differential pair used for 10Base-T, 100Base-TX,and 100Base-FX	-
121, 2, 7, 16, 21, 30, 35, 44	P0RXI+~P7RXI+	A, I	These are positive receive differential pair used for 10Base-T, 100Base-TX, and 100Base-FX	-
120, 3, 6, 17, 20, 31, 34, 45	P0RXI-~P7RXI-	A, I	These are negative receive differential pair used for 10Base-T, 100Base-TX, and 100Base-FX	-

2. Registers Description

The first seven registers of the MII registers are defined by the MII specification. Other registers are defined by IC Plus Corp. for internal use and are reserved for specific use.

Register	Description
0	Control Register
1	Status Register
2	PHY Identifier 1 Register
3	PHY Identifier 2 Register
4	Auto-Negotiation Advertisement Register
5	Auto-Negotiation Link Partner Ability Register
6	Auto-Negotiation Expansion Registers
16	PHY Specification Control Register 1
18	PHY Status Monitoring Register
20	PHY Specification Control Register 2
23	MDI/MDIX Control Register

Mode

RO : Read Only
RW : Read/Write

LL : Latch Low until cleared
LH : Latch High until cleared
SC: Self Clearing

Register0 : Control Register

Reg.bit	Name	Description	Mode	Default
0.[15]	Reset	1=PHY reset. This bit is self-clearing.	RW/SC	0
0.[14]	Loopback	1=Enable loopback. This will loopback TXD to RXD internally 0=Normal operation.	RW	0
0.[13]	Spd_Sel	Manual speed selection 1=100Mbps 0=10Mbps When Auto-Negotiation is disabled, this bit is used to select the link speed. When Auto-Negotiation is enabled, this bit can be read or written, but the state of this bit have no effect on the link configuretion. Whether Auto-Negotiation is enabled or disabled, this bit reflects the opearting speed of the link when it is read.	RW	1
0.[12]	Auto Negotiation Enable	1 = Enable auto-negotiation process. 0 = Disable auto-negotiation process. In 100BASE-FX mode, this bit was read as 0. (Read only)	RW	1
0.[11]	Power Down	1=Power down. All functions will be disabled except SMI read/write function. 0=Normal operation.	RW	0
0.[10]	Isolate	1 = Electrically isolate the PHY from SS-SMII. PHY is still able to respond to MDC/MDIO. 0 = Normal operation	RW	0
0.[9]	Restart Auto Negotiation	1=Restart Auto-Negotiation process. 0=Normal operation.	RW/SC	0
0.[8]	Duplex Mode	Manual duplex selection 1=Full duplex operation. 0=Half duplex operation. When Auto-Negotiation is disabled, this bit is used to select the duplex mode. When Auto-Negotiation is enabled, this bit can be read or written, but the state of this bit have no effect on the link configuration. Whether Auto-Negotiation is enabled or disabled, this bit reflects the operating duplex mode of the link when it is read. In 100BASE-FX mode and direct LED is disabled, the initial setting of pin93 can overwrite the default value of this bit.	RW	1
0.[7:0]	Reserved			0

*SMI : Serial Management Interface , which is composed of MDC,MDIO, allows the MAC to manage the PHY.

Register1 : Status Register

Reg.bit	Name	Description	Mode	Default
1.[15]	100Base_T4	0 = no 100Base-T4 capability.	RO	0
1.[14]	100Base_TX_FD	1=100Base-TX full duplex capable 0= not 100Base-TX full duplex capable	RO	1
1.[13]	100Base_TX_HD	1=100Base-TX half duplex capable 0= not 100Base-TX half duplex capable	RO	1
1.[12]	10Base_T_FD	1=10Base-T full duplex capable 0= not 10Base-T full duplex capable	RO	1
1.[11]	10Base_T_HD	1=10Base-T half duplex capable 0= not 10Base-T half duplex capable	RO	1
1.[10:7]	Reserved		RO	0
1.[6]	MF Preamble Suppression	The IP108A will accept management frames with preamble suppressed. IP108A accepts management frame without preamble. Minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions (as defined in IEEE802.3u spec).	RO	1
1.[5]	Auto-negotiate Complete	1=Auto-negotiation process completed. Reg.4,5 are valid if this bit is set. 0=Auto-negotiation process not completed.	RO	0
1.[4]	Remote Fault	1=Remote fault condition detected. 0=No remote fault. In 100Base-FX mode, this bit means the in-band signal Far-End-Fault is detected. Refer to FX MODE section.	RO/LH	0
1.[3]	Auto-Negotiation Ability	1= auto-negotiation capable. (permanently =1) 0=Without auto-negotiation capability.	RO	1
1.[2]	Link Status	1=Link has never failed since previous read. 0=Link has failed since previous read. If link fails, this bit will be set to 0 until bit is read.	RO/LL	0
1.[1]	Jabber Detect	1=Jabber detected. 0=No Jabber detected. The jabber function is disabled in 100Base-TX mode. Jabber is supported only in 10Base-T mode. Jabber occurs when a predefined excessive long packet is detected for 10Base-T. When the duration of TXEN exceeds the jabber timer (52ms), the transmit and loopback functions will be disabled and the COL LED starts blinking. After TXEN goes low for more than 524 ms, the transmitter will be re-enabled and the COL LED stops blinking.	RO/LH	0
1.[0]	Extended Capability	1=Extended register capable. (permanently =1) 0=Not extended register capable.	RO	1

Register2: PHY Identifier 1 Register

Reg.bit	Name	Description	Mode	Default
2.[15:0]	OUI	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively. The OUI of IC Plus Corp. is 24'h0090C3	RO	0243 h

Register3 : PHY Identifier 2 Register

Reg.bit	Name	Description	Mode	Default
3.[15:10]	OUI	Assigned to the 19th through 24th bits of the OUI.	RO	000011b
3.[9:4]	Model Number	Manufacturer's model number 18h.	RO	011000b
3.[3:0]	Revision Number	Manufacturer's revision number 00.	RO	0000 b

Register4 : Auto-Negotiation Advertisement Register

Reg.bit	Name	Description	Mode	Default
4.[15]	Next Page	0=Next Page disabled. (Permanently =0)	RO	0
4.[14]	Reserved		RO	0
4.[13]	Remote Fault	1=Advertises that IP108A has detected a remote fault. 0=No remote fault detected.	RW	0
4.[12]	Reserved		RO	0
4[11]	Asymmetric Pause	1=Advertises that IP108A support asymmetric pause operation. 0=Not support asymmetric pause operation.	RW	0
4.[10]	Pause	1=Advertises that IP108A has flow control capability. 0=Without flow control capability. When direct LED is disabled, this bit is set by pin 67 TP_PAUSE in 100BASE-TX mode or pin 85 FX_PAUSE in 100BASE-FX mode upon reset.	RW	1
4.[9]	100Base-T4	Technology not supported. (Permanently =0)	RO	0
4.[8]	100Base-TX-FD	1=100Base-TX full duplex capable. 0=Not 100Base-TX full duplex capable.	RW	1
4.[7]	100Base-TX	1=100Base-TX half duplex capable. 0=Not 100Base-TX half duplex capable.	RW	1
4.[6]	10Base-T-FD	1=10Base-T full duplex capable. 0=Not 10Base-T full duplex capable.	RW	1
4.[5]	10Base-T	1=10Base-T half duplex capable. 0=Not 10Base-T half duplex capable.	RW	1
4.[4:0]	Selector Field	[00001]=IEEE802.3	RO	00001

Register5 : Auto-Negotiation Link Partner Ability Register

Reg.bit	Name	Description	Mode	Default
5.[15]	Next Page	1=Link partner desires Next Page transfer. 0=Link partner does not desire Next Page transfer.	RO	0
5.[14]	Acknowledge	1=Link Partner acknowledges reception of FLP words. 0=Not acknowledged by Link Partner.	RO	0
5.[13]	Remote Fault	1=Remote Fault indicated by Link Partner. 0=No remote fault indicated by Link Partner.	RO	0
5.[12]	Reserved		RO	0
5.[11]	Asymmetric Pause	1=Link partner support asymmetric pause operation. 0=Link partner not support asymmetric operation. When the auto-negotiation is disabled, this bit is set to 1. After parallel detection, this bit is set to 1.	RO	0
5.[10]	Pause	1=Flow control supported by Link Partner. 0=No flow control supported by Link Partner. When the auto-negotiation is disabled, this bit is set to 1. After parallel detection, this bit is set to 1.	RO	0
5.[9]	100Base-T4	1=100Base-T4 supported by Link Partner. 0=100Base-T4 not supported by Link Partner.	RO	0
5.[8]	100Base-TX-FD	1=100Base-TX full duplex supported by Link Partner. 0=100Base-TX full duplex not supported by Link Partner. For 100Base-FX mode, this bit is set when Reg.0.8=1 or FX_DUPLEX =1. When the auto-negotiation is disabled, this bit is set when Reg.0.13=1 and Reg.0.8=1.	RO	0
5.[7]	100Base-TX	1=100Base-TX half duplex supported by Link Partner. 0=100Base-TX half duplex not supported by Link Partner. For 100Base-FX mode, this bit is set when Reg.0.8=0 or FX_DUPLEX =0. When the auto-negotiation is disabled, this bit is set when Reg.0.13=1 and Reg.0.8=0. After parallel detection, this bit is set when the result of auto-negotiation is 100BASE-TX.	RO	0
5.[6]	10Base-T-FD	1=10Base-T full duplex supported by Link Partner. 0=10Base-T full duplex not supported by Link Partner. When the auto-negotiation is disabled, this bit is set when Reg.0.13=0 and Reg.0.8=1.	RO	0
5.[5]	10Base-T	1=10Base-T half duplex supported by Link Partner. 0=10Base-T half duplex not supported by Link Partner. When the auto-negotiation disabled, this bit is set when Reg.0.13=0,and Reg.0.8=0. After parallel detection, this bit is set when the result of auto-negotiation is 10BASE-T.	RO	0
5.[4:0]	Selector Field	[00001]=IEEE802.3	RO	00001

Register6 : Auto-Negotiation Expansion Register

Reg.bit	Name	Description	Mode	Default
6.[15:5]	Reserved		RO	0
6.[4]	Parallel Detection Fault	1=A fault has been detected via the Parallel Detection function. 0=A fault has not been detected via the Parallel Detection function.	RO/LH	0
6.[3]	Link Partner Next Page Able	1= Link Partner is Next Page able. 0= Link Partner is not Next Page able. (permanently=0)	RO	0
6.[2]	Local Next Page Able	1= IP108A is Next Page able. 0= IP108A is not Next Page able.	RO	0
6.[1]	Page Received	1= A New Page has been received. 0= A New Page has not been received.	RO/LH	0
6.[0]	Link Partner Auto-Negotiation Able	If Nway is enabled, this bit means: 1= Link Partner is Auto-Negotiation able. 0= Link Partner is not Auto-Negotiation able.	RO	0

Register16 : PHY Specification Control Register 1 (default = 16'h118C)

Reg.bit	Name	Description	Mode	Default
16.[15]	DIRECTLED_BI	When the chip operates at LED direct-drive mode (LEDMODE[1:0]=11 b), this bit is set high for Bi-color LED	RW	0
16.[14]	SLEW_RATE	This bit is used to control I/O output slew rate 0= Normal Slew Rate 1= Faster Slew Rate The initial setting of pin106 can overwrite the default of this bit.	RW	1 (Pin 106)
16[13]	CONSISTENCY_RF	When this bit is set to 0, IP108A asserts consistency_match during auto negotiation process by ignoring RF bit. 0: RF bit is ignored. 1: RF bit is considered.	RW	0
16[12]	FORCE_MODE_LED	0: In force mode, IP108A LED will show the operating mode before link up. 1: In force mode, IP108A LED will not show the operating mode before link up. When direct LED is disabled, the inverse value of initial setting of pin 92 can overwrite the default of this bit.	RW	1 (Pin 92)
16.[11]	MLT3_DET_EN	Set high to enable MLT3 detection function. When MLT3 detection function is enabled, IP108A supports manually (without auto negotiation) speed change from 10Mbps to 100Mbps by link partner. 1: Enable MLT3 detection function 0: Disable MLT3 detection function When direct LED is disabled, the inverse value of initial setting of pin 105 can overwrite the default of this bit.	RW	1 (Pin 105)
16.[10]	RXCLK_INV	Set high to reverse the RXCLK in SS-SMII mode. 1: Reverse the SS-SMII receiver clock. 0: Not reverse the SS-SMII receiver clock. The initial setting of pin 66 can overwrite the default of this bit.	RW	0 (Pin 66)
16[9]	RXCLK_DLY	Set high to delay RXCLK in SS-SMII mode. 1: Delay the SS-SMII RXCLK output. 0: not delay the SS-SMII RXCLK output The initial setting of pin 84 can overwrite the default of this bit. The combination of bits 16[10] and 16[9] can adjust the SS-SMII receive timing. The detail setting of receive timing adjustment is referred to the section of "AC Characteristics".	RW	0 (Pin 84)
16.[8]	SS-SMII_MODE	This bit is used to select either SS-SMII mode 0: Reserved 1: SS-SMII mode When direct LED is disabled, the initial setting of pin 53 can overwrite the default of this bit.	RW	1 (Pin 53)

Reg.bit	Name	Description	Mode	Default
16.[7]	APS_ON	This bit is used to activate Auto Power Saving (APS) mode 0: Disable 1: Enable	RW	1
16.[6]	NWAY_PWSV_OFF	Set high to disable the power saving during Auto-Negotiation procedure 0: Enable Power Saving 1: Disable Power Saving	RW	0
16[5]	AUTO_MDIX_ALL_EN	Auto-crossover for all ports 0: Disable auto-crossover function for all ports 1: Enable auto-crossover function for all ports When this bit is set to high, auto-crossover function can be disabled per port by MII register 23 bit 15~8.	RW	1
16.[4]	FEF_DISABLE	Set high to disable the functionality of Far-End Fault when the chip operates at fiber mode 0: Enable FEF 1: Disable FEF	RW	0
16.[3]	REPEAT_MODE	Set high to let IP108A operate at repeat mode 0: Not Repeat mode 1: Repeat mode When direct LED is disabled, the initial setting of pin81 can overwrite the default of this bit.	RW	1 (Pin 81)
16.[2]	JABBER_ENA	Set high to enable jabber detection mechanism when IP108A operates at 10BASE-T 0: Disable 1: Enable	RW	1
16.[1]	HEARTBEAT_ENA	Set high to enable heartbeat detection mechanism when IP108A operates at 10BASE-T 0: Disable 1: Enable	RW	0
16.[0]	BYPASS_DSPRST	Set high to disable DSP reset watch-dog timer 0: Not Bypass 1: Bypass	RW	0

Register18 : PHY Status Monitoring Register

Reg.bit	Name	Description	Mode	Default
18.[15]	LDSP_SLEEPING	When is set to high, indicates IP108A is at link-down sleeping mode	RO	0
18.[14]	LINK_OK	When is set to high, indicates link status is OK	RO	0
18.[13]	DESCRAM_LOCK	When is set to high, indicates PCS de-scrambler is locked on data	RO	0
18.[12]	10BASE_POLARITY	When is set to high, indicates the cable polarity is reversal (this bit is meaningful only chip operates at 10BASE-T)	RO	0
18.[11]	RESLOVED_SPEED	To indicate the resolved speed mode 0: 10BASE-T 1: 100BASE-TX/FX	RO	0
18.[10]	RESLOVED_DUPLEX	To indicate the resolved duplex mode 0: Half Duplex 1: Full Duplex	RO	0
18.[9]	MDI/MDIX	To indicate either at MDI or MDIX state 0: MDI (Not Crossover) 1: MDIX(Crossover)	RO	0
18.[8:0]	NWAY_DEBUG_OUT	NWAY debug output	RO	0

Register20 : PHY Specification Control Register 2 (default = 16'h700x)

Reg.bit	Name	Description	Mode	Default
20[15]	PS_MODE_DIS	Disable 10M power saving mode 1: Disable 10M power saving mode 0: Enable 10M power saving mode (default) When PHY operates in test mode or MII loop back mode, 10M power saving is disable even though this bit is read as logic 0.	RW	0
20[14]	PS_MODE_SEL	This bit is used to select the 10M power saving mode if 10M power saving mode is enable 1: 0 to 100 mA current switch (default) 0: 40 to 100 mA current switch When direct LED is disabled, the initial setting of pin 51 can overwrite the default of this bit.	RW	1 (Pin 51)
20[13]	PS_10TX_EN	Enable 10M transmit power saving mode 1: Enable 10M transmit power saving mode (default) 0: Disable 10M transmit power saving mode	RW	1
20[12]	PS_10TX_MODE	This bit is used to select the 10M transmit power saving mode if 10M transmit power saving mode is enable. 1: Mode1 is selected (default) 0: Mode 0 is selected	RW	1
20[11:6]	Reserved	--	--	--
20[5]	SSCLK_EN	Enable spread spectrum clock function When this bit is set high, IP108A drive SS-SMII RXCLK and RXD with spread spectrum technology. It can effectively reduce EMI on SS-SMII interface. 1: Enable spread spectrum clock function 0: Disable spread spectrum clock function When direct LED is disabled, the initial setting of pin 61 can overwrite the default of this bit.	RW	0 (Pin 61)
20[4]	TX_DELAY	SS-SMII transmitting delay Set high to increase SS-SMII input delay about 4ns The initial setting of pin 98 can overwrite the default of this bit.	RW	0 (Pin 98)
20[3:2]	RX_DRIVE[1:0]	Programmable SS-SMII receiving driving capability These 2 bits are used to select SS-SMII receiving pins (RXCLK, RXD, RXSYNC) output driving capability. The initial setting of pin 60,52 can overwrite the default of these bits. The detail setting of output driving capability is referred to the section of "I/O Characteristics Adjustment".	RW	00 (Pin 60,52)
20[1]	MDIO_DRIVE	Programmable MDIO output driving capability 1: 4mA driving capability 0: 8mA driving capability (default)	RW	0
20[0]	LED_DRIVE	Programmable LED output driving capability 1: 12mA driving capability 0: 8mA driving capability (default)	RW	0

Register23 : MDI/MDIX Control Register (default = 16'hff00)

Reg.bit	Name	Description	Mode	Default
23[15:8]	Auto_MDIX	Port7~port0 auto crossover enable 1: Enable auto crossover function. 0: Disable auto crossover function.	R/W	8'hff
23[7:0]	MDIX_SEL	Port7~port0 MDI/MDIX channel selection A port can force the channel to the MDI or MDIX when the port's auto crossover function is disabled. 1: select the MDIX channel. 0: select the MDI channel.	R/W	8'h00

3. Functional description

3.1 Basic Function

3.1.1 Auto negotiation

The IP108A provides auto negotiation function to determine the highest ability between two linked devices.
In addition, the parallel detection is also supported for making a decision on the link partner's ability, which cannot be determined through the auto-negotiation.

3.1.2 4B/5B encoder

The 4B/5B encoder converts the nibble data to 5-bit code group.
The 4B/5B encoder operates on 4-bit nibble and is independent of code group boundary. This encoding method is as following: All combinations of the 4-bit nibble are mapped to 5-bit code groups, plus control code groups, are implemented for a 100Mbps operation at SS-SMII side and 125Mbps on physical medium. When the MII transmitter is enabled, the 4B data from the MII port is encoded into 5B code-groups. The transmit data is packaged by J/K codes at start of packet and by T/R codes at end of packet. When transmit error occurs during the transmitting process, the H code is sent to the medium. The idle code is sent between two packets.

3.1.3 5B/4B decoder

Performing the reverse process of the 4B/5B encoder, the 5B/4B decoder decodes the received code-groups. The 5bit data is decoded into 4 bit nibble data and then this decoded data is forwarded through to MII.
The SSD and ESD are interpreted as the preamble and termination of a packet. And the idle codes are replaced by 0h.

3.1.4 Scrambler/ de-scrambler

The repetitive patterns existing in 4B/5B encoded data results in large RF spectrum peaks. The peak in the radiated signal is reduced significantly by scrambling the transmit signal. The scrambler adds a random data generator to the data signal input, reducing the repetitive data patterns. The scrambler data is de-scrambled at receiver by adding the counterpart of the random generator at the receiver side.

3.1.5 Serial to Parallel/ Parallel to Serial

The parallel to serial block accepts the output of the scrambler, serializes the data, converts the data to NRZI and then shifts the data to the output. TXO pair carries differential NRZI data to the fiber optic transmitter or to MLT-3 transmitter.
The serial to parallel block accepts serial data from DSP receiver, or 100Base-FX receiver and converts them to parallel format for further operation.

3.1.6 Jabber

The Jabber happens while TX_EN is asserted more than 52ms. When this case occurs, the IP108A will disable transmit function and the MII Reg.1.1 is set high until the jabber disappears. The TX_EN must be kept at low for 524ms to guarantee that this bit is cleared to zero.

3.1.7 Loop back

In this loop back mode, the IP108A allows the internal test operation. By writing a 1 to bit14 of MII control register, IP108A will enter loop back mode. In this mode, the TXD data is internally transferred to RXD and the incoming packets on the cable are ignored.

3.1.8 Far End Fault Indication

While 100Base-FX is selected and the signal fault is detected, the MII register.1.4 will be set to “1”. The IP108A asserts 84 consecutive one plus zero 3 times when the signal detection fails or no idle pattern exists, which will cause remote link partner to detect Far End Fault, the IP108A watch problems on receive path. The mechanism is implemented in 100Base-FX and 100Base-TX with 100Base-FX setting to the default value.

3.1.9 Auto MDI/MDIX

In Auto MDIX mode, the IP108A detects the link activity for 80-100ms to determine whether it should swap both pairs. If no link activity is detected within this time, the IP108A waits a random time longer than 80ms and swap transmit/receive pair.

3.1.10 Auto Power Saving (APS) and Power Down mode

IP108A implements per port basis power saving function. While detecting the cable disconnection for more than 2 sec, the IP108A unconditionally enters link down power saving mode. It transmits normal link pulse (NLP)-like pulse on its TXOP/TXON pins every 48ms and detects the incoming signal at RXIP/RXIN pins. The incoming signal may be 100Base-TX MLT-3 idle pattern, 10Base-T link pulses or Nway’s FLP (fast link pulses). While detecting any incoming signals, the IP108A will be waken up from the APS mode and operate in the normal mode according to the result of the link. The APS mode is enabled by default setting and could be disabled by clearing Reg16.[7] (APS_ON) to 0

Setting MII Reg.0.[11] will force the IP108A’s corresponding port entering the power down mode, turning off all function of that port except the SMI (MDC/MDIO management interface).

3.2 I/O Interface

3.2.1 SS-SMII Interface (Source Synchronous SMII)

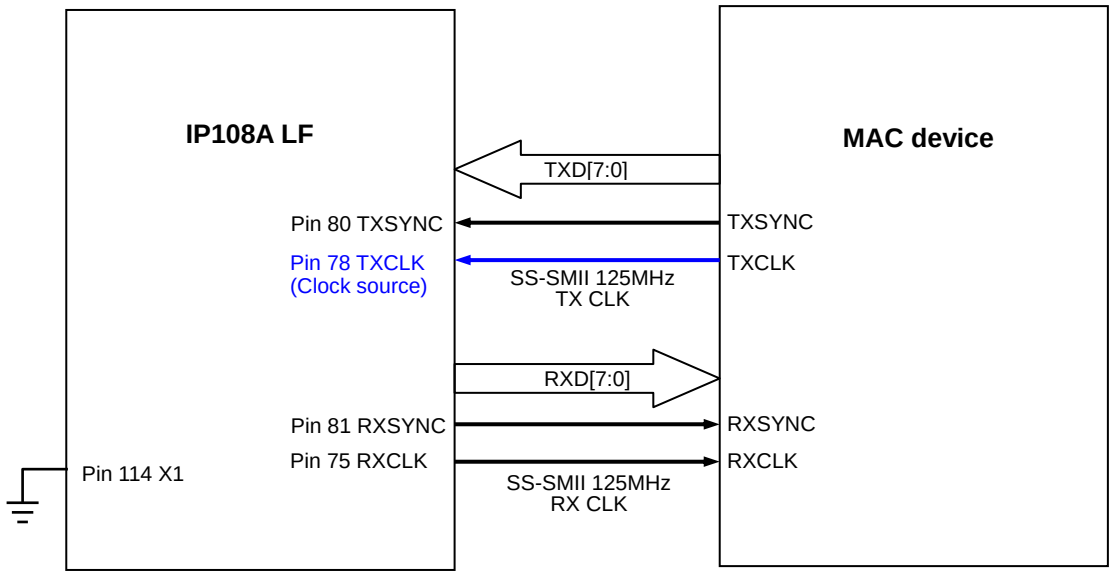
The data transfer through the SS-SMII is synchronous to both the TXCLK and the RXCLK. The TXSYNC and RXSYNC delimit the 10-bit data frame, which corresponds to 8 bit data.

For the TX operation, the IP108A detects the TXSYNC input at the rising edge of the TXCLK to synchronize the internal state machine. Upon detecting the high state of the TXSYNC, the IP108A will recognize the data present at TXD as TX-ER, followed by TXEN and finally 8-port transmit data. Only the frame in which the TXEN is sampled as “high” is recognized as a valid data field.
For the RX operation, the mechanism works in a similar way. The difference is the switch controller will recognize the first data present on RXD is CRS, followed by RXDV and finally 8-port receive data. The IP108A set the RXDV to “1” only when the valid packet is decoded.

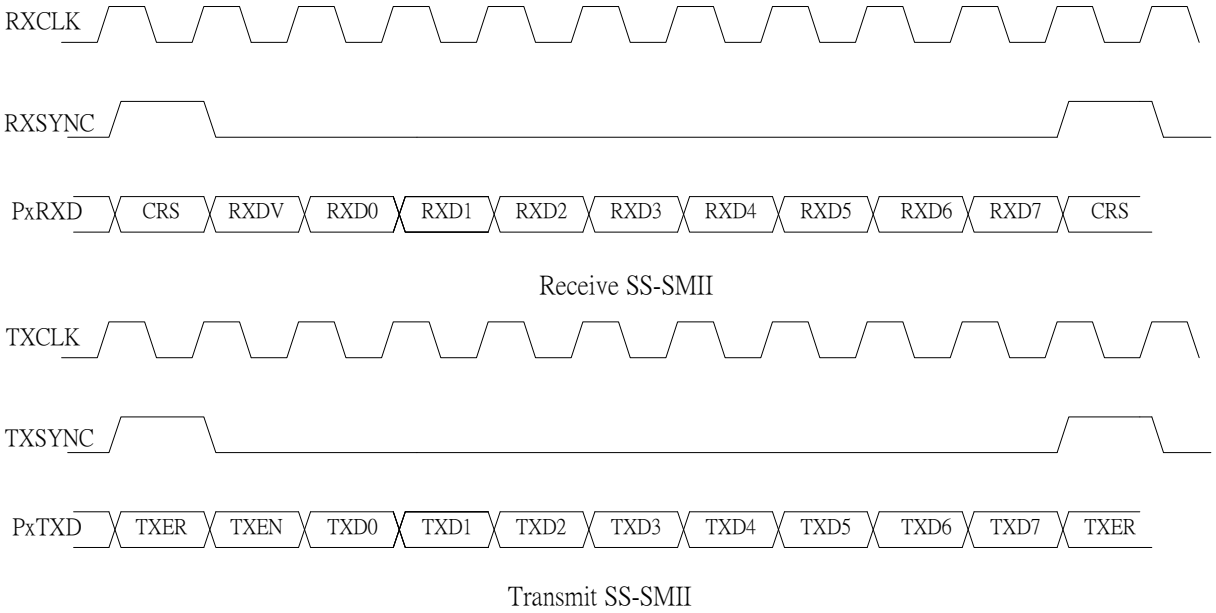
By using this clock scheme, SS-SMII timing constraints can be improved, although it will added side effect for additional traces carrying 125MHz energy.

The IP108A is configured to SS-SMII by setting pin 53 upon power on reset when direct LED is disabled.
For a given IP108A port, the SS-SMII consists of six signals.
RXD-one bit data for receiver
TXD- one bit data for transmitter
TXSYNC- This signal is driven by MAC.
RXSYNC- This signal is driven by PHY.
TXCLK- This signal is driven by MAC
RXCLK- This signal is driven by PHY.

Note that the TXCLK, RXCLK, TXSYNC and RXSYNC pins are shared by all ports.



SS-SMII application block diagram



CRS	RX_DV	RXD0	RXD1	RXD2	RXD3	RXD4	RXD5	RXD6	RXD7
X	0	RXER from previous frame	Speed 0=10Mbps 1=100Mbps	Duplex 0=Half 1=Full	Link 0=Down 1=up	Jabber 0=OK 1=Detected	Upper Nibble 0=Invalid 1=Valid	False Carrier 0=OK 1=Detected	1
X	1	One byte data							

During the idle state, RX_DV=0, the serial bits mean specified purpose.

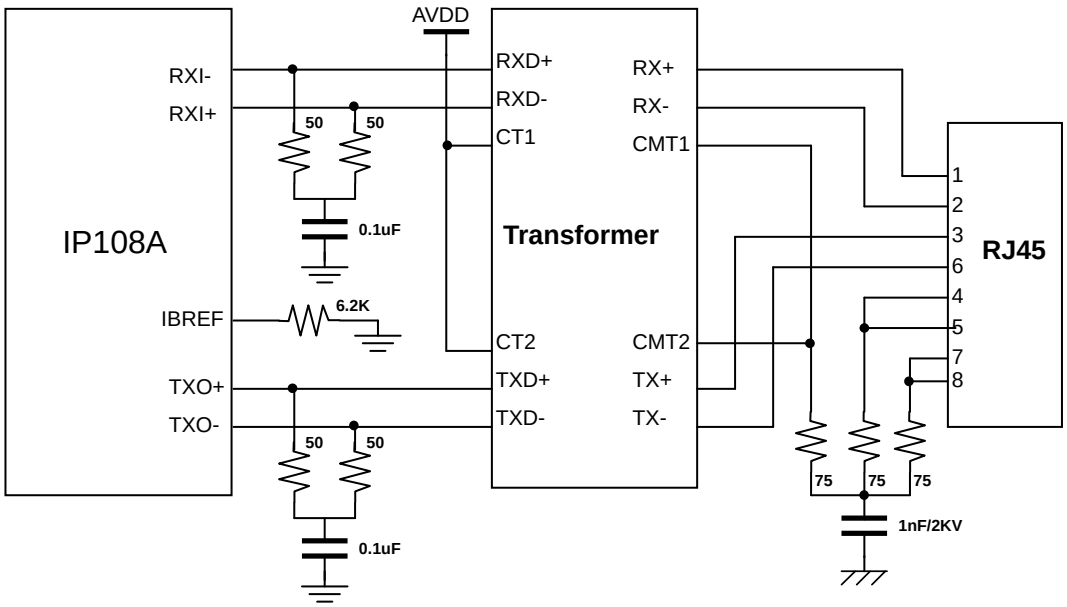
3.2.2 SMI (Serial Management interface)

SMI consists of two signals, the MDC and the MDIO. Through these two pins, the switch controller can read/configure the status of the PHY. The MDC is a clock pin, ranging from DC to 25MHz, and the MDIO is the data transferred between the switch controller and the IP108A.
The IP108A also supports preamble suppression, and it allows the Switch controller to issue read/write cycle without preamble. However, 32-bit preamble is needed for first SMI cycle after power on reset.

MII Management Interface For Read/Write Cycles								
	Preamble (32 bits)	Start bit (2 bits)	OP Code (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1……..1	01	10	AAAAA	RRRRR	Z0	D…….D	Z*
Write	1……..1	01	01	AAAAA	RRRRR	10	D…….D	Z*

MDIO must be pulled high by external 1.5Kresistor when bus is inactive. Z means high impedance

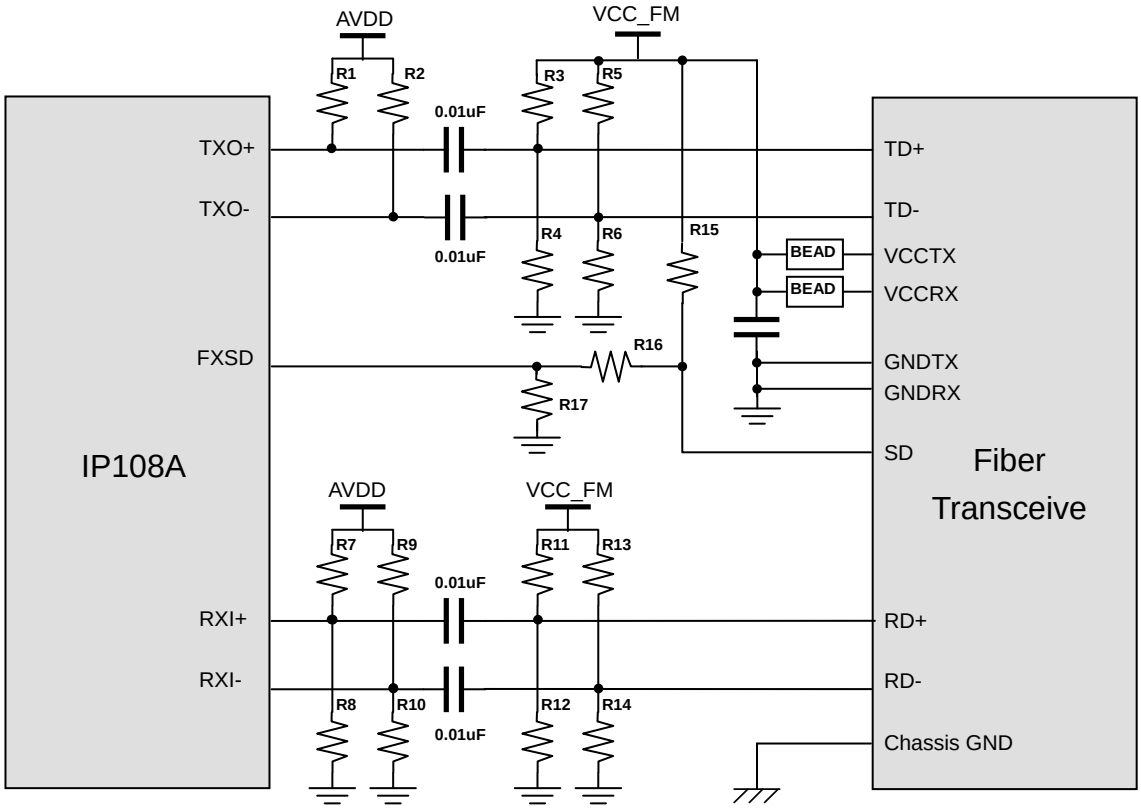
3.2.3 Guideline for the connection to a transformer



Auto MDIX Configuration

TXO+/- can be connected to the pin 1,2 of RJ-45 module, and RX+/- to pin 3,6. The auto MDIX function is enabled upon power on reset. The Central Tap (CT pin) must be tied high (1.95V AVDD) and cannot be connected to ground or unconnected.
A 75 ohm termination resistors are needed for the unused pin of RJ45, which offers balance mechanism in order to minimize common mode noise.

3.2.4 Guideline for the connection to a fiber MAU



R1,R2=100
R7,R9=10K
R8,R10=15K

Fiber MAU VCC(VCC_FM)=3.3V
R3,R5,R11,R13=130
R4,R6,R12,R14=82
R15=8.2K
R16=470
R17=10K

Fiber MAU VCC(VCC_FM)=5V
R3,R5,R11,R13=82
R4,R6,R12,R14=130
R15=22K
R16=5.9K
R17=10K

100Base-FX Configuration

3.3 Pin Setting for LED mode and driving capability

3.3.1 LED Mode Setting

IP108A supports either serial LED status streams or parallel direct-drive for LED display. The format of LED status driving modes, as shown below, are controlled by LEDMODE[1:0] and LED2_COLBLK pins, which are latched upon reset. All LED statuses are represented as active-low, except Link/Act whose polarity depends on Spd status in bi-color mode

LEDMODE[1:0]	LED2_COLBLK	Mode	Output sequences
00	No effect	3-bit serial stream	Col / Fulldup, Link/Act, Spd
01	No effect	2-bit serial stream	Spd, Link/Act
10	1	3-bit for Bi-color LED	Col / Fulldup, Link/Act, Spd
	0	3-bit for Bi-color LED	Fulldup, Link/Act, Spd
11	1	Mono-color LED direct-drive	Col / Fulldup, Link/Act, Spd

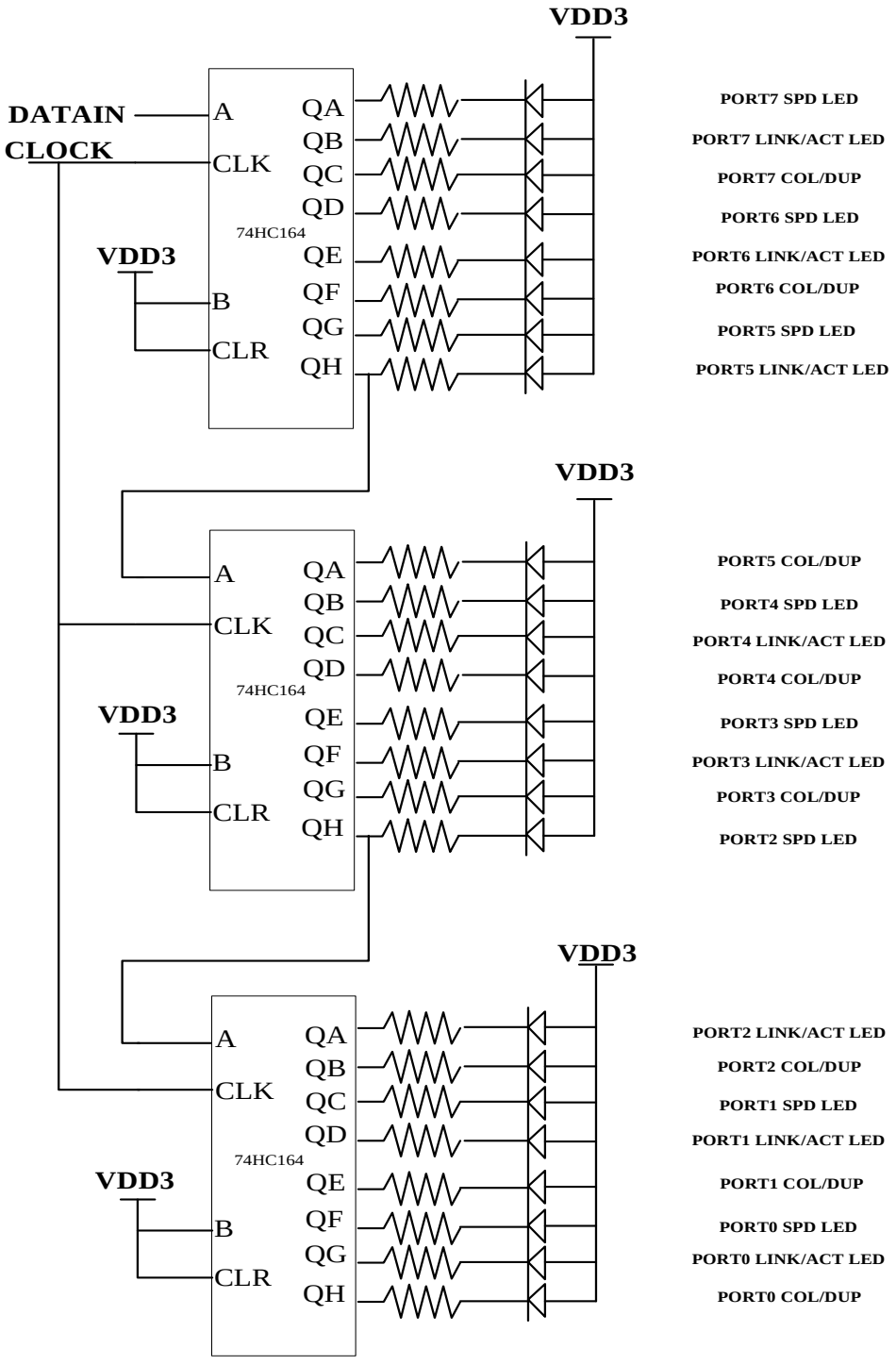
LED Indication	Description
Col / Fulldup	Col, Full duplex Indicator. Blinking every 48ms when collision happens. Low for full duplex, and high for half duplex mode. The blinking function can be disabled in 3-bit bi-color LED mode (LEDMODE[1:0]=10) if pin 74 LED2_COLBLK_EN is set to 0.
Link / Act	Link, Activity Indicator. For 3-bit serial stream mode, low for link established. For 3-bit Bi-color LED mode and 100Mbps, the Link/Act is high for link established. For 3-bit Bi-color LED mode and 10Mbps, the Link/Act is low for link established. The LED blinks every 48ms when the corresponding port is transmitting or receiving.
Spd	Speed Indicator. Low for 100Mbps, and high for 10Mbps.

3.3.2 LED blinking setting time

The IP108A also provides 48/128ms LED blinking time setting through pin 65 LED_BLK_TIME upon power on reset, The LED's blinking time of the Col/Fulldup and the Link/Act will change according to this pin setting.

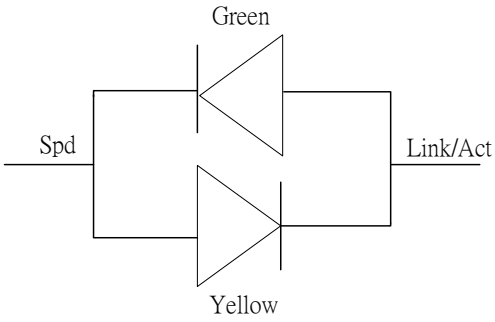
3.3.3 Serial stream sequence

Bits stream are output sequentially from port0 to port7 .For 2-bit serial stream mode, the sequence is Spd at first and then Link/Act. For 3-bit serial stream mode, the sequence is Col/Fulldup, Link/Act, then Spd.



Exteranl TTL for 3 Bit Serial Stream LED Mode

3.3.4 Bi-color Configuration



Spd	Link/Act	LED indication	Bi-color state
0	0	Unlink	Dark
1	1	Unlink	Dark
0	1	100Mbps Link	Green is light
0	1-0-1-0…	100Mbps Link and Active	Green is blinking
1	0	10Mbps Link	Yellow is light
1	0-1-0-1…	10Mbps Link and Active	Yellow is blinking

3.4 I/O characteristics Adjustment

3.4.1 SS-SMII I/O driving capability adjustment.

Driving capability control RX_DRIVE[1:0] (pin 60, 52/ register 20[3:2]) for SS-SMII pins (pin 75,52,60,66,74,84,92,98,52,60,106,81)

RX_DRIVE[1:0]	VDDIO_=1.95v		VDDIO_=3.3v	
	RXCLK	PxRXD, RXSYNC	RXCLK	PxRXD, RXSYNC
00	11mA	8mA	8mA	4mA
01	6mA	3mA	6mA	3mA
10	11mA	8mA	11mA	8mA
11	8mA	4mA	8mA	4mA

3.4.2 LED pin driving capability adjustment

Driving capability control (register 20[0]) for LED pins

Register 20[0]	Driving current of LEDDATA, LEDCLK, LINK_ACT_LED, SPD_LED, COL_FUL_LED,
0	8mA
1	12mA

3.4.3 MDIO pin driving capability adjustment

Driving capability control (register 20[1]) for MDIO pin

Register 20[1]	Driving current of MDIO
0	8mA
1	4mA

4. Operational Description

4.1 Resetting the IP108A

The IP108A can be initialized through 3 ways, including 1: power on reset, 2:Hardware reset, 3:Software reset via setting MII register. The reset must be keep low for at least 1ms. LED will blink upon power on if DISBLINK pin is set to “low” during reset.

4.2 Transmit Function and Receive Function

4.2.1 100Base-TX Mode

While TX_EN is asserted, the IP108A converts TXD data from SS-SMII interface into 5 bit code group data starting with first two code groups called SSD (J/K code groups). The data code groups following the SSD are transmitted as long as TX_EN keeps in high state. Upon TX_EN goes low, T/R code groups will be appended to the last data code group
During inter-packet gap, idle code groups are transmitted, keeping the signal transition for the link partner to synchronize the clock. The transmit path includes 4B/5B encode, Scrambler, parallel to serial, NRZ to NRZI encoder, NZRI to MLT-3 encoder. The scrambling technology can average signal’s power energy. The wave shaping filter can reduce EMI effect.
While SSD is detected at receiver side, the TX_DV is asserted within several bit time. The receive path includes MLT-3 to NRZI decode, NRZI to NRI decode, serial to parallel, De-scrambler, and 5B/4B decode, MII to SS-SMII conversion.
On chip PLL circuit extracted clock from the incoming data stream. This recovered 125MHz clock is used to generate the 25MHz RX_CLK signal for MII interface. Active hybrid DC wander correction can compensate baseline wander, reducing the bit error rate.

4.2.2 100Base-FX Mode

Operating with PECL level and NRZI code, the IP108A transceiver can interface with external fiber optic transceiver instead of the transformer used in TP cable.
The IP108A can be configured as 100Base-FX through hardware strapping pin. A port will work at 100Base-FX if its corresponding FXSD is connected to the SD signal of a fiber MAU.

In 100Base-FX mode, the serial data stream can be directly driven out through fiber transceiver driver using NRZI PECL signals, The data stream is not scrambled for fiber transmission.
Receiver accepts receive differential signals from fiber transceiver without de-scrambler, serial data is directly output to related circuit for further processing.

4.2.3 10Base-T Mode

Unlike the MLT-3 code used in 100 base-TX mode, the IP108A use Manchester encoder/decoder to transmit/receive data. The Manchester code provides enough transition for the link partner to recover the clock and keeps the power energy at the allowable level.
The operation of 10 Base-T mode follows the IEEE802.3 standard. Both full-duplex and half duplex modes are supported by the IP108A.

5. **Layout** guideline

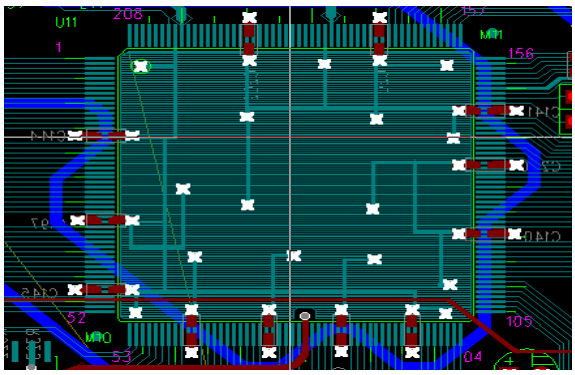
The following sections include recommendations for the IP108A board layout guidelines.
– General layout guideline
– Twisted pair guideline
– SS-SMII layout guideline
– Power filter recommendation
– MDC and MDIO recommendation

5.1 General Layout Guideline

Pay attention to layout throughout entire layout process is necessary .The following guide will help the customer achieve the maximum system performance.

-
- Use decoupling capacitors to decouple high frequency noise between chip's power and ground, must be as close as possible to IP108A. (Figure1)

Figure 1



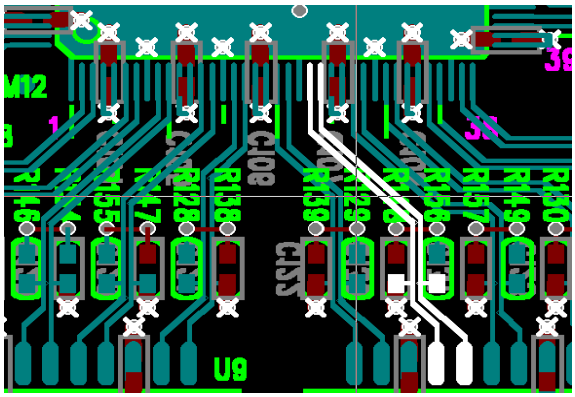
-
- Use guard traces around the clock trace to reduce the EMI effect.
- Avoid signals path parallel to clock signals path, such as MDC and X1signals. The clock signals will interfere with other parallel signals, degrading signal quality.
- Keep the clock jitter as low as possible. The clock error should be less than 100ppm for 25/50/125MHz
- Avoid high speed signal getting across ground gap to prevent large EMI effect
- Keep ground region as one continuous and unbroken plane
- Place a gap between the system ground and the chassis grounds
- No any ground loop exists on the chassis ground.
- Leave outer edge of PCB voided on all layer to minimize fringe effects.

5.2 Twisted Pair layout guideline

When routing the TXO+/- signal traces from the IP108A to transformer, you should keep the trace as short as possible. The termination resistors should be as close as possible to the output of the TXO+/- pair of IP108A, The central tap of primary winding of these transformers must be connected to analog 1.95V. It is recommended that RXI+/- trace pair be routed far away from the other pairs, separating individual trace from one another.
In order to prevent the PCB from the ESD damage, it is recommended that the traces between the phone jack and the transformer are away from other signals at least 80 mils, including power ground and

chassis ground. The trace between the transformer and the RJ-45 phone jack should not pass any via, minimizing the impedance-matching problem.

Figure 2



5.3 SS-SMI layout guideline

The IP108A provide slew rate function to adjust rise and fall times, balancing the high frequency energy and the I/O driving capability. For long distance high frequency trace, the adjustment of driving capability may be crucial to the EMI and the system stability.
In addition, the following rules can help the designer to achieve the required performance.

- Layout the traces as short as possible to minimize the high frequency energy radiation.
- Each signal trace should be matched by a series resistor to maintain the signal quality.
- Keep the TXD,TXSYNC,TXCLK signal traces matched in length as possible. Similarly the receive part behaves in the same way.

5.4 Power filter recommendation

In most application system, the power quality is very important. Because the device maybe very sensitive to power noise, the Bead and the capacitor are often used. The Bead can prevent the high frequency from entering the power source. The capacitor can decouple noise by passing the noise to ground. These devices can reduce the noise interference and enhance system performance.
The decoupling capacitor (around 0.1uf to 0.01uf) should be placed at each pair of power pins to minimize the high frequency present at the power pins. The larger value capacitors, such as 10uf, should be scattered around the chip to stabilize the power input.

5.5 MDC and MDIO recommendation

In some high port count switch system, the driving source of MDC probably is routed for a long distance. For this application, the MDC can be buffered by a low slew rate driver and the trace at each driver output is terminated by a series resistor. The MDC should be kept away from other high-speed signal, avoiding the interference to each other.

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the Recommended Operating Conditions section. Exposure to the Absolute Maximum Conditions for extended periods may affect device reliability.

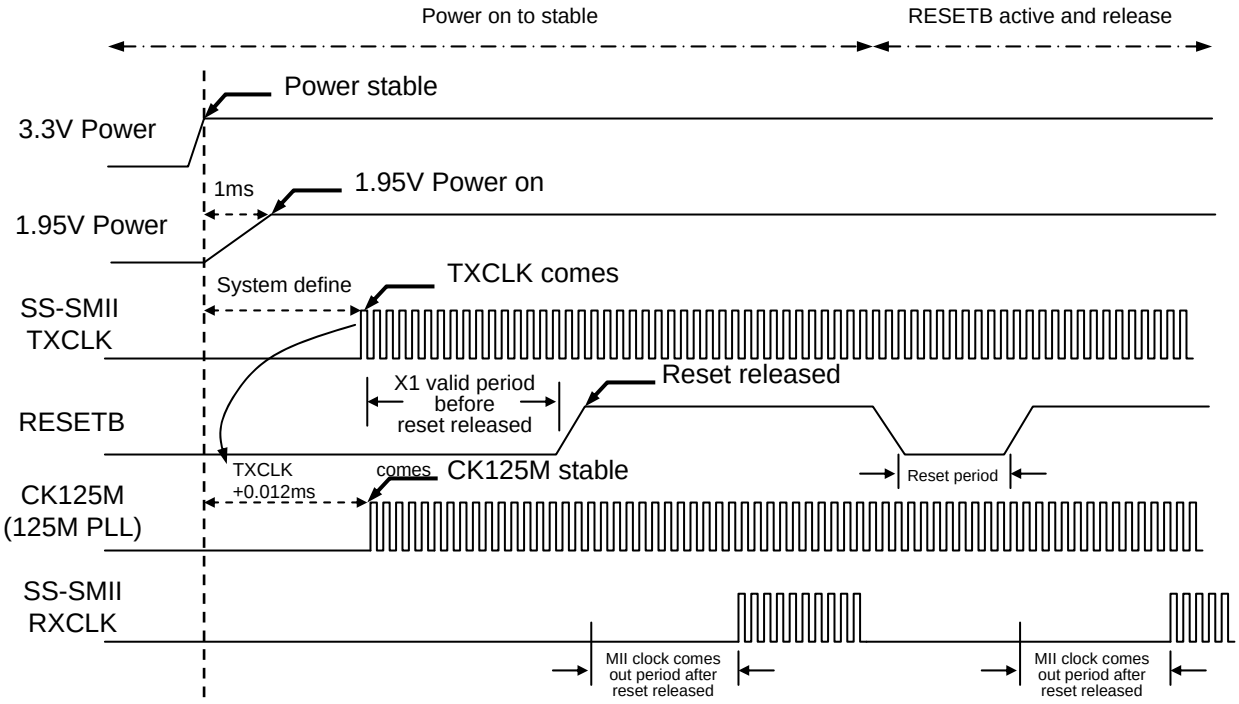
PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	I/O	VDDIO	– 0.5	+3.6V	V
	Core	VDDC	– 0.5	+2.05V	V
Input Voltage		V_I	– 0.5	$V_{DDI/O}$	V
Output Voltage		V_O	– 0.5	$V_{DDI/O}$	V
Storage Temperature		T_{STG}	-65	+150	°C
Operation Temperature		T_{OPT}	0	+70	°C
IC junction temperature		T_J	0	+125	°C

Note: The maximum ratings are the limit value that must never be exceeded even for short time.

6.2 AC Characteristics

Power On Sequence and Reset Timing

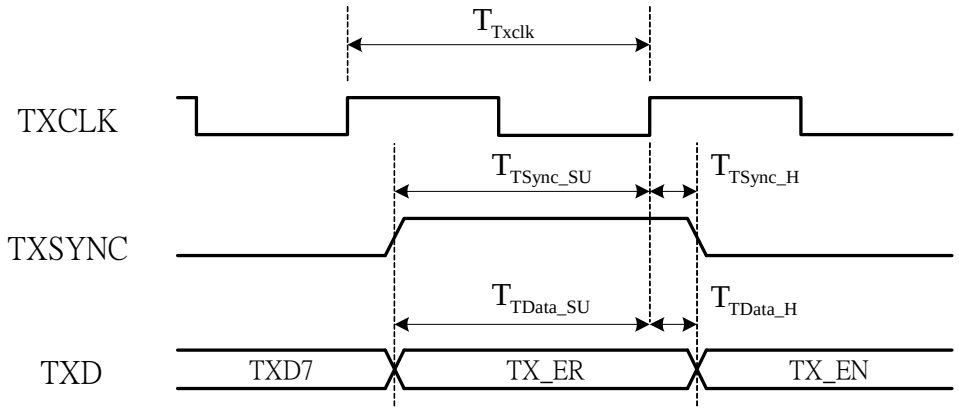
Description	Min.	Typ.	Max.	Unit
SS-SMII TXCLK valid period before reset released	10	-	-	ms
Reset period	10	-	-	ms
SS-SMII RXCLK comes out period after reset released	-	2	-	ms



SS-SMII Transmit Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{Txclk}	Transmit clock cycle time	-	8	-	ns
T_{TSync_SU}	TXSYNC Set up time	1.5			ns
T_{TSync_H}	TXSYNC Hold time	0.5	-		ns
T_{TData_SU}	TXD Set up time	1.5			ns
T_{TData_H}	TXD Hold time	0.5	-		ns

Note: The TX_DELAY function is disabled.

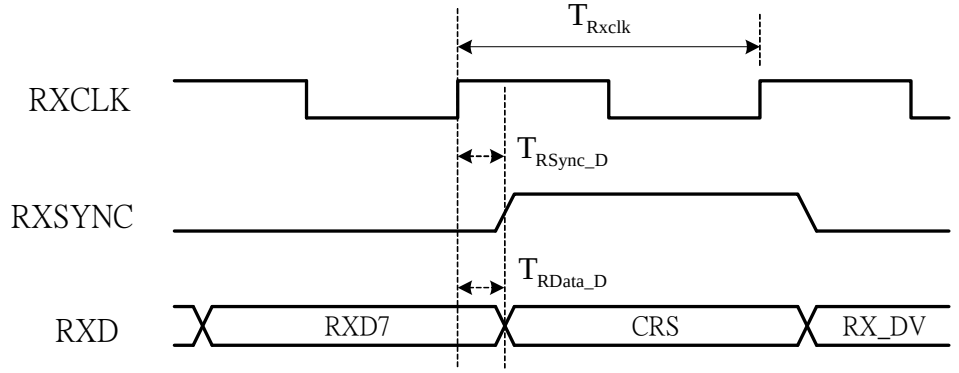


SS-SMII Transmit

SS-SMII Receive Timing

Symbol	Description	Min.	Typ.	Max.	Unit	Load
T_{Rxclk}	Receive clock cycle time	-	8	-	ns	5pF
T_{RSync_D}	RXCLK to RXSYNC output delay	1.5		5.0	ns	5pF
T_{RData_D}	RXCLK to RXD output delay	1.5	-	5.0	ns	5pF

Note: 1. The I/O driving capability is set to {00}.
2. The RX_CLK_INV and RX_DELAY function are disabled.



SS-SMII Receive

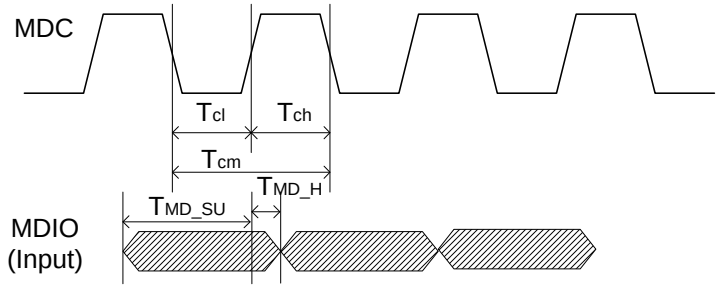
SS-SMII receive timing adjustment

The SS-SMII receive timing can be adjust by change the initial setting of pin {66,84} or modify the value of MII registers 16[10] and 16[9] through serial management interface (SMI).

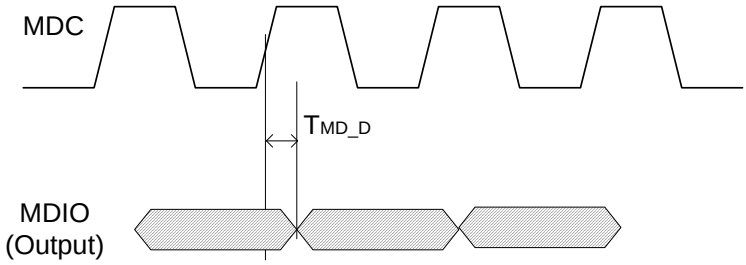
Pin setting	MII Register	RXCLK to RXSYNC and RXD output delay			
Pin {66.84}	**Reg 16[10:9]**	**Min.**	**Max.**	**Unit**	**Load**
00	00	1.5	5.0	ns	5pF
01	01	3.0	6.5	ns	5pF
10	10	5.5	1.0 (Next clock edge)	ns	5pF
11	11	7.5	3.0 (Next clock edge)	ns	5pF

PHY Management (MDIO) Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{ch}	MDC High Time		200		ns
T_{cl}	MDC Low Time		200		ns
T_{cm}	MDC Cycle Time		400		ns
T_{MD_SU}	MDIO set up time	10	-		ns
T_{MD_H}	MDIO hold time	10	-	-	ns
T_{MD_D}	MDIO output delay time (relative to rising edge of MDC)	2	-	20	ns



MDIO Input Cycle



MDIO Output Cycle

6.3 DC Characteristics

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Output low voltage		V_{OL}	-	-	0.4	V
Output high voltage		V_{OH}	0.9 VDDIO I/O supply voltage	-	-	V
Low level output current		I_{OL}	-	24	-	mA
High level output current		I_{OH}	-	13	-	mA
Input Low Voltage	VDDIO =3.3V	V_{IL}	-	-	1.1	V
Input High Voltage		V_{IH}	2.4	-	-	V
Input Low Voltage	VDDIO =1.95V	V_{IL}	-	-	0.7	V
Input High Voltage		V_{IH}	1.5	-	-	V
RESET Threshold		V_{RST}	0.7*VDDC		0.85*VDDC	
X1 Input Low Voltage		V_{ILX1}			0.6	V
X1 Input High Voltage		V_{IHX1}	1.5			V
VDDIO supply current 10M Full active*1 10M Full idle 100M Full active 100M Full idle		I_{VDDIO}	-	 20 20 20 20	-	mA
VDDC supply current 10M Full active 10M Full idle 100M Full active 100M Full idle		I_{VDDC}	-	 60 63 154 152	-	mA
AVDD supply current 10M Full active 10M Full idle 100M Full active 100M Full idle		I_{AVDD}	-	 879 421 503 503	-	mA
Power consumption 10M Full active 10M Full idle 100M Full active 100M Full idle		P	-	 1756 937 1249 1245	-	mW
VDDIO supply voltage		V_{VDDIO}	1.85		3.6	V
VDDC supply voltage		V_{VDDC}	1.85	1.95	2.1	V
AVDD supply voltage		V_{AVDD}	1.85	1.95	2.1	V
Input Threshold point		V_T	1.46	1.60	1.76	V
SS-SMII Input Low to High threshold point [*1]		V_{T+}	1.66	1.75	1.79	V
SS-SMII Input High to Low threshold point [*1]		V_{T-}	0.93	1.01	1.06	V
Fiber/TP mode and Fiber Link detect threshold	FX/TP Selection	V_{FXSD}	0.8		1	V
	FX Link detect		1.72		1.8	V
Fiber Rx common mode Voltage		V_{FRC}	-	AVDD*0.6	-	V
Fiber Rx differential mode Voltage		V_{FRD}	0.4	-	-	V
Pull-down resistor		R_{PD}	51	-	127	KΩ

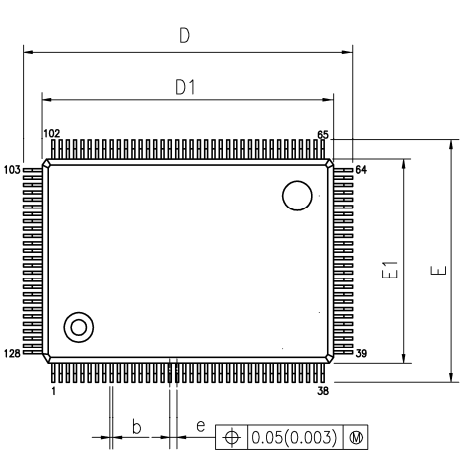
***1 : At SS-SMII interface / Random Packet length / Random Packet**

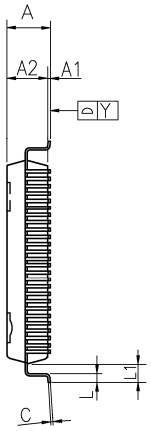
7. Order Information

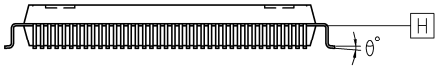
Part No.	Package	Notice
IP108A LF	128 PIN PQFP	Lead-Free
IP108AL LF	128 PIN LQFP	EPAD Lead-Free

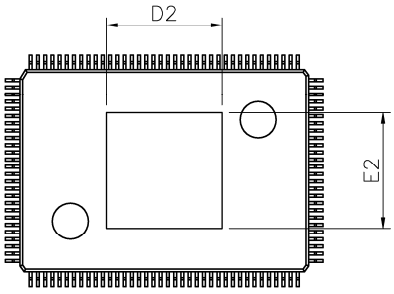
8. Package Detail

128 Pin LQFP Outline Dimensions









EPAD size:270milx270mil

(THERMALLY ENHANCED VARIATIONS ONLY)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
C	0.10	0.15	0.20
D1		20.00 BSC	
E1		14.00 BSC	
e		0.50 BSC	
D		22.00 BSC	
E		16.00 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
Y	–	–	0.08
θ°	0°	3.5°	7°

UNIT : mm

THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
27*X27*	5.83	7.01	5.83	7.01
31*X31*	6.80	8.15	6.80	8.15

⚠ "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,
實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES:
1.JEDEC OUTLINE:
MS-026 BHB.
MS-026 BHB-HD(THERMALLY ENHANCED VARIATIONS ONLY).
2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS E1 AND D1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS E AND E DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .

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