Description

DM6359 combines a highly integrated current mode PWM controller with a high voltage power MOS. it is optimized for high performance,low standby power,and cost effective off line flyback converter application in sub 28W range.

VDD low startup current and low operating current contribute to a reliable power on startup and low standby design with DM6359.

DM6359 offers complete protection coverage with automatic self recovery feature including Cycle-by-Cycle current limiting(OCP),over load protection(OLP),VDD under voltage lockout (UVLO), over temperature protection (OTP), and over voltage protection (OVP). Excellent EMI performance is achieved with internal frequency jitter technique and soft switching control at the totem pole gate drive output.

The tone energy at below 22KHz is minimized in the design and audio noise is eliminated.

DM6359 is offered in DIP-8 package.

Features

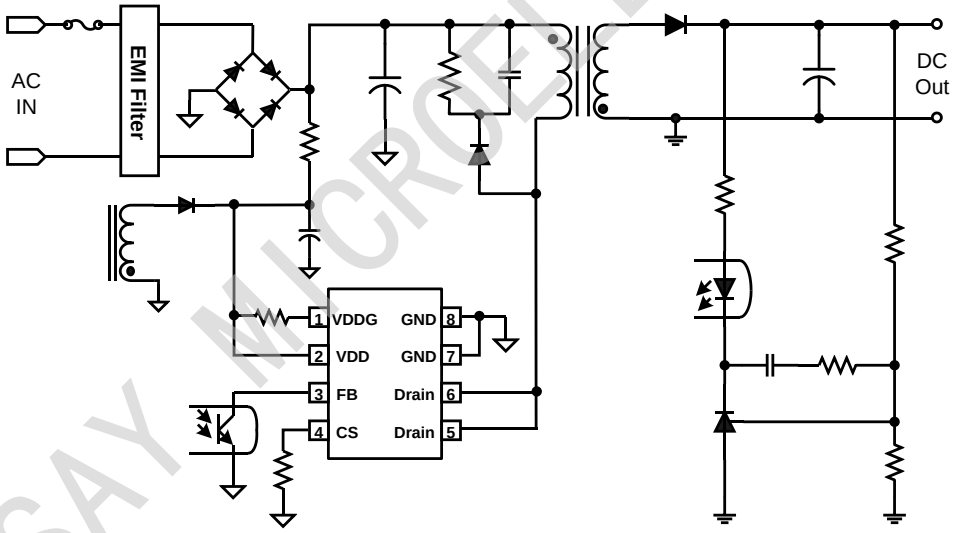
- Extra Low Standby(<75mW)
- Power-on Soft Start Reducing MOS Stress
- Built-in 650V power MOS
- Fixed 50KHz Switching Frequency
- Low VDD startup and operating current
- Frequency jitter to Minimize EMI
- Leading edge blanking on current sense
- Audio Noise Free Operation
- VDD Under Voltage Lockout with Hysteresis
- Cycle-by-Cycle over current Protection
- Over load Protection (OLP)
- Over Temperature Protection (OTP)
- VDD Over Voltage Protection (OVP)

Applications

Offline AC/DC flyback converter for

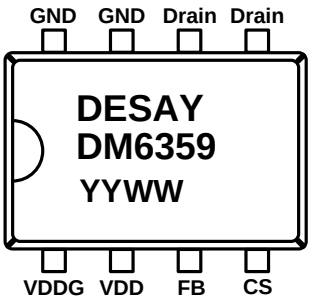
- AC/DC Adapter
- Set-Top Box Power Supplies
- Auxiliary Power Supply
- Open-frame SMPS

Typical Application



Pin Configuration

DIP-8 (TOP VIEW)

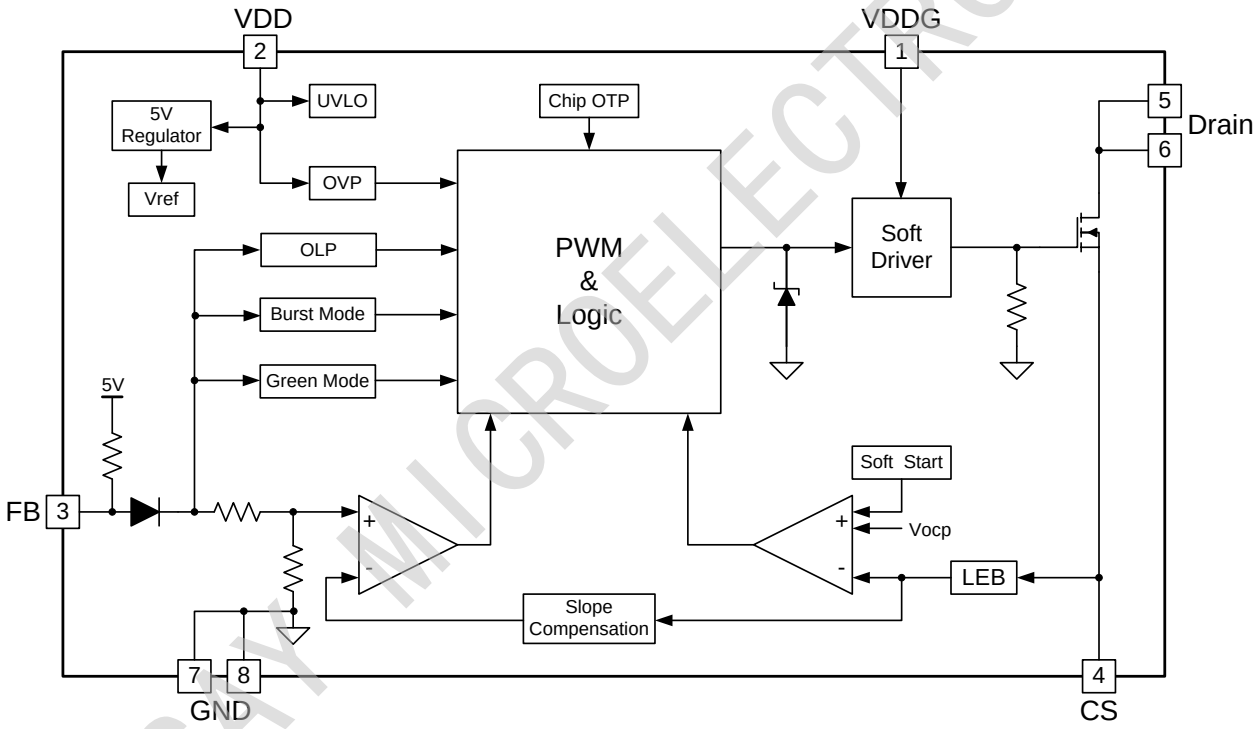


YY: Year Code(2018=18) WW: Week Code(01-52)

Ordering Information

Part number	Package		Shipping
DM6359	DIP-8	Pb-free	Tube & Carton

Block Diagram



Pin Descriptions

Name	Pin	Description
VDDG	1	Internal Gate Driver Power Supply
VDD	2	Power Supply
FB	3	Feedback input pin
CS	4	Current sense input and Power MOS Source
Drain	5、6	Power MOS Drain
GND	7、8	Ground

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{Drain}	Drain Voltage(off state)		BVdss	V
I_{Drain}	DM6359 Continuous Drain Current		4	A
V_{DD}	DC Supply Voltage		30	V
I_{DD}	VDD DC Clamp Current		10	mA
V_{DDG}	VDDG Input Voltage	-0.3V	30	V
V_{FB}	FB Input Voltage	-0.3V	5	V
V_{CS}	CS Input Voltage	-0.3V	5	V
R_{JA}	DIP-8 Thermal Resistance (Junction-to-Air)		75	℃/W
T_J	Operating Junction Temperature	-20	150	℃
T_{STG}	Storage Temperature Range	-55	160	℃
T_L	Lead Temperature (Wave Soldering or IR,10Seconds)		260	℃
ESD	Human Body Model,JEDEC:JESD22-A114		2.5	KV
	Machine Model, JEDEC:JESD22- A115		250	V

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended period may affect device’s reliability.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage	10	26	V
T_A	Operating Ambient Temperature	-20	85	℃
C_{VDD}	VDD Capacitor	4.7	10	uF
P_{OMAX}	DM6359, Output Power@90~264V Input		24	W
	DM6359, Output Power@230V Input		28	W

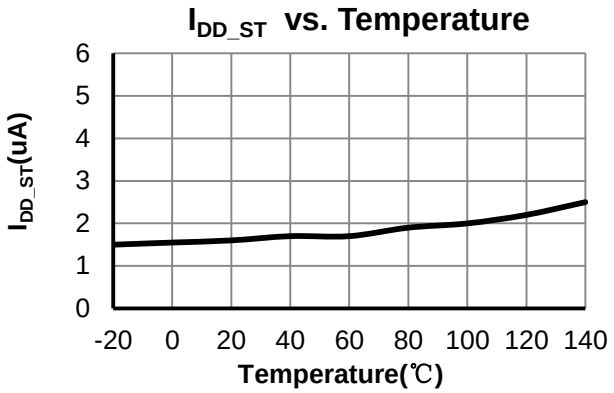
Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink, at 45℃ ambient.Higher output power is possible with extra added heat sink or air circulation to reduce thermal resistance.

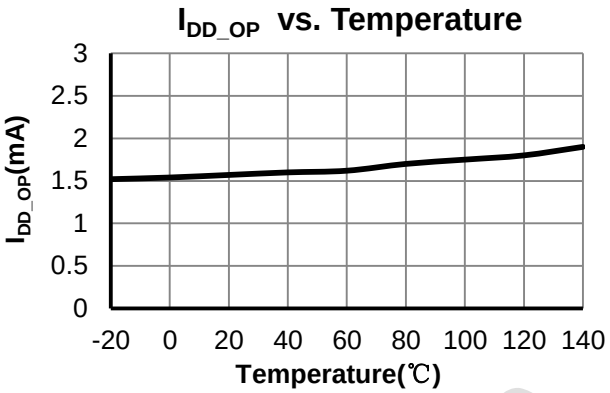
Electrical Characteristics(T_A = 25℃, V_{DD}=18V, unless otherwise noted)

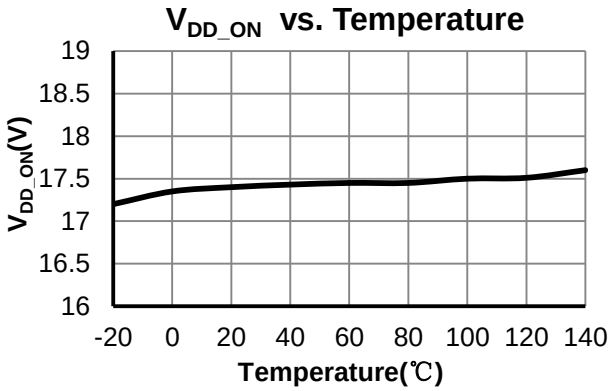
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage (VDD)						
I_{DD_ST}	Startup Current	VDD=V_{DD_ON}-1V		2	5	uA
I_{DD_OP}	Operation Current	VFB=3V		2.5	3.0	mA
I_{DD_Burst}	Burst Current	VCS=0V,VFB=0.5V		0.6	0.7	mA
V_{DD_ON}	Threshold Voltage to Startup	VDD Rising	16.3	17.3	18.3	V
V_{DD_OFF}	Threshold Voltage to Stop Switching in Normal Mode	VDD Falling	7.0	8.0	9.0	V
$V_{Pull-up}$	Pull-up PMOS active			10		V
V_{DD_OVP}	Over voltage protection voltage		27.0	28.0	29.0	V
V_{DD_Clamp}	VDD Clamp voltage	I_{DD}=10mA		30.0		V
Feedback Input Section(FB Pin)						
V_{FB_Open}	FB Open Loop Voltage			4.8		V
A_V	PWM input gain ΔVFB/ ΔVCS			1.71		V/V
D_{MAX}	Max duty cycle	VFB=3V,VCS=0.3V	77	80	83	%
V_{Ref_Green}	The threshold enter green mode			2.1		V
$V_{Ref\_Burst\_H}$	The threshold exit Burst mode			1.35		V
$V_{Ref\_Burst\_L}$	The threshold enter Burst mode			1.25		V
I_{FB_Short}	FB pin short circuit current	Short FB pin to GND		0.3		mA
V_{TH_PL}	Power Limiting FB Threshold Voltage			3.6		V
T_{D_PL}	Power limiting Debounce Time			60		mS
Z_{FB_IN}	Input Impedance			20		KΩ
Current Sense Input(CS Pin)						
T_{SS}	Soft start time			5		ms
T_{LEB}	Leading edge blanking time			300		ns
T_{D_OC}	Over Current Detection and Control Delay			90		ns
V_{TH_OC}	Current Limiting Threshold Voltage with zero duty cycle			0.75		V
V_{OCP_Clamp}	CS voltage clamper			0.9		V
Oscillator						
F_{OSC}	Normal Oscillation Frequency	VFB=3V,VCS=0V	45	50	55	KHz
F_{JR}	Frequency jitter range			+/-4		%
F_{Jitter}	jitter frequency			25		Hz
F_{DT}	Frequency Variation vs. Temperature Deviation			5		%
F_{DV}	Frequency Variation vs. V_{DD} Deviation			1		%

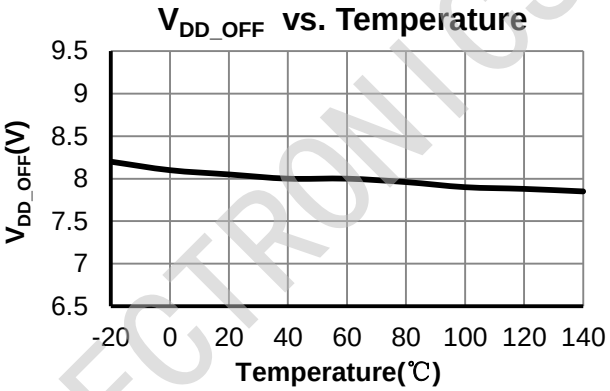
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F_{Burst}	Burst Mode Switch Frequency			22		KHz
Power MOS						
BVdss	Drain-CS Breakdown voltage	I_{Drain}=250uA	650			V
$R_{DS(ON)}$	Drain-CS ON resistance	Only DM6359, I_D=2A		2.1	2.4	Ω
In-chip OTP						
T_{OTP_EN}	OTP enter			150		℃
T_{OTP_EX}	OTP exit			120		℃

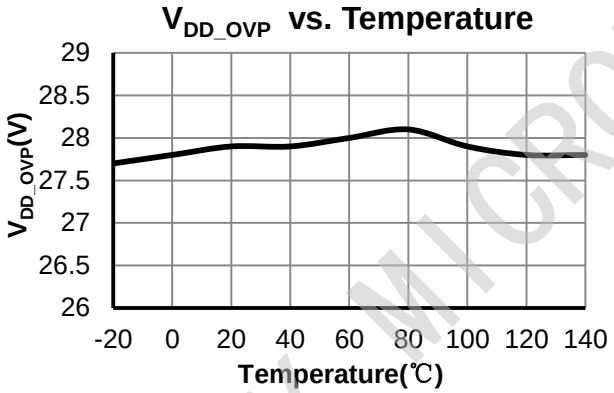
Typical Performance Characteristics(T_A = 25℃, V_{DD}=18V, unless otherwise noted)

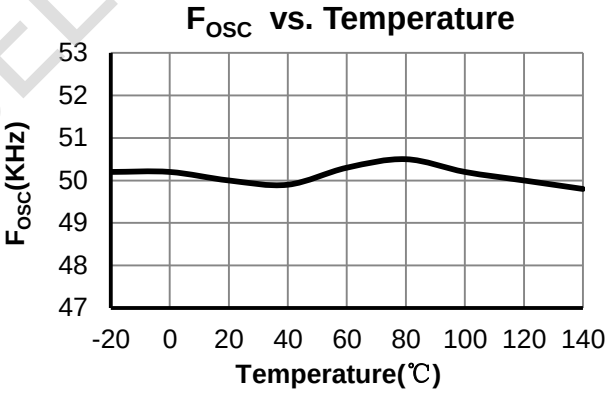


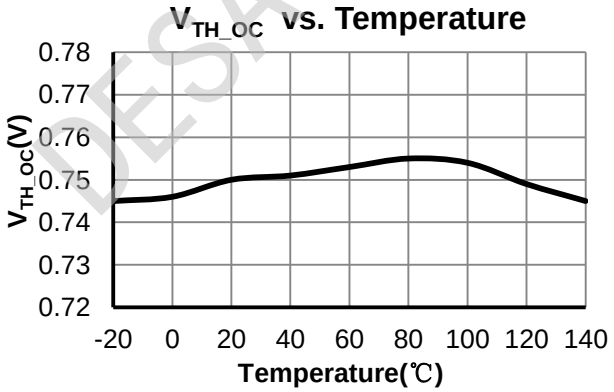


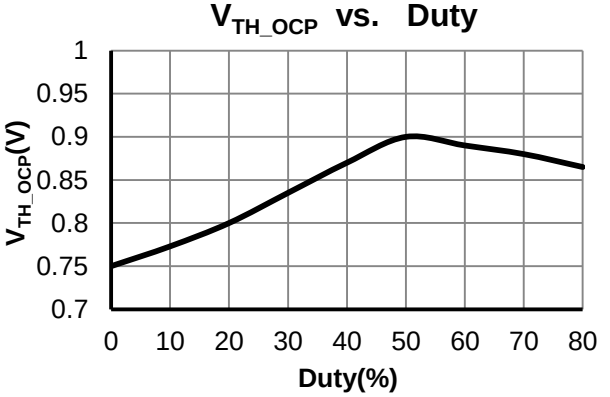












Functional Description

The DM6359 is a low power off-line SMPS Switcher optimized for off-line flyback converter applications in sub 28W power range. The Burst Mode control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of DM6359 is designed to be very low so that VDD could be charged up above V_{DD_ON} and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

Operating Current

The Operating current of DM6359 is low at 2.5mA (typical). Good efficiency is achieved with DM6359 low operation current together with the Burst Mode control features.

Soft Start

DM6359 features an internal 4ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches V_{DD_ON}, the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

Frequency jitter for EMI improvement

The frequency jitter is implemented in DM6359. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Oscillator Operation

The switching frequency of DM6359 is internally fixed at 50KHz. No external frequency setting components are required for PCB design simplification.

Multi-mode Operation for High Efficiency

DM6359 is a multi-mode controller. The controller changes the mode of operation according to the FB pin voltage. At the normal operating condition, the IC operates in traditional fix frequency（50KHz）PWM mode. As the output load current is decreased, the IC enter into green mode smoothly from the PWM mode. In this mode, the switching frequency will start to linearly decrease from 50KHz to 22KHz. So the switching loss is minimized and the high conversion efficiency can be achieved. At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOS, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy. The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency.

At light load or no load condition, the FB input drops below $V_{Ref\_Burst\_L}$ and device enters Burst Mode control. The Gate drive output switches when FB input rises back to $V_{Ref\_Burst\_H}$. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in DM6359 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Driver

The internal power MOSFET in DM6359 is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

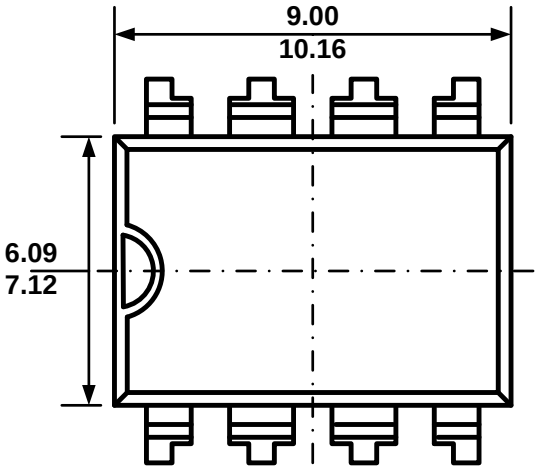
In addition to the gate drive control scheme mentioned,the gate drive strength can also be adjusted externally by a resistor connected between VDD and VDDG, the falling edge of the Drain output can be well controlled. It provides great flexibility for system EMI design.

Protection Controls

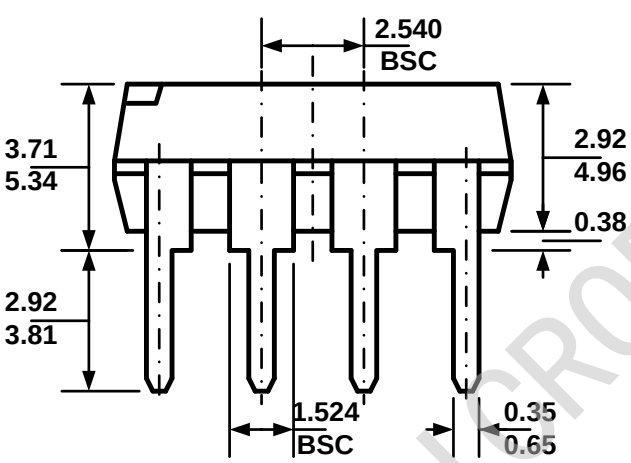
Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP), VDD Over Voltage Protection (OVP). The OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range. At overload condition when FB input voltage exceeds power limit threshold value for more than T_{D_PL}, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

Package Information

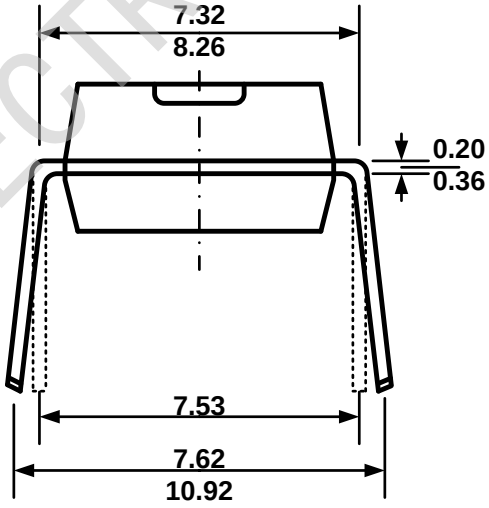
DIP-8



TOP VIEW



FRONT VIEW



SIDE VIEW

Note:

1. All dimensions are in millimeters
2. Package length does not include mold flash protrusion or gate burr
3. Package WIDTH does not include mold flash protrusion
4. Drawing is not to scale