1 kV RMS Six-Channel Digital Isolators

Data Sheet

ADuM7640/ADuM7641/ADuM7642/ADuM7643

FEATURES

- Small 20-lead QSOP
- 1000 V rms isolation rating
- Safety and regulatory approvals (pending):
  - UL recognition (pending)
    - 1000 V rms for 1 minute per UL 1577
- Low power operation
  - 3.3 V operation
    - 1.6 mA per channel maximum at 0 Mbps to 1 Mbps
    - 7.8 mA per channel maximum at 25 Mbps
  - 5 V operation
    - 2.2 mA per channel maximum at 0 Mbps to 1 Mbps
    - 11.2 mA per channel maximum at 25 Mbps
- Bidirectional communication
- Up to 25 Mbps data rate (NRZ)
- 3 V/5 V level translation
- High temperature operation: 105°C
- High common-mode transient immunity: >15 kV/µs

APPLICATIONS

- General-purpose, multichannel isolation
- SPI interface/data converter isolation
- RS-232/RS-422/RS-485 transceivers
- Industrial field bus isolation

GENERAL DESCRIPTION

The ADuM7640/ADuM7641/ADuM7642/ADuM7643[1] are 6-channel digital isolators based on the Analog Devices, Inc., *i*Coupler® technology. These 1 kV digital isolation devices are packaged in a small 20-lead QSOP. They offer space savings and a lower price than 2.5 kV or 5 kV isolation solutions when only functional isolation is needed.

This family, like many Analog Devices isolators, offers very low power consumption, using one-tenth to one-sixth the power of other digital isolators, with the supply voltage on either side ranging from 3.0 V to 5.5 V. Despite their low power consumption, the ADuM7640/ADuM7641/ADuM7642/ADuM7643 provide low pulse width distortion (< 6 ns for C grade) and a channel-by-channel glitch filter to protect the device against extraneous noise disturbances. Four channel direction combinations are available with a maximum data rate of 1 Mbps or 25 Mbps. All products have a default output high logic state in the absence of input power.

FUNCTIONAL BLOCK DIAGRAMS

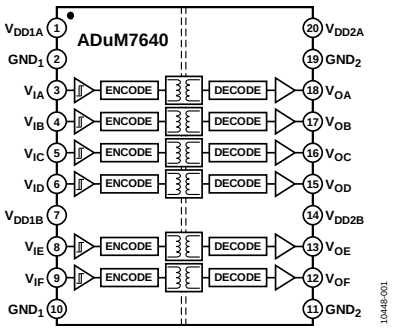

Figure 1. ADuM7640

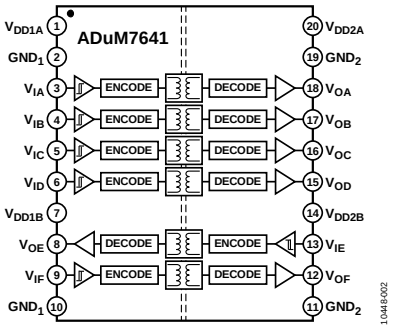

Figure 2. ADuM7641

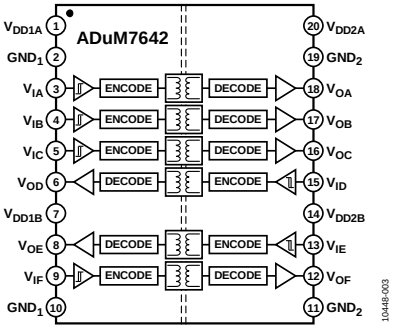

Figure 3. ADuM7642

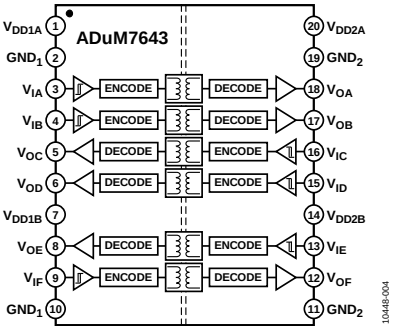

Figure 4. ADuM7643

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329. Other patents pending.

Rev. 0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

9/12—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 1.

		A Grade			C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									
Pulse Width	PW	250			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			75	28	40	50	ns	50% input to 50% output
Pulse Width Distortion	PWD			25		2	6	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5			3		ps/°C	
Propagation Delay Skew[1]	t_{PSK}			20			14	ns	
Channel Matching									
Codirectional[2]	t_{PSKCD}			25		6	12	ns	
Opposing Directional[3]	t_{PSKOD}			30		7	12	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[2] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.
[3] Opposing directional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposite sides of the isolation barrier.

Table 2.

		1 Mbps—A and C Grades			25 Mbps—C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT									No load
ADuM7640	I_{DD1}		5.7	7.0		44	54	mA	
	I_{DD2}		4.4	5.9		11	13	mA	
ADuM7641	I_{DD1}		5.5	6.8		38	46	mA	
	I_{DD2}		4.6	5.7		15	19	mA	
ADuM7642	I_{DD1}		5.2	6.3		31	38	mA	
	I_{DD2}		4.8	6.0		19	24	mA	
ADuM7643	I_{DD1}		4.8	6.0		24	30	mA	
	I_{DD2}		5.0	6.3		22	29	mA	

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Voltage Threshold						
Logic High	V_{IH}	0.7 V_{DDx}			V	
Logic Low	V_{IL}			0.3 V_{DDx}	V	
Output Voltages						
Logic High	V_{OH}	V_{DDx} − 0.1	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.4	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Supply Current						
Input	$I_{DDI (Q)}$		0.95	1.16	mA	
Output	$I_{DDO (Q)}$		0.73	0.98	mA	
Dynamic Supply Current						
Input	$I_{DDI (D)}$		0.26		mA/Mbps	
Output	$I_{DDO (D)}$		0.04		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.0		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	15	25		kV/μs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		600		kHz	DC data inputs

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{OL} < 0.8 × V_{DDLx} or V_{OH} > 0.7 × V_{DDIx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 4.

		A Grade			C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									
Pulse Width	PW	250			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			85	33	49	66	ns	50% input to 50% output
Pulse Width Distortion	PWD			25		2	6	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5			3		ps/°C	
Propagation Delay Skew[1]	t_{PSK}			20			14	ns	
Channel Matching									
Codirectional[2]	t_{PSKCD}			25		6	12	ns	
Opposing Directional[3]	t_{PSKOD}			30		6	15	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[2] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.
[3] Opposing directional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposite sides of the isolation barrier.

Table 5.

		1 Mbps—A and C Grades			25 Mbps—C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT									No load
ADuM7640	I_{DD1}		4.1	5.2		32	38	mA	
	I_{DD2}		3.3	4.3		7.2	8.7	mA	
ADuM7641	I_{DD1}		3.9	4.9		27	33	mA	
	I_{DD2}		3.4	4.2		11	13	mA	
ADuM7642	I_{DD1}		3.7	4.7		23	27	mA	
	I_{DD2}		3.5	4.4		14	16	mA	
ADuM7643	I_{DD1}		3.5	4.4		18	21	mA	
	I_{DD2}		3.6	4.5		16	20	mA	

Table 6.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Voltage Threshold						
Logic High	V_{IH}	0.7 V_{DDx}			V	
Logic Low	V_{IL}			0.3 V_{DDx}	V	
Output Voltages						
Logic High	V_{OH}	V_{DDx} − 0.2	3.3		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	3.1		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
Supply Current per Channel						
Quiescent Supply Current						
Input	$I_{DDI (Q)}$		0.68	0.87	mA	
Output	$I_{DDO (Q)}$		0.55	0.72	mA	
Dynamic Supply Current						
Input	$I_{DDI (D)}$		0.19		mA/Mbps	
Output	$I_{DDO (D)}$		0.03		mA/Mbps	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.8		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	15	20		kV/μs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		550		kHz	DC data inputs

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{OL} < 0.8 V_{DDLx} or V_{OH} > 0.7 × V_{DDIx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 7.

Parameter	Symbol	A Grade Min	A Grade Typ	A Grade Max	C Grade Min	C Grade Typ	C Grade Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									
Pulse Width	PW	250			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			80	30	42	58	ns	50% input to 50% output
Pulse Width Distortion	PWD			25		2	6	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5			3		ps/°C	
Propagation Delay Skew[1]	t_{PSK}			20			14	ns	
Channel Matching									
Codirectional[2]	t_{PSKCD}			25		5	15	ns	
Opposing Directional[3]	t_{PSKOD}			30		8	15	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[2] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.
[3] Opposing directional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposite sides of the isolation barrier.

Table 8.

Parameter	Symbol	1 Mbps—A, C Grades Min	1 Mbps—A, C Grades Typ	1 Mbps—A, C Grades Max	25 Mbps—C Grade Min	25 Mbps—C Grade Typ	25 Mbps—C Grade Max	Unit	Test Conditions/Comments
SUPPLY CURRENT									No load
ADuM7640	I_{DD1}		5.7	7.0		44	54	mA	
	I_{DD2}		3.3	4.1		7.5	8.7	mA	
ADuM7641	I_{DD1}		5.4	6.8		38	46	mA	
	I_{DD2}		3.4	4.0		11	13	mA	
ADuM7642	I_{DD1}		5.1	6.3		31	38	mA	
	I_{DD2}		3.5	4.3		14	16	mA	
ADuM7643	I_{DD1}		4.8	6.0		24	30	mA	
	I_{DD2}		3.6	4.3		16	20	mA	

Table 9.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Voltage Threshold						
Logic High	V_{IH}	0.7 V_{DDx}			V	
Logic Low	V_{IL}			0.3 V_{DDx}	V	
Output Voltages						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	15	20		kV/μs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		600		kHz	DC data inputs

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{OL} < 0.8 V_{DDLx} or V_{OH} > 0.7 × V_{DDIx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +105°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted.

Table 10.

		A Grade			C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SWITCHING SPECIFICATIONS									
Pulse Width	PW	250			40			ns	Within PWD limit
Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			80	29	46	60	ns	50% input to 50% output
Pulse Width Distortion	PWD			25		2	6	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Change vs. Temperature			5			3		ps/°C	
Propagation Delay Skew[1]	t_{PSK}			20			14	ns	
Channel Matching									
Codirectional[2]	t_{PSKCD}			25		6	13	ns	
Opposing Directional[3]	t_{PSKOD}			30		9	18	ns	
Jitter			2			2		ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.
[2] Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.
[3] Opposing directional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposite sides of the isolation barrier.

Table 11.

		1 Mbps—A, C Grades			25 Mbps—C Grade				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
SUPPLY CURRENT									No load
ADuM7640	I_{DD1}		4.1	4.9		32	38	mA	
	I_{DD2}		4.5	5.9		11	13	mA	
ADuM7641	I_{DD1}		3.9	4.7		27	33	mA	
	I_{DD2}		4.6	5.7		15	19	mA	
ADuM7642	I_{DD1}		3.7	4.4		23	27	mA	
	I_{DD2}		4.8	6.0		19	24	mA	
ADuM7643	I_{DD1}		3.5	4.2		18	21	mA	
	I_{DD2}		5.0	6.2		22	29	mA	

Table 12.

Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DC SPECIFICATIONS						
Input Voltage Threshold						
Logic High	V_{IH}	0.7 V_{DDx}			V	
Logic Low	V_{IL}			0.3 V_{DDx}	V	
Output Voltages						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DDx} − 0.5	V_{DDx} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
Input Current per Channel	I_I	−10	+0.01	+10	μA	0 V ≤ V_{Ix} ≤ V_{DDx}
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	15	20		kV/μs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		550		kHz	DC data inputs

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining VOL < 0.8 VDDLx or VOH > 0.7 × VDDIx. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 13.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		76		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device: Pin 1 through Pin 10 are shorted together, and Pin 11 through Pin 20 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM7640/ADuM7641/ADuM7642/ADuM7643 are approved by the organizations listed in Table 14. See Table 18 and the Insulation Lifetime section for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 14.

UL (Pending)
Recognized Under UL 1577 Component Recognition Program[1]
Single Protection,1000 V rms Isolation Voltage
File E274400

[1] In accordance with UL 1577, each ADuM7640/ADuM7641/ADuM7642/ADuM7643 is proof tested by applying an insulation test voltage ≥ 1200 V rms for 1 sec (current leakage detection limit = 5 µA).

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 15.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		1000	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	3.8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	2.8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		2.6	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

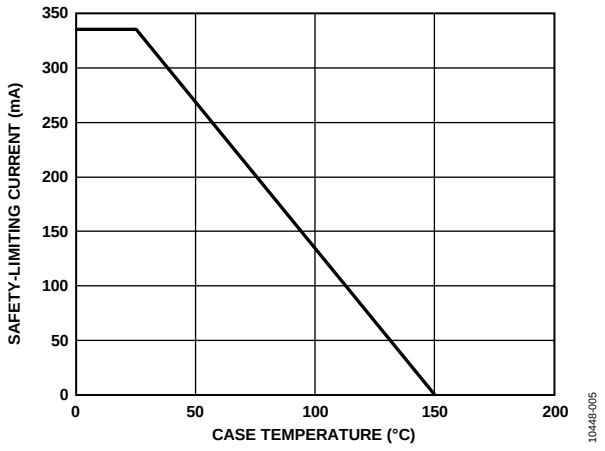

Figure 5. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 16.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	3.0	5.5	V
Input Signal Rise and Fall Times			1.0	ms

[1] All voltages are relative to their respective grounds. See the DC Correctness section for information about immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 17.

Parameter	Rating
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +105°C
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{IE}, V_{IF})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB}, V_{OC}, V_{OD}, V_{IE}, V_{IF})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 (I_{O1})	−10 mA to +10 mA
Side 2 (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[3]	−100 kV/µs to +100 kV/µs

[1] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the Printed Circuit Board Layout section.
[2] See Figure 5 for maximum rated current values for various temperatures.
[3] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 18. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	420	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform			
Basic Insulation	420	V peak	50-year minimum lifetime
DC Voltage			
Basic Insulation	420	V peak	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

Table 19. Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{DDI} State[2]	V_{DDO} State[3]	V_{Ox} Output[1]	Description
H	Powered	Powered	H	Normal operation; data is high.
L	Powered	Powered	L	Normal operation; data is low.
X	Unpowered	Powered	H	Input unpowered. Output pins are in the default high state. Outputs return to input state within 1.6 µs of V_{DDI} power restoration. See the pin function descriptions (Table 20 through Table 23) for more information.
X	Powered	Unpowered	Z	Output unpowered. Output pins are in high impedance state. Outputs return to input state within 1.6 µs of V_{DDO} power restoration. See the pin function descriptions (Table 20 through Table 23Table 22) for more information.

[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, D, E or F).
[2] V_{DDI} refers to the supply voltage on the input side of a given channel (A, B, C, D, E or F).
[3] V_{DDO} refers to the supply voltage on the output side of a given channel (A, B, C, D, E or F).