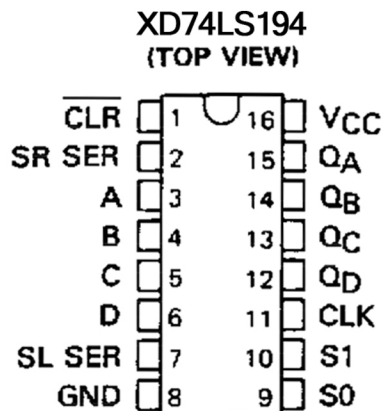


- Parallel Inputs and Outputs
- Four Operating Modes:
Synchronous Parallel Load
Right Shift
Left Shift
Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
74LS194	36 MHz	75 mW



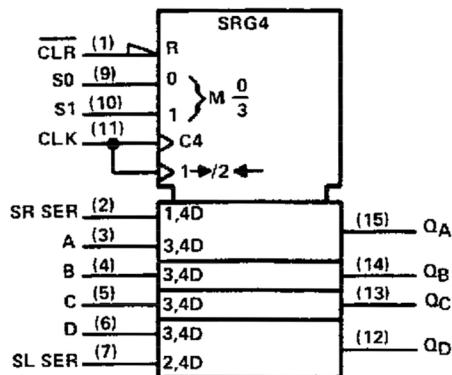
description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. They contain 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operation-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Inhibit clock (do nothing)
 Shift right (in the direction Qa toward Qd)
 Shift left (in the direction Qq toward Qa)
 Parallel (broadside) load
 Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the shift register is inhibited when both mode control inputs are low. The mode controls of the XD74LS194 should be changed only when the clock input is high.

logic symbol†



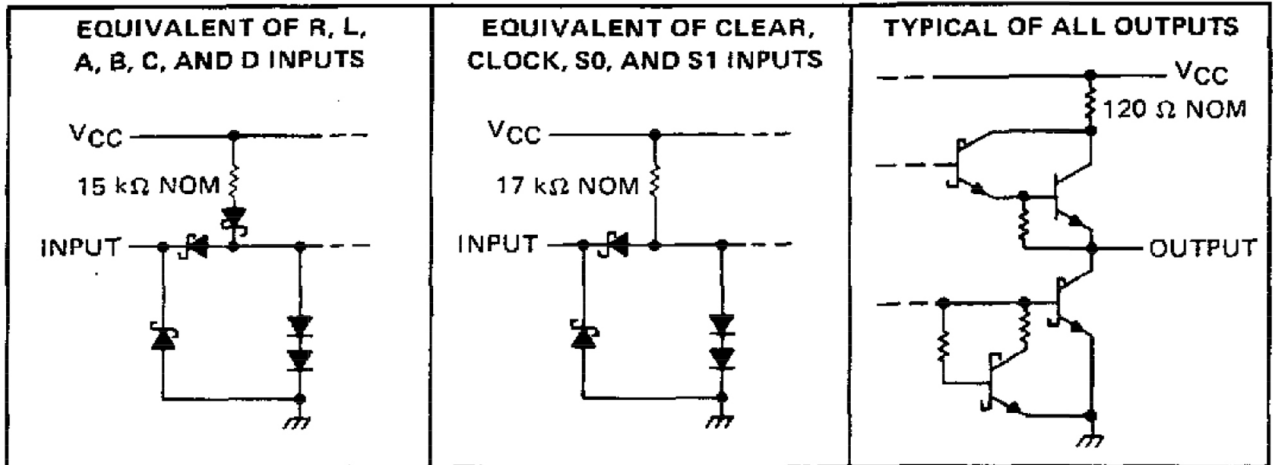
FUNCTION TABLE

CLEAR	MODE		CLOCK	INPUTS				OUTPUTS					
				SERIAL		PARALLEL		Q _A	Q _B	Q _C	Q _D		
	S1	S0		LEFT	RIGHT	A	B					C	D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}
H	H	L	↑	H	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

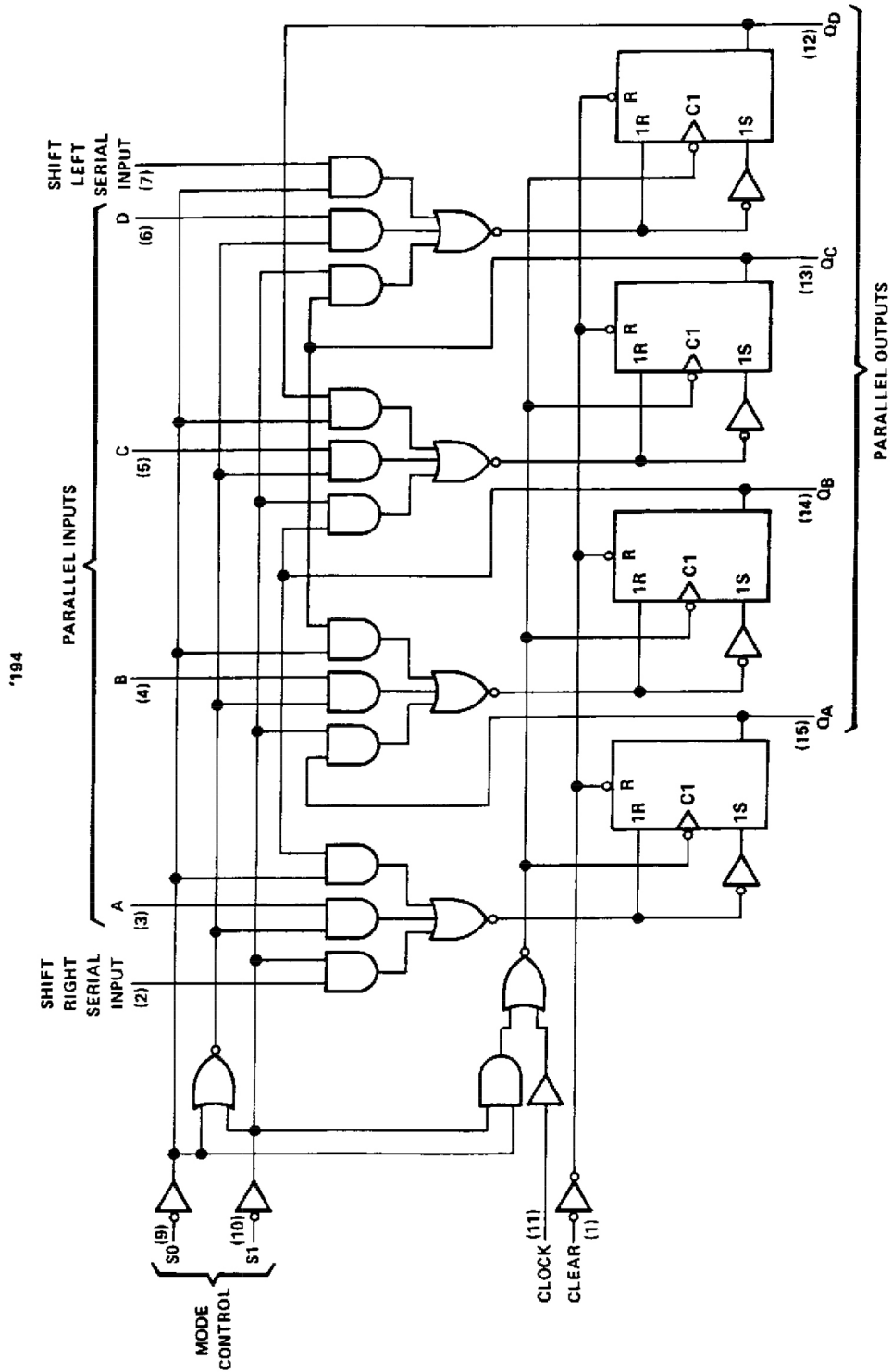
H = high level (steady state)
 L = low level (steady state)
 X = irrelevant (any input, including transitions)
 ↑ = transition from low to high level
 a,b,c,d = the level of steady-state input at input A,B,C,orD, respectively.
 Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
 A_n, B_n, C_n, D_n = the level of A, B, C, respectively, before the most-recent ↑ transition of the clock.

schematics of inputs and outputs

74LS194

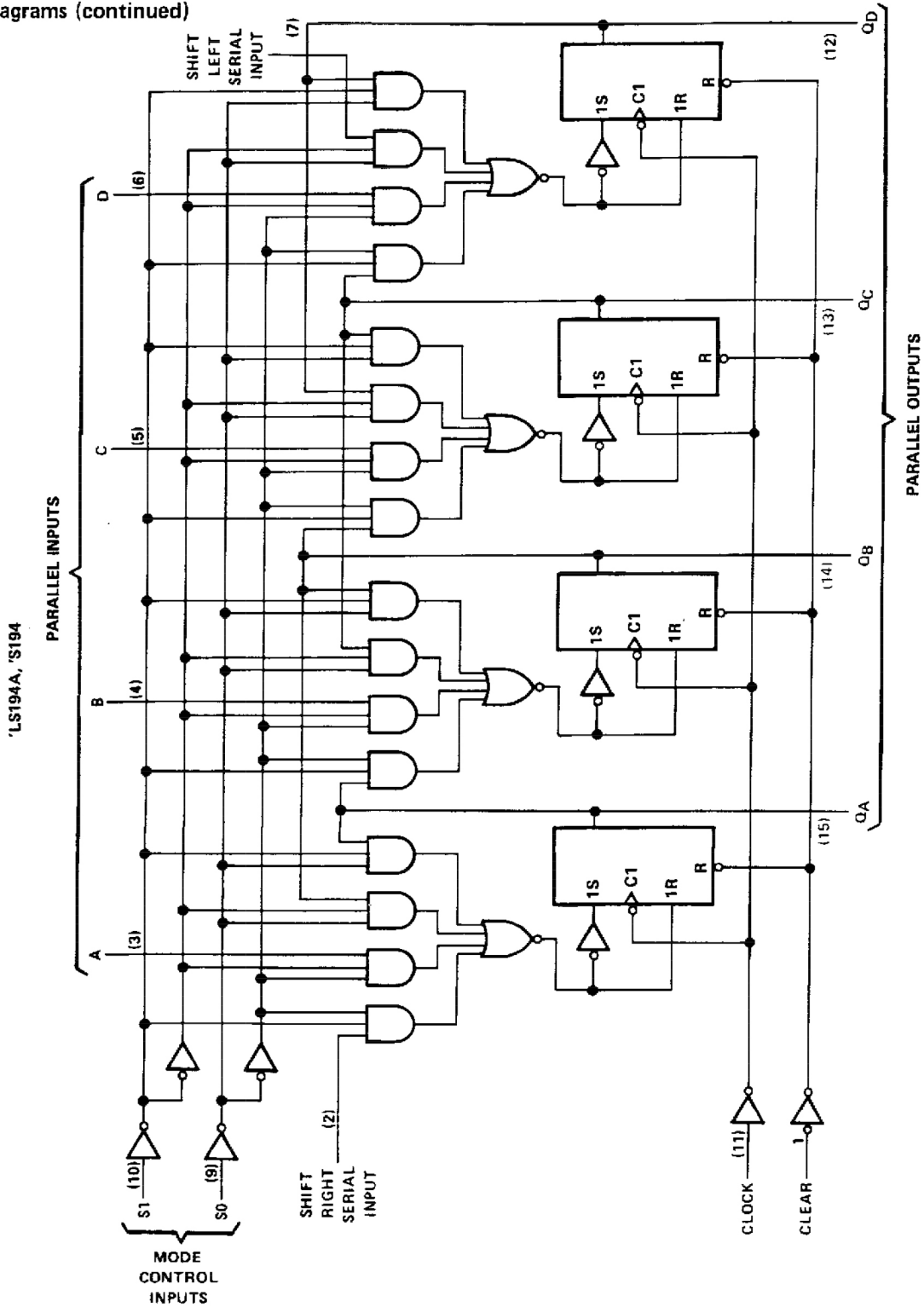


logic diagrams (positive logic)



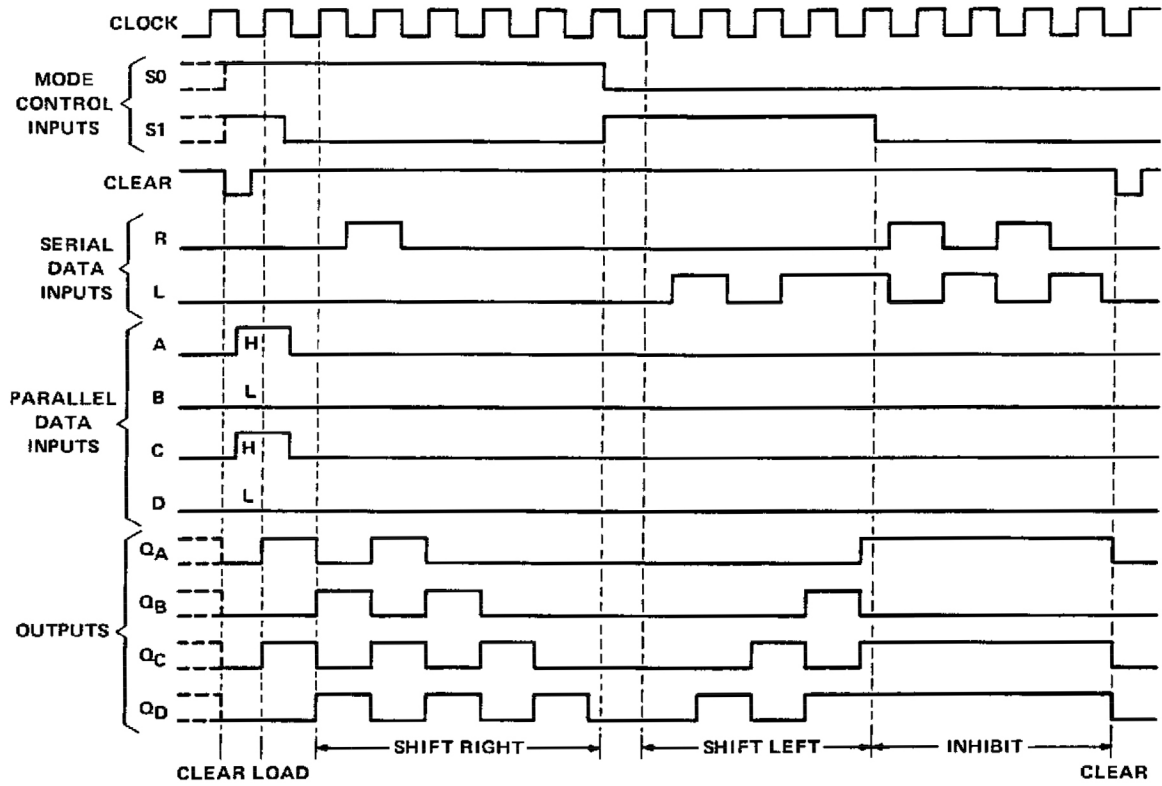
Pin numbers shown are for D, J, N, and W packages.

logic diagrams (continued)



Pin numbers shown on logic notation are for D, J or N, and W packages.

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: XD74LS194	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	XD74LS164			UNIT
	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			-400	μA
Low-level output current, I_{OL}			8	mA
Clock frequency, f_{clock}	0		25	MHz
Width of clock or clear pulse, t_w	20			ns
Setup time, t_{SU}	Mode control	30		ns
	Serial and parallel data	20		ns
	Clear inactive state	25		ns
Hold time at any input, t_h	0			ns
Operating free-air temperature, T_A	0		70	$^{\circ}\text{C}$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	XD74LS164			UNIT
		MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage				0.8	V
V_I Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V},$ $V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$	0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2		15	23	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

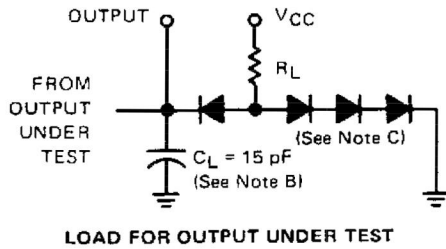
[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

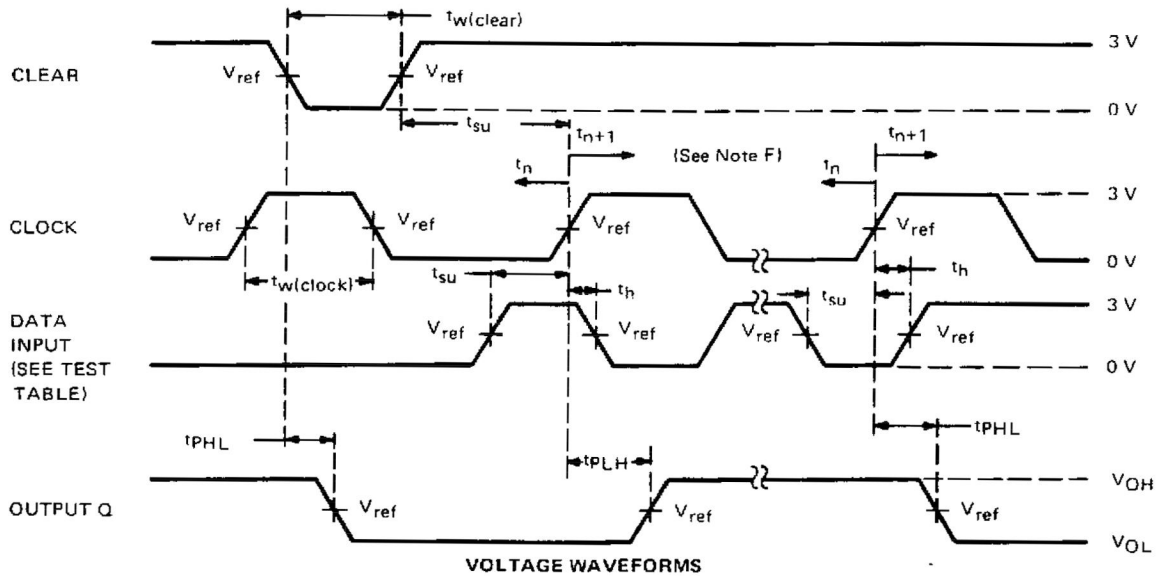
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega,$ See Figure 1	25	36		MHz
t_{PHL} Propagation delay time, high-to-low level output from clear			19	30	ns
t_{PLH} Propagation delay time, low-to-high level output from clock			14	22	ns
t_{PHL} Propagation delay time, high-to-low level output from clock			17	26	ns

PARAMETER MEASUREMENT INFORMATION



TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+4}
R Serial Input	0 V	4.5 V	Q_D at t_{n+4}

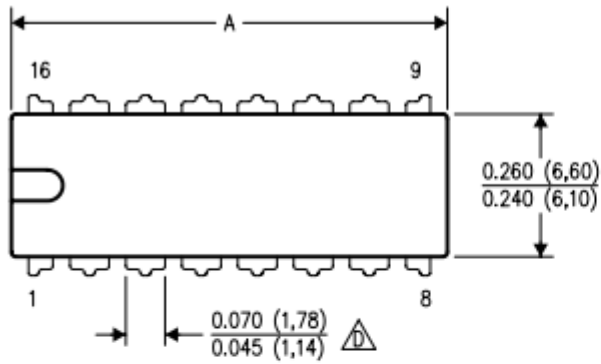


- NOTES:
- A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50 \Omega$ and $PRR \leq 1$ MHz. For 'XD74LS194, $t_p \leq 7$ ns and $t_r \leq 7$ ns. For XD74LS194, $t_r \leq 15$ ns and $t_f \leq 6$ ns. For XD74LS194, $t_p \leq 2.5$ ns and $t_f \leq 2.5$ ns. When testing f_{max} , vary PRR.
 - B. C_L includes probe and jig capacitance.
 - C. All diodes are 1N3064 or 1N916.
 - D. A clear pulse is applied prior to each test.
 - E. For XD74LS194, $V_{ref} = 1.5$ V; for XD74LS194, $V_{ref} = 1.3$ V.
 - F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} . Proper shifting of data is verified at t_{n+4} with a functional test.
 - G. t_n = bit time before clocking transition.
 t_{n+1} = bit time after one clocking transition.
 t_{n+4} = bit time after four clocking transitions.

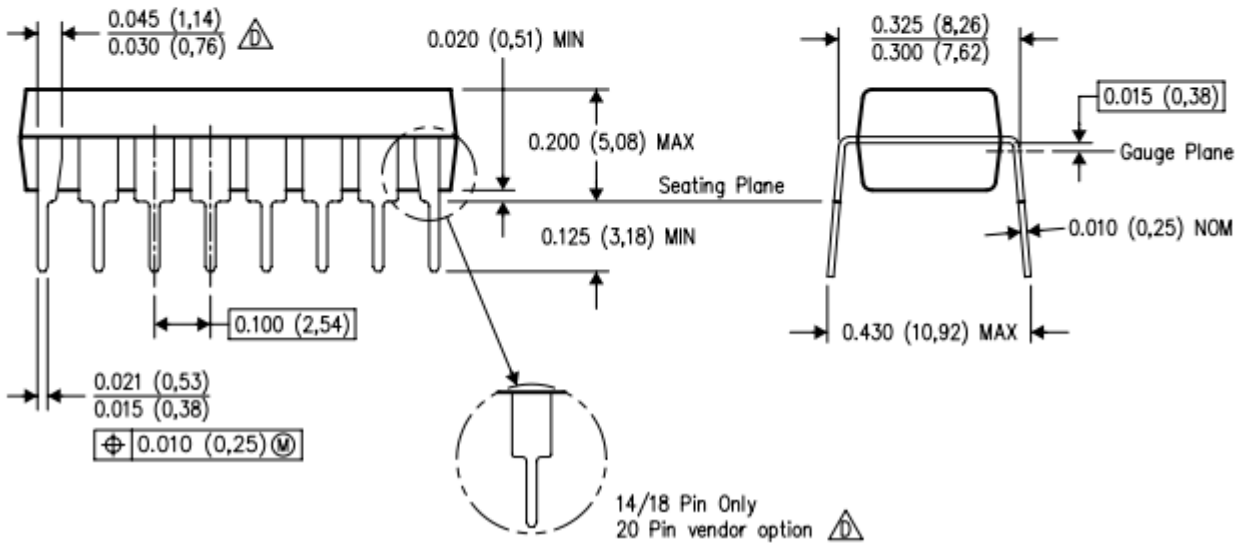
FIGURE 1—SWITCHING TIMES

XD74LS194 DIP-16

DIP



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



以上信息仅供参考. 如需帮助联系客服人员。谢谢 XINLUDA