

# 74LV7032A

## Quad 2-input OR gate with Schmitt trigger inputs

Rev. 1 — 19 December 2018

Product data sheet

### 1. General description

The 74LV7032A is a quad 2-input OR function with Schmitt-trigger inputs, capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

This device is fully specified for partial power down applications using  $I_{OFF}$ . The  $I_{OFF}$  circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

### 2. Features and benefits

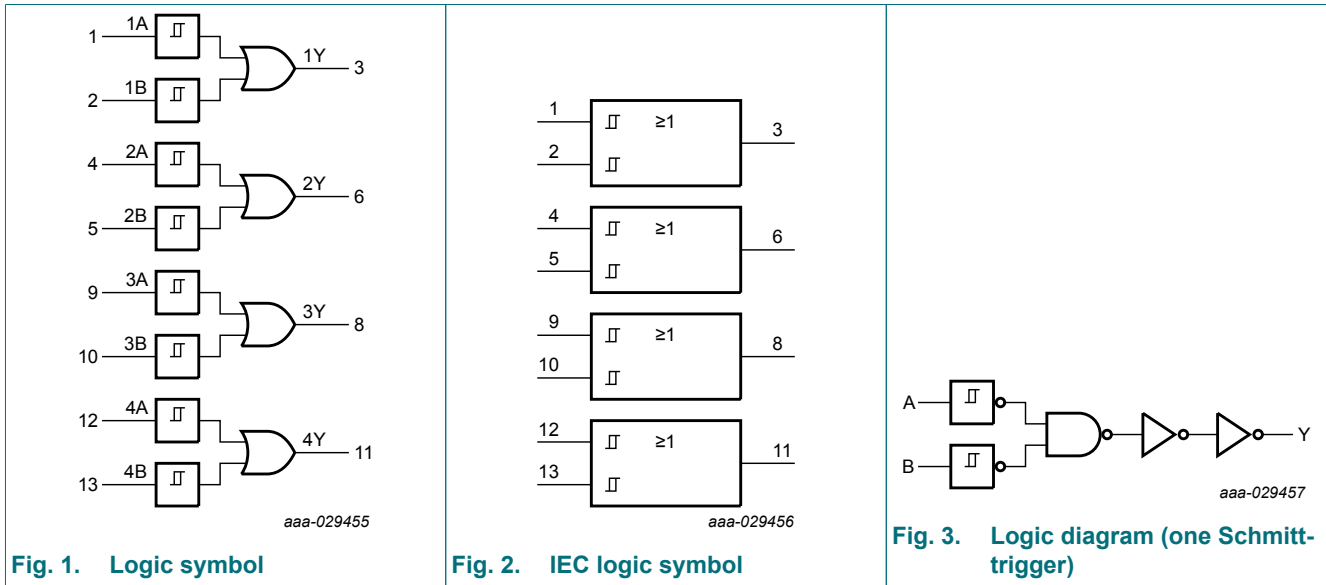
- Wide supply voltage range from 2.0 V to 5.5 V
- Maximum  $t_{pd}$  of 9.5 ns at 5 V
- Typical  $V_{OL(p)} < 0.8$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  °C
- Typical  $V_{OH(v)} > 2.3$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25$  °C
- Supports mixed-mode voltage operation on all ports
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
  - MM: MM JESD22-A115-B exceeds 200 V
  - HBM: ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 4 kV
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2 kV
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

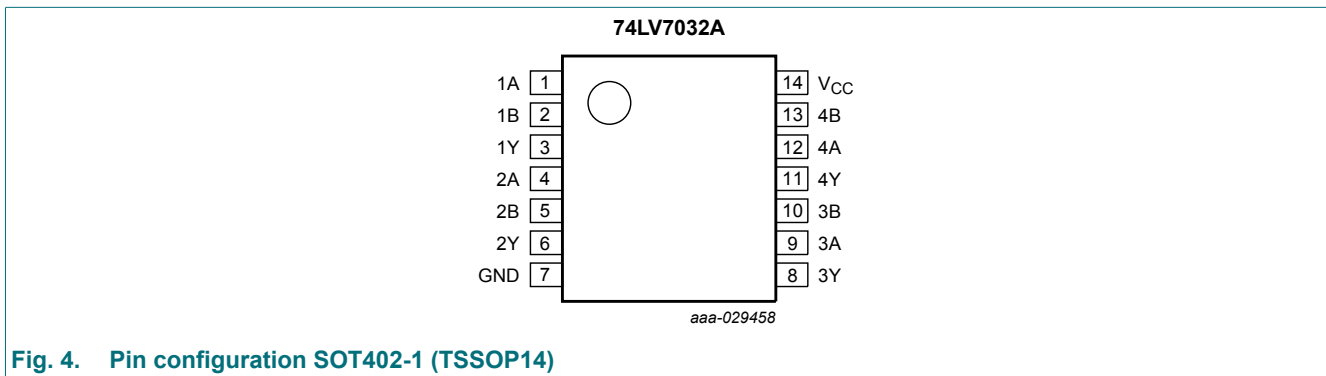
Type number	Package			
	Temperature range	Name	Description	Version
74LV7032APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

### 4. Functional diagram



### 5. Pinning information

#### 5.1. Pinning



#### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

## 6. Functional description

**Table 3. Function table**

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input		Output
nA	nB	nY
L	L	L
X	H	H
H	X	H

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		[1] -0.5	+7.0	V
$V_O$	output voltage	output HIGH or LOW state	[2] -0.5	$V_{CC} + 0.5$	V
		output power-down	[2] -0.5	+7.0	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-20	-	mA
$I_{OK}$	output clamping current	$V_O < 0$ V	-50	-	mA
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 35$	mA
$I_{CC}$	supply current		-	70	mA
$I_{GND}$	ground current		-70	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[4] -	500	mW

[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

[2] If the output current ratings are observed, the output voltage ratings may be exceeded.

[3] This value is limited to 7 V maximum.

[4] For SOT402-1 package: above 116 °C, the value of  $P_{tot}$  derates linearly at 7.3 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.0	5.0	5.5	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	output HIGH or LOW state	0	-	$V_{CC}$	V
		output power-down	0	-	5.5	V
$T_{amb}$	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 2.7 V	-	-	50	ms/V
		$V_{CC} = 3.0$ V to 3.6 V	-	-	20	ms/V
		$V_{CC} = 4.5$ V to 5.5 V	-	-	1	ms/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>T+</sub>	positive-going threshold voltage	V <sub>CC</sub> = 2.5 V	-	-	1.75	-	1.75	-	1.75	V
		V <sub>CC</sub> = 3.3 V	-	-	2.31	-	2.31	-	2.31	V
		V <sub>CC</sub> = 5.0 V	-	-	3.5	-	3.5	-	3.5	V
V <sub>T-</sub>	negative-going threshold voltage	V <sub>CC</sub> = 2.5 V	0.75	-	-	0.75	-	0.75	-	V
		V <sub>CC</sub> = 3.3 V	0.99	-	-	0.99	-	0.99	-	V
		V <sub>CC</sub> = 5.0 V	1.5	-	-	1.5	-	1.5	-	V
V <sub>H</sub>	hysteresis voltage	V <sub>CC</sub> = 2.5 V	0.25	-	-	0.25	-	0.25	-	V
		V <sub>CC</sub> = 3.3 V	0.33	-	-	0.33	-	0.33	-	V
		V <sub>CC</sub> = 5.0 V	0.5	-	-	0.5	-	0.5	-	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		V <sub>CC</sub> = 2.0 V to 5.5 V; I <sub>O</sub> = -50 µA	V <sub>CC</sub> -0.1	-	-	V <sub>CC</sub> -0.1	-	V <sub>CC</sub> -0.1	-	V
		V <sub>CC</sub> = 2.3 V; I <sub>O</sub> = -2 mA	2	-	-	2	-	2	-	V
		V <sub>CC</sub> = 3.0 V; I <sub>O</sub> = -6 mA	2.48	-	-	2.48	-	2.48	-	V
		V <sub>CC</sub> = 4.5 V; I <sub>O</sub> = -12 mA	3.8	-	-	3.8	-	3.8	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		V <sub>CC</sub> = 2.0 V to 5.5 V; I <sub>O</sub> = 50 µA	-	-	0.1	-	0.1	-	0.1	V
		V <sub>CC</sub> = 2.3 V; I <sub>O</sub> = 2 mA	-	-	0.4	-	0.4	-	0.4	V
		V <sub>CC</sub> = 3.0 V; I <sub>O</sub> = 6 mA	-	-	0.44	-	0.44	-	0.44	V
		V <sub>CC</sub> = 4.5 V; I <sub>O</sub> = 12 mA	-	-	0.55	-	0.55	-	0.55	V
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = GND to 5.5 V; V <sub>CC</sub> = 0 V	-	-	0.5	-	5	-	5	µA
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 0 V to 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	2	-	20	-	20	µA

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nA, nB to nY; see Fig. 5 [2]								
		V <sub>CC</sub> = 2.3 V to 2.7 V								
		C <sub>L</sub> = 15 pF	-	5.6	12.8	1	15	1	16	ns
		C <sub>L</sub> = 50 pF	-	7.8	16.2	1	19	1	20	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V								
		C <sub>L</sub> = 15 pF	-	4.3	7.9	1	9.5	1	10.5	ns
		C <sub>L</sub> = 50 pF	-	6.1	11.4	1	13	1	14	ns
		V <sub>CC</sub> = 4.5 V to 5.5 V								
		C <sub>L</sub> = 15 pF	-	3.4	5.5	1	6.5	1	7.5	ns
		C <sub>L</sub> = 50 pF	-	4.8	7.5	1	8.5	1	9.5	ns
C <sub>I</sub>	input capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 3.3 V	-	2	6	-	6	-	6	pF
C <sub>O</sub>	output capacitance	V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 3.3 V	-	5.6	-	-	-	-	-	pF
C <sub>PD</sub>	power dissipation capacitance	per buffer; C <sub>L</sub> = 50 pF; f = 10 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> [3]								
		V <sub>CC</sub> = 3.3 V	-	9.8	-	-	-	-	-	pF
		V <sub>CC</sub> = 5.0 V	-	10.3	-	-	-	-	-	pF

[1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 2.5 V, 3.3 V, and 5 V respectively, unless otherwise specified.

[2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

C<sub>L</sub> = output load capacitance in pF;

V<sub>CC</sub> = supply voltage in V;

N = number of inputs switching;

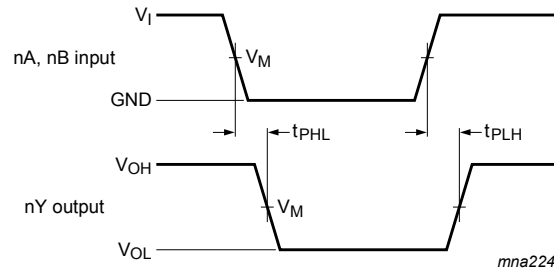
∑(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs.

**Table 8. Noise characteristics at T<sub>amb</sub> = 25 °C**

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>OL(p)</sub>	LOW-level output voltage (peak)	V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 50 pF	-	0.2	0.8	V
V <sub>OL(v)</sub>	LOW-level output voltage (valley)	V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 50 pF	-0.8	-0.1	-	V
V <sub>OH(v)</sub>	HIGH-level output voltage (valley)	V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 50 pF	-	3.1	-	V
V <sub>IH(AC)</sub>	AC HIGH-level input voltage	V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 50 pF	2.31	-	-	V
V <sub>IL(AC)</sub>	AC LOW-level input voltage	V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 50 pF	-	-	0.99	V

10.1. Waveforms and test circuit



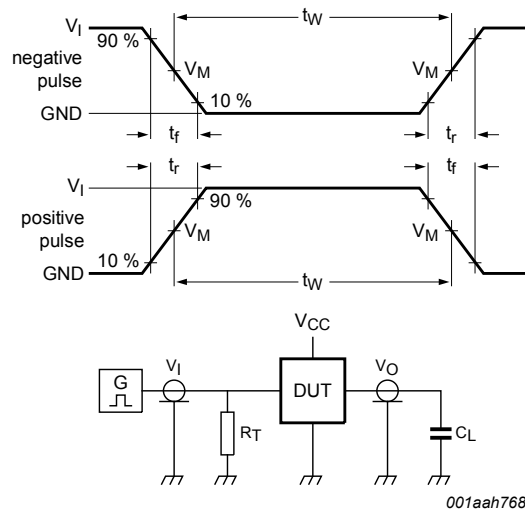
Measurement points are given in [Table 9](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

Fig. 5. Input (nA, nB) to output (nY) propagation delays

Table 9. Measurement points

Input	Output
$V_M$	$V_M$
$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 10](#).

Definitions test circuit:

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator

$C_L$  = Load capacitance including jig and probe capacitance

Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Input		Load	Test
$V_I$	$t_r, t_f$	$C_L$	
GND to $V_{CC}$	3.0 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

### 11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

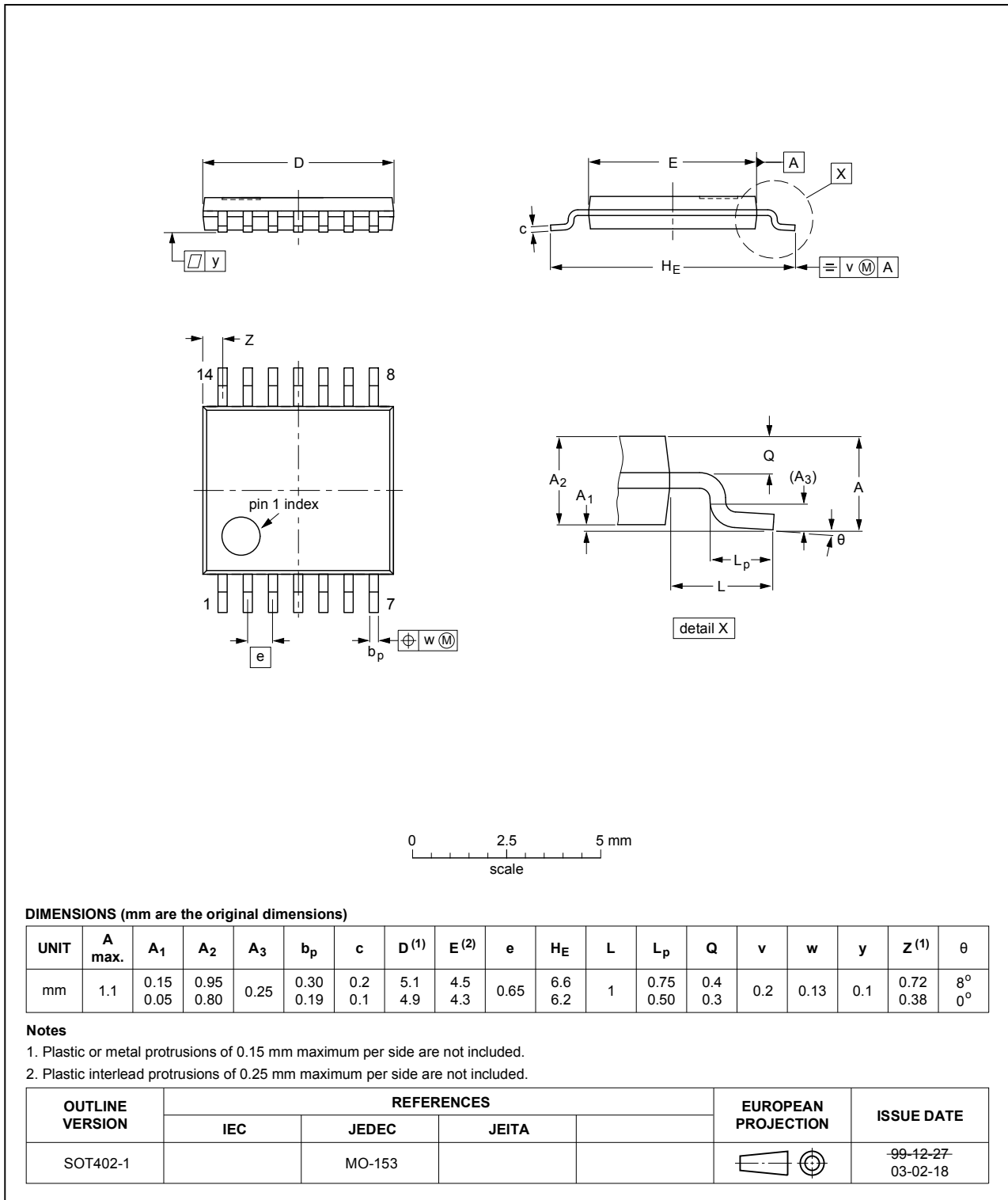


Fig. 7. Package outline SOT402-1 (TSSOP14)

## 12. Abbreviations

**Table 11. Abbreviations**

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TBD	To Be Determined

## 13. Revision history

**Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV7032A v.1	20181219	Product data sheet	-	-



## Quad 2-input OR gate with Schmitt trigger inputs

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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