ACPL-P480 and ACPL-W480

High CMR Intelligent Power Module and Gate Drive Interface Optocoupler

Data Sheet

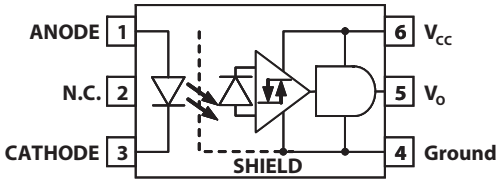
Description

The high-speed ACPL-P480/W480 optocoupler contains a GaAsP LED, a photo detector, and a Schmitt trigger that eliminates the requirement for external waveform conditioning circuits. The totem pole output eliminates the need for a pull-up resistor and allows for a direct-drive Intelligent Power Module or gate drive. Propagation delay difference between devices has been minimized to maximize inverter efficiency through reduced switching dead time.

Applications

- IPM Interface Isolation
- Isolated IGBT/MOSFET Gate Drive
- AC and Brushless DC Motor Drives
- Industrial Inverters
- General Digital Isolation

Functional Diagram



Note: A 0.1 µF bypass capacitor must be connected between pins 4 and 6.

Truth Table (Non-Inverting Logic)

LED	V0
ON	HIGH
OFF	LOW

Features

- Performance Specified for Common IPM Applications Over Industrial Temperature Range
- Short Maximum Propagation Delays
- Minimized Pulse Width Distortion (PWD)
- Very High Common Mode Rejection (CMR)
- Hysteresis
- Totem Pole Output (No Pull-up Resistor Required)
- Available in Stretched SO-6 Package
- Package Clearance/Creepage at 8 mm (ACPL-W480)
- Safety Approval:
  - UL Recognized with 3750V_{RMS} for 1 minute (5000V_{RMS} for 1 minute for all ACPL-W480 devices and Option 020 device for ACPL-P480) per UL1577
  - CSA Approved
  - IEC/EN/DIN EN 60747-5-5 approved with V_{IORM} = 891V_{peak} for ACPL-P480 and V_{IORM} = 1140V_{peak} for ACPL-W480

Specifications

- Wide Operating Temperature Range: –40°C to 100°C
- Maximum Propagation Delay t_{PHL}/t_{PLH} = 350 ns
- Maximum Pulse Width Distortion (PWD) = 250 ns
- Propagation Delay Difference: Min. –100 ns, Max. 250 ns
- Wide Operating V_{CC} Range: 4.5V to 20V
- 20 kV/µs Minimum Common Mode Rejection (CMR) at V_{CM} = 1000V

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

ACPL-P480 is UL Recognized with 3750V_{RMS} for 1 minute and ACPL-W480 is UL Recognized with 5000V_{RMS} for 1 minute per UL1577. Both are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option	Package	Surface Mount	Tape and Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant					
ACPL-P480	-000E	7 mm Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per tube
	-020E		X			100 per tube
	-520E		X	X		1000 per tube
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per tube
ACPL-W480	-000E	8 mm Stretched SO-6	X			100 per tube
	-500E		X	X		1000 per tube
	-060E		X		X	100 per tube
	-560E		X	X	X	1000 per tube

To order, choose a part number from the part number column and combine with the desired option from the option column to form an ordering part number.

Example 1:

ACPL-P480-560E to order product of Stretched SO-6 package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

ACPL-P480-000E to order product of Stretched SO-6 package in tube packaging and RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

Solder Reflow Profile

The recommended reflow profile is per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

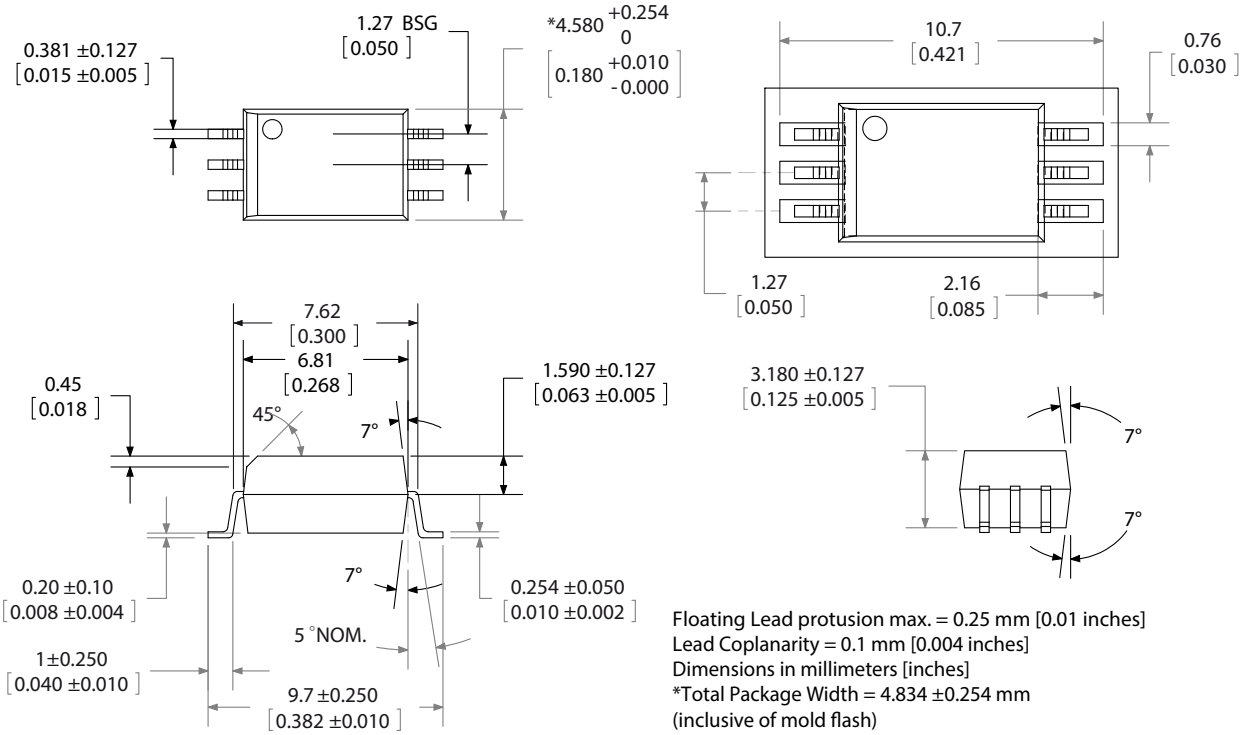
Regulatory Information

The ACPL-P480 and ACPL-W480 are approved by the following organizations:

- IEC/EN/DIN EN 60747-5-5 (Option 060 only):
  - IEC 60747-5-5: 2007
  - EN 60747-5-5: 2011
  - DIN EN 60747-5-5 (VDE 0884-5): 2011-11
- UL:
  - ACPL-P480: Approval under UL 1577, component recognition program up to V_{ISO} = 3750V_{RMS}. File E55361.
  - ACPL-W480 and ACPL-P480 (option 020): Approval under UL 1577, component recognition program up to V_{ISO} = 5000V_{RMS}. File E55361.
- CSA: Approval under CSA Component Acceptance Notice #5, File CA 88324.

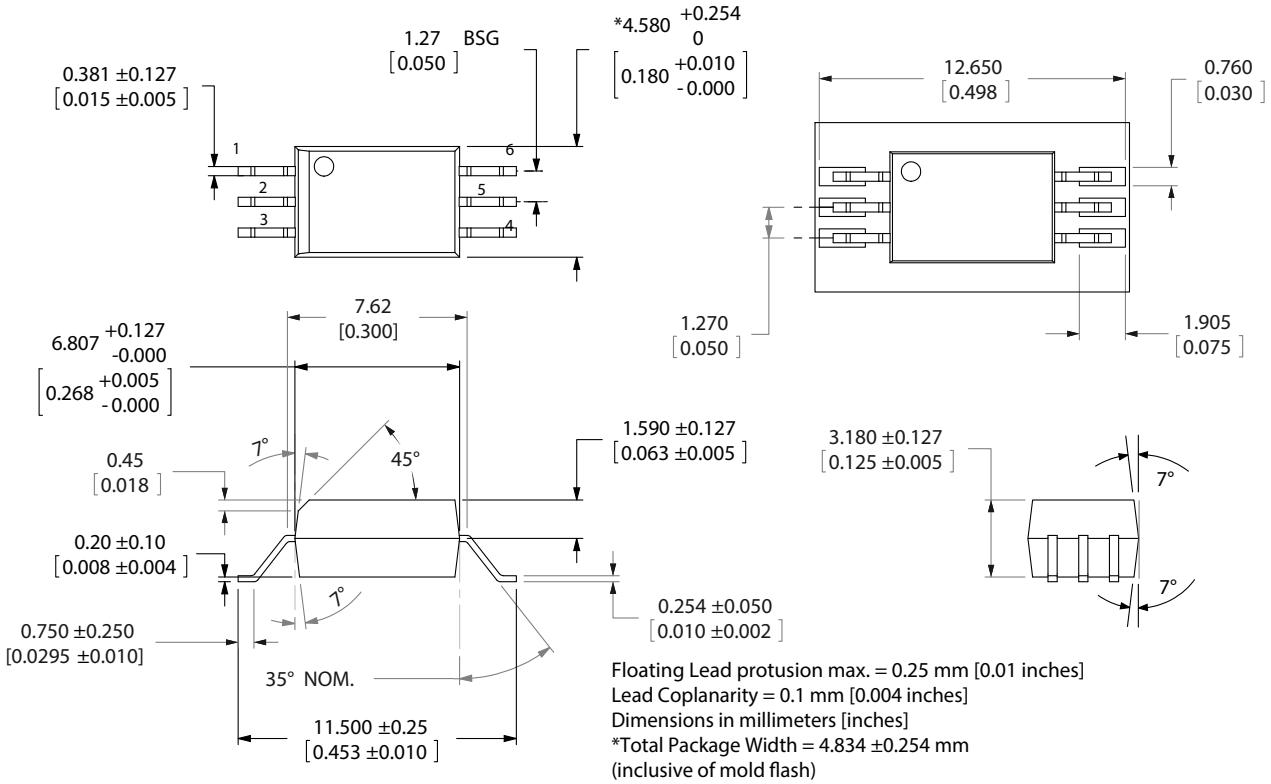
Package Outline Drawings

ACPL-P480 Stretched SO-6 Package (7 mm Clearance)



Floating Lead protusion max. = 0.25 mm [0.01 inches]
Lead Coplanarity = 0.1 mm [0.004 inches]
Dimensions in millimeters [inches]
*Total Package Width = 4.834 ±0.254 mm
(inclusive of mold flash)

ACPL-W480 Stretched SO-6 Package (8 mm Clearance)



Floating Lead protusion max. = 0.25 mm [0.01 inches]
Lead Coplanarity = 0.1 mm [0.004 inches]
Dimensions in millimeters [inches]
*Total Package Width = 4.834 ±0.254 mm
(inclusive of mold flash)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics (Option 060)

Description	Symbol	ACPL-P480	ACPL-W480	Unit
Installation Classification per DIN VDE 0110/39, Table 1 for rated mains voltage ≤ 150V_{RMS} for rated mains voltage ≤ 300V_{RMS} for rated mains voltage ≤ 600V_{RMS}		 I– IV I – IV I – III	 I – IV I – IV I – IV	
Climatic Classification	55/100/21			
Pollution Degree (DIN VDE 0110/39)	2			
Maximum Working Insulation Voltage	V_{IORM}	891	1140	V_{peak}
Input to Output Test Voltage, Method b[a] V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1670	2137	V_{peak}
Input to Output Test Voltage, Method a[a] V_{IORM} x 1.6=V_{PR}, Type and Sample Test, t_m = 10 sec, Partial Discharge < 5 pC	V_{PR}	1426	1824	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	6000	8000	V_{peak}
Safety-limiting Values – maximum values allowed in the event of a failure				
Case Temperature	T_S	175		°C
Input Current	$I_{S, INPUT}$	230		mA
Output Power	$P_{S, OUTPUT}$	600		mW
Insulation Resistance at T_S, V_{IO} = 500V	R_S	$>10^9$		Ω

a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under the Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5), for a detailed description of Method a and Method b partial discharge test profiles.

Insulation and Safety Related Specifications

Parameter	Symbol	ACPL-P480	ACPL-W480	Unit	Condition
Minimum External Air Gap (External Clearance)	L(101)	7.0	8.0	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	8.0	8.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08		mm	Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector.
Minimum Internal Tracking (Internal Creepage)		N/A		mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	>175		V	DIN IEC 112/VDE 0303 Part 1.
Isolation Group		IIIa			Material Group (DIN VDE 0110, 1/89, Table 1).

UL 1577 Specification Sheet

Model	Package Type	Current, mA		Power, mW		Isolation Voltage 1 min, V_{RMS}	Maximum Operating Temperature, °C	Maximum Junction Temperature, °C	Maximum Storage Temperature, °C
		Emitter	Sensor	Emitter	Sensor				
P480	3	10	25	15	560	5000	110	125	125

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	–55	+125	°C
Operating Temperature	T_A	–40	+100	°C
Average Input Current	$I_{F(AVG)}$		10	mA
Peak Transient Input Current (<1 µs pulse width, 300 pps) (<200 µs pulse width, <1% duty cycle)	$I_{F(TRAN)}$		 1.0 40	 A mA
Reverse Input Voltage	V_R		5	V
Average Output Current	I_O		25	mA
Supply Voltage	V_{CC}	0	25	V
Output Voltage	V_O	–0.5	+25	V
Total Package Power Dissipation[a]	P_T		210	mW

a. Derate total package power dissipation, PT, linearly above 70°C free-air temperature at a rate of 4.5 mW/°C.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{CC}	4.5	20	V	
Forward Input Current (OFF)	$I_{F(OFF)}$	6	10	mA	
Forward Input Voltage (ON)	$V_{F(ON)}$		0.8	V	
Operating Temperature	T_A	–40	+100	°C	

Electrical Specifications

Over recommended operating conditions T_A = –40°C to +100°C, V_{CC} = +4.5V to 20V, $I_{F(ON)}$ = 6 mA to 10 mA, $V_{F(OFF)}$ = 0V to 0.8V, unless otherwise specified. All typicals at T_A = 25°C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Logic Low Output Voltage	V_{OL}			0.5	V	I_{OL} = 6.4 mA	1, 3, 9, 10	
Logic High Output Voltage	V_{OH}	2.4	V_{CC} – 1.1		V	I_{OH} = –2.6 mA	2, 3, 7, 9, 10	
ACPL-P480		2.7				I_{OH} = –0.4 mA		
ACPL-W480		2.7				I_{OH} = –1.6 mA		

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Threshold Input Current Low to High			2.2	5.5	mA			
Output Leakage Current ($V_O = V_{CC} + 0.5V$)	I_{OHH}			100	µA	$V_{CC} = 5V$, $I_F = 10$ mA		
				500	µA	$V_{CC} = 20V$, $I_F = 10$ mA		
Logic Low Supply Current	I_{CCL}		1.9	3.0	mA	$V_{CC} = 5.5V$, $V_F = 0V$, I_O = Open		
			2.0	3.0	mA	$V_{CC} = 20V$, $V_F = 0V$, I_O = Open		
Logic High Supply Current	I_{CCH}		1.5	2.5	mA	$V_{CC} = 5.5V$, $I_F = 10$ mA, I_O = Open		
			1.6	2.5	mA	$V_{CC} = 20V$, $I_F = 10$ mA, I_O = Open		
Logic Low Short Circuit Output Current	I_{OSL}	25			mA	$V_O = V_{CC} = 5.5V$, $V_F = 0V$		a
		50			mA	$V_O = V_{CC} = 20V$, $V_F = 0V$		
Logic High Short Circuit Output Current	I_{OSH}			–25	mA	$V_{CC} = 5.5V$, $I_F = 10$ mA, I_O = Open		a
				–50	mA	$V_{CC} = 20V$, $I_F = 10$ mA, I_O = Open		
Input Forward Voltage	V_F		1.5	1.7	V	$T_A = 25°C$, $I_F = 6$ mA	4	
				1.85	V	$I_F = 6$ mA		
Input Reverse Breakdown Voltage	BV_R	5			V	$I_R = 10$ µA		
Input Diode Temperature Coefficient	$\Delta V_F/\Delta T_A$		1.7		mV/°C	$I_F = 6$ mA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, $V_F = 0V$		b

a. Duration of output short circuit time should not exceed 10 ms.

b. Input capacitance is measured between pin 1 and pin 3.

Switching Specifications

Over recommended operating conditions T_A = –40°C to +100°C, V_{CC} = +4.5V to 20V, $I_{F(ON)}$ = 6 mA to 10 mA, $V_{F(OFF)}$ = 0V to 0.8V, unless otherwise specified. All typicals at T_A = 25 °C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		150	350	ns	with Peaking Capacitor	5, 6	1
Propagation Delay Time to Logic High Output Level	t_{PLH}		110	350	ns	with Peaking Capacitor	5, 6	1
Pulse Width Distortion	$\lvert t_{PHL} - t_{PLH} \rvert = PWD$			250	ns			2
Propagation Delay Difference Between Any Two Parts	PDD	–100		+250	ns			3
Output Rise Time (10% to 90%)	t_r		16		ns		5, 8	
Output Fall Time (90% to 10%)	t_f		20		ns		5, 8	
Logic High Common Mode Transient Immunity	$\lvert CM_H \rvert$	20			kV/µs	$\lvert V_{CM} \rvert = 1000V$, $I_F = 6.0$ mA $V_{CC} = 5V$, $T_A = 25°C$	11	4
Logic Low Common Mode Transient Immunity	$\lvert CM_L \rvert$	20			kV/µs	$\lvert V_{CM} \rvert = 1000V$, $V_F = 0V$, $V_{CC} = 5V$, $T_A = 25°C$	11	4

Package Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage[a]	V_{ISO}	3750[b] 5000[c]			V_{RMS}	RH < 50%, t = 1 min. T_A = 25°C		5, 6
Input-Output Resistance	R_{I-O}		10^{12}			V_{I-O} = 500V_{DC}		5
Input-Output Capacitance	C_{I-O}		0.6			f = 1 MHz, V_{I-O} = 0V_{DC}		5

a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable).

b. For all ACPL-P480 devices except Option 020.

c. For ACPL-W480 and Option 020 of ACPL-P480)

Notes:

1. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3V point on the trailing edge of the output pulse.
2. Pulse Width Distortion (PWD) is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
3. The difference between t_{PLH} and t_{PHL} between any two devices under the same test condition.
4. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state, V_O > 2.0V. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state, V_O < 0.8V.
5. Device considered a two-terminal device: pins 1, 2, and 3 shorted together and pins 4, 5, and 6 shorted together.
6. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage 4500V_{RMS} for one second (leakage detection current limit, $I_{I-O} \leq 5$ µA); each optocoupler with option 020 is proof tested by applying an insulation test voltage. 6000V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-2 Insulation Characteristics Table, if applicable.
7. Use of a 0.1 µF bypass capacitor connected between pins 4 and 6 is recommended.

Figure 1 Typical Logic Low Output Voltage vs. Temperature

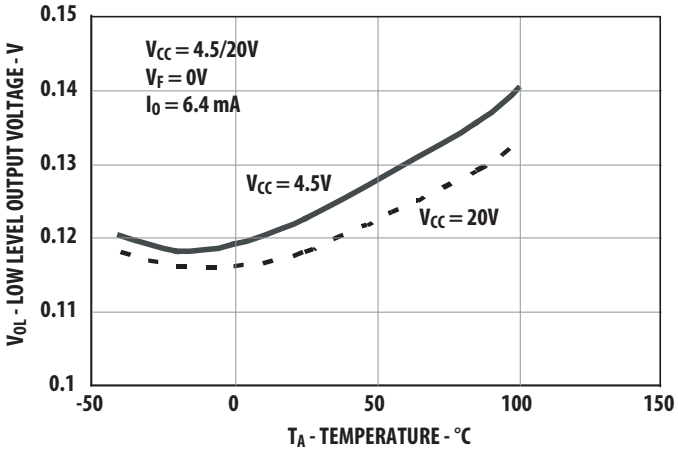


Figure 2 Typical Logic High Output Current vs. Temperature

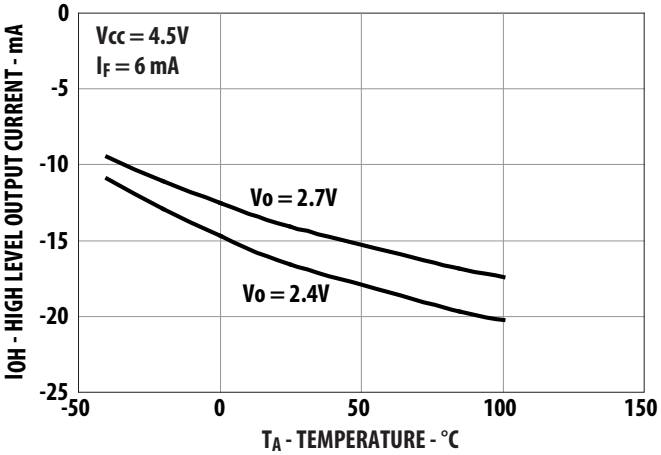


Figure 3 Typical Output Voltage vs. Forward Input Current

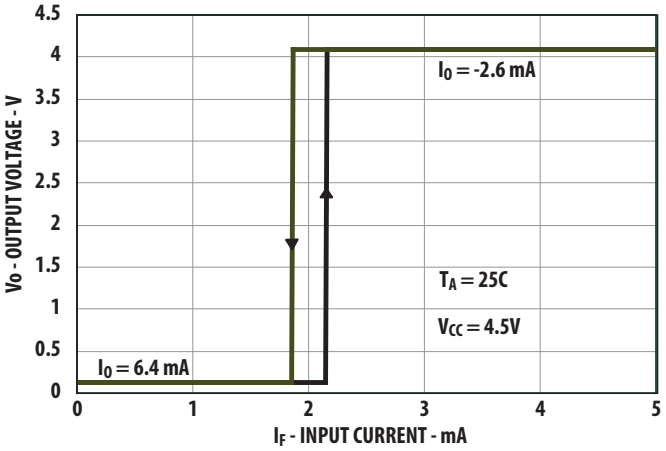


Figure 4 Typical Input Diode Forward Characteristic

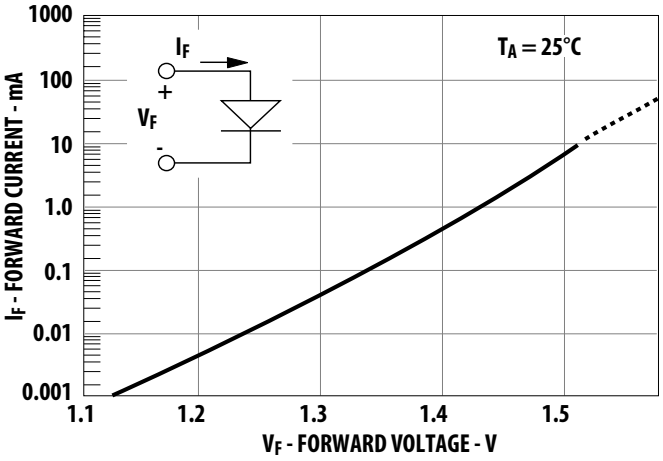
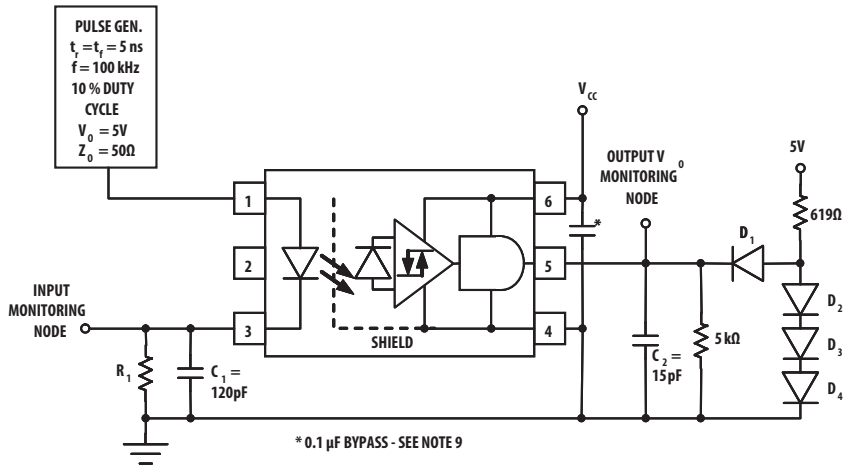


Figure 5 Test Circuit for t_{PLH}, t_{PHL}, t_r, and t_f



THE PROBE AND JIG CAPACITANCES ARE INCLUDED IN C_1 AND C_2.

R_1	580Ω	330Ω
$I_{F(ON)}$	6 mA	10 mA

ALL DIODES ARE 1N916 OR 1N3064.

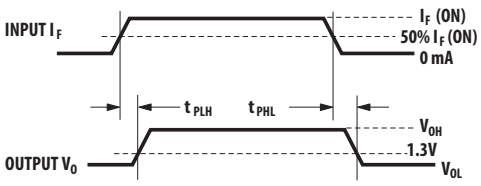


Figure 6 Typical Propagation Delays vs. Temperature

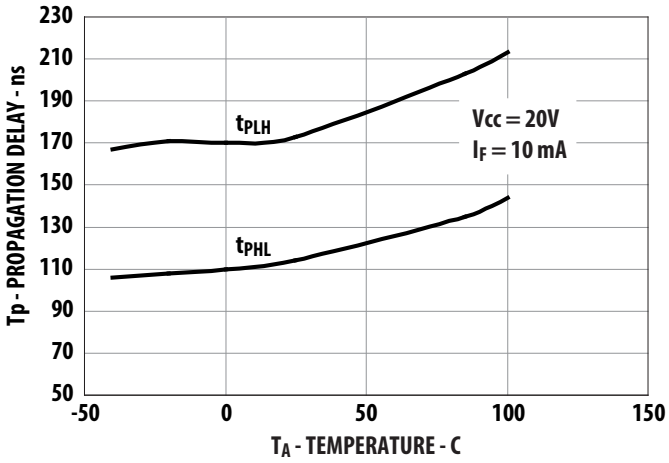


Figure 7 Typical Logic High Output Voltage vs. Supply Voltage

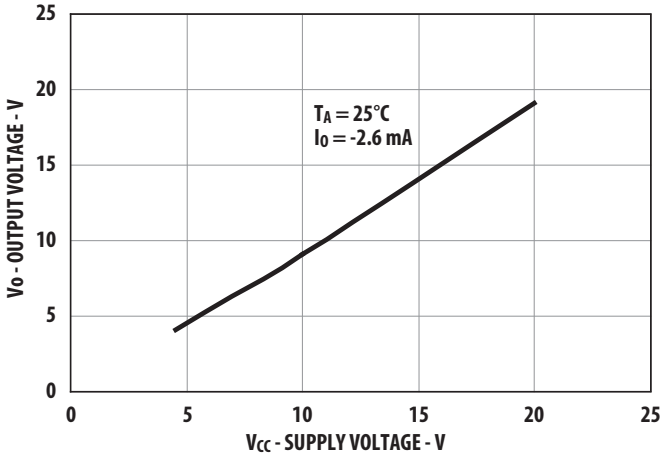


Figure 8 Typical Propagation Delay vs. Supply Voltage

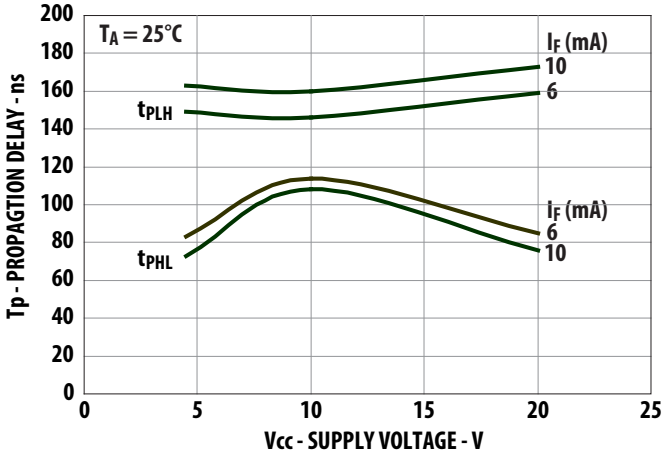


Figure 9 V_{OH} vs. I_{OH} Across Temperatures

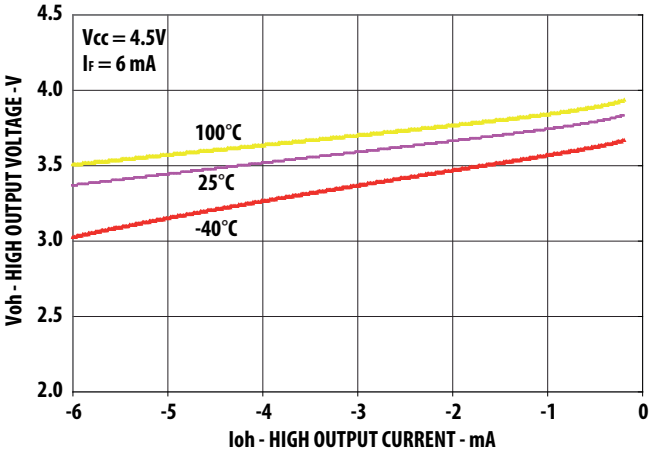


Figure 10 V_{OL} vs. I_{OL} Across Temperatures

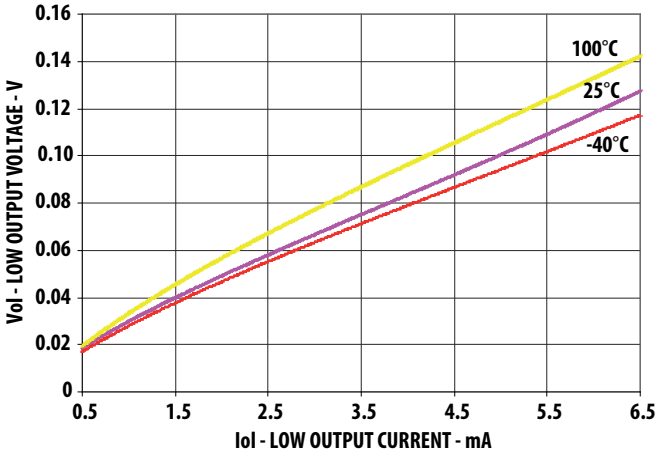
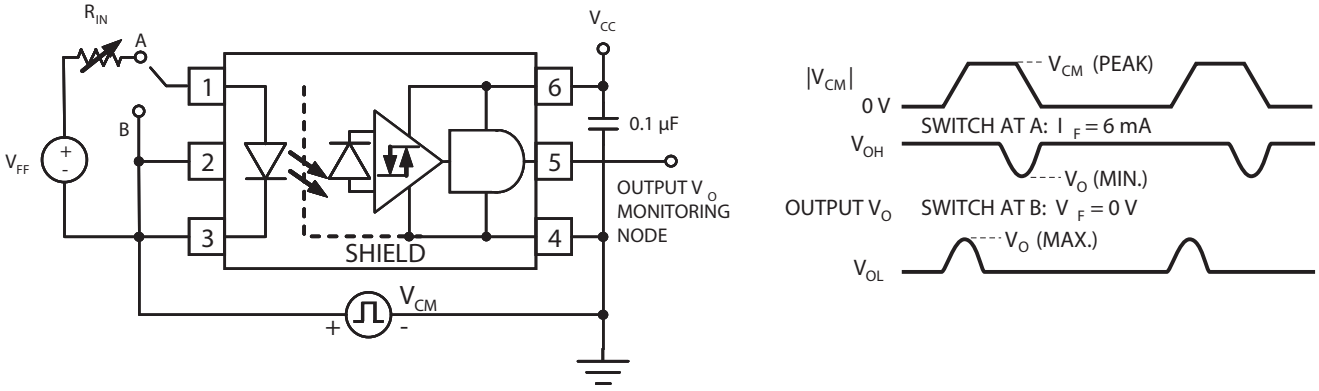


Figure 11 Test Circuit for Common Mode Transient Immunity and Typical Waveforms



For product information and a complete list of distributors, please go to our web site: www.broadcom.com.

AV02-1305EN – August 24, 2017

Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product