TEXAS INSTRUMENTS

OPA171-Q1, OPA2171-Q1, OPA4171-Q1

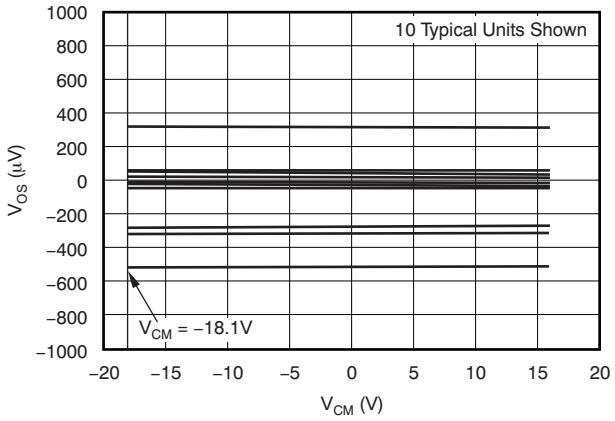
ZHCS213C – JUNE 2011 – REVISED DECEMBER 2015

OPAx171-Q1 36V 单电源通用运算放大器

1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 测试指导的以下结果：
  - 器件温度 1 级：-40°C 至 +125°C 的环境运行温度范围
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级：
    - 等级 3A：针对 OPA171-Q1
    - 等级 3A：针对 OPA2171-Q1
    - 等级 2：针对 OPA4171-Q1
  - 器件充电器件模型 (CDM) ESD 分类等级
    - 等级 C4A：针对 OPA171-Q1
    - 等级 C6：针对 OPA2171-Q1
    - 等级 C6：针对 OPA4171-Q1
- 电源电压范围：2.7V 至 36V，±1.35V 至 ±18V
- 低噪声：14nV/√Hz
- 低偏移漂移：0.3μV/°C（典型值）
- 已过滤的射频干扰 (RFI) 输入
- 输入范围包括负电源
- 输入范围运行至正电源
- 轨至轨输出
- 增益带宽：3MHz
- 低静态电流：每个放大器 475μA
- 高共模抑制：120dB（典型值）
- 低输入偏置电流：8pA
- 行业标准封装：
  - 5 引脚小外形尺寸晶体管 SOT-23 (DBV) 封装

偏移电压与共模电压间的关系



2 应用范围

- 电源模块内的跟踪放大器
- 商用电源
- 变频器放大器
- 桥式放大器
- 温度测量
- 应力计放大器
- 精密积分器
- 电池供电仪器
- 测试设备

3 说明

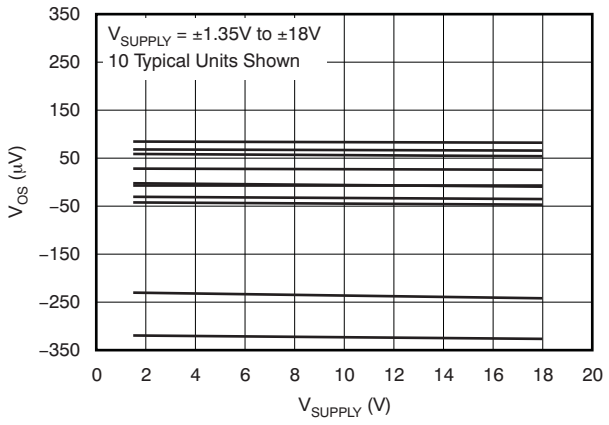
OPA171-Q1 系列器件是 36V 单电源低噪声运算放大器 (op amp)，能够在 2.7V (±1.35V) 至 36V (±18V) 的电源电压范围内运行。该器件采用微型封装，并且具有低偏移、低漂移、低带宽以及低静态电流特性。单通道、双通道和四通道版本均具有相同的技术规格，可最大程度地提高设计灵活性。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA171-Q1	SOT-23 (5)	2.90mm x 1.60mm
OPA2171-Q1	SOIC (8)	4.90mm x 3.91mm
	VSSOP (8)	3.00mm × 3.00mm
OPA4171-Q1	SOIC (14)	8.65mm x 3.91mm
	薄型小外形尺寸封装 (TSSOP) (14)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

偏移电压与电源间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (December 2014) to Revision C **Page**

- 已更改 特性列表中 HBM 和 CDM 的*ESD*分类等级 ... 1
- 已添加 8 引脚 VSSOP (DGK) 封装至 OPA2171-Q1 器件的封装选项 ... 1
- Clarified the ESD values for each device in the *ESD Ratings* table ... 5

Changes from Revision A (September 2012) to Revision B **Page**

- 已添加 *处理额定值*表，*特性 描述*部分，*器件功能模式*部分，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Original (June, 2011) to Revision A **Page**

- 已在 特性：“具有下列结果的 AEC-Q100 测试指南”中增加了第二项特性要点：– 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围/– 器件 HBM ESD 分类等级 H2/– 器件 CDM ESD 分类等级 C3A ... 1
- 已添加 PA2171-Q1 以及 OPA4171-Q1 器件到本数据表 ... 1
- Added classification levels to ESD ratings in Absolute Maximum Ratings table. ... 4
- Added row to Absolute Maximum Ratings table: Latch-up per JESD78D with Class 1 value. ... 4

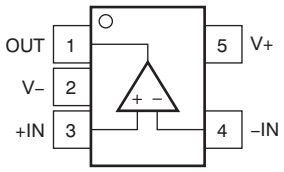
5 说明（续）

大多数运算放大器仅有一个指定的电源电压，OPAx171-Q1 系列则有所不同，其可在 2.7V 至 36V 电压范围内可额定运行。超过电源轨的输入信号并不会导致反相。OPAx171-Q1 系列器件与高达 300pF 的电容性负载搭配使用时可保持稳定。输入信号可在负电源轨以下 100mV 到正电源轨以上 2V 范围内保持正常运行。该器件可在正电源轨之上 100mV 轨到轨满输入电压下运行，但在正电源轨 2V 范围内运行时会降低性能。

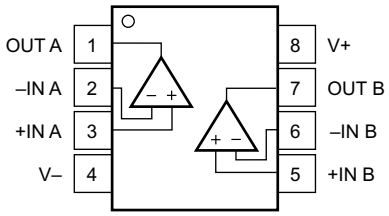
OPAx171-Q1 运算放大器的额定工作温度范围为 -40°C 至 +125°C。

6 Pin Configuration and Functions

DBV Package
5-Pin SOT23
OPA171-Q1 Top View



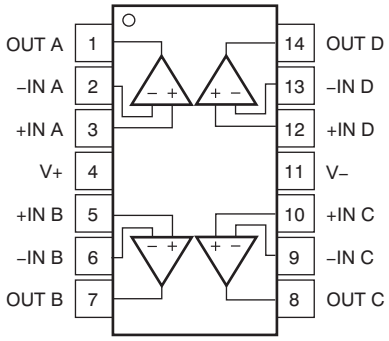
D or DGK Package
8-Pin SOIC or VSSOP
OPA2171-Q1 Top View



Pin Functions — SOT-23 (5), SOIC (8), and VSSOP (8) Packages

PIN			I/O	DESCRIPTION
NAME	OPA171-Q1 SOT-23 (5)	OPA2171-Q1 SOIC AND VSSOP (8)		
+IN	3	—	I	Noninverting input
+IN A	—	3	I	Noninverting input, channel A
+IN B	—	5	I	Noninverting input, channel B
–IN	4	—	I	Inverting input
–IN A	—	2	I	Inverting input, channel A
–IN B	—	6	I	Inverting input, channel B
OUT	1	—	O	Output
OUT A	—	1	O	Output, channel A
OUT B	—	7	O	Output, channel B
V+	5	7	—	Positive (highest) power supply
V–	2	4	—	Negative (lowest) power supply

D and PW Packages
14-Pin SOIC and TSSOP
OPA4171-Q1 Top View



Pin Functions — SOIC (14) and TSSOP (14) Packages

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
+IN C	10	I	Noninverting input, channel C
+IN D	12	I	Noninverting input, channel D
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
–IN C	9	I	Inverting input, channel C
–IN D	13	I	Inverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V+	4	—	Positive (highest) power supply
V–	11	—	Negative (lowest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Supply voltage			40	V
Signal input terminals	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current		±10	mA
Output short circuit(2)		Continuous		
Operating temperature		–55	150	°C
Junction temperature			150	°C
Latch-up per JESD78D		Class 1		
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
OPA171-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±4000	V
		Charged device model (CDM), per AEC Q100-011	±500	
OPA2171-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±4000	V
		Charged device model (CDM), per AEC Q100-011	±1000	
OPA4171-Q1				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature	–40		125	°C

7.4 Thermal Information — OPA171-Q1 and OPA2171-Q1

THERMAL METRIC (1)		OPA171-Q1	OPA2171-Q1		UNIT
		DBV (SOT-23)	D (SOIC)	DGK (VSSOP)	
		5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	277.3	116.1	186.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	193.3	69.8	78	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	121.2	56.6	107.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	51.8	22.5	15.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	109.5	56.1	106.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Thermal Information — OPA4171-Q1

THERMAL METRIC (1)		OPA4171-Q1		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	106.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	51.8	24.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	59.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.5	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.2	54.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.6 Electrical Characteristics

At T_A = 25°C, V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted. The specified temperature range is T_A = –40°C to +125°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			0.25	±1.8	mV
	Input offset voltage over temperature			0.3	±2	mV

Electrical Characteristics (接下页)

At T_A = 25°C, V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted. The specified temperature range is T_A = –40°C to +125°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
dV_{OS}/dT	Input offset voltage drift (over temperature)			0.3	±2(1)	µV/°C
PSRR	Input offset voltage over temperature vs power supply	V_S = 4 to 36 V		1	±3	µV/V
	Channel separation, DC			5		µV/V

(1) Not production tested.

Electrical Characteristics (接下页)

At T_A = 25°C, V_S = 2.7 to 36 V, V_{CM} = V_{OUT} = V_S / 2, and R_{LOAD} = 10 kΩ connected to V_S / 2, unless otherwise noted. The specified temperature range is T_A = –40°C to +125°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT BIAS CURRENT						
I_B	Input bias current			±8	±15	pA
	Input bias current over temperature				±3.5	nA
I_{OS}	Input offset current			±4		pA
	Input offset current over temperature				±3.5	nA
NOISE						
	Input voltage noise	f = 0.1 Hz to 10 Hz		3		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz		25		nV/√Hz
		f = 1 kHz		14		nV/√Hz
INPUT VOLTAGE						
V_{CM}	Common-mode voltage range[(2)]		(V–) – 0.1		(V+) – 2	V
CMRR	Common-mode rejection ratio (over temperature)	V_S = ±2 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V	90	104		dB
		V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V	104	120		dB
INPUT IMPEDANCE						
	Differential			100 || 3		MΩ || pF
	Common-mode			6 || 3		10^{12}Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain (over temperature)	V_S = +4V to +36V, (V–) + 0.35V < V_O < (V+) – 0.35V	110	130		dB
FREQUENCY RESPONSE						
GBP	Gain bandwidth product			3.0		MHz
SR	Slew rate	G = 1		1.5		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = 1, 10-V step		6		µs
		To 0.01% (12 bit), V_S = ±18 V, G = 1, 10-V step		10		µs
	Overload recovery time	$V_{±IN}$ × Gain > V_S		2		µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3 V_{RMS}		0.0002%		
OUTPUT						
V_O	Voltage output swing from rail (over temperature)	R_L = 10 kΩ, A_{OL} ≥ 110 dB	(V–) + 0.35		(V+) – 0.35	V
I_{SC}	Short-circuit current	Sourcing		25		mA
		Sinking		–35		
C_{LOAD}	Capacitive load drive		See the *Typical Characteristics* section			pF
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0 A		150		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.7		36	V
I_Q	Quiescent current per amplifier	I_O = 0 A		475	595	µA
	Quiescent current per amplifier (over temperature)	I_O = 0 A			650	µA
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–55		150	°C

(2) The input range can be extended beyond (V+) – 2 V up to V+. See the *Typical Characteristics* and *Detailed Description* sections for additional information.

7.7 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

表 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	图 1
Offset Voltage Drift Distribution	图 2
Offset Voltage vs Temperature	图 3
Offset Voltage vs Common-Mode Voltage	图 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	图 5
Offset Voltage vs Power Supply	图 6
I_B and I_{OS} vs Common-Mode Voltage	图 7
Input Bias Current vs Temperature	图 8
Output Voltage Swing vs Output Current (Maximum Supply)	图 9
CMRR and PSRR vs Frequency (Referred-to Input)	图 10
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0.1Hz to 10Hz Noise	图 13
Input Voltage Noise Spectral Density vs Frequency	图 14
THD+N Ratio vs Frequency	图 15
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Open-Loop Output Impedance vs Frequency	图 22
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	图 23, 图 24
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Positive Overload Recovery	图 26
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Small-Signal Step Response (100 mV)	图 28, 图 29
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Large-Signal Settling Time (10-V Positive Step)	图 32
Large-Signal Settling Time (10-V Negative Step)	图 33
Short-Circuit Current vs Temperature	图 34
Maximum Output Voltage vs Frequency	图 35
Channel Separation vs Frequency	图 36

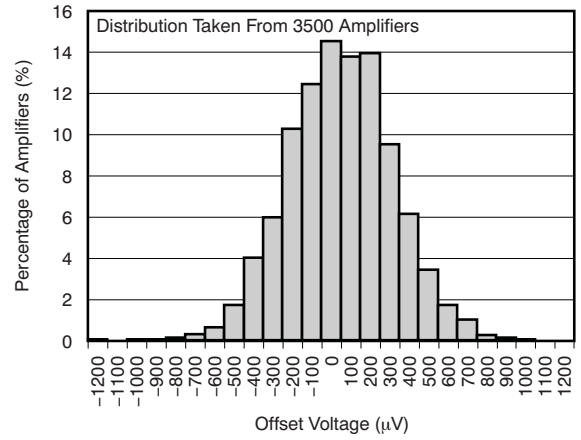


图 1. Offset Voltage Production Distribution

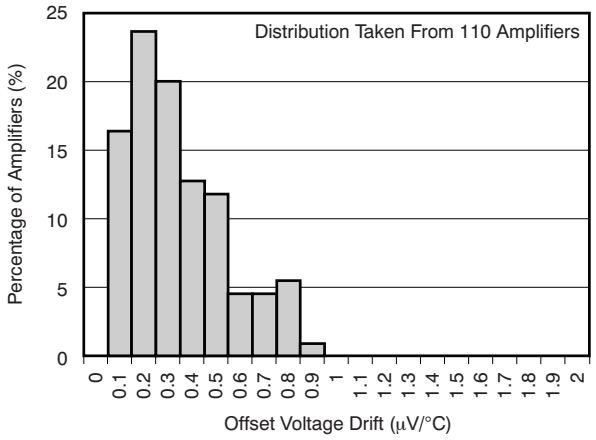


图 2. Offset Voltage Drift Distribution

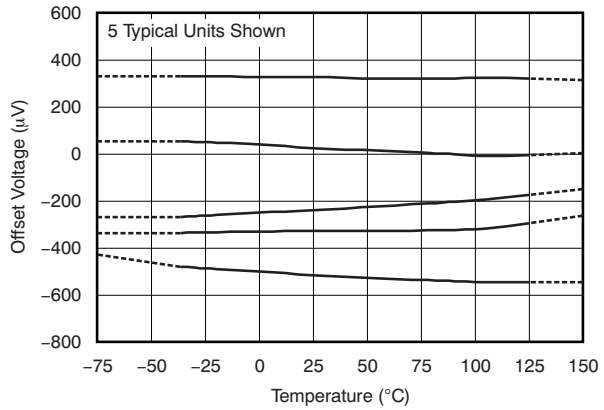


图 3. Offset Voltage vs Temperature

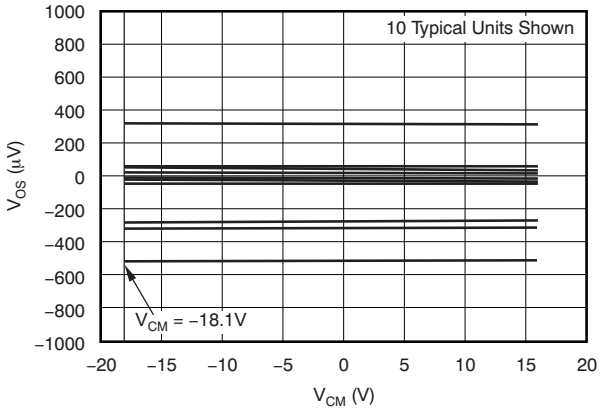


图 4. Offset Voltage vs Common-Mode Voltage

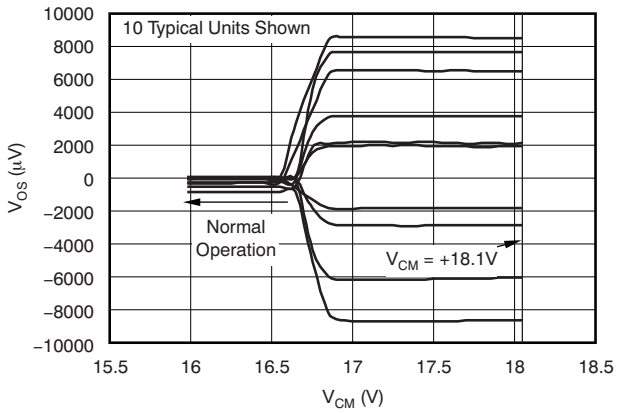


图 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

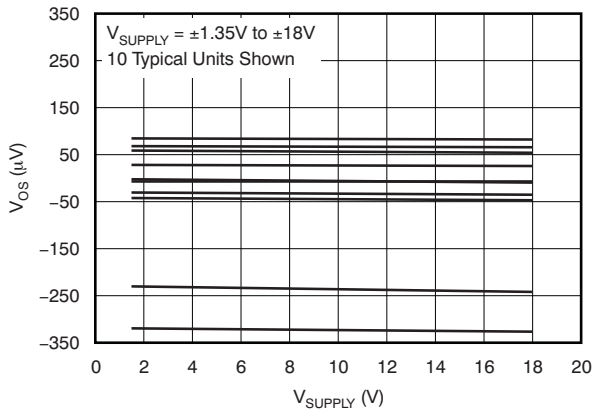


图 6. Offset Voltage vs Power Supply

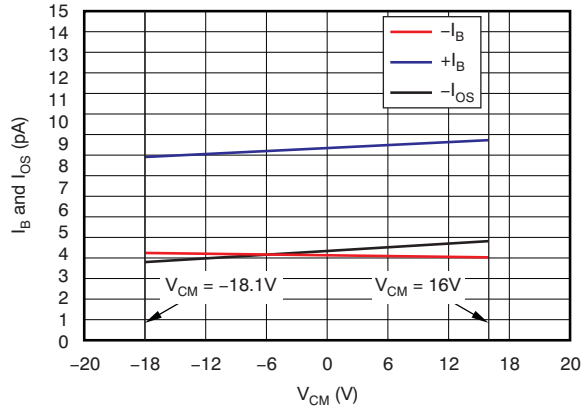


图 7. I_B and I_{OS} vs Common-Mode Voltage

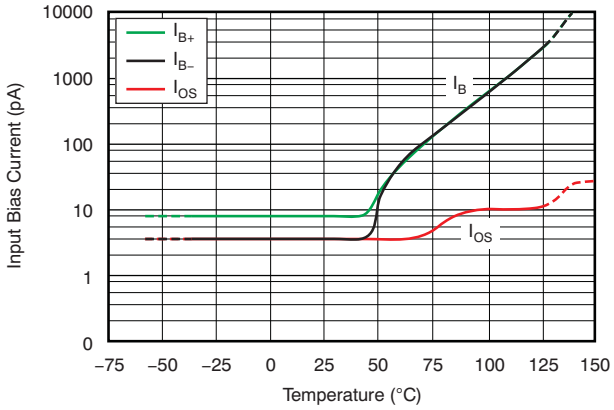


图 8. Input Bias Current vs Temperature

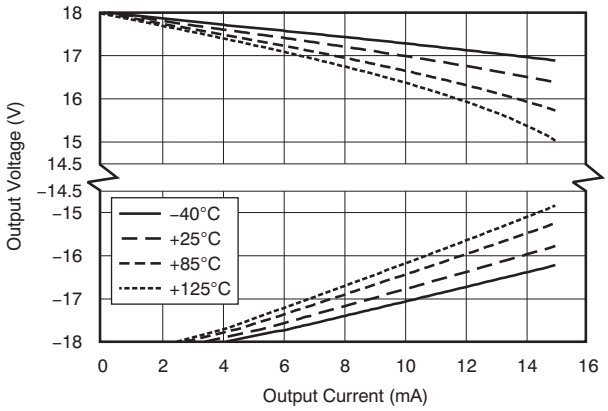


图 9. Output Voltage Swing vs Output Current (Maximum Supply)

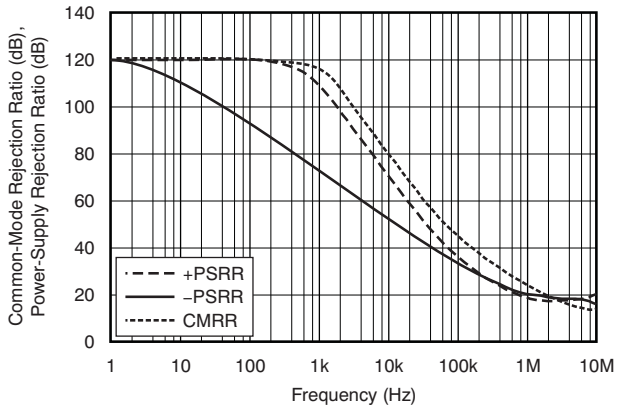


图 10. CMRR and PSRR vs Frequency (Referred-to Input)

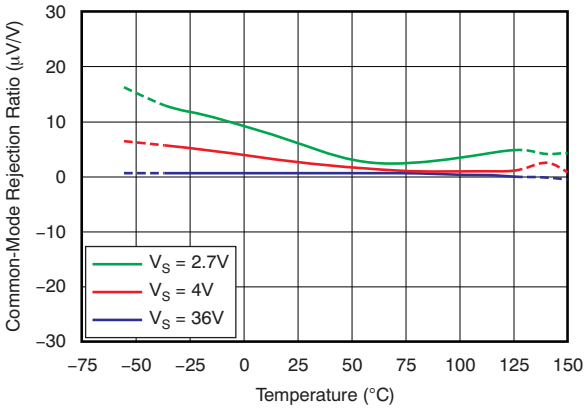


图 11. CMRR vs Temperature

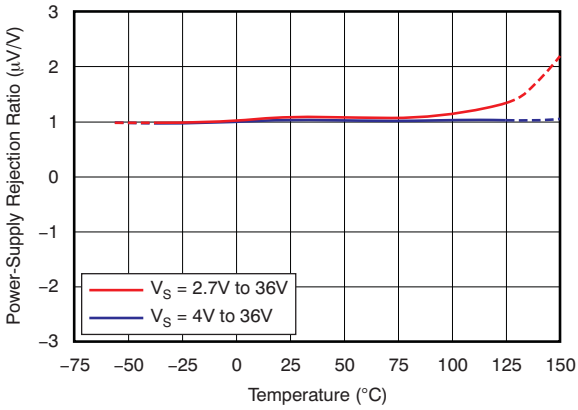


图 12. PSRR vs Temperature

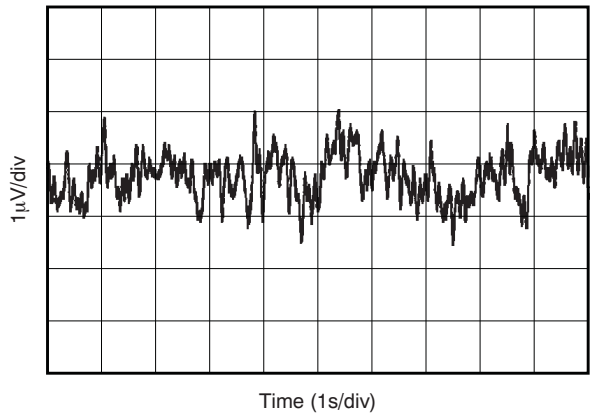


图 13. 0.1- to 10-Hz Noise

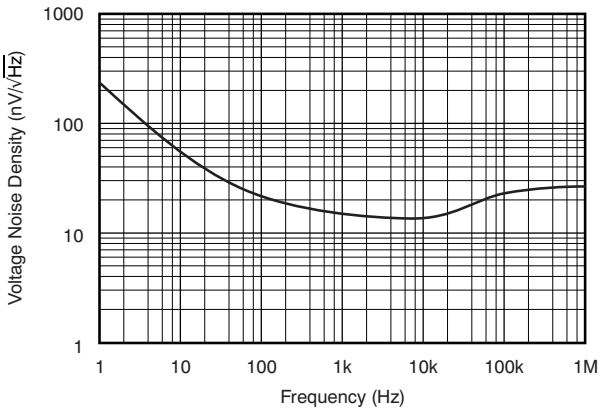


图 14. Input Voltage Noise Spectral Density vs Frequency

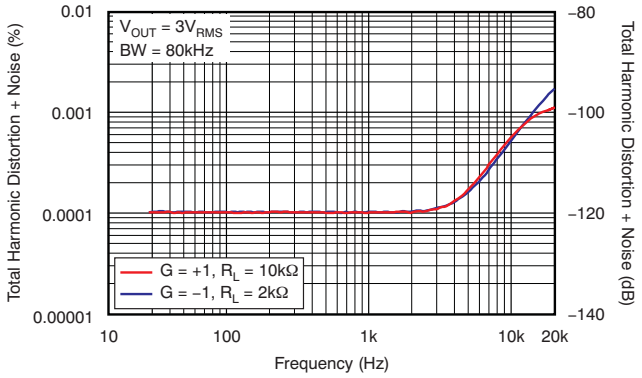


图 15. THD+N Ratio vs Frequency

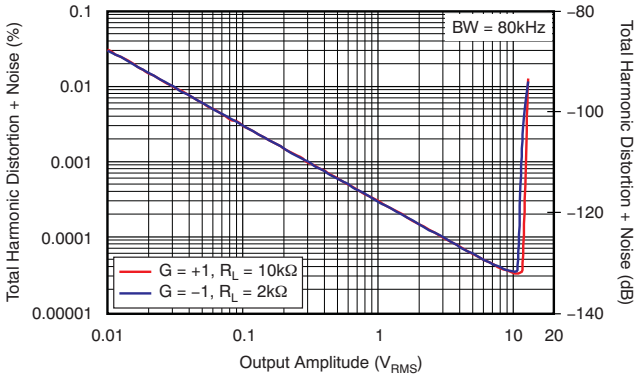


图 16. THD+N vs Output Amplitude

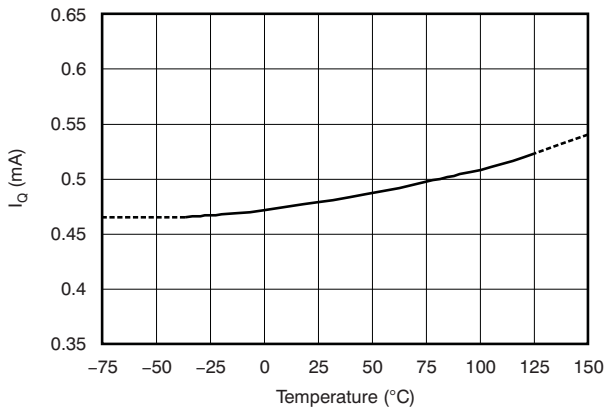


图 17. Quiescent Current vs Temperature

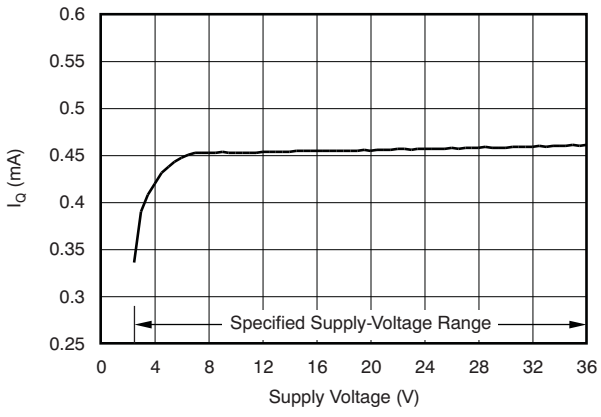


图 18. Quiescent Current vs Supply Voltage

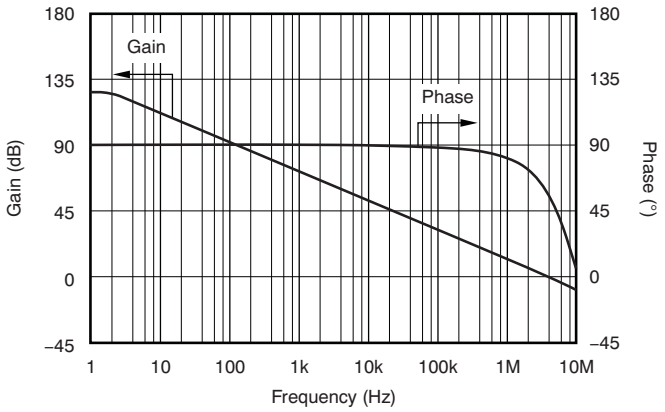


图 19. Open-Loop Gain and Phase vs Frequency

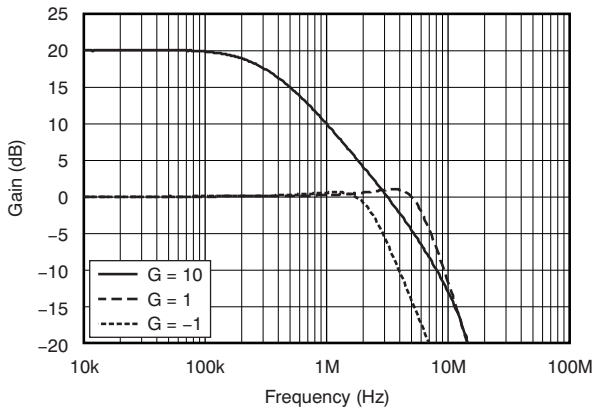


图 20. Closed-Loop Gain vs Frequency

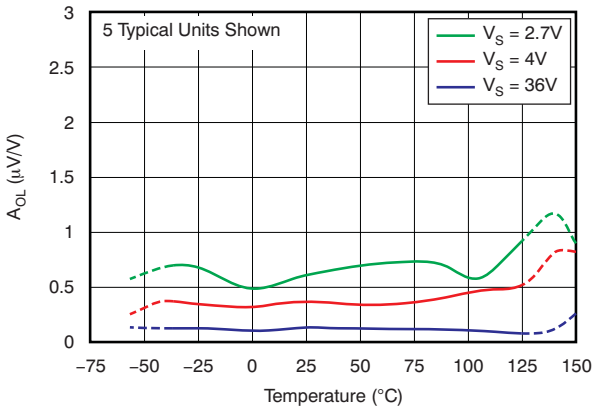


图 21. Open-Loop Gain vs Temperature

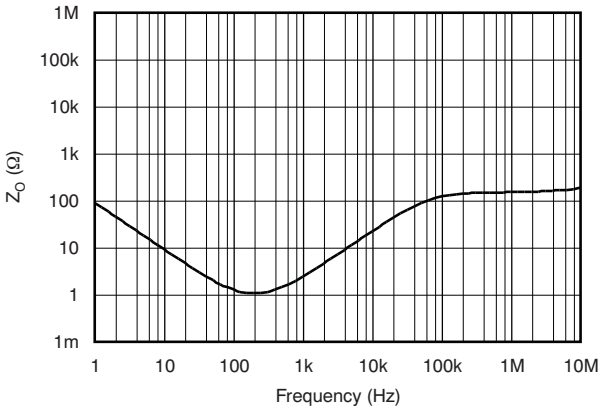


图 22. Open-Loop Output Impedance vs Frequency

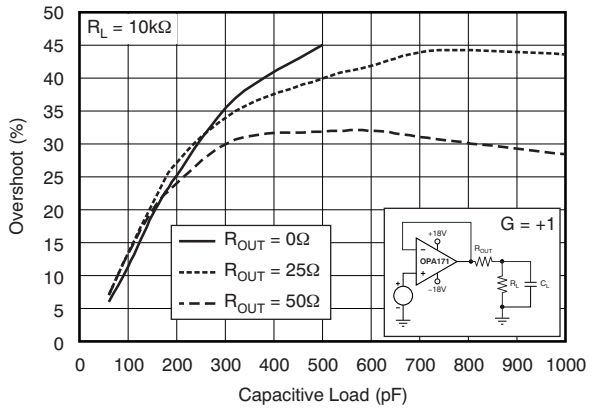


图 23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

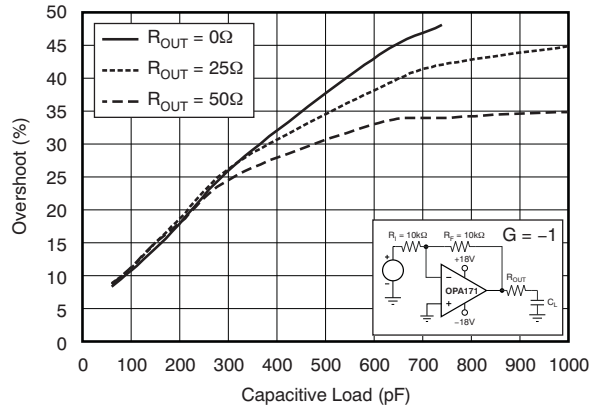


图 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

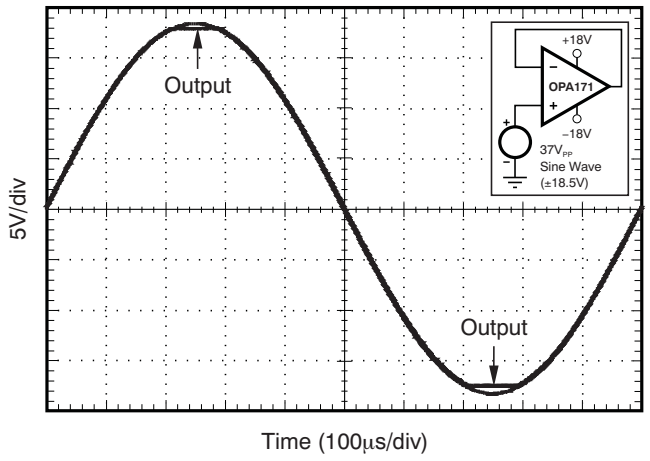


图 25. No Phase Reversal

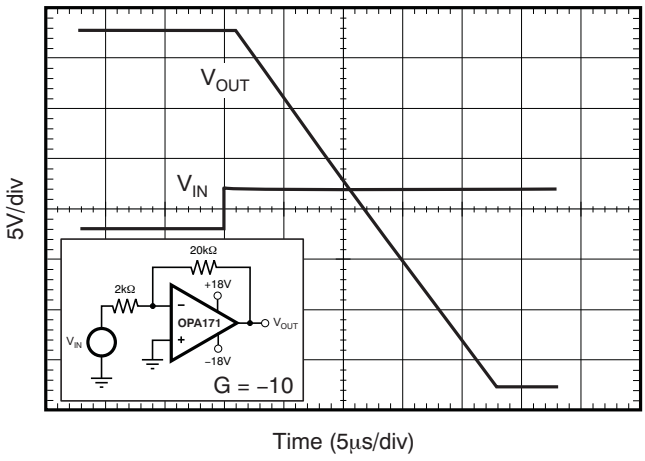


图 26. Positive Overload Recovery

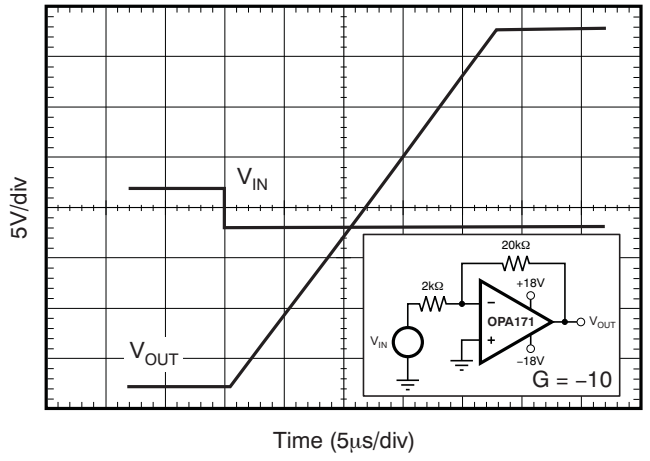


图 27. Negative Overload Recovery

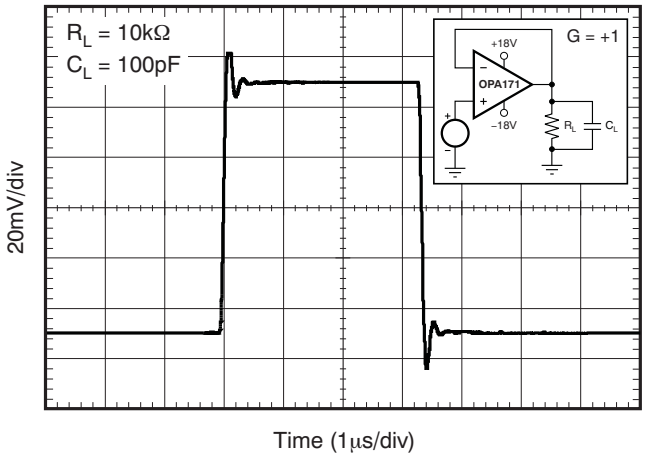


图 28. Small-Signal Step Response (100 mV)

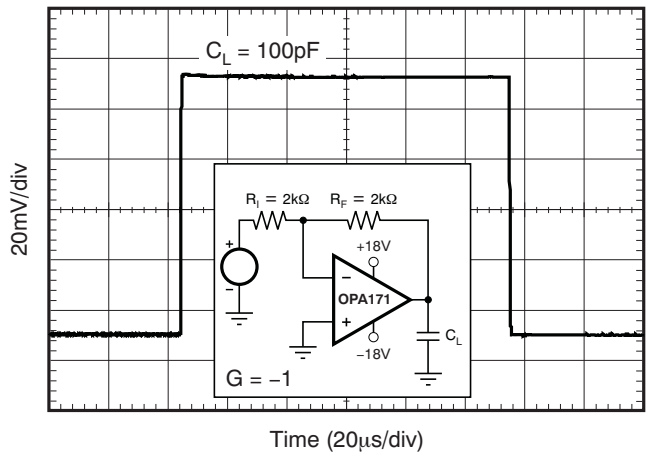


图 29. Small-Signal Step Response (100 mV)

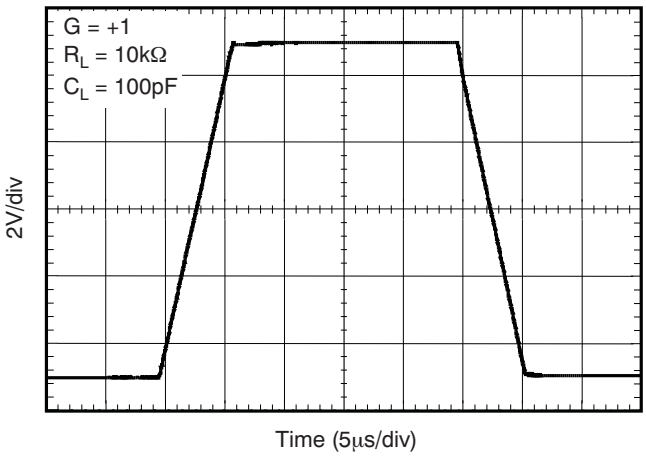


图 30. Large-Signal Step Response

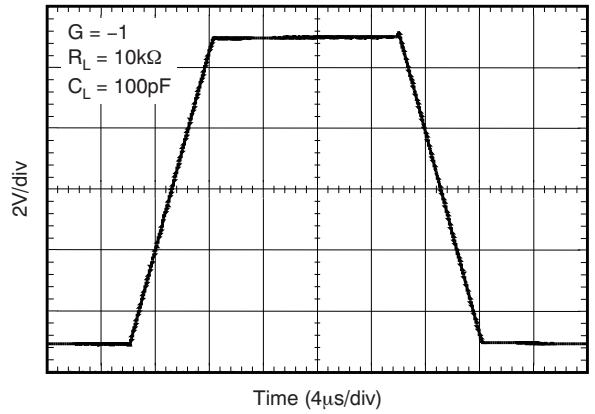


图 31. Large-Signal Step Response

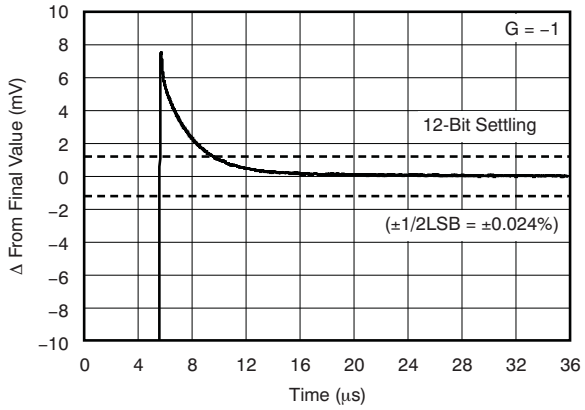


图 32. Large-Signal Settling Time (10-V Positive Step)

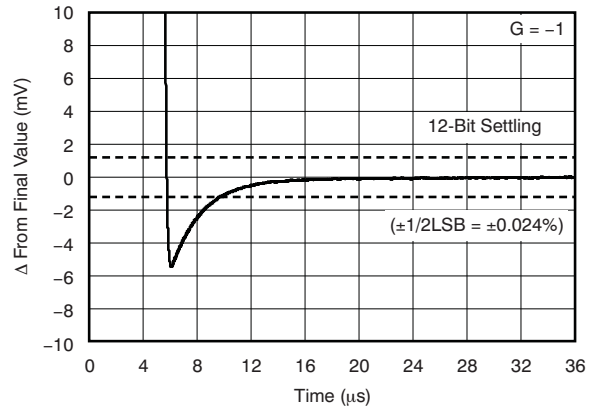


图 33. Large-Signal Settling Time (10-V Negative Step)

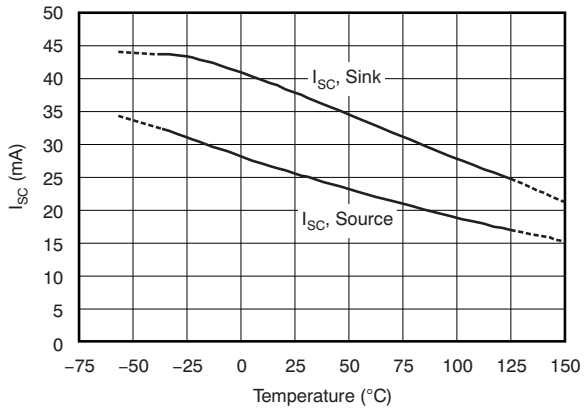


图 34. Short-Circuit Current vs Temperature

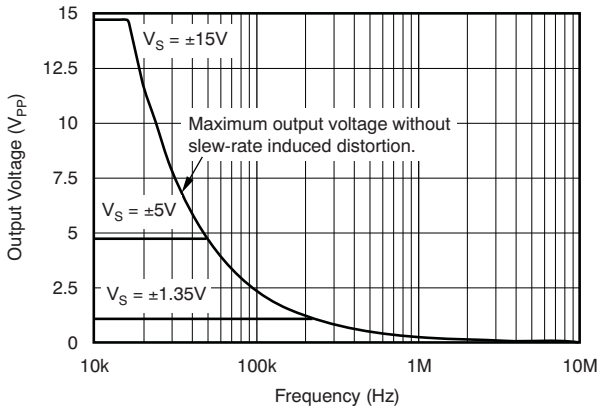


图 35. Maximum Output Voltage vs Frequency

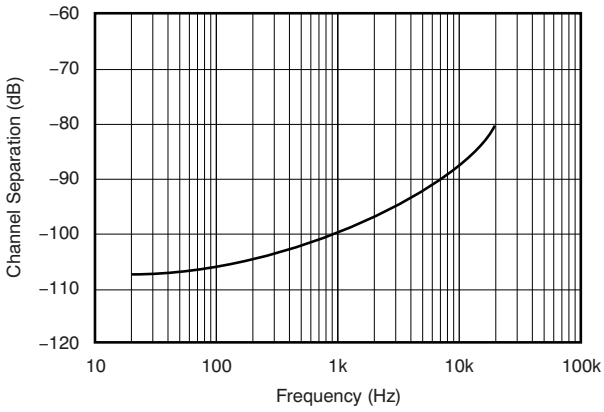


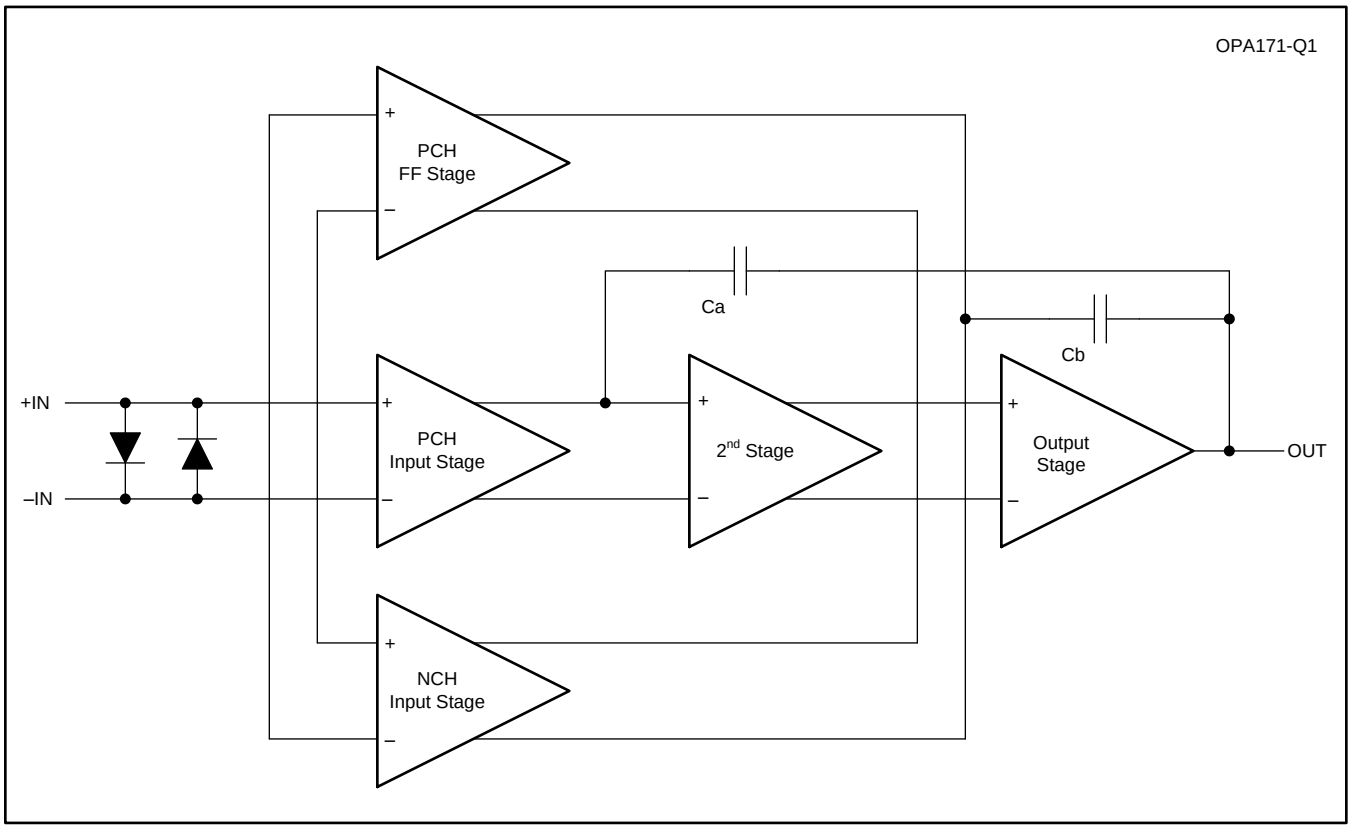
图 36. Channel Separation vs Frequency

8 Detailed Description

8.1 Overview

The OPAx171-Q1 family of operational amplifiers provide high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 1.5 μV/°C (maximum) provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, AOL, and superior THD.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Characteristics

The OPAx171-Q1 family of devices is specified for operation from 2.7 to 36 V (±1.35 to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are shown in the *Typical Characteristics* section.

8.3.2 Phase-Reversal Protection

The OPAx171-Q1 family of devices has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx171-Q1 family of devices prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. 图 37 shows this performance.

Feature Description (接下页)

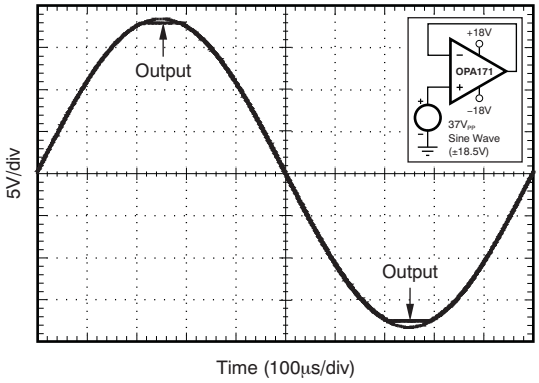


图 37. No Phase Reversal

8.3.3 Capacitive Load and Stability

The dynamic characteristics of the OPAx171-Q1 family of devices have been optimized for commonly encountered operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. 图 38 and 图 39 show small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, for details of analysis techniques and application circuits, refer to the *Applications Bulletin AB-028* (SBOA015), available for download from TI.com.

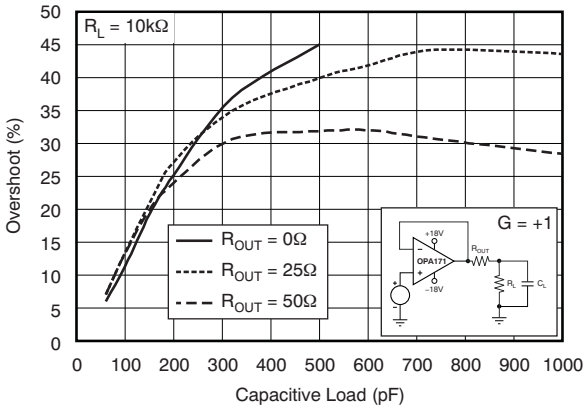


图 38. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

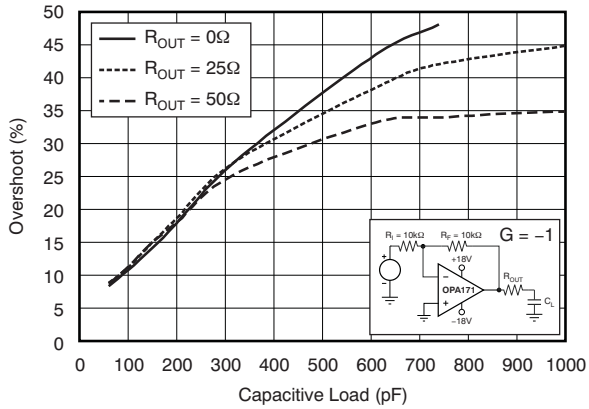


图 39. Small-Signal Overshoot versus Capacitive Load (100-mV Output Step)

8.4 Device Functional Modes

8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx171-Q1 family of devices extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in 表 2.

表 2. Typical Performance Range

PARAMETER	MIN	TYP	MAX	UNIT
Input common-mode voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		7		mV
Offset voltage vs temperature		12		µV/°C
Common-mode rejection		65		dB
Open-loop gain		60		dB
GBW		0.7		MHz
Slew rate		0.7		V/µs
Noise at f = 1kHz		30		nV/$\sqrt{\text{Hz}}$

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx171-Q1 operational amplifier provides high overall performance, making it ideal for many general-purpose applications. The excellent offset drift of only 2 µV/°C provides excellent stability over the entire temperature range. In addition, the device offers very-good overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

9.1.1 Electrical Overstress

Designers often ask questions about the capability of an op amp to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. 图 40 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

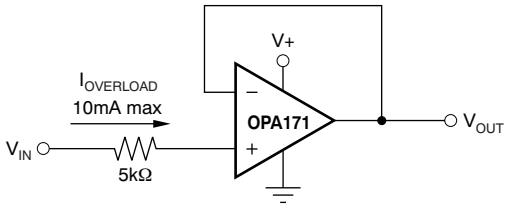


图 40. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If the ability of the supply to absorb this current is uncertain, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, the zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

9.2 Typical Application

9.2.1 Capacitive Load Drive Solution Using an Isolation Resistor

The OPA171-Q1 device can be used capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open loop gain of the system to ensure the circuit has sufficient phase margin.

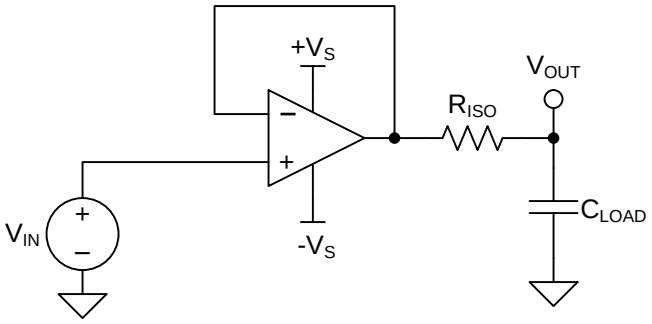


图 41. Unity-Gain Buffer with R_{ISO} Stability Compensation

9.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 µF, 0.1 µF, and 1 µF
- Phase margin: 45° and 60°

9.2.1.2 Detailed Design Procedure

图 42 shows a unity-gain buffer driving a capacitive load. 公式 1 shows the transfer function for the circuit in 图 42. Not shown in 图 42 is the open-loop output resistance of the op amp, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + \left(R_o + R_{ISO}\right) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in 公式 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB/decade. 图 42 shows the concept. The 1/β curve for a unity-gain buffer is 0 dB.

Typical Application (接下页)

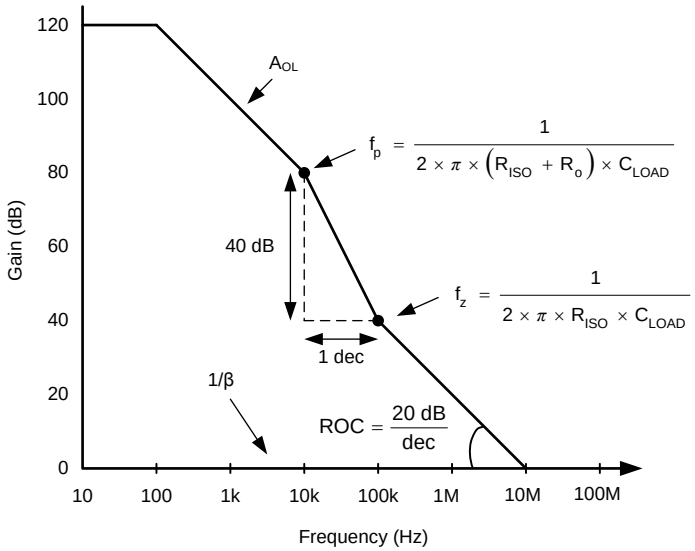


图 42. Unity-Gain Amplifier with R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and AC gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. 表 3 lists the overshoot percentage and AC gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA171, refer to the Precision Design, *Capacitive Load Drive Solution using an Isolation Resistor* (TIPD128).

表 3. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

9.2.1.3 Application Curve

The OPA171-Q1 device meets the supply voltage requirements of 30 V. The OPA171-Q1 device was tested for various capacitive loads and R_{ISO} was adjusted to achieve an overshoot corresponding to 表 3. 图 43 shows the test results.

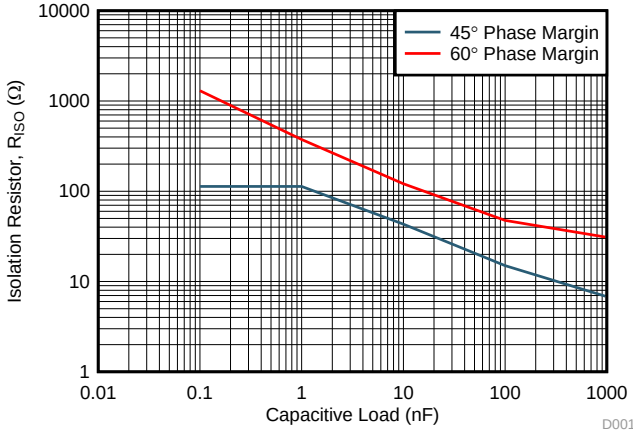


图 43. R_{ISO} vs C_{LOAD}

10 Power Supply Recommendations

The OPAx171-Q1 family of devices is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For detailed information on bypass capacitor placement, see the *Layout* section.

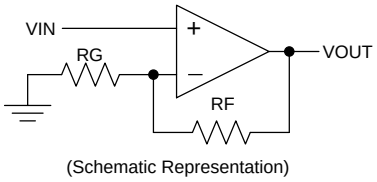
11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. See *Circuit Board Layout Techniques*, SLOA089, for detailed information.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 图 44, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example



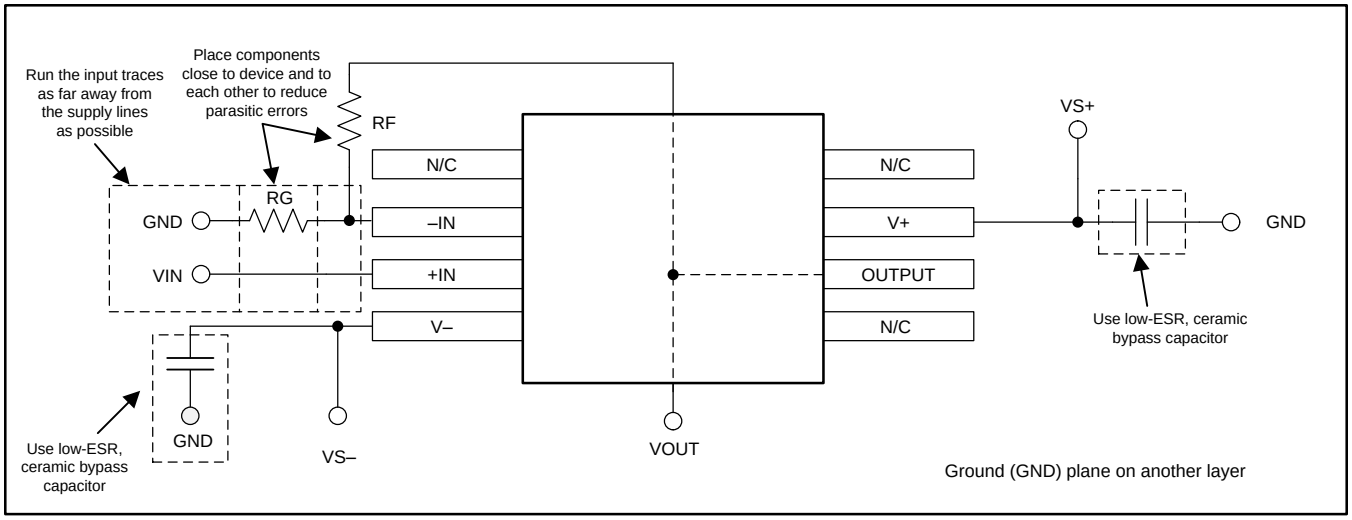


图 44. Operational Amplifier Board Layout for Noninverting Configuration

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- 《应用 公告 AB-028》，SBOA015
- 《采用隔离电阻的电容式负载驱动器解决方案》，TIDU032
- 《电路板布局布线技巧》，SLOA089

12.2 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 4. 相关链接

器件	产品文件夹	样片与购买	技术文章	工具与软件	支持与社区
OPA171-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA2171-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
OPA4171-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA171AQDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OULQ	Samples
OPA2171AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2171	Samples
OPA2171AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	2171AQ	Samples
OPA4171AQDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4171Q1	Samples
OPA4171AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	O4171Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

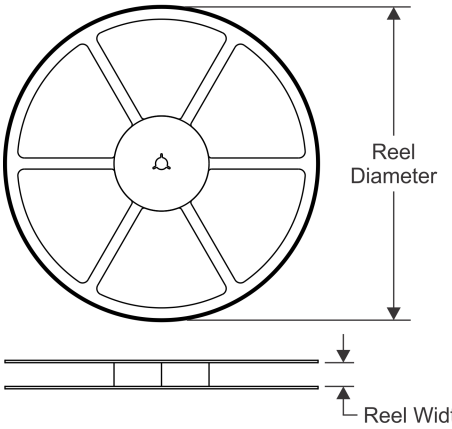
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

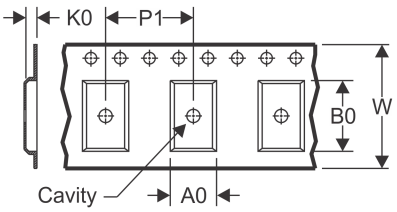
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

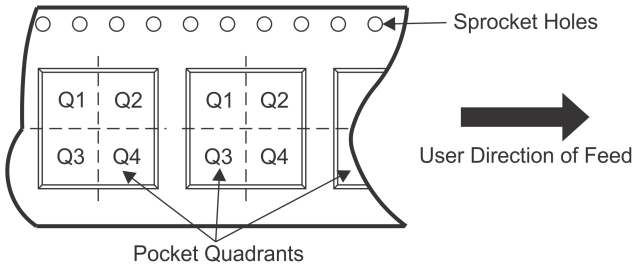


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

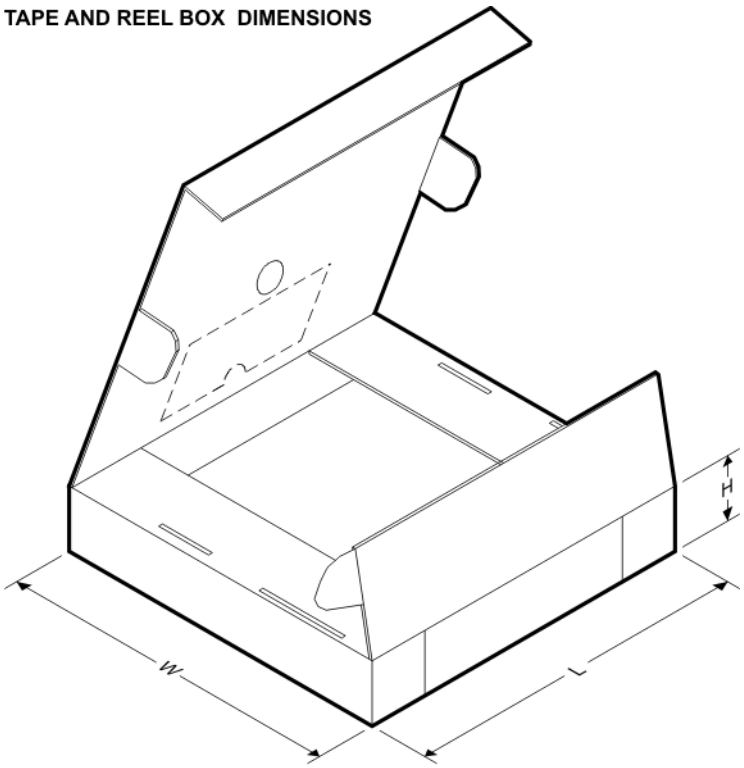
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA171AQDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA2171AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2171AQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4171AQDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4171AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

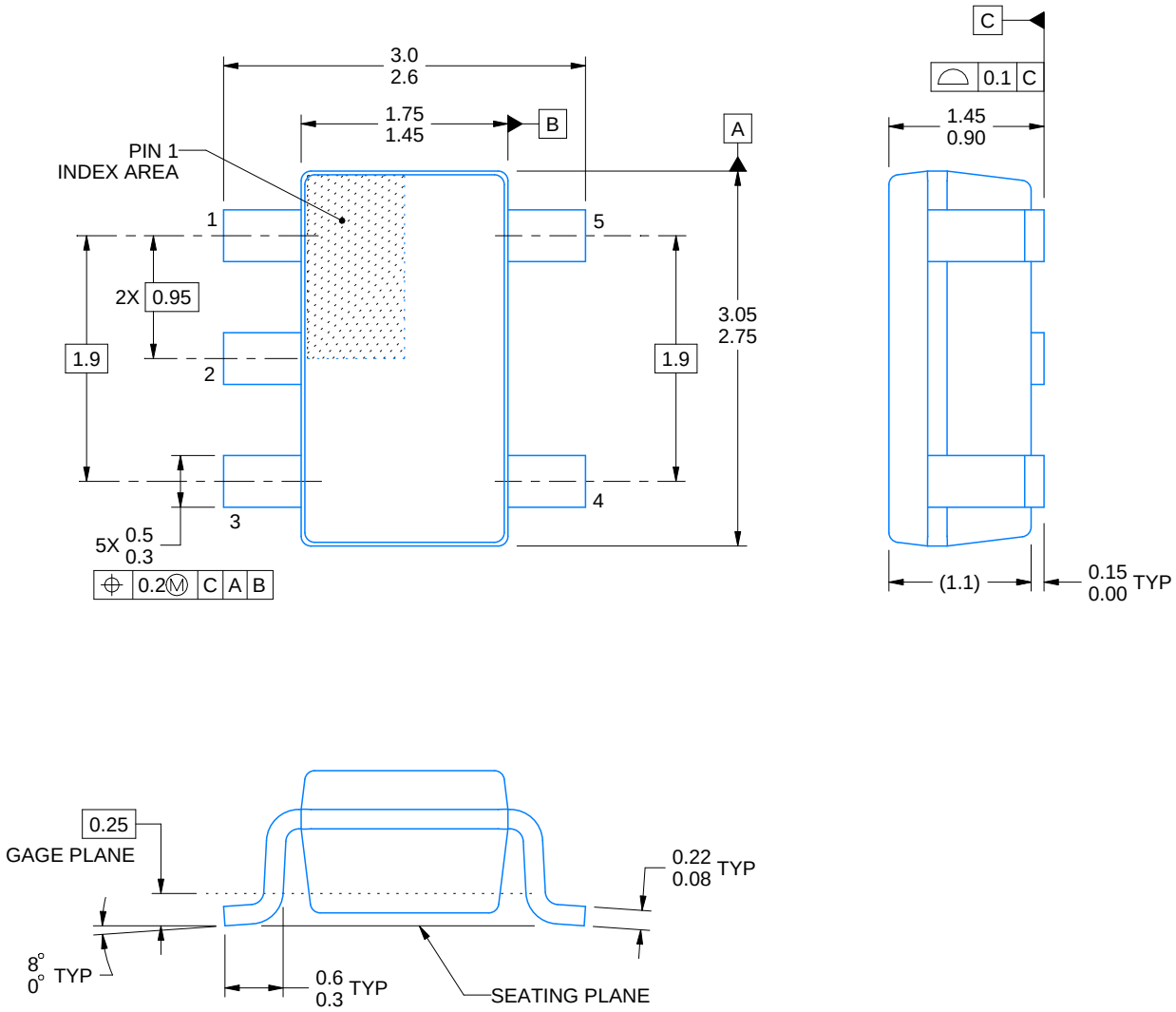
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA171AQDBVRQ1	SOT-23	DBV	5	3000	202.0	201.0	28.0
OPA2171AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2171AQDRQ1	SOIC	D	8	2500	367.0	367.0	35.0
OPA4171AQDRQ1	SOIC	D	14	2500	367.0	367.0	38.0
OPA4171AQPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

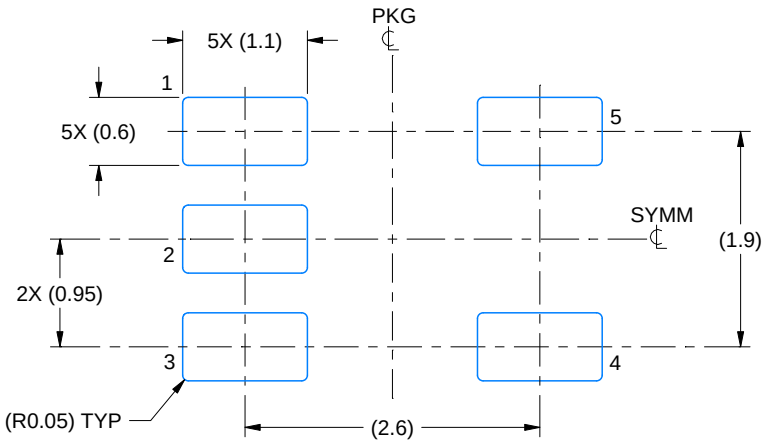
SMALL OUTLINE TRANSISTOR



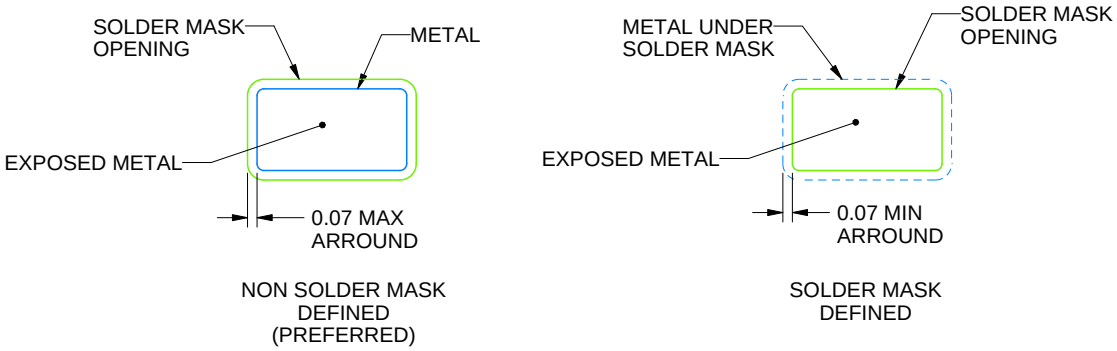
4214839/E 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

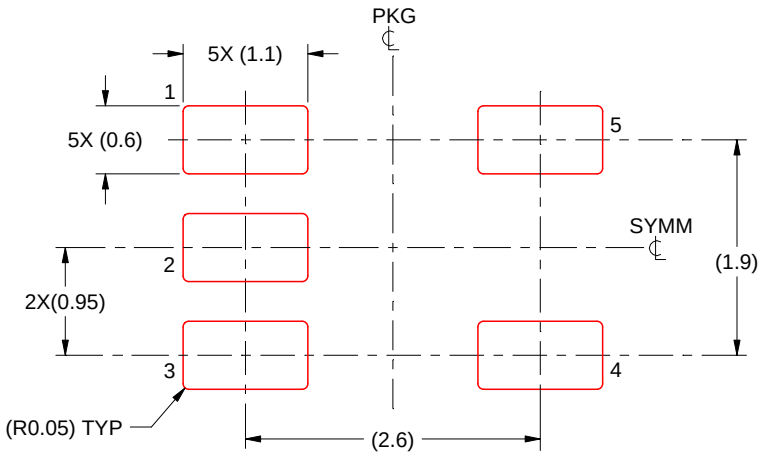


SOLDER MASK DETAILS

4214839/E 09/2019

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



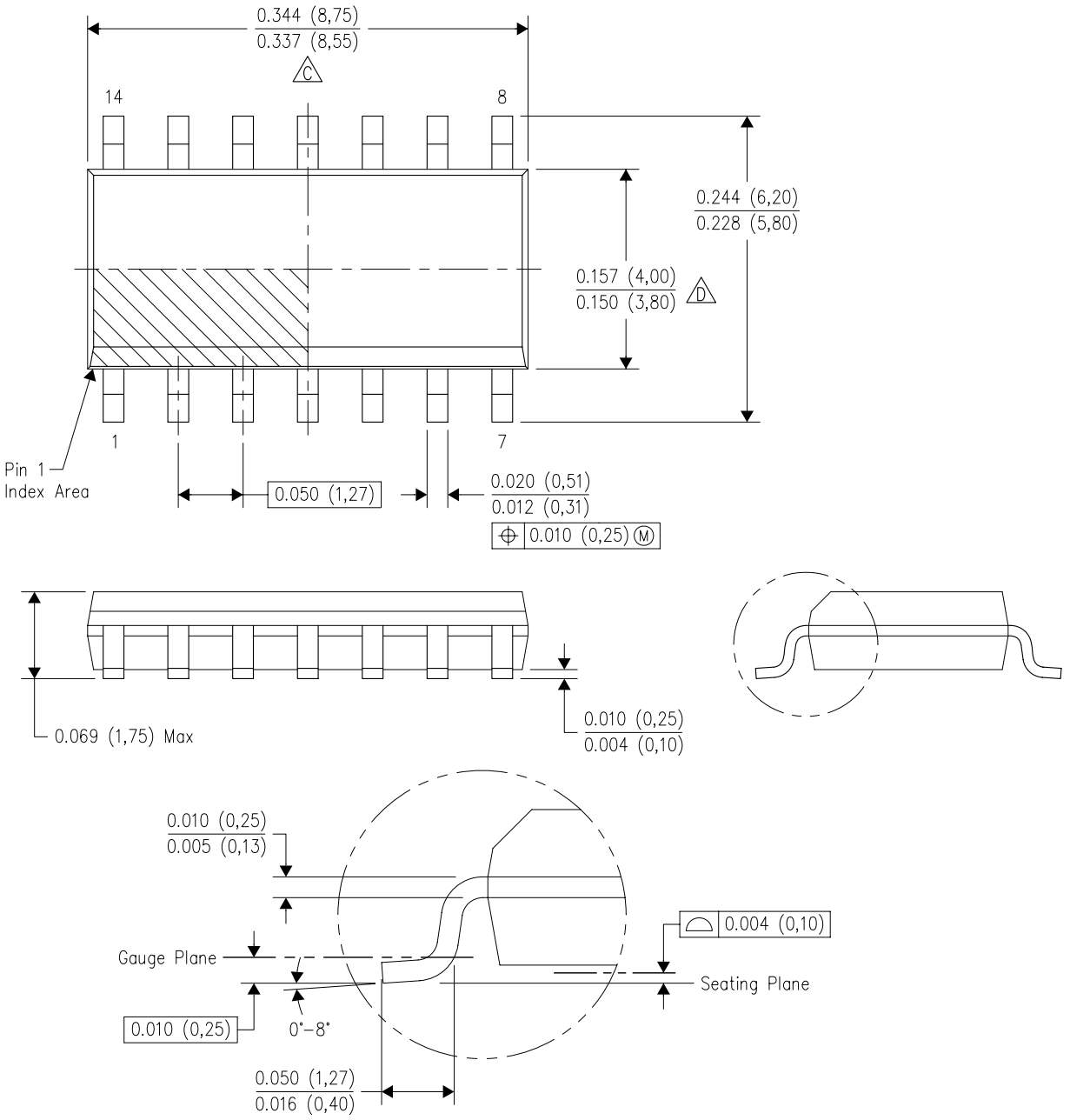
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/E 09/2019

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

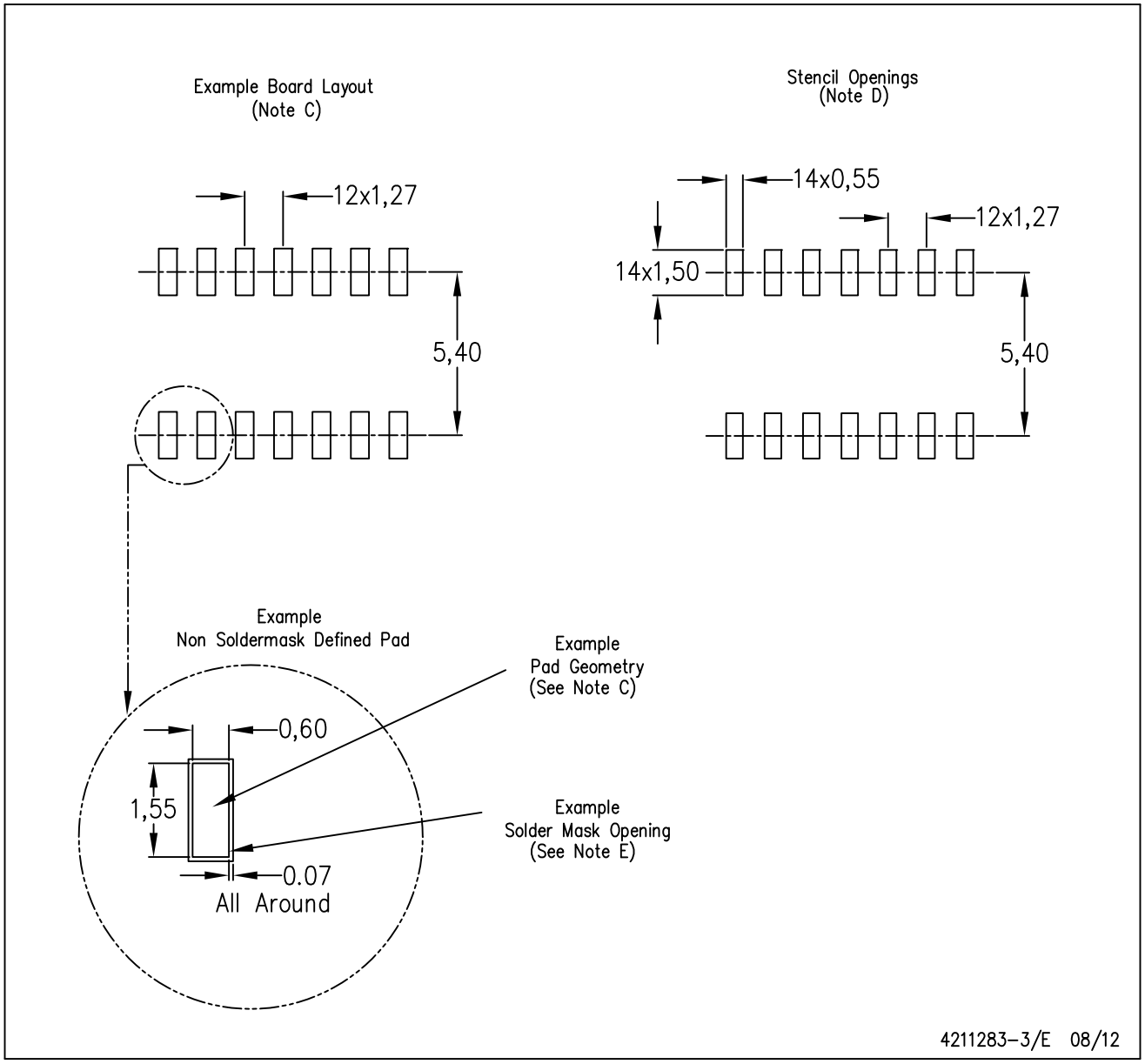
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

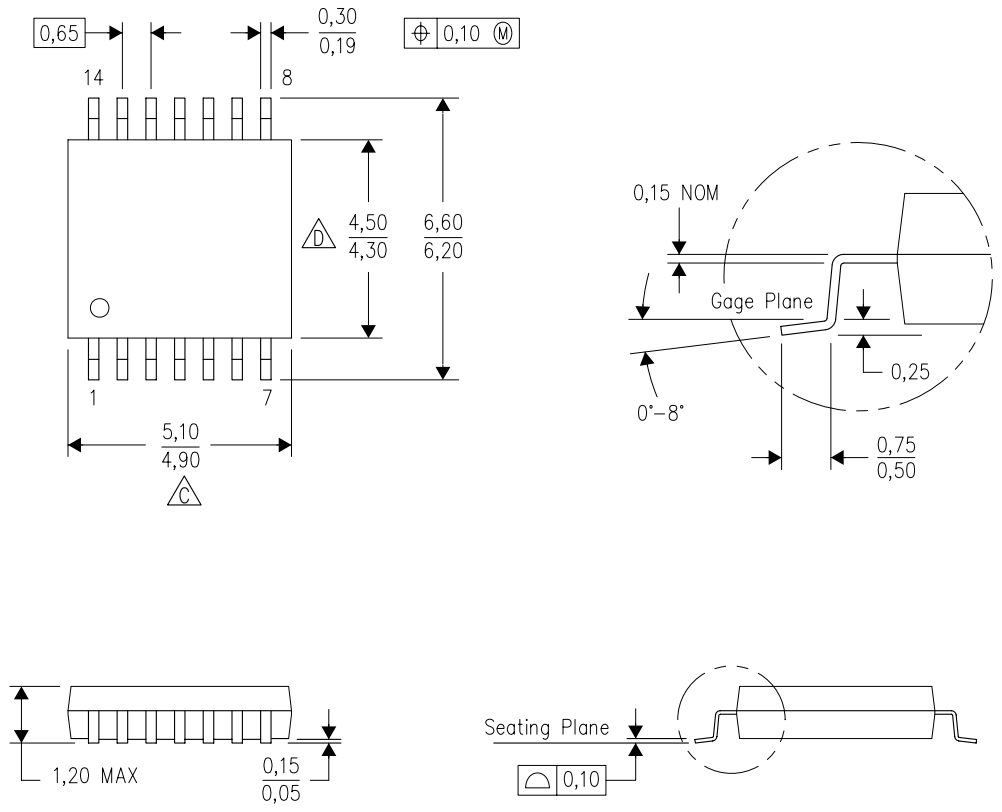
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

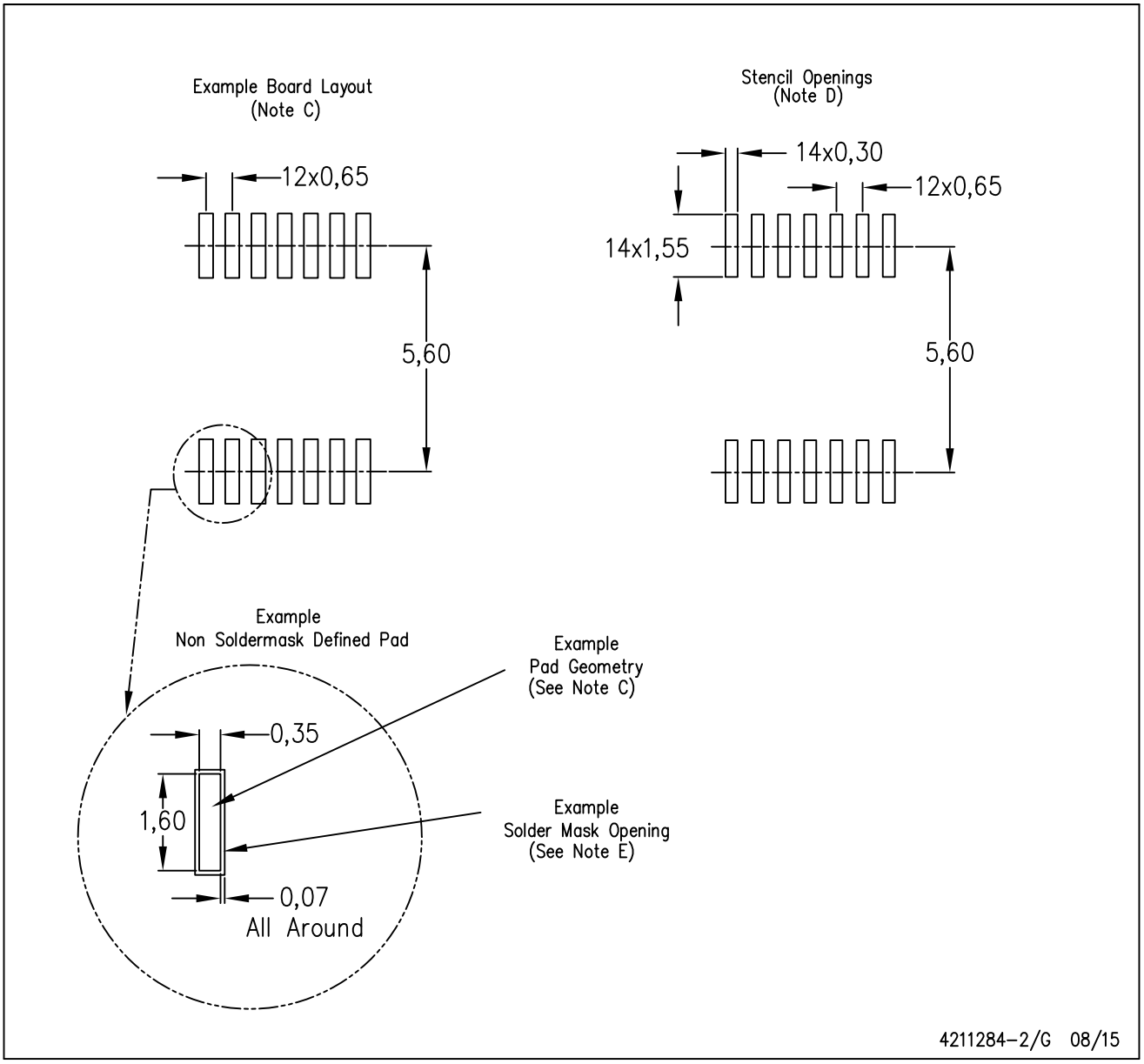
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



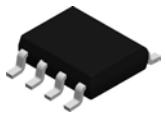
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

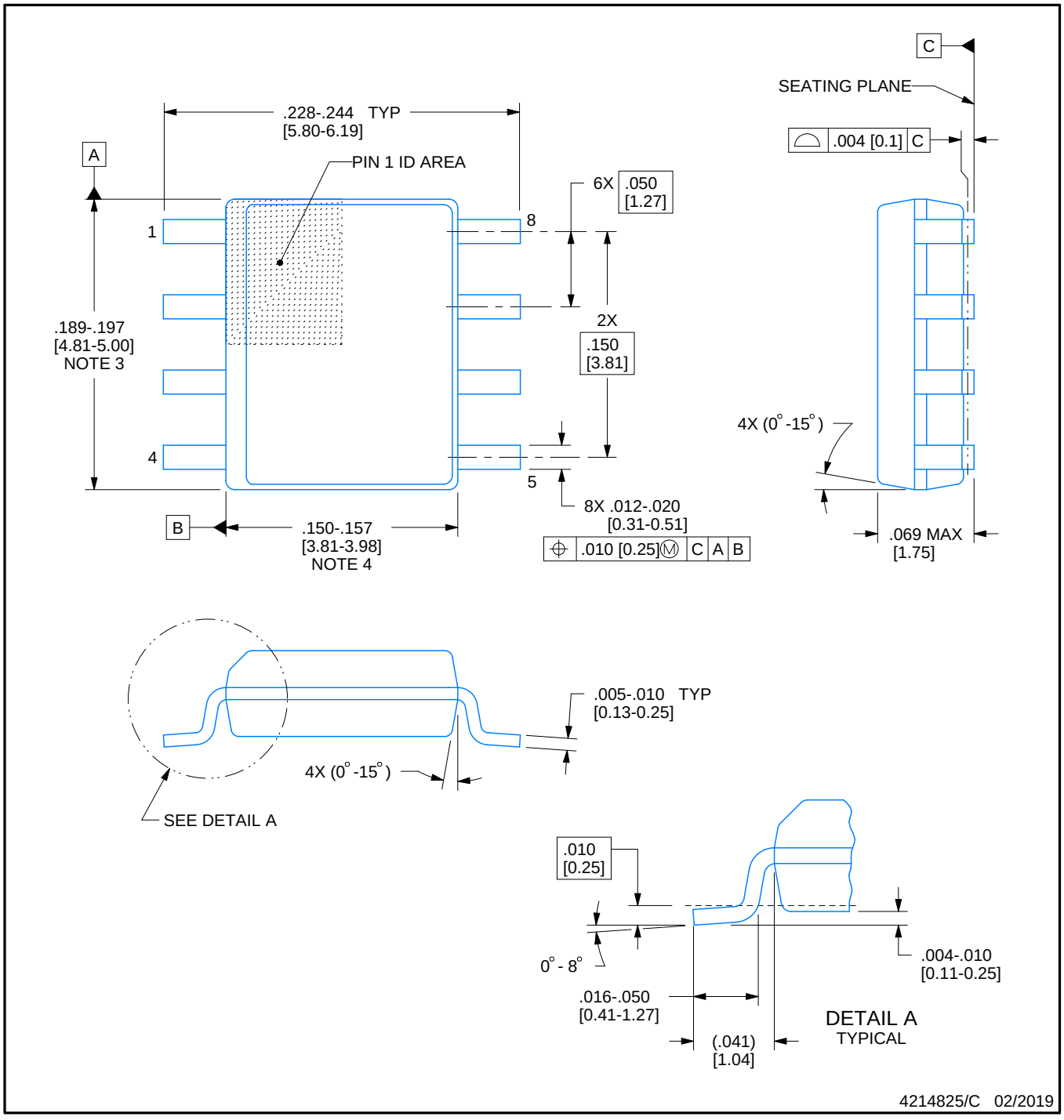


PACKAGE OUTLINE

D0008A

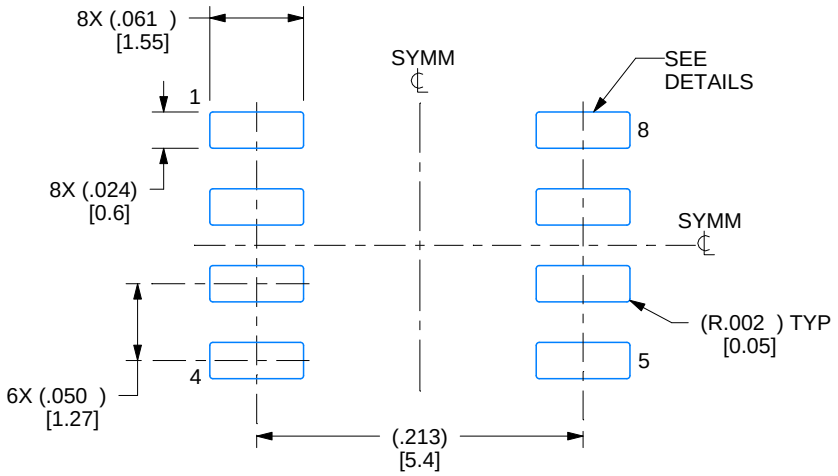
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

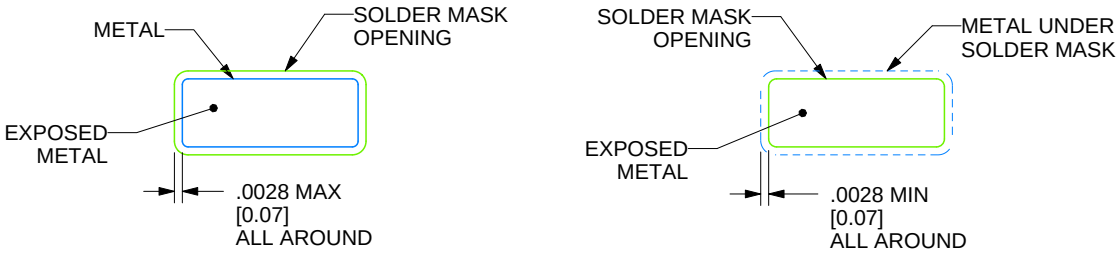


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

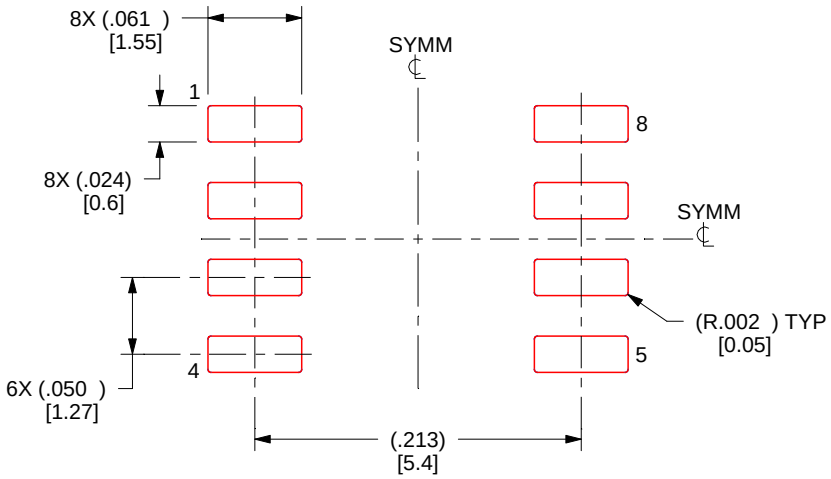
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



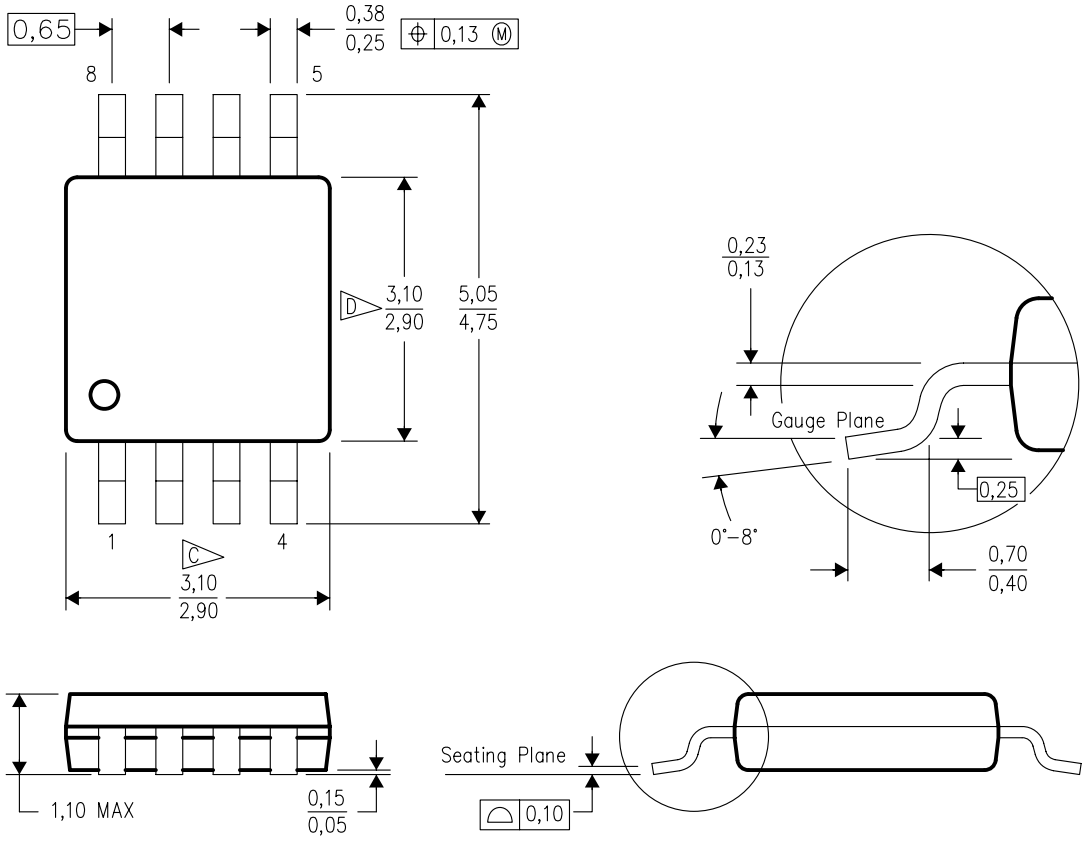
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

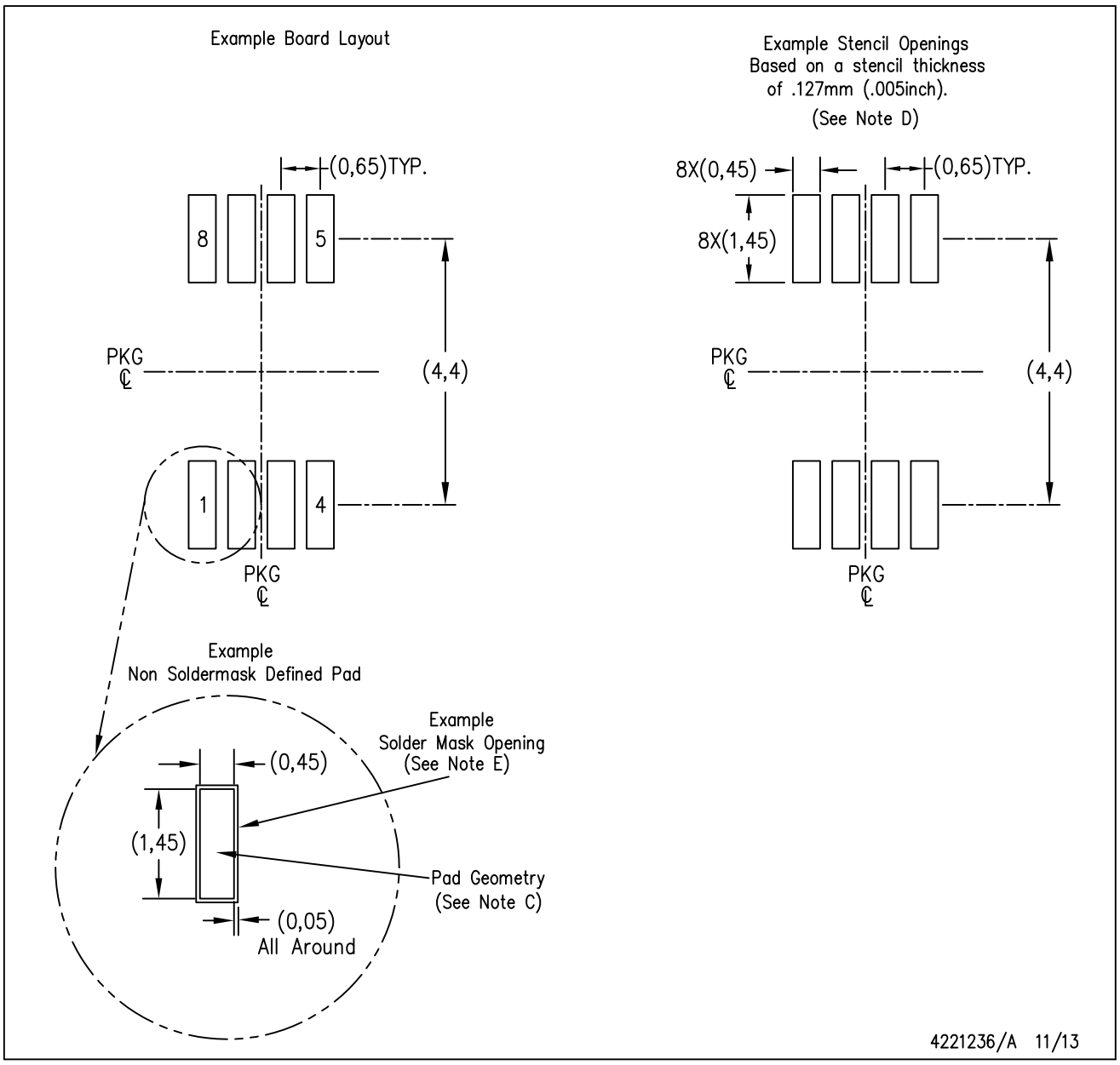
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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