CMOS, 330 MHz Triple 8-Bit High Speed Video DAC

Data Sheet **ADV7125**

FEATURES

- 330 MSPS throughput rate
- Triple 8-bit DACs
- RS-343A-/RS-170-compatible output
- Complementary outputs
- DAC output current range: 2.0 mA to 26.5 mA
- TTL-compatible inputs
- Internal reference (1.235 V)
- Single-supply +5 V/+3.3 V operation
- 48-lead LQFP and LFCSP
- Low power dissipation (30 mW minimum at 3 V)
- Low power standby mode (6 mW typical at 3 V)
- Industrial temperature range (−40°C to +85°C)
- RoHS compliant packages
- Qualified for automotive applications

APPLICATIONS

- Digital video systems
- High resolution color graphics
- Digital radio modulation
- Image processing
- Instrumentation
- Video signal reconstruction
- Automotive infotainment units

FUNCTIONAL BLOCK DIAGRAM

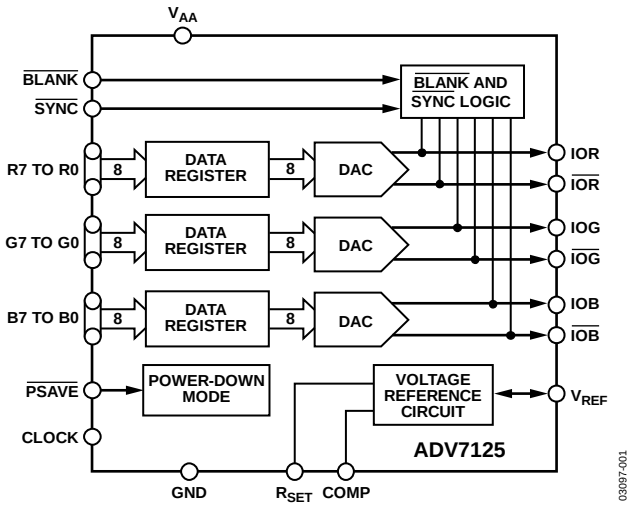

Figure 1.

GENERAL DESCRIPTION

The ADV7125 (ADV®) is a triple high speed, digital-to-analog converter (DAC) on a single monolithic chip. It consists of three high speed, 8-bit video DACs with complementary outputs, a standard TTL input interface, and a high impedance, analog output current source.

The ADV7125 has three separate 8-bit-wide input ports. A single +5 V/+3.3 V power supply and clock are all that are required to make the device functional. The ADV7125 has additional video control signals, composite $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$, as well as a power save mode.

The ADV7125 is fabricated in a 5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. The ADV7125 is available in 48-lead LQFP and 48-lead LFCSP packages.

PRODUCT HIGHLIGHTS

1. 330 MSPS (3.3 V only) throughput.
2. Guaranteed monotonic to eight bits.
3. Compatible with a wide variety of high resolution color graphics systems, including RS-343A and RS-170.

Rev. D

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SPECIFICATIONS

5 V ELECTRICAL CHARACTERISTICS

V_{AA} = 5 V ± 5%, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX},[1] unless otherwise noted, $T_{J\,MAX}$ = 110°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments[1]
STATIC PERFORMANCE					
Resolution (Each DAC)	8			Bits	
Integral Nonlinearity (BSL)	−1	±0.4	+1	LSB	
Differential Nonlinearity	−1	±0.25	+1	LSB	Guaranteed Monotonic
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Current, I_{IN}	−1		+1	μA	V_{IN} = 0.0 V or V_{DD}
$\overline{PSAVE}$ Pull-Up Current		20		μA	
Input Capacitance, C_{IN}		10		pF	
ANALOG OUTPUTS					
Output Current	2.0		26.5	mA	Green DAC, $\overline{SYNC}$ = high
	2.0		18.5	mA	RGB DAC, $\overline{SYNC}$ = low
DAC-to-DAC Matching		1.0	5	%	
Output Compliance Range, V_{OC}	0		1.4	V	
Output Impedance, R_{OUT}		100		kΩ	
Output Capacitance, C_{OUT}		10		pF	I_{OUT} = 0 mA
Offset Error	−0.025		+0.025	% FSR	Tested with DAC output = 0 V
Gain Error[2]	−5.0		+5.0	% FSR	FSR = 18.62 mA
VOLTAGE REFERENCE, EXTERNAL AND INTERNAL					
Reference Range, V_{REF}	1.12	1.235	1.35	V	
POWER DISSIPATION					
Digital Supply Current[3]		3.4	9	mA	f_{CLK} = 50 MHz
		10.5	15	mA	f_{CLK} = 140 MHz
		18	25	mA	f_{CLK} = 240 MHz
Analog Supply Current		67	72	mA	R_{SET} = 530 Ω
		8		mA	R_{SET} = 4933 Ω
Standby Supply Current[4]		2.1	5.0	mA	$\overline{PSAVE}$ = low, digital, and control inputs at V_{DD}
Power Supply Rejection Ratio		0.1	0.5	%/%	

[1] Temperature range T_{MIN} to T_{MAX}: −40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz and 330 MHz.
[2] Gain error = ((Measured (FSC)/Ideal (FSC) − 1) × 100), where Ideal = $V_{REF}/R_{SET} \times K \times (0xFFH) \times 4$ and K = 7.9896.
[3] Digital supply is measured with a continuous clock that has data input corresponding to a ramp pattern and with an input level at 0 V and V_{DD}.
[4] These maximum/minimum specifications are guaranteed by characterization in the 4.75 V to 5.25 V range.

3.3 V ELECTRICAL CHARACTERISTICS

V_{AA} = 3.0 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX},[1] unless otherwise noted, $T_{J\,MAX}$ = 110°C.

Table 2.

Parameter[2]	Min	Typ	Max	Unit	Test Conditions/Comments[1]
STATIC PERFORMANCE					
Resolution (Each DAC)			8	Bits	R_{SET} = 680 Ω
Integral Nonlinearity (BSL)	−1	±0.5	+1	LSB	R_{SET} = 680 Ω
Differential Nonlinearity	−1	±0.25	+1	LSB	R_{SET} = 680 Ω
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2.0			V	
Input Low Voltage, V_{IL}		0.8		V	
Input Current, I_{IN}	−1		+1	μA	V_{IN} = 0.0 V or V_{DD}
$\overline{PSAVE}$ Pull-Up Current		20		μA	
Input Capacitance, C_{IN}		10		pF	
ANALOG OUTPUTS					
Output Current	2.0		26.5	mA	Green DAC, $\overline{SYNC}$ = high
	2.0		18.5	mA	RGB DAC, $\overline{SYNC}$ = low
DAC-to-DAC Matching		1.0		%	
Output Compliance Range, V_{OC}	0		1.4	V	
Output Impedance, R_{OUT}		70		kΩ	
Output Capacitance, C_{OUT}		10		pF	
Offset Error		0	0	% FSR	Tested with DAC output = 0 V
Gain Error[3]		0		% FSR	FSR = 18.62 mA
VOLTAGE REFERENCE, EXTERNAL					
Reference Range, V_{REF}	1.12	1.235	1.35	V	
VOLTAGE REFERENCE, INTERNAL					
Voltage Reference, V_{REF}		1.235		V	
POWER DISSIPATION					
Digital Supply Current[4]		2.2	5.0	mA	f_{CLK} = 50 MHz
		6.5	12.0	mA	f_{CLK} = 140 MHz
		11	15	mA	f_{CLK} = 240 MHz
		16		mA	f_{CLK} = 330 MHz
Analog Supply Current		67	72	mA	R_{SET} = 560 Ω
		8		mA	R_{SET} = 4933 Ω
Standby Supply Current		2.1	5.0	mA	$\overline{PSAVE}$ = low, digital, and control inputs at V_{DD}
Power Supply Rejection Ratio		0.1	0.5	%/%	

[1] Temperature range T_{MIN} to T_{MAX}: −40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz and 330 MHz.
[2] These max/min specifications are guaranteed by characterization in the 3.0 V to 3.6 V range.
[3] Gain error = ((Measured (FSC)/Ideal (FSC) −1) × 100), where Ideal = $V_{REF}/R_{SET} \times K \times$ (0xFFH) × 4 and K = 7.9896.
[4] Digital supply is measured with continuous clock that has data input corresponding to a ramp pattern and with an input level at 0 V and V_{DD}.

5 V TIMING SPECIFICATIONS

V_{AA} = 5 V ± 5%,[1] V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX},[2] unless otherwise noted, $T_{J\,MAX}$ = 110°C.

Table 3.

Parameter[3]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG OUTPUTS						
Analog Output Delay	t_6		5.5		ns	
Analog Output Rise/Fall Time[4]	t_7		1.0		ns	
Analog Output Transition Time[5]	t_8		15		ns	
Analog Output Skew[6]	t_9		1	2	ns	
CLOCK CONTROL						
CLOCK Frequency[7]	f_{CLK}	0.5		50	MHz	50 MHz grade
		0.5		140	MHz	140 MHz grade
		0.5		240	MHz	240 MHz grade
Data and Control Setup[6]	t_1	0.5			ns	
Data and Control Hold[6]	t_2	1.5			ns	
CLOCK Period	t_3	4.17			ns	
CLOCK Pulse Width High[6]	t_4	1.875			ns	f_{CLK_MAX} = 240 MHz
CLOCK Pulse Width Low[6]	t_5	1.875			ns	f_{CLK_MAX} = 240 MHz
CLOCK Pulse Width High[6]	t_4	2.85			ns	f_{CLK_MAX} = 140 MHz
CLOCK Pulse Width Low[6]	t_5	2.85			ns	f_{CLK_MAX} = 140 MHz
CLOCK Pulse Width High	t_4	8.0			ns	f_{CLK_MAX} = 50 MHz
CLOCK Pulse Width Low	t_5	8.0			ns	f_{CLK_MAX} = 50 MHz
Pipeline Delay[6]	t_{PD}	1.0	1.0	1.0	Clock cycles	
$\overline{\text{PSAVE}}$ Up Time[6]	t_{10}		2	10	ns	

[1] The maximum and minimum specifications are guaranteed over this range.
[2] Temperature range T_{MIN} to T_{MAX}: −40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz.
[3] Timing specifications are measured with input levels of 3.0 V (V_{IH}) and 0 V (V_{IL}) for both 5 V and 3.3 V supplies.
[4] Rise time was measured from the 10% to 90% point of zero to full-scale transition, fall time from the 90% to 10% point of a full-scale transition.
[5] Measured from 50% point of full-scale transition to 2% of final value.
[6] Guaranteed by characterization.
[7] f_{CLK} maximum specification production tested at 125 MHz and 5 V. Limits specified here are guaranteed by characterization.

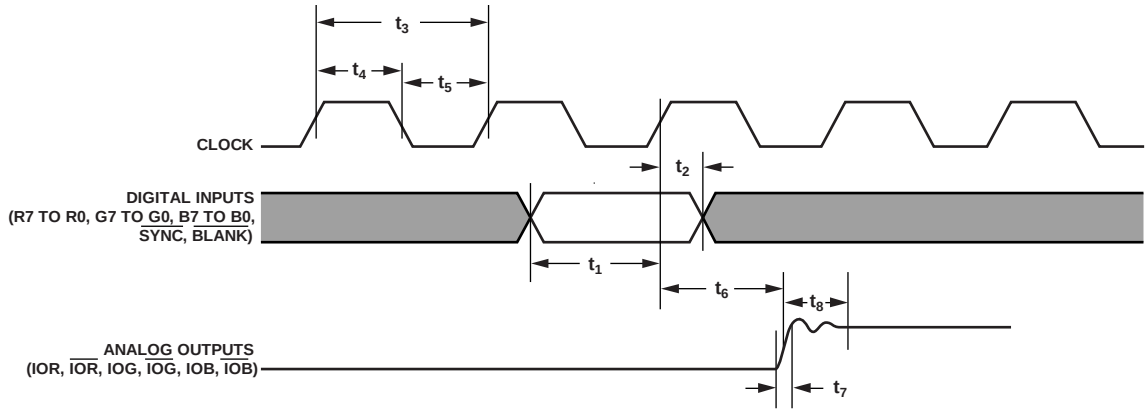
3.3 V TIMING SPECIFICATIONS

V_{AA} = 3.0 V to 3.6 V,[1] V_{REF} = 1.235 V, R_{SET} = 560 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX},[2] unless otherwise noted, $T_{J\,MAX}$ = 110°C.

Table 4.

Parameter[3]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG OUTPUTS						
Analog Output Delay,	t_6		7.5		ns	
Analog Output Rise/Fall Time[4]	t_7		1.0		ns	
Analog Output Transition Time[5]	t_8		15		ns	
Analog Output Skew[6]	t_9		1	2	ns	
CLOCK CONTROL						
CLOCK Frequency[7]	f_{CLK}			50	MHz	50 MHz grade
				140	MHz	140 MHz grade
				240	MHz	240 MHz grade
				330	MHz	330 MHz grade
Data and Control Setup[6]	t_1	0.2			ns	
Data and Control Hold[6]	t_2	1.5			ns	
CLOCK Period	t_3	3			ns	
CLOCK Pulse Width High[6]	t_4	1.4			ns	f_{CLK_MAX} = 330 MHz
CLOCK Pulse Width Low[6]	t_5	1.4			ns	f_{CLK_MAX} = 330 MHz
CLOCK Pulse Width High[6]	t_4	1.875			ns	f_{CLK_MAX} = 240 MHz
CLOCK Pulse Width Low[6]	t_5	1.875			ns	f_{CLK_MAX} = 240 MHz
CLOCK Pulse Width High[6]	t_4	2.85			ns	f_{CLK_MAX} = 140 MHz
CLOCK Pulse Width Low[6]	t_5	2.85			ns	f_{CLK_MAX} = 140 MHz
CLOCK Pulse Width High	t_4	8.0			ns	f_{CLK_MAX} = 50 MHz
CLOCK Pulse Width Low	t_5	8.0			ns	f_{CLK_MAX} = 50 MHz
Pipeline Delay[6]	t_{PD}	1.0	1.0	1.0	Clock cycles	
$\overline{\text{PSAVE}}$ Up Time[6]	t_{10}		4	10	ns	

[1] These maximum and minimum specifications are guaranteed over this range.
[2] Temperature range: T_{MIN} to T_{MAX}: −40°C to +85°C at 50 MHz and 140 MHz, 0°C to +70°C at 240 MHz and 330 MHz.
[3] Timing specifications are measured with input levels of 3.0 V (V_{IH}) and 0 V (V_{IL}) for 3.3 V supplies.
[4] Rise time was measured from the 10% to 90% point of zero to full-scale transition, fall time from the 90% to 10% point of a full-scale transition.
[5] Measured from 50% point of full-scale transition to 2% of final value.
[6] Guaranteed by characterization.
[7] f_{CLK} maximum specification production tested at 125 MHz and 5 V. Limits specified here are guaranteed by characterization.



NOTES
1. OUTPUT DELAY (t_6) MEASURED FROM THE 50% POINT OF THE RISING EDGE OF CLOCK TO THE 50% POINT OF FULL-SCALE TRANSITION.
2. OUTPUT RISE/FALL TIME (t_7) MEASURED BETWEEN THE 10% AND 90% POINTS OF FULL-SCALE TRANSITION.
3. TRANSITION TIME (t_8) MEASURED FROM THE 50% POINT OF FULL-SCALE TRANSITION TO WITHIN 2% OF THE FINAL OUTPUT VALUE.

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Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{AA} to GND	7 V
Voltage on Any Digital Pin	GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Junction Temperature (T_J)	150°C
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase Soldering (1 Minute)	220°C
I_{OUT} to GND[1]	0 V to V_{AA}

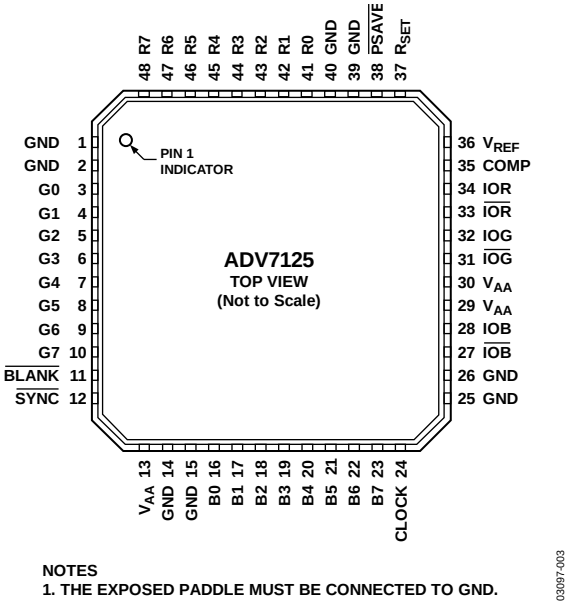
[1] Analog output short circuit to any power supply or common GND can be of an indefinite duration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

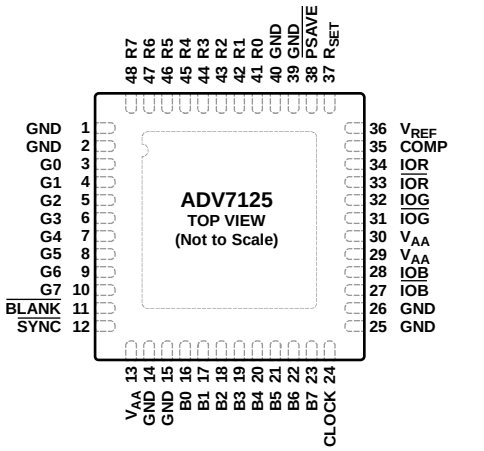
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PADDLE MUST BE CONNECTED TO GND.

Figure 3. LFCSP Pin Configuration (CP-48-1)



NOTES
1. THE EXPOSED PADDLE MUST BE CONNECTED TO GND.

Figure 4. LFCSP Pin Configuration (CP-48-4)

Table 6. LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 14, 15, 25, 26, 39, 40	GND	Ground. All GND pins must be connected.
3 to 10, 16 to 23, 41 to 48	G0 to G7, B0 to B7, R0 to R7	Red, Green, and Blue Pixel Data Inputs (TTL Compatible). Pixel data is latched on the rising edge of CLOCK. R0, G0, and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular printed circuit board (PCB) power or ground plane.
11	$\overline{\text{BLANK}}$	Composite Blank Control Input (TTL Compatible). A Logic 0 on this control input drives the analog outputs, IOR, IOB, and IOG, to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is a Logic 0, the R0 to R7, G0 to G7, and B0 to B7 pixel inputs are ignored.
12	$\overline{\text{SYNC}}$	Composite Sync Control Input (TTL Compatible). A Logic 0 on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source. This is internally connected to the IOG analog output. $\overline{\text{SYNC}}$ does not override any other control or data input; therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK. If sync information is not required on the green channel, the $\overline{\text{SYNC}}$ input should be tied to Logic 0.
13, 29, 30	V_{AA}	Analog Power Supply (5 V ± 5%). All V_{AA} pins on the ADV7125 must be connected.
24	CLOCK	Clock Input (TTL Compatible). The rising edge of CLOCK latches the R0 to R7, G0 to G7, B0 to B7, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
27, 31, 33	$\overline{\text{IOB}}$, $\overline{\text{IOG}}$, $\overline{\text{IOR}}$	Differential Blue, Green, and Red Current Outputs (High Impedance Current Sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into a doubly terminated 75 Ω load. If the complementary outputs are not required, these outputs should be tied to ground.
28, 32, 34	IOB, IOG, IOR	Blue, Green, and Red Current Outputs. These high impedance current sources are capable of directly driving a doubly terminated 75 Ω coaxial cable. All three current outputs should have similar output loads whether or not they are all being used.
35	COMP	Compensation Pin. This is a compensation pin for the internal reference amplifier. A 0.1 µF ceramic capacitor must be connected between COMP and V_{AA}.
36	V_{REF}	Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).

Pin No.	Mnemonic	Description
37	R_{SET}	A resistor (R_{SET}) connected between this pin and GND controls the magnitude of the full-scale video signal. Note that the IRE relationships are maintained, regardless of the full-scale output current. The relationship between R_{SET} and the full-scale output current on IOG (assuming I_{SYNC} is connected to IOG) is given by: R_{SET} (Ω) = 11,445 × V_{REF} (V)/*IOG* (mA) The relationship between R_{SET} and the full-scale output current on IOR, IOG, and IOB is given by: *IOG* (mA) = 11,444.8 × V_{REF} (V)/R_{SET} (Ω) ($\overline{\text{SYNC}}$ being asserted) *IOR*, *IOB* (mA) = 7989.6 × V_{REF} (V)/R_{SET} (Ω) The equation for IOG is the same as that for IOR and IOB when $\overline{\text{SYNC}}$ is not being used, that is, $\overline{\text{SYNC}}$ tied permanently low.
38	$\overline{\text{PSAVE}}$	Power Save Control Pin. Reduced power consumption is available on the ADV7125 when this pin is active.
0	EPAD	Exposed Paddle. The exposed paddle must be connected to GND.

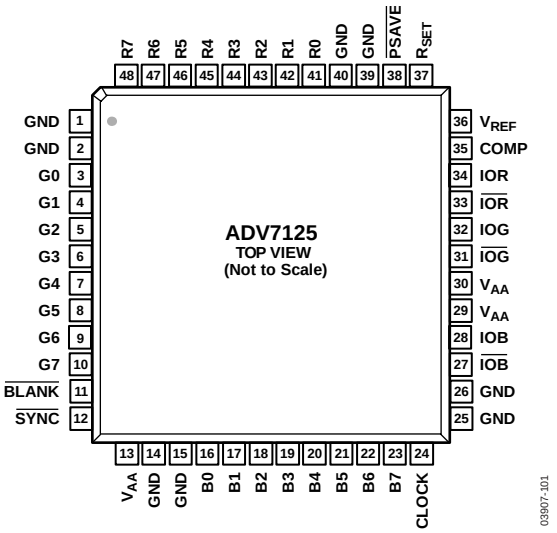


Figure 5. LQFP Pin Configuration

Table 7. LQFP Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 14, 15, 25, 26, 39, 40	GND	Ground. All GND pins must be connected.
3 to 10, 16 to 23, 41 to 48	G0 to G7, B0 to B7, R0 to R7	Red, Green, and Blue Pixel Data Inputs (TTL Compatible). Pixel data is latched on the rising edge of CLOCK. R0, G0, and B0 are the least significant data bits. Unused pixel data inputs should be connected to either the regular printed circuit board (PCB) power or ground plane.
11	$\overline{\text{BLANK}}$	Composite Blank Control Input (TTL Compatible). A Logic 0 on this control input drives the analog outputs, IOR, IOB, and IOG, to the blanking level. The $\overline{\text{BLANK}}$ signal is latched on the rising edge of CLOCK. While $\overline{\text{BLANK}}$ is a Logic 0, the R0 to R7, G0 to G7, and B0 to B7 pixel inputs are ignored.
12	$\overline{\text{SYNC}}$	Composite Sync Control Input (TTL Compatible). A Logic 0 on the $\overline{\text{SYNC}}$ input switches off a 40 IRE current source. This is internally connected to the IOG analog output. $\overline{\text{SYNC}}$ does not override any other control or data input; therefore, it should only be asserted during the blanking interval. $\overline{\text{SYNC}}$ is latched on the rising edge of CLOCK. If sync information is not required on the green channel, the $\overline{\text{SYNC}}$ input should be tied to Logic 0.
13, 29, 30	V_{AA}	Analog Power Supply (5 V ± 5%). All V_{AA} pins on the ADV7125 must be connected.
24	CLOCK	Clock Input (TTL Compatible). The rising edge of CLOCK latches the R0 to R7, G0 to G7, B0 to B7, $\overline{\text{SYNC}}$, and $\overline{\text{BLANK}}$ pixel and control inputs. It is typically the pixel clock rate of the video system. CLOCK should be driven by a dedicated TTL buffer.
27, 31, 33	$\overline{\text{IOB}}$, $\overline{\text{IOG}}$, $\overline{\text{IOR}}$	Differential Blue, Green, and Red Current Outputs (High Impedance Current Sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into a doubly terminated 75 Ω load. If the complementary outputs are not required, these outputs should be tied to ground.
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38	$\overline{\text{PSAVE}}$	Power Save Control Pin. Reduced power consumption is available on the ADV7125 when this pin is active.

TERMINOLOGY

Blanking Level
The level separating the $\overline{\text{SYNC}}$ portion from the video portion of the waveform. Usually referred to as the front porch or back porch. At 0 IRE units, it is the level that shuts off the picture tube, resulting in the blackest possible picture.

Color Video (RGB)
This refers to the technique of combining the three primary colors of red, green, and blue to produce color pictures within the usual spectrum. In RGB monitors, three DACs are required, one for each color.

Sync Signal ($\overline{\text{SYNC}}$)
The position of the composite video signal that synchronizes the scanning process.

Gray Scale
The discrete levels of video signal between reference black and reference white levels. An 8-bit DAC contains 256 different levels.

Raster Scan
The most basic method of sweeping a CRT one line at a time to generate and display images.

Reference Black Level
The maximum negative polarity amplitude of the video signal.

Reference White Level
The maximum positive polarity amplitude of the video signal.

Sync Level
The peak level of the $\overline{\text{SYNC}}$ signal.

Video Signal
The portion of the composite video signal that varies in gray scale levels between reference white and reference black. Also referred to as the picture signal, this is the portion that can be visually observed.

CIRCUIT DESCRIPTION AND OPERATION

The ADV7125 contains three 8-bit DACs, with three input channels, each containing an 8-bit register. Also integrated on board the device is a reference amplifier. The CRT control functions, $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$, are integrated on board the ADV7125.

DIGITAL INPUTS

There are 24 bits of pixel data (color information), R0 to R7, G0 to G7, and B0 to B7, latched into the device on the rising edge of each clock cycle. This data is presented to the three 8-bit DACs and then converted to three analog (RGB) output waveforms (see Figure 6).

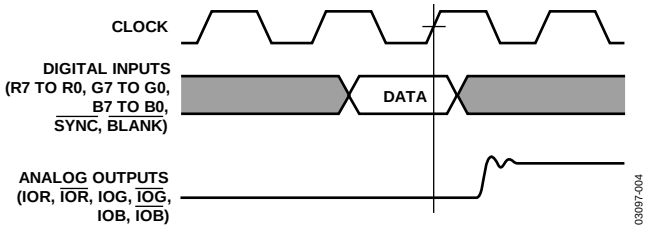


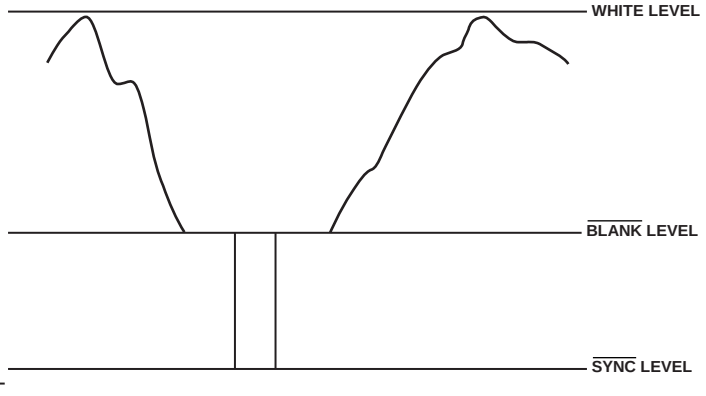
Figure 6. Video Data Input/Output

The ADV7125 has two additional control signals that are latched to the analog video outputs in a similar fashion. $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ are each latched on the rising edge of CLOCK to maintain synchronization with the pixel data stream.

The $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ functions allow for the encoding of these video synchronization signals onto the RGB video output. This is done by adding appropriately weighted current sources to the analog outputs, as determined by the logic levels on the $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ digital inputs.

Figure 7 shows the analog output, RGB video waveform of the ADV7125. The influence of $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ on the analog video waveform is illustrated.

RED AND BLUE		GREEN	
mA	V	mA	V
18.67	0.7	26.0	0.975
0	0	7.2	0.271
		0	0



NOTES
1. OUTPUTS CONNECTED TO A DOUBLY TERMINATED 75Ω LOAD.
2. V_{REF} = 1.235V, R_{SET} = 530Ω.
3. RS-343 LEVELS AND TOLERANCES ASSUMED ON ALL LEVELS.

03097-005

Figure 7. Typical RGB Video Output Waveform

Table 8 details the resultant effect on the analog outputs of $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$.

All these digital inputs are specified to accept TTL logic levels.

CLOCK INPUT

The CLOCK input of the ADV7125 is typically the pixel clock rate of the system. It is also known as the dot rate. The dot rate, and thus the required CLOCK frequency, is determined by the on-screen resolution, according to the following equation:

$$Dot\ Rate = (Horiz\ Res) \times (Vert\ Res) \times (Refresh\ Rate)/(Retrace\ Factor)$$

where:

Horiz Res is the number of pixels per line.
Vert Res is the number of lines per frame.
Refresh Rate is the horizontal scan rate. This is the rate at which the screen must be refreshed, typically 60 Hz for a noninterlaced system, or 30 Hz for an interlaced system.
Retrace Factor is the total blank time factor. This takes into account that the display is blanked for a certain fraction of the total duration of each frame (for example, 0.8).

Therefore, for a graphics system with a 1024 × 1024 resolution, a noninterlaced 60 Hz refresh rate, and a retrace factor of 0.8,

$$Dot\ Rate = 1024 \times 1024 \times 60/0.8 = 78.6\ MHz$$

The required CLOCK frequency is thus 78.6 MHz. All video data and control inputs are latched into the ADV7125 on the rising edge of CLOCK, as previously described in the Digital Inputs section. It is recommended that the CLOCK input to the ADV7125 be driven by a TTL buffer (for example, the 74F244).

Table 8. Typical Video Output Truth Table (R_{SET} = 530 Ω, R_{LOAD} = 37.5 Ω)

Video Output Level	IOG (mA)	$\overline{IOG}$ (mA)	IOR/IOB (mA)	$\overline{IOR}/\overline{IOB}$ (mA)	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
White Level	26.0	0	18.67	0	1	1	0xFFH
Video	Video + 7.2	18.67 – Video	Video	18.67 – Video	1	1	Data
Video to $\overline{BLANK}$	Video	18.67 – Video	Video	18.67 – Video	0	1	Data
Black Level	7.2	18.67	0	18.67	1	1	0x00H
Black to $\overline{BLANK}$	0	18.67	0	18.67	0	1	0x00H
$\overline{BLANK}$ Level	7.2	18.67	0	18.67	1	0	0xXXH (don't care)
$\overline{SYNC}$ Level	0	18.67	0	18.67	0	0	0xXXH (don't care)

VIDEO SYNCHRONIZATION AND CONTROL

The ADV7125 has a single composite sync ($\overline{SYNC}$) input control. Many graphics processors and CRT controllers have the ability to generate horizontal sync (HSYNC), vertical sync (VSYNC), and composite $\overline{SYNC}$.

In a graphics system that does not automatically generate a composite $\overline{SYNC}$ signal, the inclusion of some additional logic circuitry enables the generation of a composite $\overline{SYNC}$ signal.

The sync current is internally connected directly to the IOG output, thus encoding video synchronization information onto the green video channel. If it is not required to encode sync information onto the ADV7125, the $\overline{SYNC}$ input should be tied to logic low.

REFERENCE INPUT

The ADV7125 contains an on-board voltage reference. The V_{REF} pin should be connected as shown in Figure 12.

A resistance, R_{SET}, connected between the R_{SET} pin and GND, determines the amplitude of the output video level according to Equation 1 and Equation 2 for the ADV7125.

$$IOG\ (\text{mA}) = 11{,}444.8 \times V_{REF}\ (V)/R_{SET}\ (\Omega) \quad (1)$$

$$IOR,\ IOB\ (\text{mA}) = 7989.6 \times V_{REF}\ (\text{V})/R_{SET}\ (\Omega) \quad (2)$$

Equation 1 applies to the ADV7125 only, when $\overline{SYNC}$ is being used. If $\overline{SYNC}$ is not being encoded onto the green channel, Equation 1 is similar to Equation 2.

Using a variable value of R_{SET} allows for accurate adjustment of the analog output video levels. Use of a fixed 560 Ω R_{SET} resistor yields the analog output levels quoted in the Specifications section. These values typically correspond to the RS-343A video waveform values, as shown in Figure 7.

DACs

The ADV7125 contains three matched 8-bit DACs. The DACs are designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either the analog output (bit = 1) or GND (bit = 0) by a sophisticated decoding scheme. Because all this circuitry is on one monolithic device, matching between the three DACs is optimized. As well as matching, the use of identical current sources in a monolithic design guarantees monotonicity and low glitch. The on-board operational amplifier stabilizes the full-scale output current against temperature and power supply variations.

ANALOG OUTPUTS

The ADV7125 has three analog outputs, corresponding to the red, green, and blue video signals.

The red, green, and blue analog outputs of the ADV7125 are high impedance current sources. Each one of these three RGB current outputs is capable of directly driving a 37.5 Ω load, such as a doubly terminated 75 Ω coaxial cable. Figure 8 shows the required configuration for each of the three RGB outputs connected into a doubly terminated 75 Ω load. This arrangement develops RS-343A video output voltage levels across a 75 Ω monitor.

A suggested method of driving RS-170 video levels into a 75 Ω monitor is shown in Figure 9. The output current levels of the DACs remain unchanged, but the source termination resistance, Z_S, on each of the three DACs is increased from 75 Ω to 150 Ω.

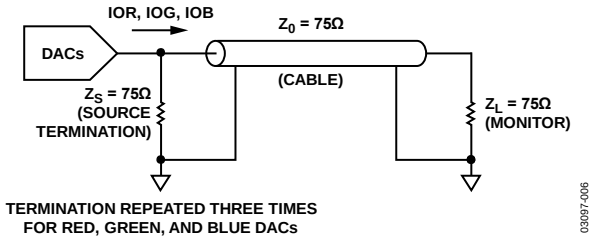


Figure 8. Analog Output Termination for RS-343A

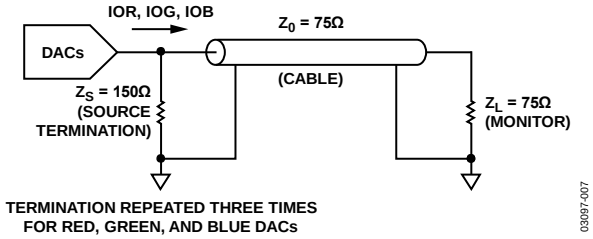


Figure 9. Analog Output Termination for RS-170

More detailed information regarding load terminations for various output configurations, including RS-343A and RS-170, is available in the AN-205 Application Note, *Video Formats and Required Load Terminations*.

Figure 7 shows the video waveforms associated with the three RGB outputs driving the doubly terminated 75 Ω load of Figure 8. As well as the gray scale levels (black level to white

level), Figure 7 also shows the contributions of $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ for the ADV7125. These control inputs add appropriately weighted currents to the analog outputs, producing the specific output level requirements for video applications. Table 8 details how the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs modify the output levels.

GRAY SCALE OPERATION

The ADV7125 can be used for standalone, gray scale (monochrome) or composite video applications (that is, only one channel used for video information). Any one of the three channels, red, green, or blue, can be used to input the digital video data. The two unused video data channels should be tied to Logic 0. The unused analog outputs should be terminated with the same load as that for the used channel, that is, if the red channel is used and IOR is terminated with a doubly terminated 75 Ω load (37.5 Ω), IOB and IOG should be terminated with 37.5 Ω resistors (see Figure 10).

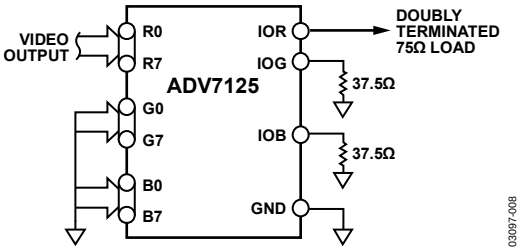


Figure 10. Input and Output Connections for Standalone Gray Scale or Composite Video

VIDEO OUTPUT BUFFERS

The ADV7125 is specified to drive transmission line loads. The analog output configuration to drive such loads is described in the Analog Outputs section and illustrated in Figure 11. However, in some applications, it may be required to drive long transmission line cable lengths. Cable lengths greater than 10 meters can attenuate and distort high frequency analog output pulses. The inclusion of output buffers compensates for some cable distortion. Buffers with large full power bandwidths and gains between two and four are required. These buffers also need to be able to supply sufficient current over the complete output voltage swing. Analog Devices produces a range of suitable op amps for such applications. These include the AD843, AD844, AD847, and AD848 series of monolithic op amps. In very high frequency applications (80 MHz), the AD8061 is recommended. More information on line driver buffering circuits is given in the relevant op amp data sheets.

Use of buffer amplifiers also allows implementation of other video standards besides RS-343A and RS-170. Altering the gain components of the buffer circuit results in any desired video level.

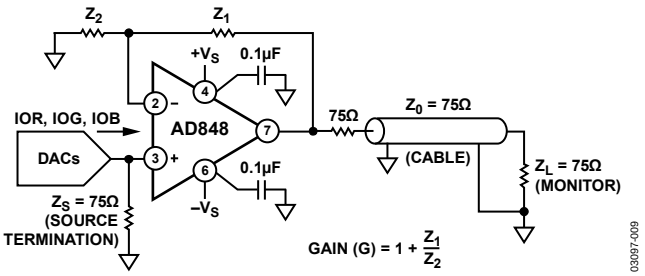


Figure 11. AD848 as an Output Buffer

PCB LAYOUT CONSIDERATIONS

The ADV7125 is optimally designed for lowest noise performance, both radiated and conducted noise. To complement the excellent noise performance of the ADV7125, it is imperative that great care be given to the PCB layout. Figure 12 shows a recommended connection diagram for the ADV7125.

The layout should be optimized for lowest noise on the ADV7125 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. Shorten the lead length between groups of V_{AA} and GND pins to minimize inductive ringing.

It is recommended to use a 4-layer printed circuit board with a single ground plane. The ground and power planes should separate the signal trace layer and the solder side layer. Noise on the analog power plane can be further reduced by using multiple decoupling capacitors (see Figure 12). Optimum performance is achieved by using 0.1 µF and 0.01 µF ceramic capacitors. Individually decouple each V_{AA} pin to ground by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance. It is important to note that while the ADV7125 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, pay close attention to reducing power supply noise. A dc power supply filter (Murata BNX002) provides EMI suppression between the switching power supply and the main PCB. Alternatively, consideration can be given to using a 3-terminal voltage regulator.

DIGITAL SIGNAL INTERCONNECT

Isolate the digital signal lines to the ADV7125 as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates used, long clock lines to the ADV7125 should be avoided to minimize noise pickup.

Connect any active pull-up termination resistors for the digital inputs to the regular PCB power plane (V_{CC}) and not to the analog power plane.

ANALOG SIGNAL INTERCONNECT

Place the ADV7125 as close as possible to the output connectors, thus minimizing noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane and not the analog power plane, thereby maximizing the high frequency power supply rejection.

For optimum performance, the analog outputs should each have a source termination resistance to ground of 75 Ω (doubly terminated 75 Ω configuration). This termination resistance should be as close as possible to the ADV7125 to minimize reflections.

Additional information on PCB design is available in the AN-333 Application Note, *Design and Layout of a Video Graphics System for Reduced EMI*.

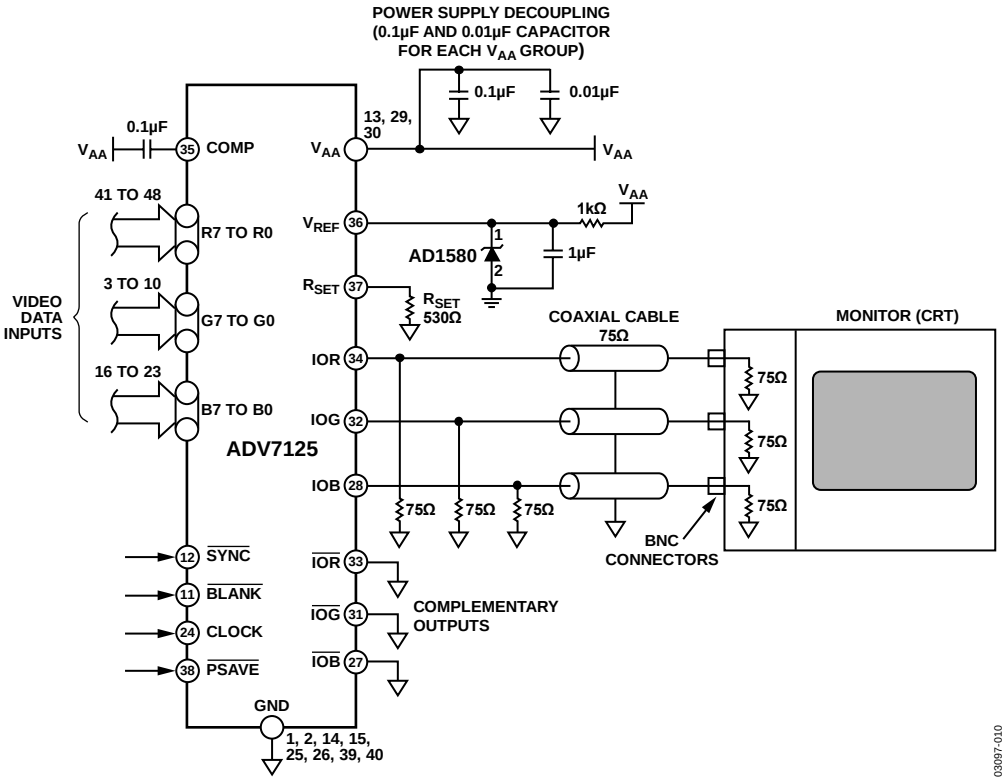


Figure 12. Typical Connection Diagram

OUTLINE DIMENSIONS

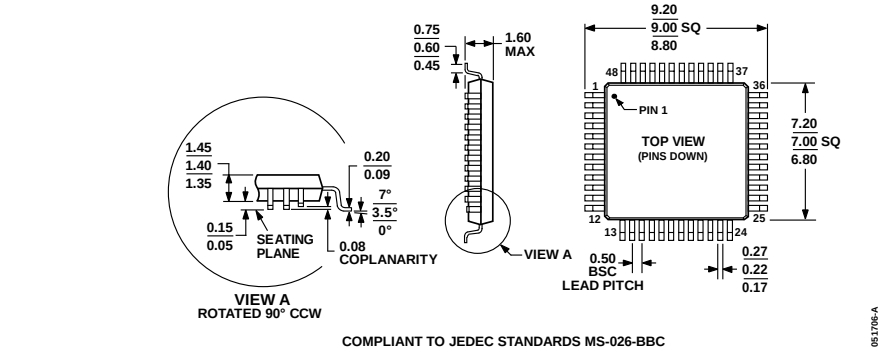


Figure 13. 48-Lead Low Profile Quad Flat Package [LQFP]
(ST-48)
Dimensions shown in millimeters

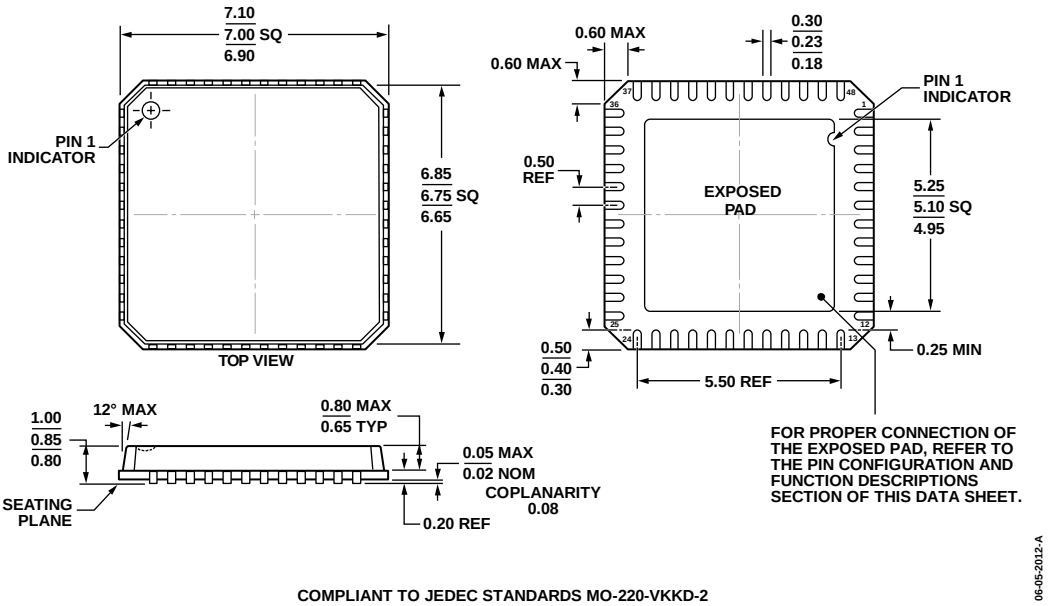


Figure 14. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.85 mm Package Height
(CP-48-1)
Dimensions shown in millimeters

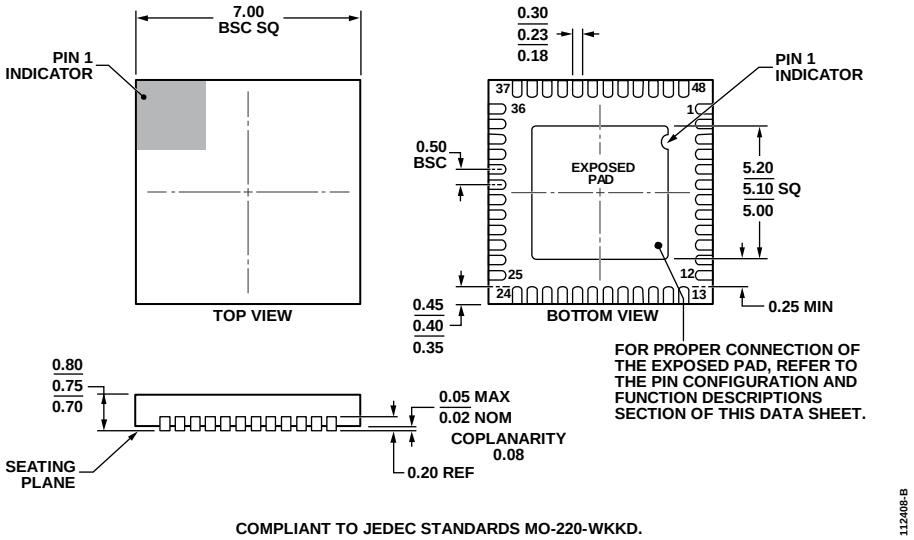


Figure 15. 48-Lead Lead Frame Chip Scale Package [LFCSP]
7 mm × 7 mm Body and 0.75 mm Package Height
(CP-48-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Speed Option	Package Option
ADV7125KSTZ50	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	50 MHz	ST-48
ADV7125KSTZ50-REEL	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	50 MHz	ST-48
ADV7125KSTZ140	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	140 MHz	ST-48
ADV7125JSTZ240	0°C to +70°C	48-Lead Low Profile Quad Flat Package [LQFP]	240 MHz	ST-48
ADV7125JSTZ330	0°C to +70°C	48-Lead Low Profile Quad Flat Package [LQFP]	330 MHz	ST-48
ADV7125WBSTZ170	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	170 MHz	ST-48
ADV7125WBSTZ170-RL	−40°C to +85°C	48-Lead Low Profile Quad Flat Package [LQFP]	170 MHz	ST-48
ADV7125BCPZ170	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	170 MHz	CP-48-1
ADV7125BCPZ170-RL	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	170 MHz	CP-48-1
ADV7125WBCPZ170	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	170 MHz	CP-48-4
ADV7125WBCPZ170-RL	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP]	170 MHz	CP-48-4

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.
[3] ADV7125JSTZ330 is available in a 3.3 V option only.

AUTOMOTIVE PRODUCTS

The ADV7125W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.