# dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X

# 16-Bit Microcontrollers and Digital Signal Controllers with High-Speed PWM, Op Amps and Advanced Analog

## Operating Conditions

- 3.0V to 3.6V, -40°C to +85°C, DC to 70 MIPS
- 3.0V to 3.6V, -40°C to +125°C, DC to 60 MIPS
- 3.0V to 3.6V, -40°C to +150°C, DC to 40 MIPS

## Core: 16-Bit dsPIC33E/PIC24E CPU

- Code Efficient (C and Assembly) Architecture
- Two 40-Bit Wide Accumulators
- Single Cycle (MAC/MPY) with Dual Data Fetch
- Single-Cycle, Mixed-Sign MUL plus Hardware Divide
- 32-Bit Multiply Support

## Clock Management

- 1.0% Internal Oscillator
- Programmable PLLs and Oscillator Clock Sources
- Fail-Safe Clock Monitor (FSCM)
- Independent Watchdog Timer (WDT)
- Fast Wake-up and Start-up

## Power Management

- Low-Power Management modes (Sleep, Idle, Doze)
- Integrated Power-on Reset and Brown-out Reset
- 0.6 mA/MHz Dynamic Current (typical)
- 30 µA $I_{PD}$ Current (typical)

## High-Speed PWM

- Up to Three PWM Pairs with Independent Timing
- Dead Time for Rising and Falling Edges
- 7.14 ns PWM Resolution
- PWM Support for:
  - DC/DC, AC/DC, Inverters, PFC, Lighting
  - BLDC, PMSM, ACIM, SRM
- Programmable Fault Inputs
- Flexible Trigger Configurations for ADC Conversions

## Advanced Analog Features

- ADC module:
  - Configurable as 10-bit, 1.1 Msps with four S&H or 12-bit, 500 ksps with one S&H
  - Six analog inputs on 28-pin devices and up to 16 analog inputs on 64-pin devices
- Flexible and Independent ADC Trigger Sources
- Up to Three Op Amp/Comparators with Direct Connection to the ADC module:
  - Additional dedicated comparator
  - Programmable references with 32 voltage points
- Charge Time Measurement Unit (CTMU):
  - Supports mTouch® capacitive touch sensing
  - Provides high-resolution time measurement (1 ns)
  - On-chip temperature measurement

## Timers/Output Compare/Input Capture

- 12 General Purpose Timers:
  - Five 16-bit and up to two 32-bit timers/counters
  - Four Output Compare (OC) modules, configurable as timers/counters
  - PTG module with two configurable timers/counters
  - 32-bit Quadrature Encoder Interface (QEI) module, configurable as a timer/counter
- Four Input Capture (IC) modules
- Peripheral Pin Select (PPS) to allow Function Remap
- Peripheral Trigger Generator (PTG) for Scheduling Complex Sequences

## Communication Interfaces

- Two UART modules (17.5 Mbps):
  - With support for LIN/J2602 protocols and IrDA®
- Two Four-Wire SPI modules (15 Mbps)
- ECAN™ module (1 Mbaud) CAN 2.0B Support
- Two $I^2C$ modules (up to 1 Mbaud) with SMBus Support
- PPS to allow Function Remap
- Programmable Cyclic Redundancy Check (CRC)

## Direct Memory Access (DMA)

- 4-Channel DMA with User-Selectable Priority Arbitration
- UART, SPI, ADC, ECAN, IC, OC and Timers

## Input/Output

- Sink/Source 12 mA or 6 mA, Pin-Specific for Standard $V_{OH}/V_{OL}$, Up to 22 or 14 mA, respectively for Non-Standard $V_{OH}1$
- 5V Tolerant Pins
- Peripheral Pin Select (PPS) to allow Digital Function Remapping
- Selectable Open-Drain, Pull-ups and Pull-Downs
- Up to 5 mA Overvoltage Clamp Current
- Change Notification Interrupts on All I/O Pins

## Qualification and Class B Support

- AEC-Q100 REVG (Grade 1, -40°C to +125°C)
- AEC-Q100 REVG (Grade 0, -40°C to +150°C)
- Class B Safety Library, IEC 60730

## Debugger Development Support

- In-Circuit and In-Application Programming
- Two Program and Two Complex Data Breakpoints
- IEEE 1149.2 Compatible (JTAG) Boundary Scan
- Trace and Run-Time Watch

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## dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X PRODUCT FAMILIES

The device names, pin counts, memory sizes and peripheral availability of each device are listed in Table 1 (General Purpose Families) and Table 2 (Motor Control Families). Their pinout diagrams appear on the following pages.

**TABLE 1: dsPIC33EPXXXGP50X and PIC24EPXXXGP20X GENERAL PURPOSE FAMILIES**

| Device | Page Erase Size (Instructions) | Program Flash Memory (Kbytes) | RAM (Kbyte) | Remappable Peripherals | | | | | | | $I^2C$ | CRC Generator | 10-Bit/12-Bit ADC (Channels) | Op Amps/Comparators | CTMU | PTG | I/O Pins | Pins | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 16-Bit/32-Bit Timers | Input Capture | Output Compare | UART | SPI(2) | ECAN™ Technology | External Interrupts(3) | | | | | | | | | |
| PIC24EP32GP202 | 512 | 32 | 4 | 5 | 4 | 4 | 2 | 2 | — | 3 | 2 | 1 | 6 | 2/3(1) | Yes | Yes | 21 | 28 | SPDIP, SOIC, SSOP(4), QFN-S |
| PIC24EP64GP202 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | |
| PIC24EP128GP202 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | |
| PIC24EP256GP202 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | |
| PIC24EP512GP202 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | |
| PIC24EP32GP203 | 512 | 32 | 4 | 5 | 4 | 4 | 2 | 2 | — | 3 | 2 | 1 | 8 | 2/4 | Yes | Yes | 25 | 36 | VTLA, UQFN |
| PIC24EP64GP203 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | |
| PIC24EP32GP204 | 512 | 32 | 4 | 5 | 4 | 4 | 2 | 2 | — | 3 | 2 | 1 | 9 | 3/4 | Yes | Yes | 35 | 44/48 | VTLA(4), TQFP, QFN, UQFN |
| PIC24EP64GP204 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | |
| PIC24EP128GP204 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | |
| PIC24EP256GP204 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | |
| PIC24EP512GP204 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | |
| PIC24EP64GP206 | 1024 | 64 | 8 | 5 | 4 | 4 | 2 | 2 | — | 3 | 2 | 1 | 16 | 3/4 | Yes | Yes | 53 | 64 | TQFP, QFN |
| PIC24EP128GP206 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | |
| PIC24EP256GP206 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | |
| PIC24EP512GP206 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | |
| dsPIC33EP32GP502 | 512 | 32 | 4 | 5 | 4 | 4 | 2 | 2 | 1 | 3 | 2 | 1 | 6 | 2/3(1) | Yes | Yes | 21 | 28 | SPDIP, SOIC, SSOP(4), QFN-S |
| dsPIC33EP64GP502 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | |
| dsPIC33EP128GP502 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | |
| dsPIC33EP256GP502 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | |
| dsPIC33EP512GP502 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | |
| dsPIC33EP32GP503 | 512 | 32 | 4 | 5 | 4 | 4 | 2 | 2 | 1 | 3 | 2 | 1 | 8 | 2/4 | Yes | Yes | 25 | 36 | VTLA, UQFN |
| dsPIC33EP64GP503 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | |
| dsPIC33EP32GP504 | 512 | 32 | 4 | 5 | 4 | 4 | 2 | 2 | 1 | 3 | 2 | 1 | 9 | 3/4 | Yes | Yes | 35 | 44/48 | VTLA(4), TQFP, QFN, UQFN |
| dsPIC33EP64GP504 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | |
| dsPIC33EP128GP504 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | |
| dsPIC33EP256GP504 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | |
| dsPIC33EP512GP504 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | |
| dsPIC33EP64GP506 | 1024 | 64 | 8 | 5 | 4 | 4 | 2 | 2 | 1 | 3 | 2 | 1 | 16 | 3/4 | Yes | Yes | 53 | 64 | TQFP, QFN |
| dsPIC33EP128GP506 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | |
| dsPIC33EP256GP506 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | |
| dsPIC33EP512GP506 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | |

**Note 1:** On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 "Op Amp/Comparator Module"** for details.
**2:** Only SPI2 is remappable.
**3:** INT0 is not remappable.
**4:** The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.


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**TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES**

| Device | Page Erase Size (Instructions) | Program Flash Memory (Kbytes) | RAM (Kbytes) | Remappable Peripherals | | | | | | | | | $I^2C$ | CRC Generator | 10-Bit/12-Bit ADC (Channels) | Op Amps/Comparators | CTMU | PTG | I/O Pins | Pins | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 16-Bit/32-Bit Timers | Input Capture | Output Compare | Motor Control PWM(4) (Channels) | Quadrature Encoder Interface | UART | SPI(2) | ECAN™ Technology | External Interrupts(3) | | | | | | | | | |
| PIC24EP32MC202 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 6 | 2/3(1) | Yes | Yes | 21 | 28 | SPDIP, SOIC, SSOP(5), QFN-S |
| PIC24EP64MC202 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| PIC24EP128MC202 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| PIC24EP256MC202 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| PIC24EP512MC202 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| PIC24EP32MC203 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 8 | 2/4 | Yes | Yes | 25 | 36 | VTLA, UQFN |
| PIC24EP64MC203 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| PIC24EP32MC204 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 9 | 3/4 | Yes | Yes | 35 | 44/48 | VTLA(5), TQFP, QFN, UQFN |
| PIC24EP64MC204 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| PIC24EP128MC204 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| PIC24EP256MC204 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| PIC24EP512MC204 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| PIC24EP64MC206 | 1024 | 64 | 8 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 16 | 3/4 | Yes | Yes | 53 | 64 | TQFP, QFN |
| PIC24EP128MC206 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| PIC24EP256MC206 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| PIC24EP512MC206 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP32MC202 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 6 | 2/3(1) | Yes | Yes | 21 | 28 | SPDIP, SOIC, SSOP(5), QFN-S |
| dsPIC33EP64MC202 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP128MC202 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP256MC202 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP512MC202 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP32MC203 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 8 | 2/4 | Yes | Yes | 25 | 36 | VTLA, UQFN |
| dsPIC33EP64MC203 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP32MC204 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 9 | 3/4 | Yes | Yes | 35 | 44/48 | VTLA(5), TQFP, QFN, UQFN |
| dsPIC33EP64MC204 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP128MC204 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP256MC204 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP512MC204 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP64MC206 | 1024 | 64 | 8 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | — | 3 | 2 | 1 | 16 | 3/4 | Yes | Yes | 53 | 64 | TQFP, QFN |
| dsPIC33EP128MC206 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP256MC206 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP512MC206 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP32MC502 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | 1 | 3 | 2 | 1 | 6 | 2/3(1) | Yes | Yes | 21 | 28 | SPDIP, SOIC, SSOP(5), QFN-S |
| dsPIC33EP64MC502 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP128MC502 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP256MC502 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP512MC502 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP32MC503 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | 1 | 3 | 2 | 1 | 8 | 2/4 | Yes | Yes | 25 | 36 | VTLA, UQFN |
| dsPIC33EP64MC503 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |

**Note 1:** On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 "Op Amp/Comparator Module"** for details.
**2:** Only SPI2 is remappable.
**3:** INT0 is not remappable.
**4:** Only the PWM Faults are remappable.
**5:** The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.

**TABLE 2: dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X MOTOR CONTROL FAMILIES (CONTINUED)**

| Device | Page Erase Size (Instructions) | Program Flash Memory (Kbytes) | RAM (Kbytes) | Remappable Peripherals | | | | | | | | | I²C | CRC Generator | 10-Bit/12-Bit ADC (Channels) | Op Amps/Comparators | CTMU | PTG | I/O Pins | Pins | Packages |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 16-Bit/32-Bit Timers | Input Capture | Output Compare | Motor Control PWM(4) (Channels) | Quadrature Encoder Interface | UART | SPI(2) | ECAN™ Technology | External Interrupts(3) | | | | | | | | | |
| dsPIC33EP32MC504 | 512 | 32 | 4 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | 1 | 3 | 2 | 1 | 9 | 3/4 | Yes | Yes | 35 | 44/48 | VTLA(5), TQFP, QFN, UQFN |
| dsPIC33EP64MC504 | 1024 | 64 | 8 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP128MC504 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP256MC504 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP512MC504 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP64MC506 | 1024 | 64 | 8 | 5 | 4 | 4 | 6 | 1 | 2 | 2 | 1 | 3 | 2 | 1 | 16 | 3/4 | Yes | Yes | 53 | 64 | TQFP, QFN |
| dsPIC33EP128MC506 | 1024 | 128 | 16 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP256MC506 | 1024 | 256 | 32 | | | | | | | | | | | | | | | | | | |
| dsPIC33EP512MC506 | 1024 | 512 | 48 | | | | | | | | | | | | | | | | | | |

**Note 1:** On 28-pin devices, Comparator 4 does not have external connections. Refer to **Section 25.0 "Op Amp/Comparator Module"** for details.
**2:** Only SPI2 is remappable.
**3:** INT0 is not remappable.
**4:** Only the PWM Faults are remappable.
**5:** The SSOP and VTLA packages are not available for devices with 512 Kbytes of memory.


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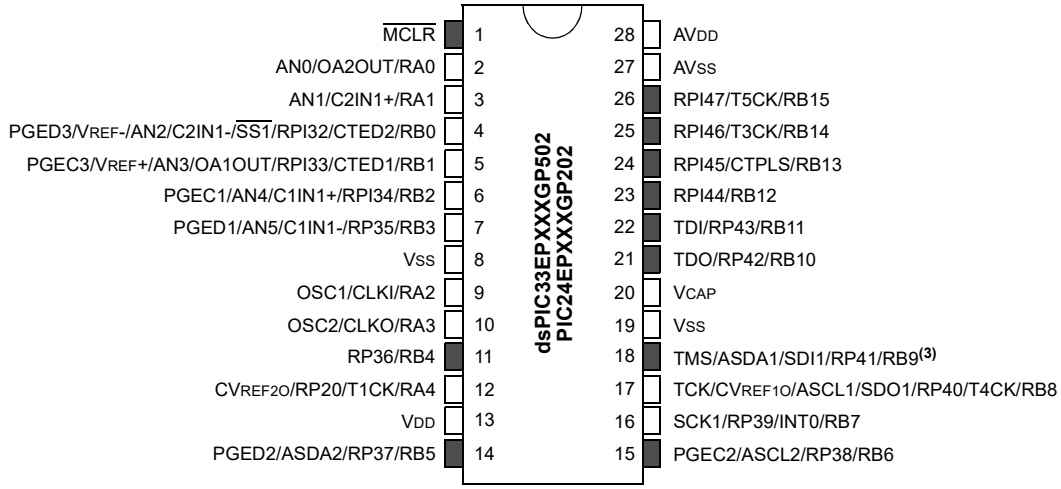
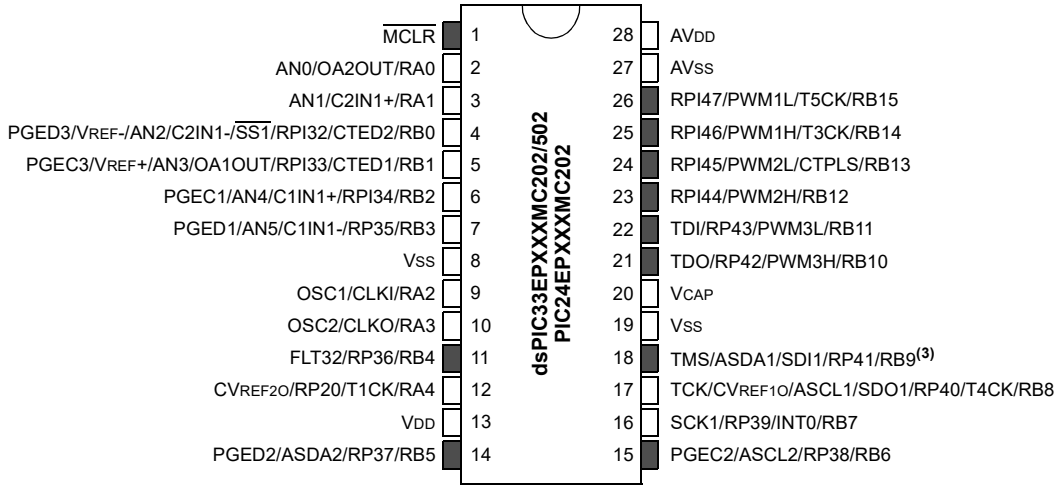
## Pin Diagrams

**28-Pin SPDIP/SOIC/SSOP(1,2)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

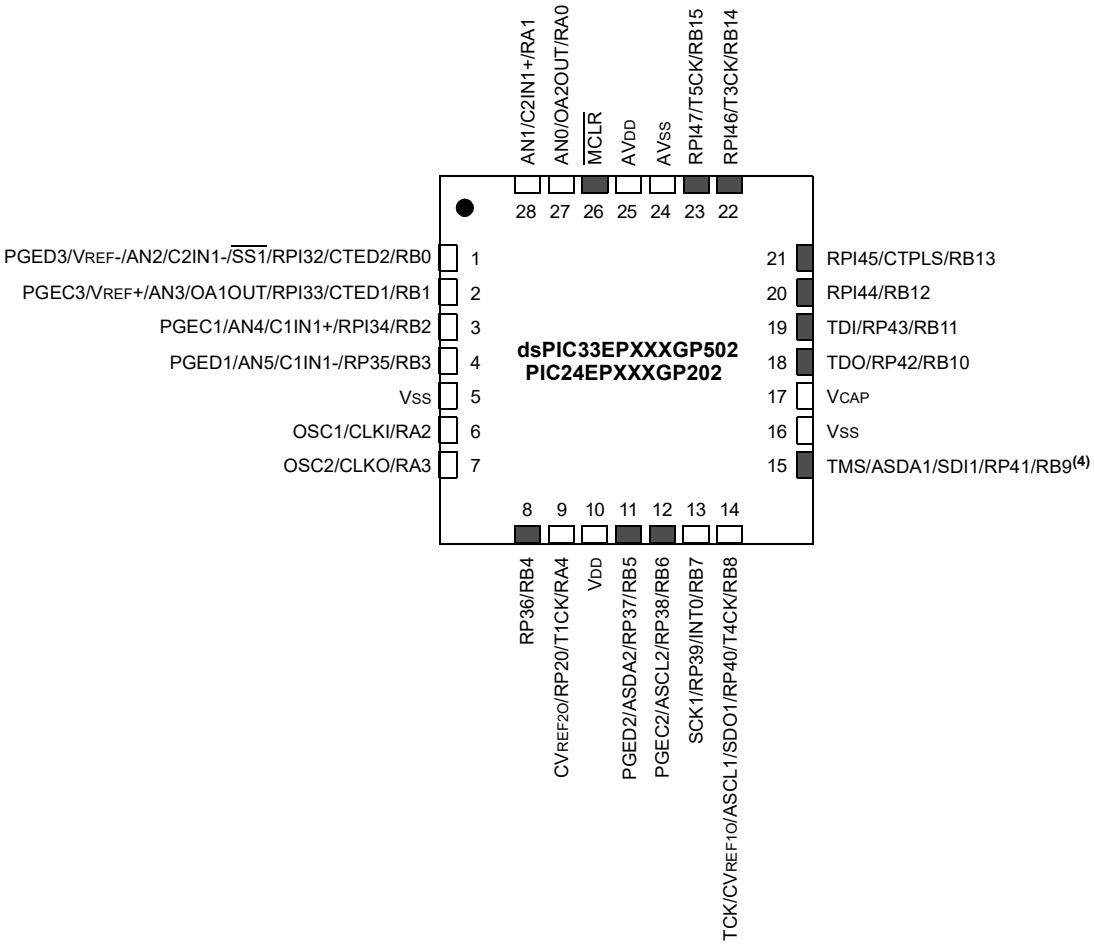
**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## Pin Diagrams (Continued)

**28-Pin QFN-S(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.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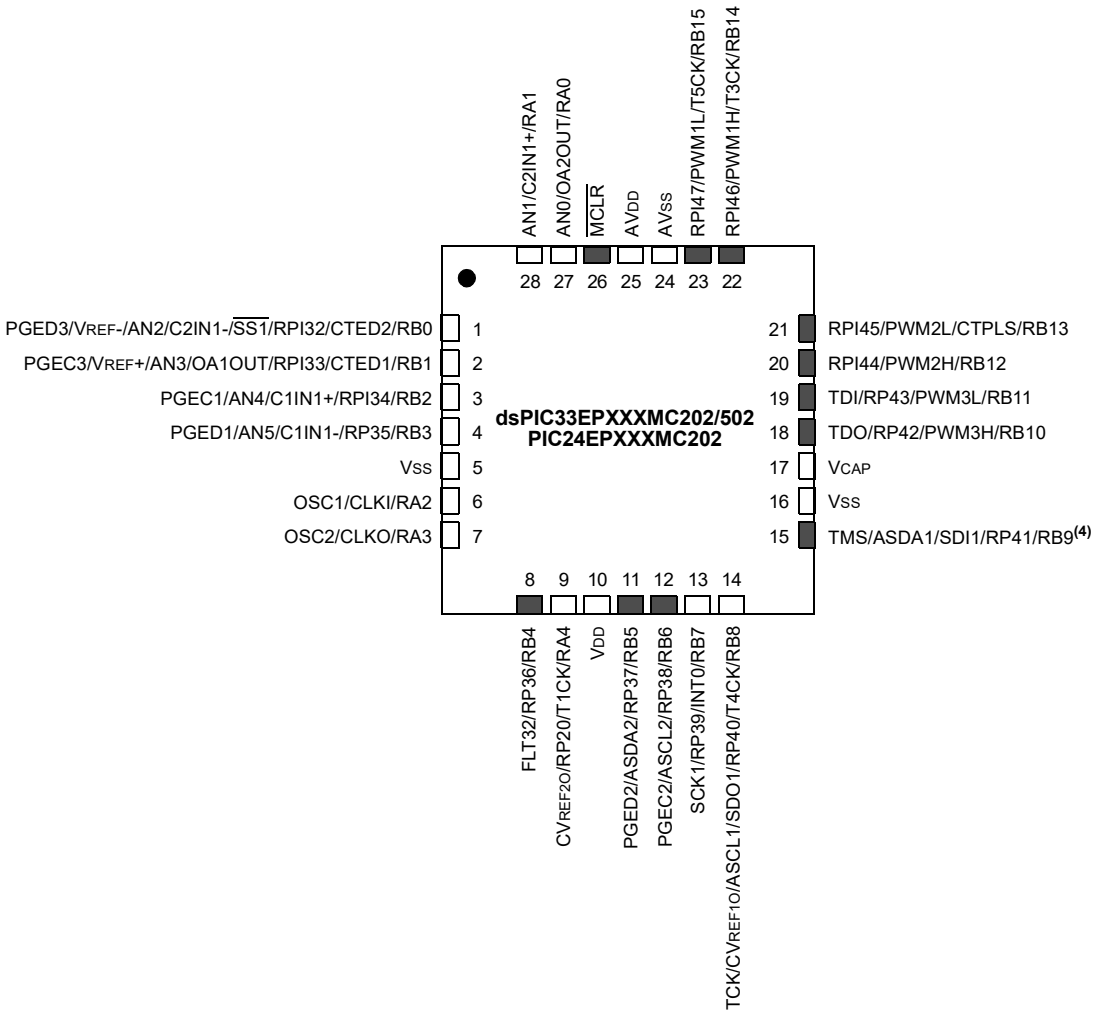
## Pin Diagrams (Continued)

**28-Pin QFN-S(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

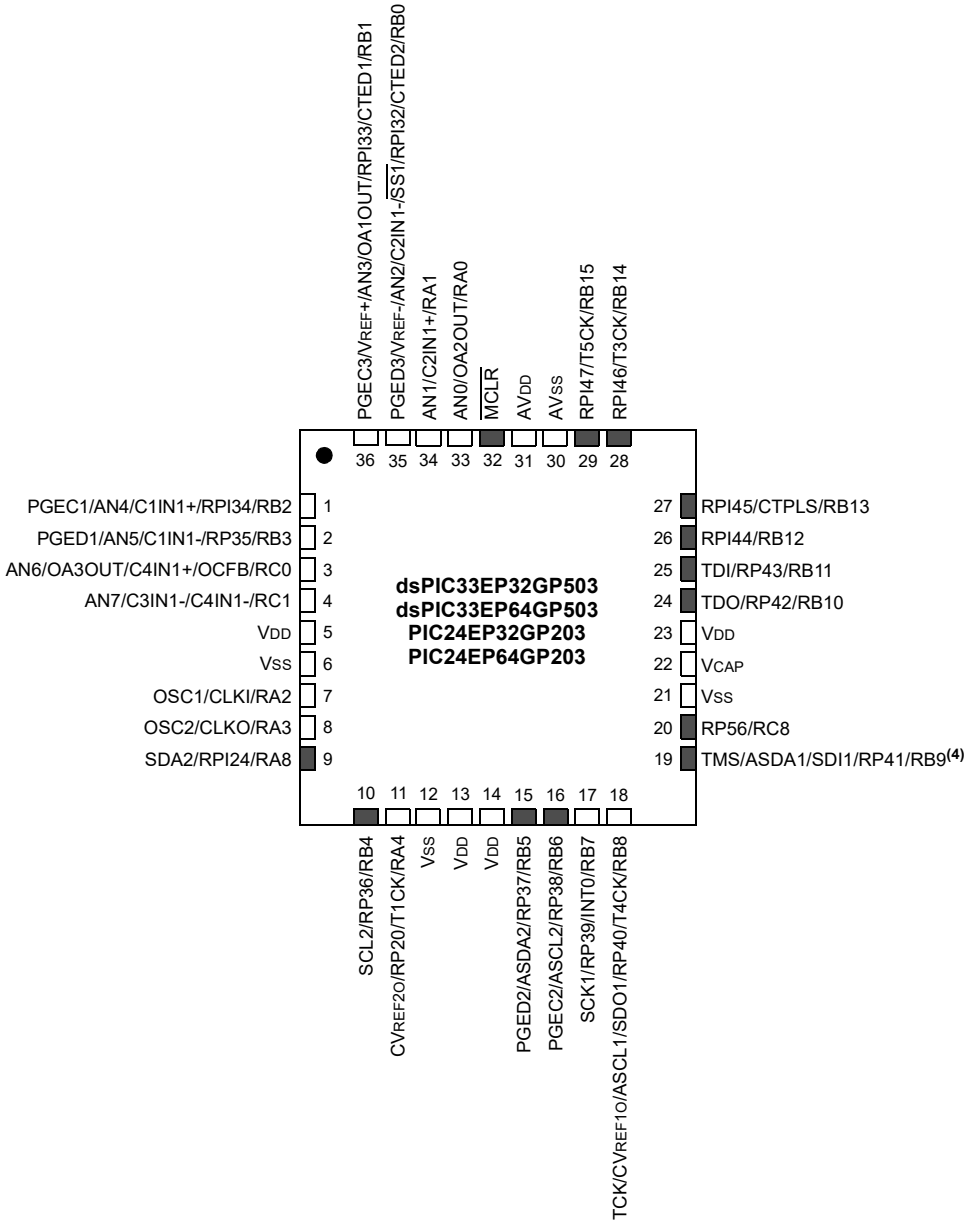
**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## Pin Diagrams (Continued)

**36-Pin UQFN(1,2,3)**

= Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** If the op amp is selected when OPMODE (CMxCON[10]) = 1, the OAx input is used; otherwise, the ANx input is used.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.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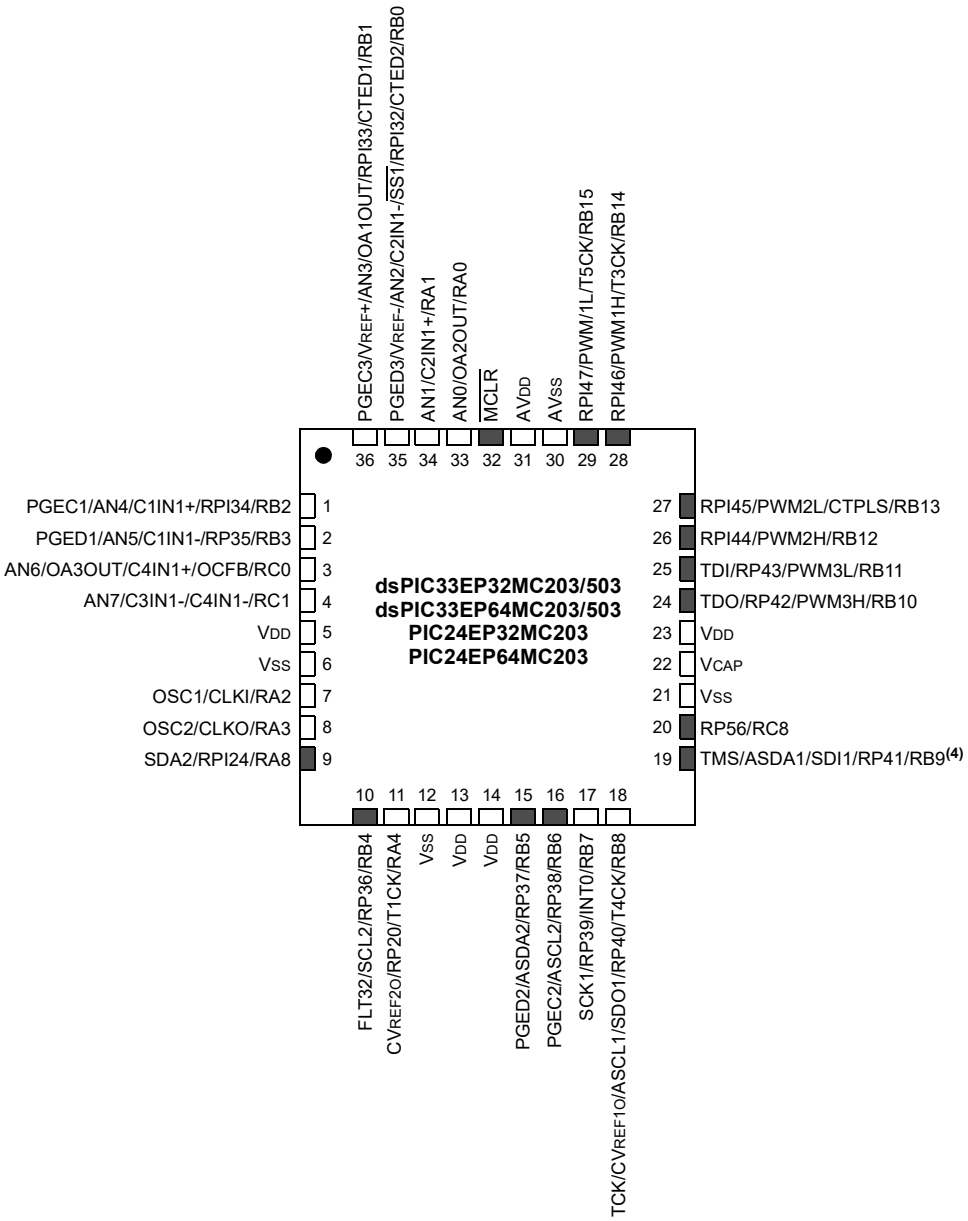
## Pin Diagrams (Continued)

**36-Pin UQFN(1,2,3)**

= Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

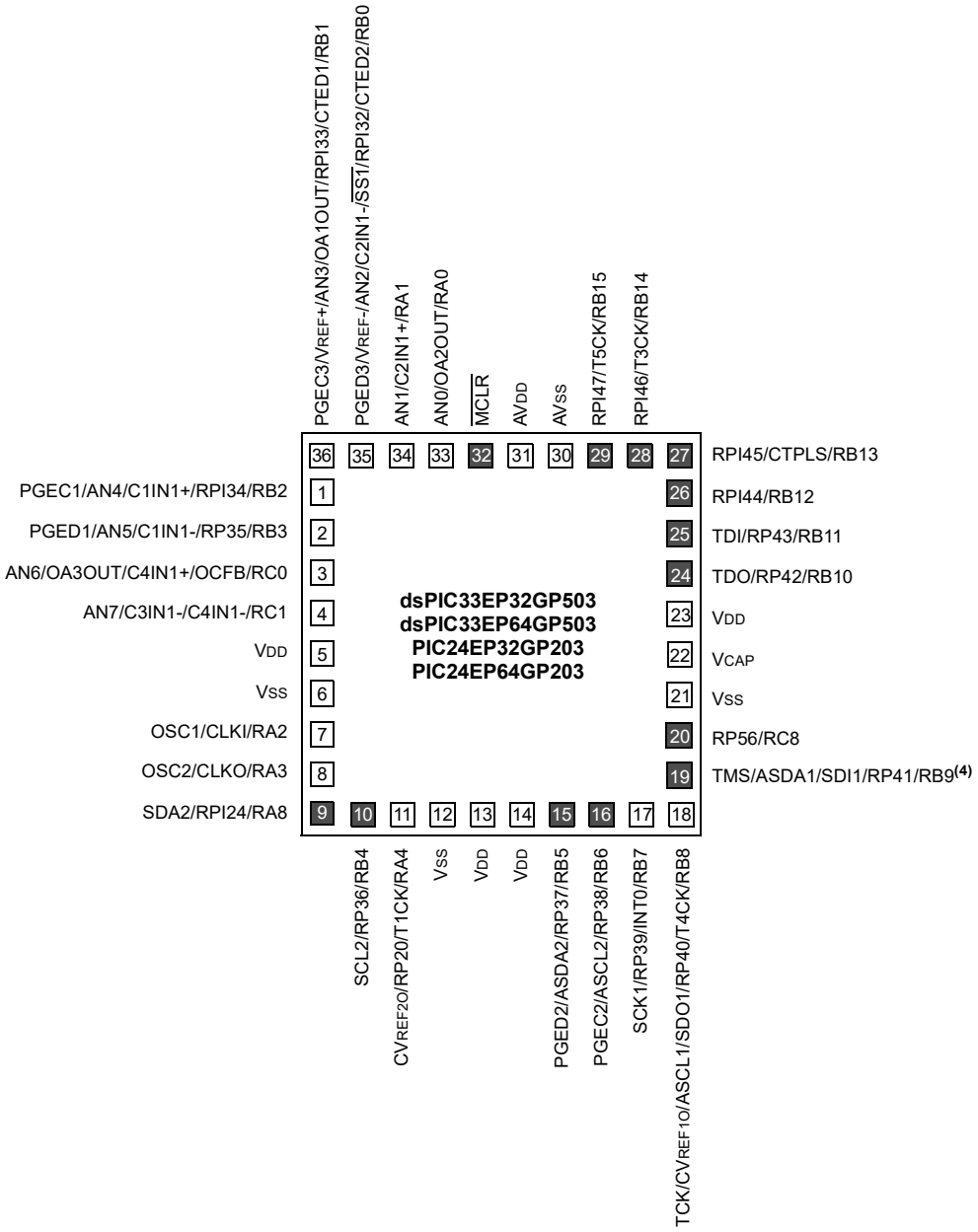
**3:** If the op amp is selected when OPMODE (CMxCON[10]) = 1, the OAx input is used; otherwise, the ANx input is used.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## Pin Diagrams (Continued)

**36-Pin VTLA(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.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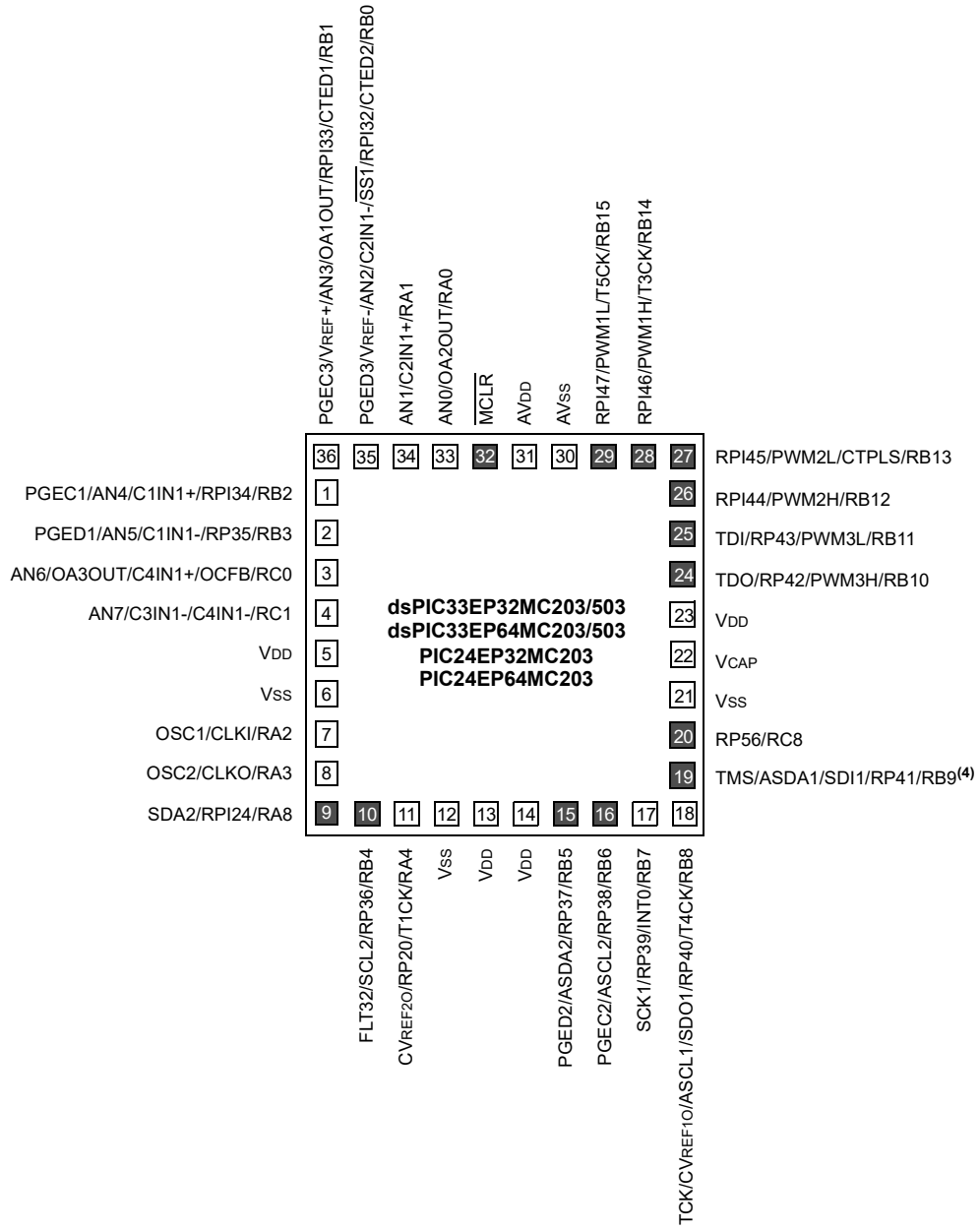
## Pin Diagrams (Continued)

**36-Pin VTLA(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

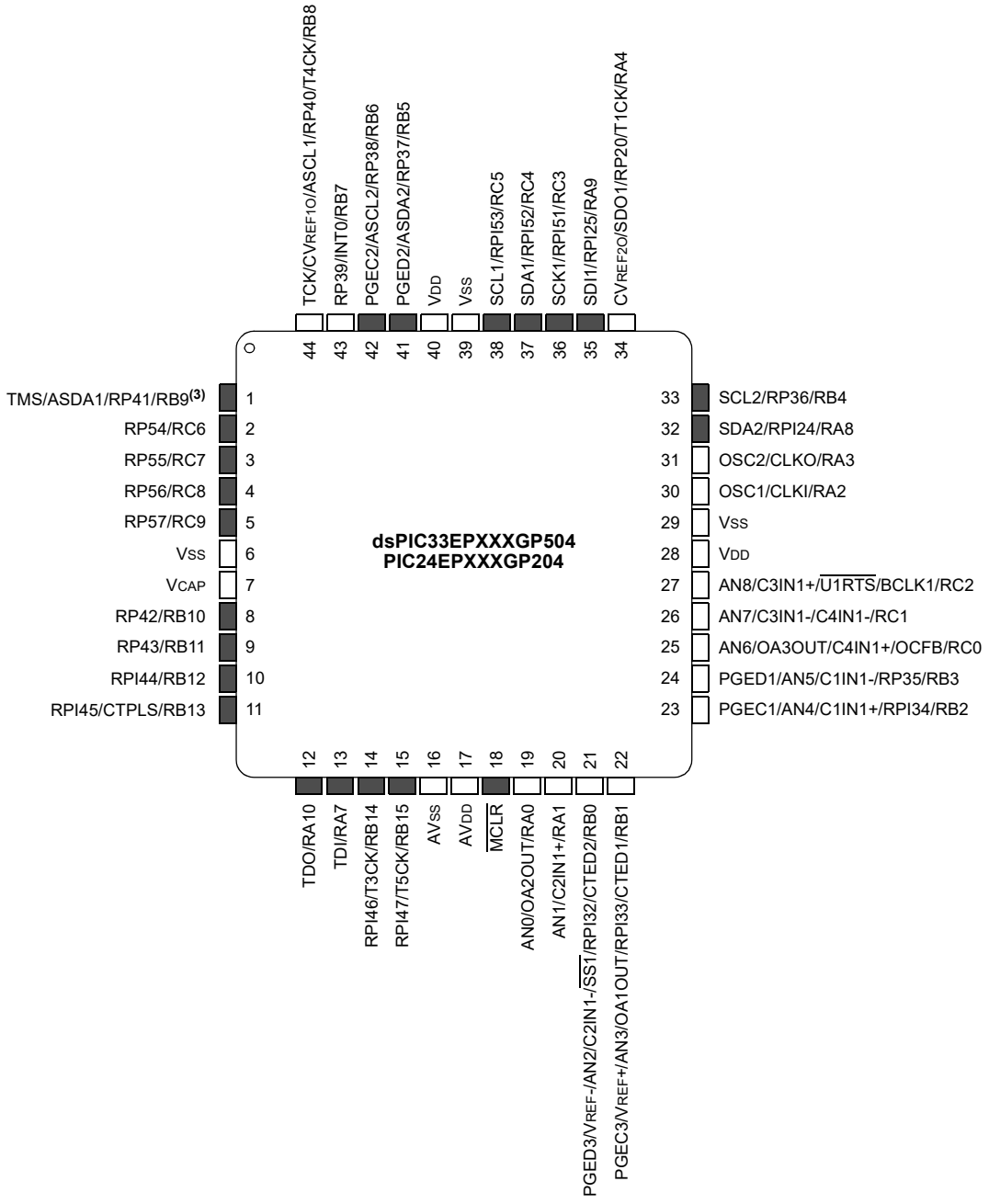
**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## Pin Diagrams (Continued)

**44-Pin TQFP(1,2)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.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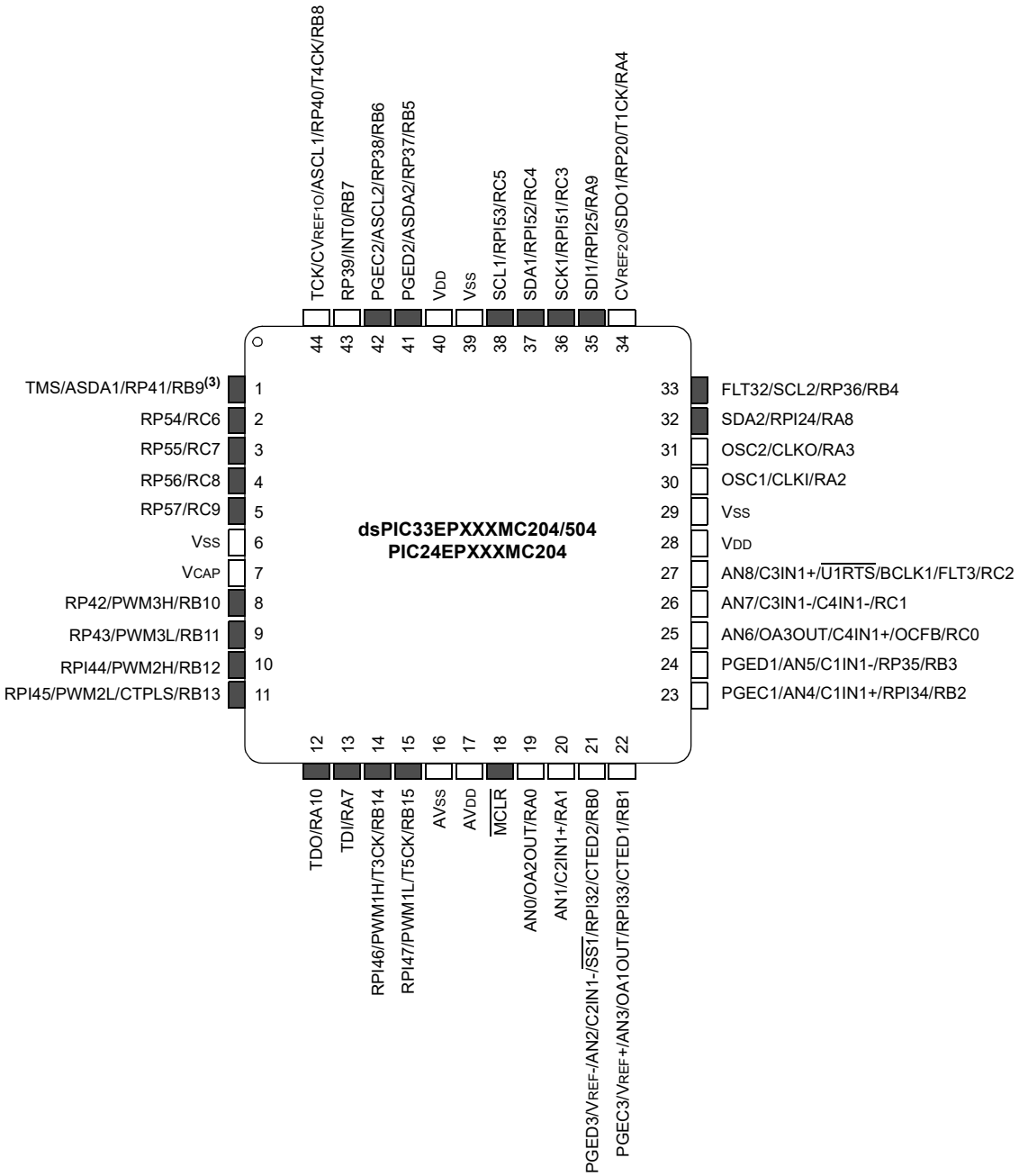
## Pin Diagrams (Continued)

**44-Pin TQFP(1,2)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

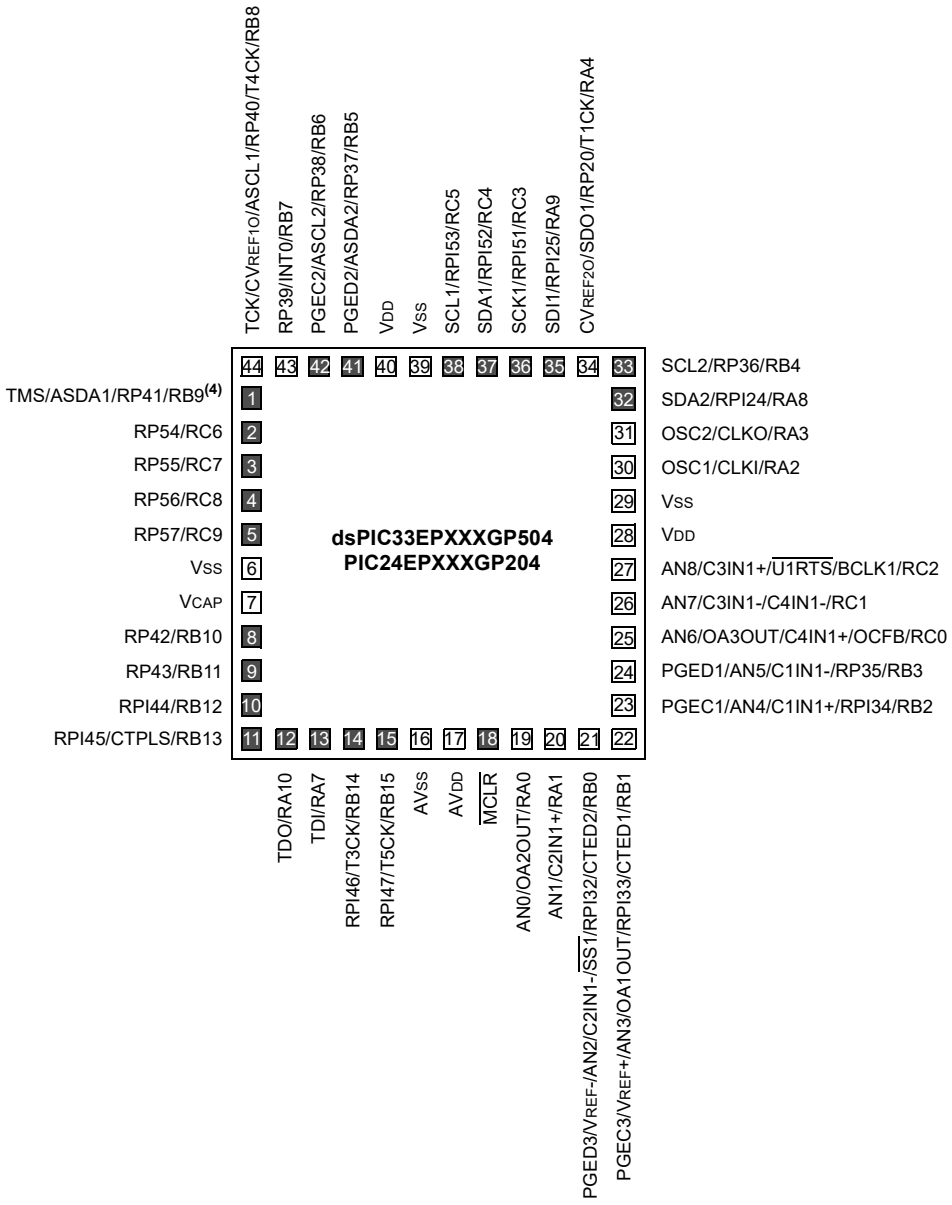
**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## Pin Diagrams (Continued)

**44-Pin VTLA(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.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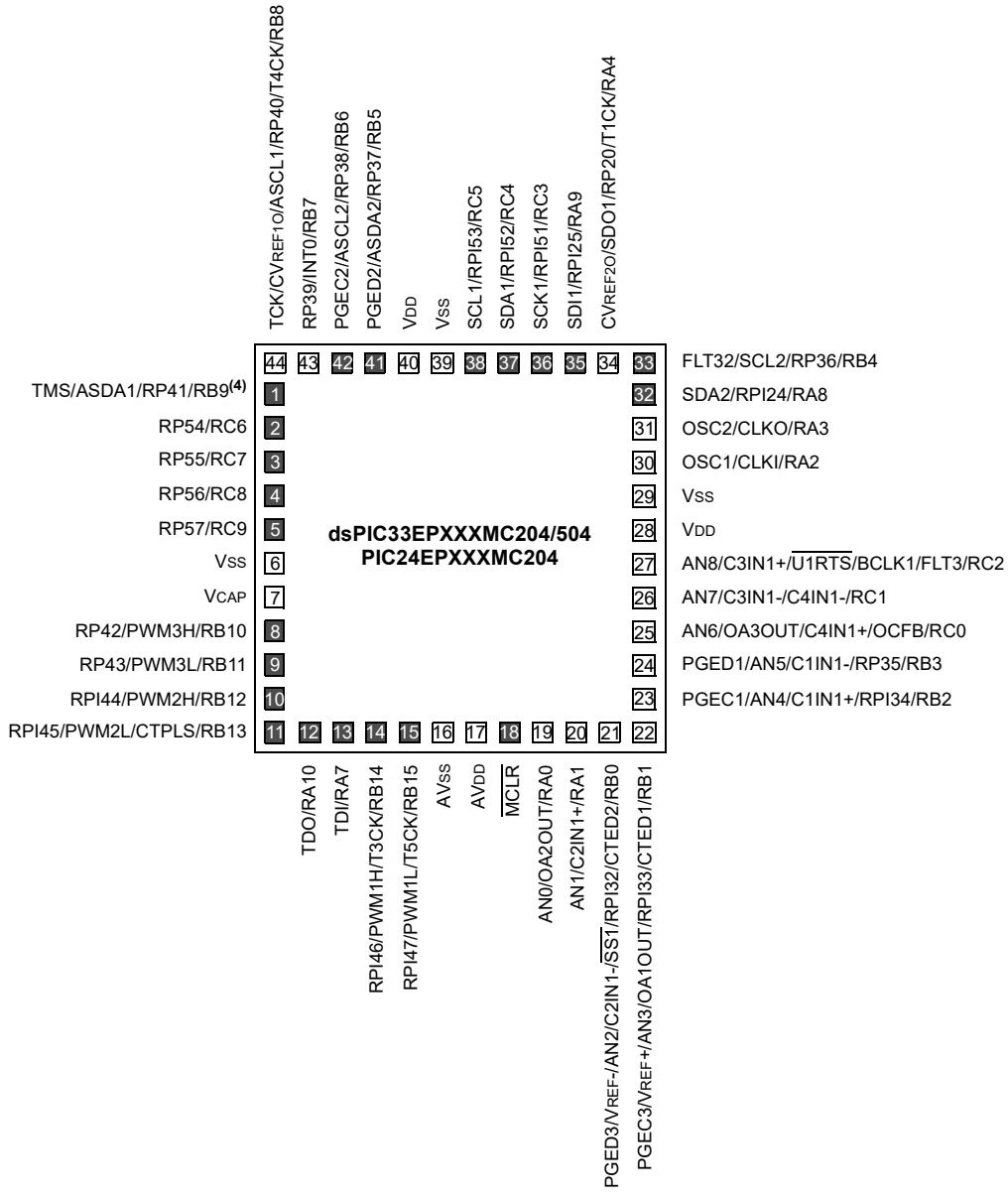
## Pin Diagrams (Continued)

**44-Pin VTLA(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

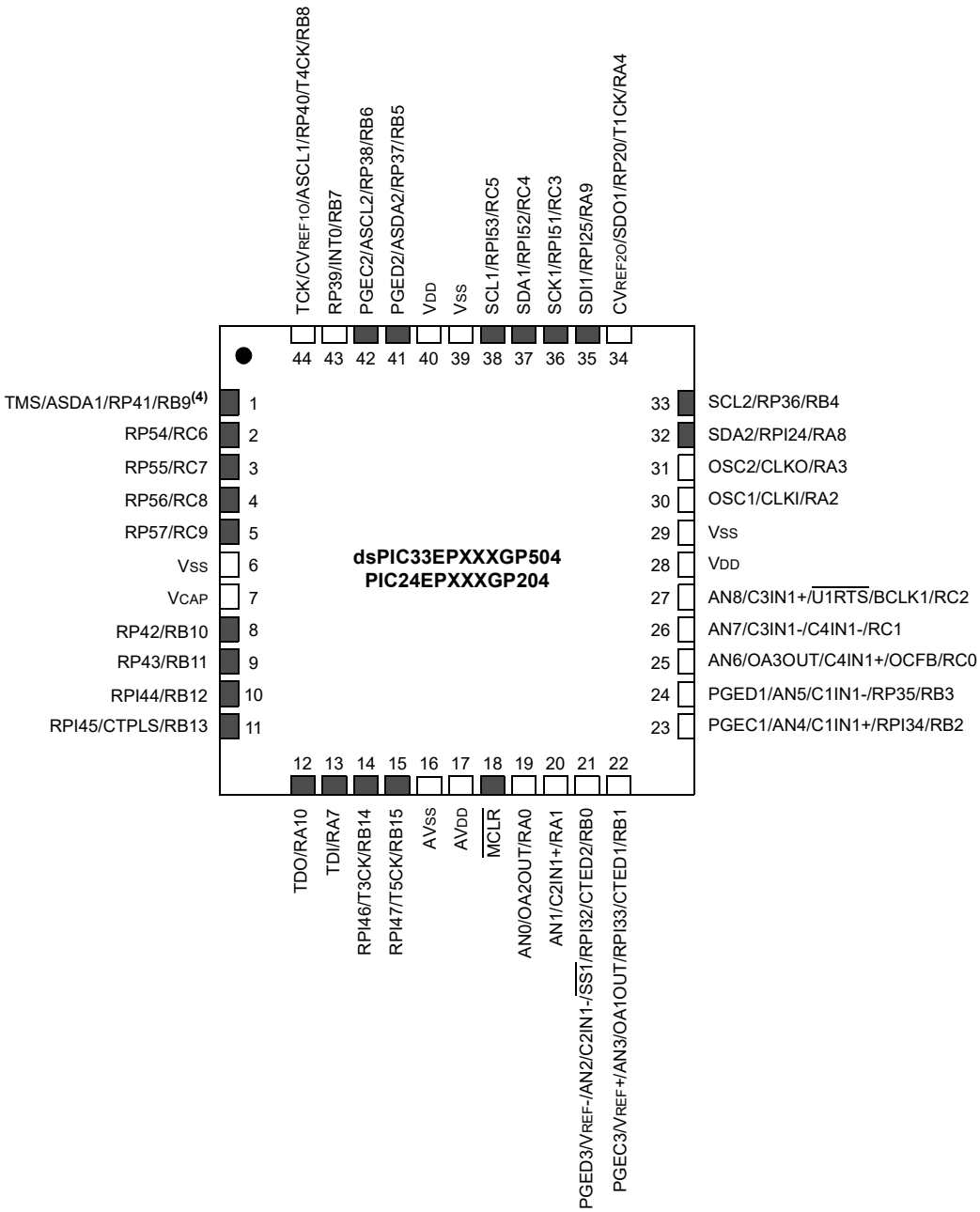
**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## Pin Diagrams (Continued)

**44-Pin QFN(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.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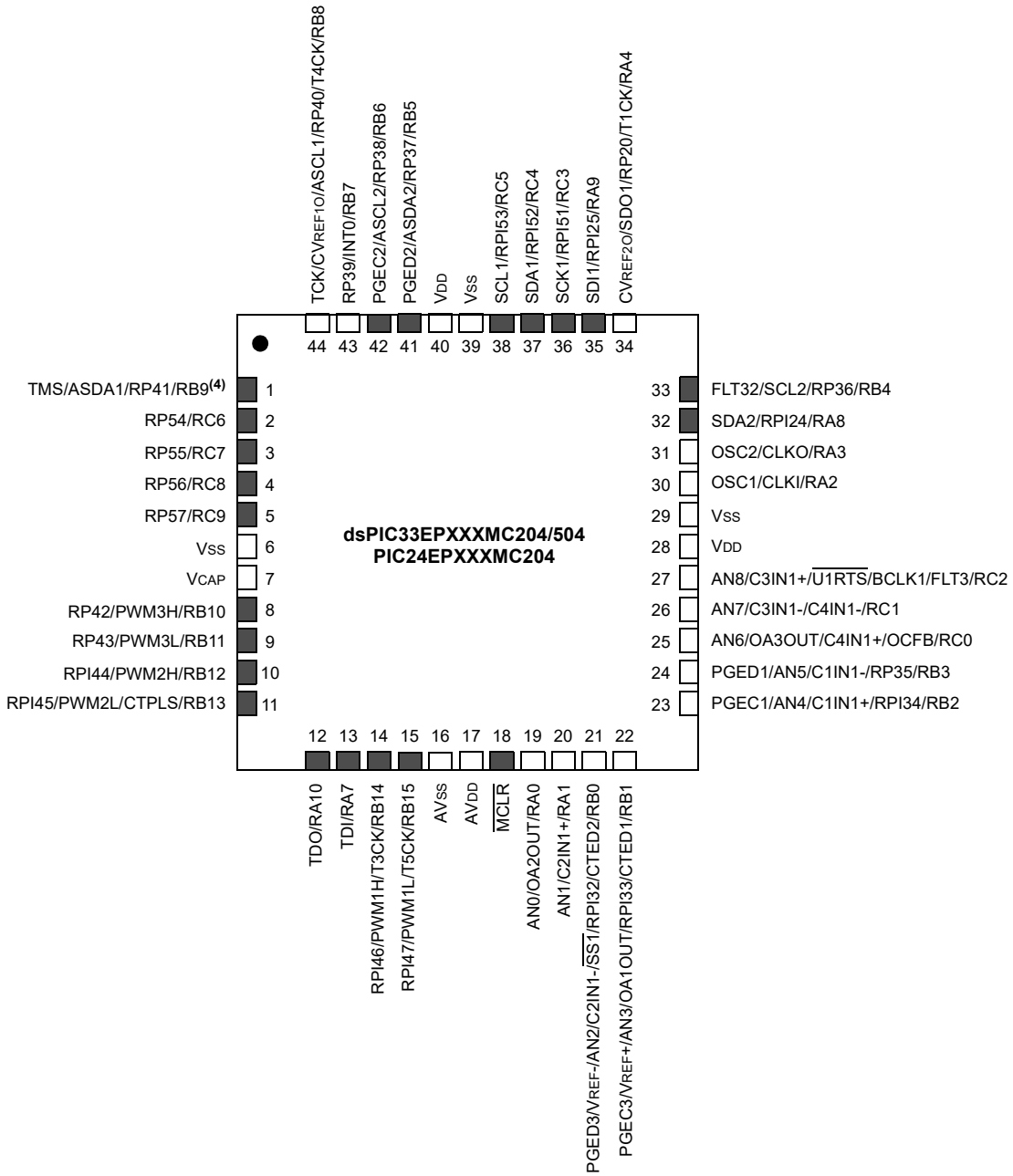
## Pin Diagrams (Continued)

**44-Pin QFN(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

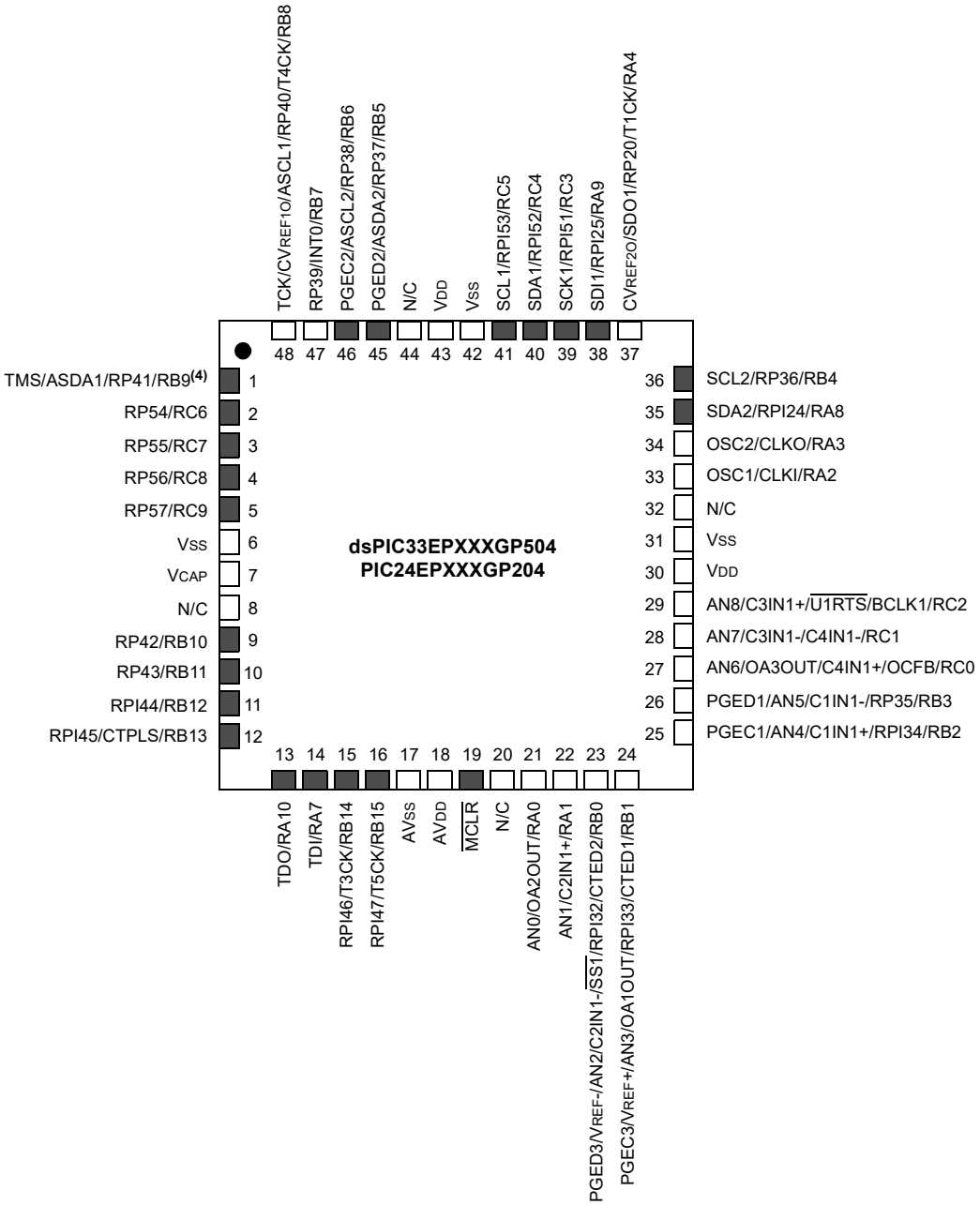
**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## Pin Diagrams (Continued)

**48-Pin UQFN(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.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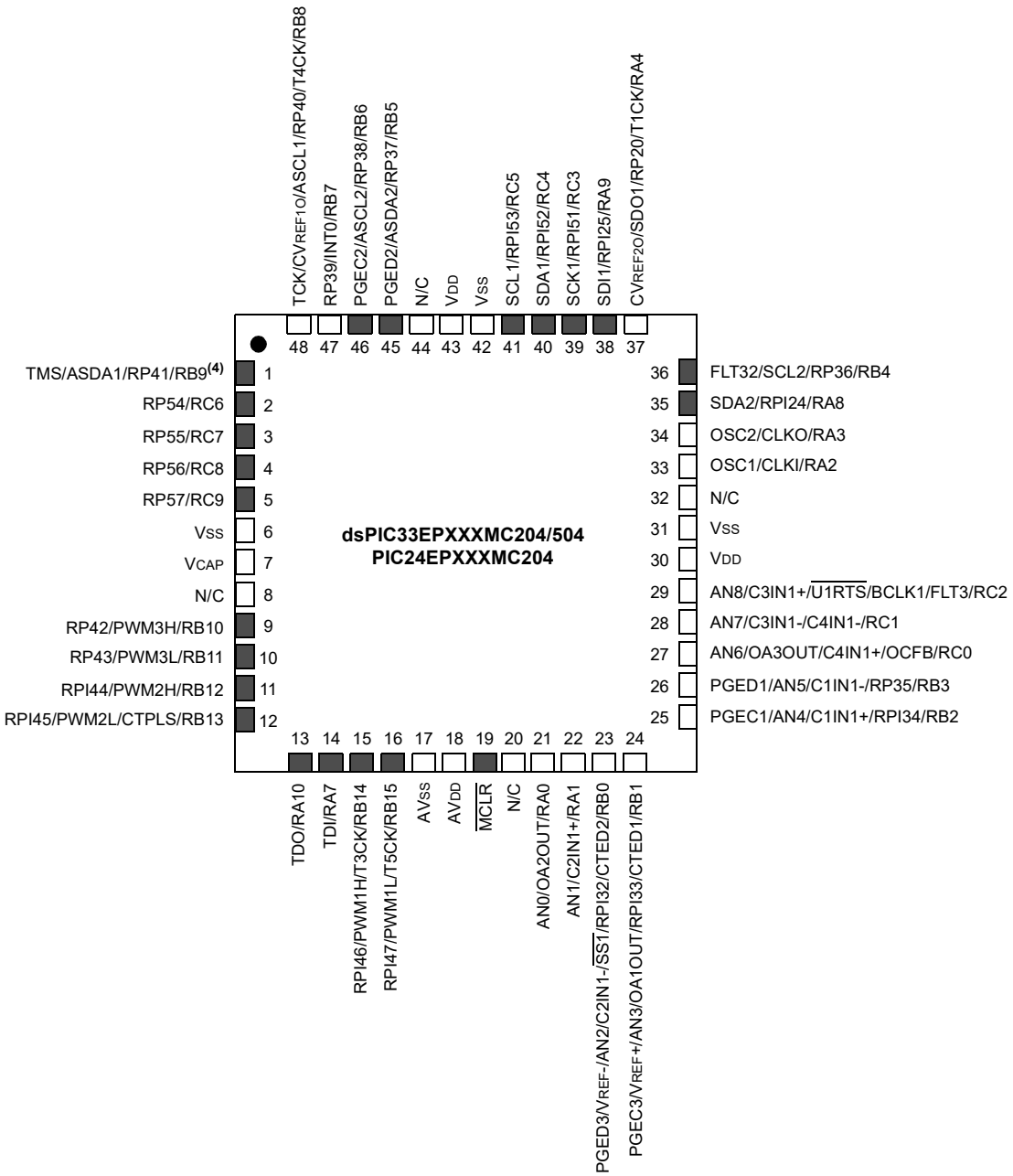
## Pin Diagrams (Continued)

**48-Pin UQFN(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

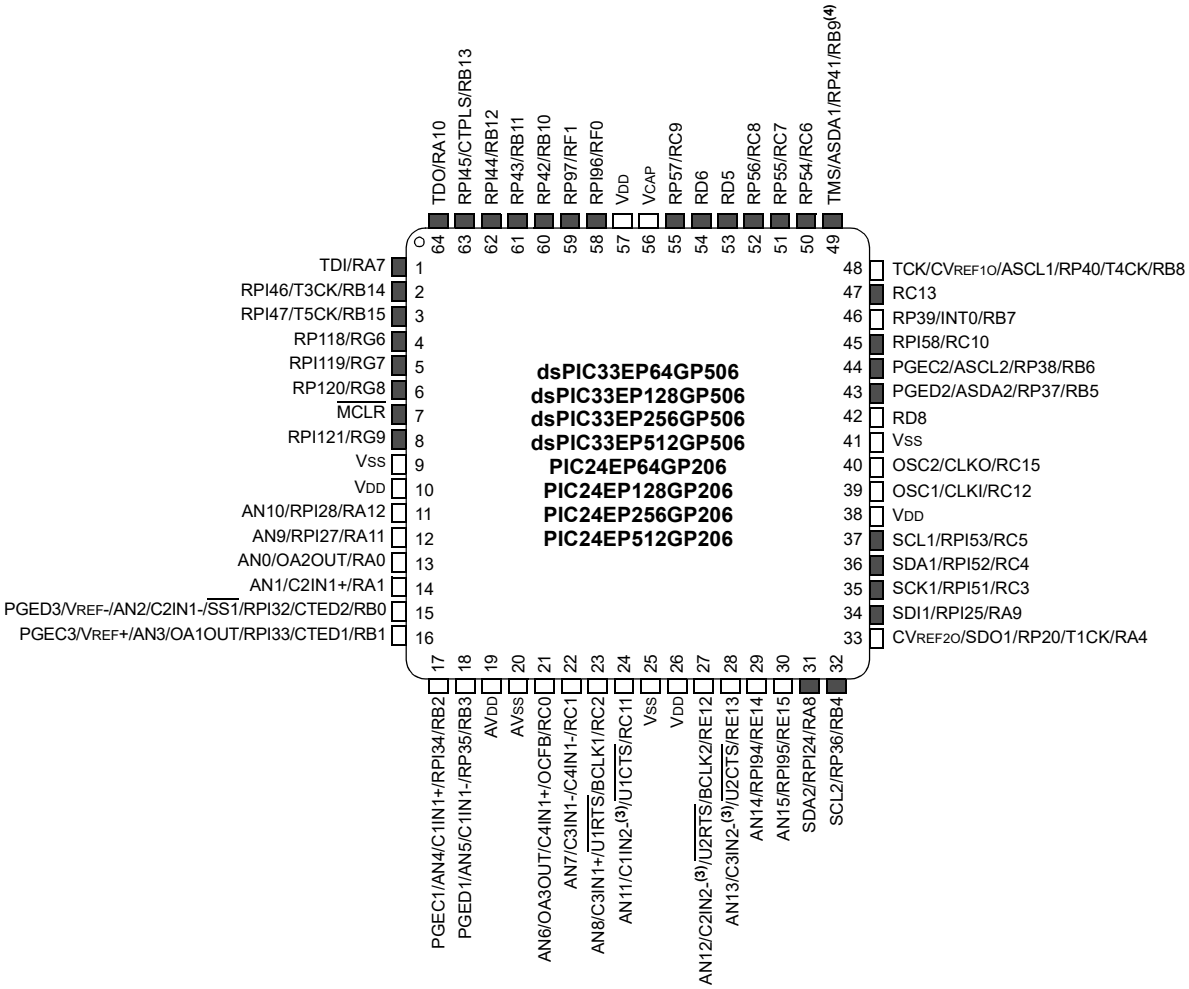
**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## Pin Diagrams (Continued)

**64-Pin TQFP(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.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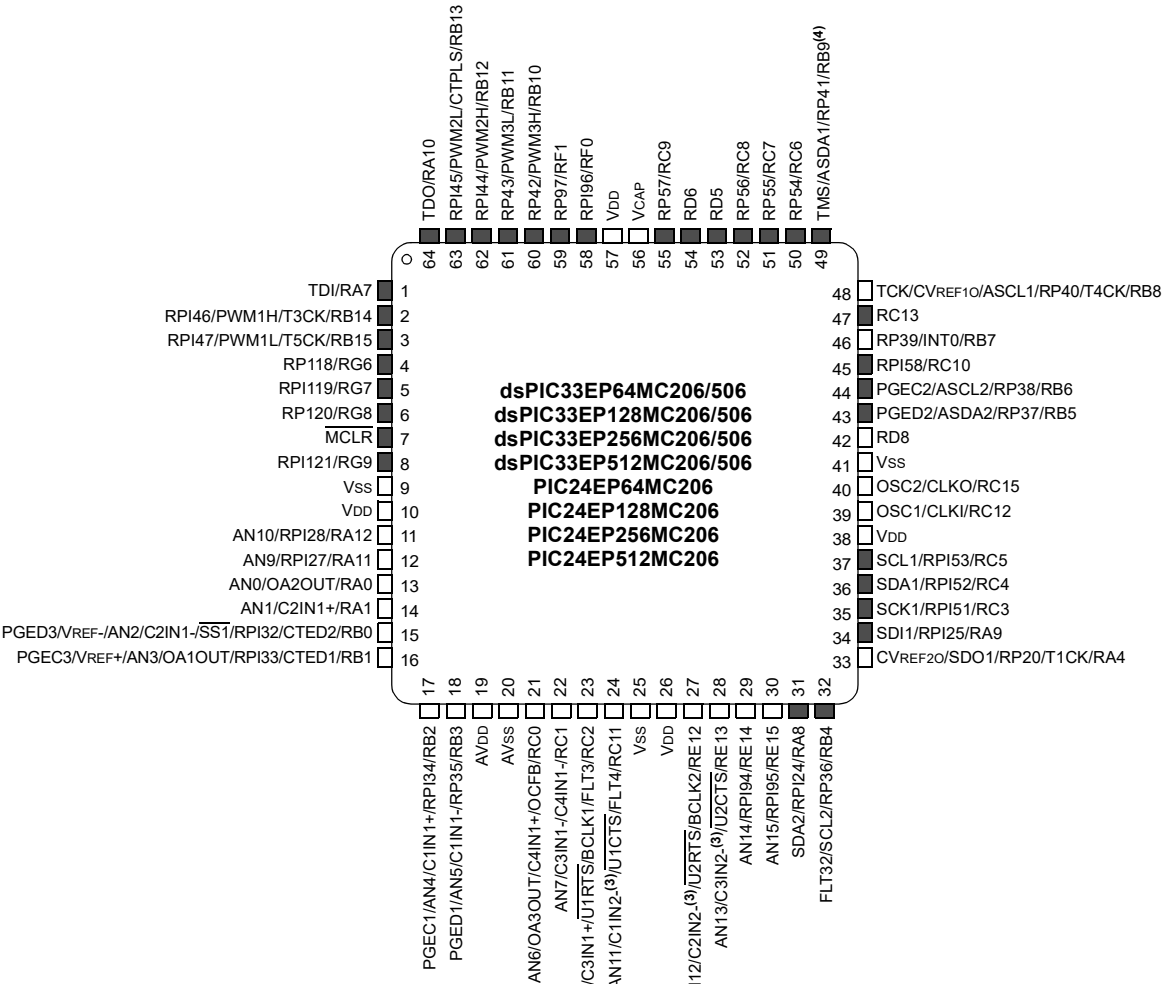
## Pin Diagrams (Continued)

**64-Pin TQFP(1,2,3)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

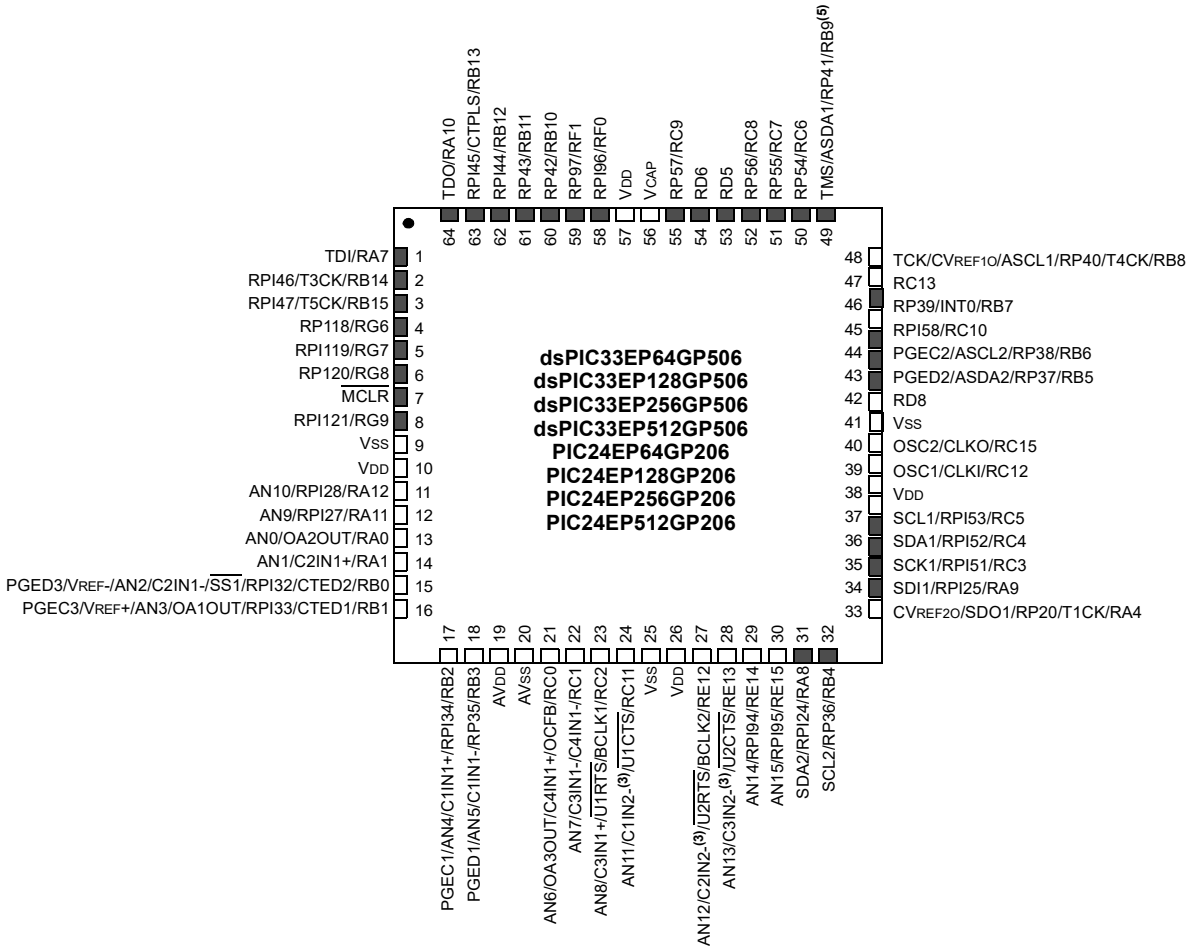
**3:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**4:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

## Pin Diagrams (Continued)

**64-Pin QFN(1,2,3,4)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** This pin is not available as an input when OPMODE (CMxCON[10]) = 1.

**4:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

**5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.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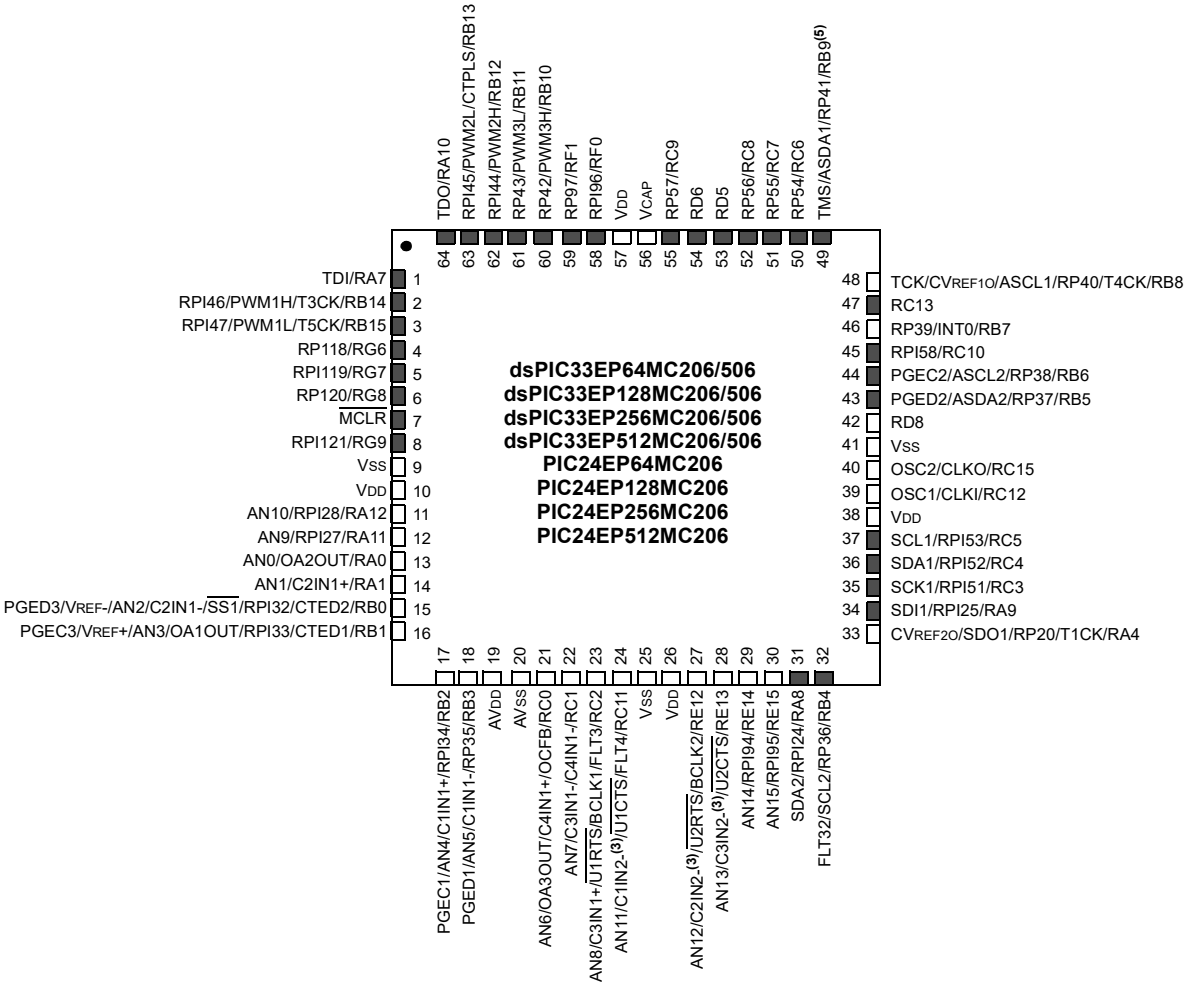
## Pin Diagrams (Continued)

**64-Pin QFN(1,2,3,4)**

■ = Pins are up to 5V tolerant




**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** This pin is not available as an input when OPMODE (CMxCON[10]) = 1.

**4:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

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## Referenced Sources

This device data sheet is based on the following individual chapters of the *"dsPIC33/PIC24 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

**Note 1:** To access the documents listed below, browse to the documentation section of the dsPIC33EP64MC506 product page of the Microchip website (www.microchip.com) or select a family reference manual section from the following list.

In addition to parameters, features and other documentation, the resulting page provides links to the related family reference manual sections.

- **"Introduction"** (www.microchip.com/DS70573)
- **"CPU"** (www.microchip.com/DS70359)
- **"Data Memory"** (www.microchip.com/DS70595)
- **"dsPIC33/PIC24 Program Memory"** (www.microchip.com/DS70000613)
- **"Flash Programming"** (www.microchip.com/DS70000609)
- **"Interrupts"** (www.microchip.com/DS70000600)
- **"Oscillator"** (www.microchip.com/DS70580)
- **"Reset"** (www.microchip.com/DS70602)
- **"Watchdog Timer and Power-Saving Modes"** (www.microchip.com/DS70615)
- **"I/O Ports"** (www.microchip.com/DS70000598)
- **"Timers"** (www.microchip.com/DS70362)
- **"Input Capture with Dedicated Timer"** (www.microchip.com/DS70000352)
- **"Output Compare"** (www.microchip.com/DS70000358)
- **"High-Speed PWM"** (www.microchip.com/DS70645)
- **"Quadrature Encoder Interface (QEI)"** (www.microchip.com/DS70000601)
- **"Analog-to-Digital Converter (ADC)"** (www.microchip.com/DS70621)
- **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582)
- **"Serial Peripheral Interface (SPI)"** (www.microchip.com/DS70005185)
- **"Inter-Integrated Circuit ($I^2C$)"** (www.microchip.com/DS70000195)
- **"Enhanced Controller Area Network (ECAN™)"** (www.microchip.com/DS70353)
- **"Direct Memory Access (DMA)"** (www.microchip.com/DS70348)
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- **"Programming and Diagnostics"** (www.microchip.com/DS70608)
- **"Op Amp/Comparator"** (www.microchip.com/DS70000357)
- **"Programmable Cyclic Redundancy Check (CRC)"** (www.microchip.com/DS70346)
- **"Device Configuration"** (www.microchip.com/DS70000618)
- **"Peripheral Trigger Generator (PTG)"** (www.microchip.com/DS70000669)
- **"Charge Time Measurement Unit (CTMU)"** (www.microchip.com/DS70661)


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## 1.0 DEVICE OVERVIEW

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive resource. To complement the information in this data sheet, refer to the related section of the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip website (www.microchip.com)

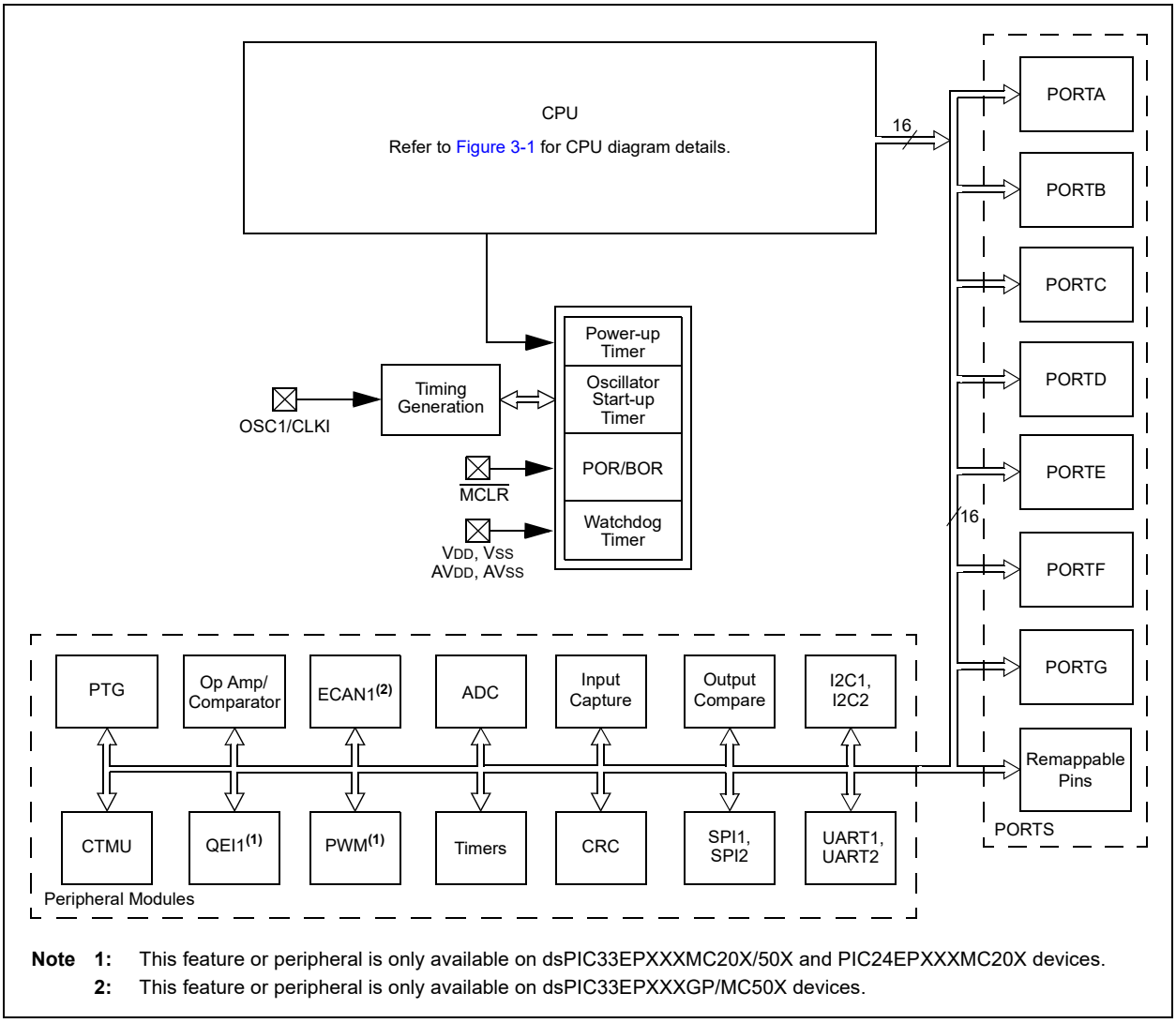
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

This document contains device-specific information for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Digital Signal Controller (DSC) and Microcontroller (MCU) devices.

dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices contain extensive Digital Signal Processor (DSP) functionality with a high-performance, 16-bit MCU architecture.

Figure 1-1 shows a general block diagram of the core and peripheral modules. Table 1-1 lists the functions of the various pins shown in the pinout diagrams.

**FIGURE 1-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X BLOCK DIAGRAM**




**Note 1:** This feature or peripheral is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**2:** This feature or peripheral is only available on dsPIC33EPXXXGP/MC50X devices.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS**

| Pin Name[(4)] | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| AN0-AN15 | I | Analog | No | Analog input channels. |
| CLKI | I | ST/ CMOS | No | External clock source input. Always associated with OSC1 pin function. |
| CLKO | O | — | No | Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. Always associated with OSC2 pin function. |
| OSC1<br><br>OSC2 | I<br><br>I/O | ST/ CMOS<br><br>— | No<br><br>No | Oscillator crystal input. ST buffer when configured in RC mode; CMOS otherwise.<br>Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. Optionally functions as CLKO in RC and EC modes. |
| REFCLKO | O | — | Yes | Reference clock output. |
| IC1-IC4 | I | ST | Yes | Capture Inputs 1 through 4. |
| OCFA<br>OCFB<br>OC1-OC4 | I<br>I<br>O | ST<br>ST<br>— | Yes<br>No<br>Yes | Compare Fault A input (for Compare channels).<br>Compare Fault B input (for Compare channels).<br>Compare Outputs 1 through 4. |
| INT0<br>INT1<br>INT2 | I<br>I<br>I | ST<br>ST<br>ST | No<br>Yes<br>Yes | External Interrupt 0.<br>External Interrupt 1.<br>External Interrupt 2. |
| RA0-RA4, RA7-RA12 | I/O | ST | No | PORTA is a bidirectional I/O port. |
| RB0-RB15 | I/O | ST | No | PORTB is a bidirectional I/O port. |
| RC0-RC13, RC15 | I/O | ST | No | PORTC is a bidirectional I/O port. |
| RD5, RD6, RD8 | I/O | ST | No | PORTD is a bidirectional I/O port. |
| RE12-RE15 | I/O | ST | No | PORTE is a bidirectional I/O port. |
| RF0, RF1 | I/O | ST | No | PORTF is a bidirectional I/O port. |
| RG6-RG9 | I/O | ST | No | PORTG is a bidirectional I/O port. |
| T1CK<br>T2CK<br>T3CK<br>T4CK<br>T5CK | I<br>I<br>I<br>I<br>I | ST<br>ST<br>ST<br>ST<br>ST | No<br>Yes<br>No<br>No<br>No | Timer1 external clock input.<br>Timer2 external clock input.<br>Timer3 external clock input.<br>Timer4 external clock input.<br>Timer5 external clock input. |
| CTPLS<br>CTED1<br>CTED2 | O<br>I<br>I | ST<br>ST<br>ST | No<br>No<br>No | CTMU pulse output.<br>CTMU External Edge Input 1.<br>CTMU External Edge Input 2. |
| $\overline{\text{U1CTS}}$<br>$\overline{\text{U1RTS}}$<br>U1RX<br>U1TX<br>BCLK1 | I<br>O<br>I<br>O<br>O | ST<br>—<br>ST<br>—<br>ST | No<br>No<br>Yes<br>Yes<br>No | UART1 Clear-to-Send.<br>UART1 Ready-to-Send.<br>UART1 receive.<br>UART1 transmit.<br>UART1 IrDA® baud clock output. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.

**3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"** for more information.

**4:** Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

**5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.


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**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name[4] | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| U2CTS | I | ST | No | UART2 Clear-to-Send. |
| U2RTS | O | — | No | UART2 Ready-to-Send. |
| U2RX | I | ST | Yes | UART2 receive. |
| U2TX | O | — | Yes | UART2 transmit. |
| BCLK2 | O | ST | No | UART2 IrDA® baud clock output. |
| SCK1 | I/O | ST | No | Synchronous serial clock input/output for SPI1. |
| SDI1 | I | ST | No | SPI1 data in. |
| SDO1 | O | — | No | SPI1 data out. |
| SS1 | I/O | ST | No | SPI1 slave synchronization or frame pulse I/O. |
| SCK2 | I/O | ST | Yes | Synchronous serial clock input/output for SPI2. |
| SDI2 | I | ST | Yes | SPI2 data in. |
| SDO2 | O | — | Yes | SPI2 data out. |
| SS2 | I/O | ST | Yes | SPI2 slave synchronization or frame pulse I/O. |
| SCL1 | I/O | ST | No | Synchronous serial clock input/output for I2C1. |
| SDA1 | I/O | ST | No | Synchronous serial data input/output for I2C1. |
| ASCL1 | I/O | ST | No | Alternate synchronous serial clock input/output for I2C1. |
| ASDA1 | I/O | ST | No | Alternate synchronous serial data input/output for I2C1. |
| SCL2 | I/O | ST | No | Synchronous serial clock input/output for I2C2. |
| SDA2 | I/O | ST | No | Synchronous serial data input/output for I2C2. |
| ASCL2 | I/O | ST | No | Alternate synchronous serial clock input/output for I2C2. |
| ASDA2 | I/O | ST | No | Alternate synchronous serial data input/output for I2C2. |
| TMS[5] | I | ST | No | JTAG Test mode select pin. |
| TCK | I | ST | No | JTAG test clock input pin. |
| TDI | I | ST | No | JTAG test data input pin. |
| TDO | O | — | No | JTAG test data output pin. |
| C1RX[2] | I | ST | Yes | ECAN1 bus receive pin. |
| C1TX[2] | O | — | Yes | ECAN1 bus transmit pin. |
| FLT1[1], FLT2[1] | I | ST | Yes | PWM Fault Inputs 1 and 2. |
| FLT3[1], FLT4[1] | I | ST | No | PWM Fault Inputs 3 and 4. |
| FLT32[1,3] | I | ST | No | PWM Fault Input 32 (Class B Fault). |
| DTCMP1-DTCMP3[1] | I | ST | Yes | PWM Dead-Time Compensation Inputs 1 through 3. |
| PWM1L-PWM3L[1] | O | — | No | PWM Low Outputs 1 through 3. |
| PWM1H-PWM3H[1] | O | — | No | PWM High Outputs 1 through 3. |
| SYNCI1[1] | I | ST | Yes | PWM Synchronization Input 1. |
| SYNCO1[1] | O | — | Yes | PWM Synchronization Output 1. |
| INDX1[1] | I | ST | Yes | Quadrature Encoder Index1 pulse input. |
| HOME1[1] | I | ST | Yes | Quadrature Encoder Home1 pulse input. |
| QEA1[1] | I | ST | Yes | Quadrature Encoder Phase A input in QEI1 mode. Auxiliary timer external clock/gate input in Timer mode. |
| QEB1[1] | I | ST | Yes | Quadrature Encoder Phase B input in QEI1 mode. Auxiliary timer external clock/gate input in Timer mode. |
| CNTCMP1[1] | O | — | Yes | Quadrature Encoder Compare Output 1. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.

**3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"** for more information.

**4:** Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

**5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name[4] | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| C1IN1-<br>C1IN2-<br>C1IN1+<br>OA1OUT<br>C1OUT | I<br>I<br>I<br>O<br>O | Analog<br>Analog<br>Analog<br>Analog<br>— | No<br>No<br>No<br>No<br>Yes | Op Amp/Comparator 1 Negative Input 1.<br>Comparator 1 Negative Input 2.<br>Op Amp/Comparator 1 Positive Input 1.<br>Op Amp 1 output.<br>Comparator 1 output. |
| C2IN1-<br>C2IN2-<br>C2IN1+<br>OA2OUT<br>C2OUT | I<br>I<br>I<br>O<br>O | Analog<br>Analog<br>Analog<br>Analog<br>— | No<br>No<br>No<br>No<br>Yes | Op Amp/Comparator 2 Negative Input 1.<br>Comparator 2 Negative Input 2.<br>Op Amp/Comparator 2 Positive Input 1.<br>Op Amp 2 output.<br>Comparator 2 output. |
| C3IN1-<br>C3IN2-<br>C3IN1+<br>OA3OUT<br>C3OUT | I<br>I<br>I<br>O<br>O | Analog<br>Analog<br>Analog<br>Analog<br>— | No<br>No<br>No<br>No<br>Yes | Op Amp/Comparator 3 Negative Input 1.<br>Comparator 3 Negative Input 2.<br>Op Amp/Comparator 3 Positive Input 1.<br>Op Amp 3 output.<br>Comparator 3 output. |
| C4IN1-<br>C4IN1+<br>C4OUT | I<br>I<br>O | Analog<br>Analog<br>— | No<br>No<br>Yes | Comparator 4 Negative Input 1.<br>Comparator 4 Positive Input 1.<br>Comparator 4 output. |
| CVREF1O<br>CVREF2O | O<br>O | Analog<br>Analog | No<br>No | Op amp/comparator voltage reference output.<br>Op amp/comparator voltage reference divided by 2 output. |
| PGED1<br>PGEC1<br>PGED2<br>PGEC2<br>PGED3<br>PGEC3 | I/O<br>I<br>I/O<br>I<br>I/O<br>I | ST<br>ST<br>ST<br>ST<br>ST<br>ST | No<br>No<br>No<br>No<br>No<br>No | Data I/O pin for Programming/Debugging Communication Channel 1.<br>Clock input pin for Programming/Debugging Communication Channel 1.<br>Data I/O pin for Programming/Debugging Communication Channel 2.<br>Clock input pin for Programming/Debugging Communication Channel 2.<br>Data I/O pin for Programming/Debugging Communication Channel 3.<br>Clock input pin for Programming/Debugging Communication Channel 3. |
| $\overline{\text{MCLR}}$ | I/P | ST | No | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| AVDD | P | P | No | Positive supply for analog modules. This pin must be connected at all times. |
| AVSS | P | P | No | Ground reference for analog modules. This pin must be connected at all times. |
| VDD | P | — | No | Positive supply for peripheral logic and I/O pins. |
| VCAP | P | — | No | CPU logic filter capacitor connection. |
| VSS | P | — | No | Ground reference for logic and I/O pins. |
| VREF+ | I | Analog | No | Analog voltage reference (high) input. |
| VREF- | I | Analog | No | Analog voltage reference (low) input. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**Note 1:** This pin is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** This pin is available on dsPIC33EPXXXGP/MC50X devices only.

**3:** This is the default Fault on Reset for dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices. See **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"** for more information.

**4:** Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

**5:** There is an internal pull-up resistor connected to the TMS pin when the JTAG interface is active. See the JTAGEN bit field in Table 27-2.


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# 2.0 GUIDELINES FOR GETTING STARTED WITH 16-BIT DIGITAL SIGNAL CONTROLLERS AND MICROCONTROLLERS

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip website (www.microchip.com)

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

## 2.1 Basic Connection Requirements

Getting started with the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins (regardless if ADC module is not used) (see **Section 2.2 "Decoupling Capacitors"**)
- VCAP (see **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.4 "Master Clear (MCLR) Pin"**)
- PGECx/PGEDx pins used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins when external oscillator source is used (see **Section 2.6 "External Oscillator Pins"**)

Additionally, the following pins may be required:

- VREF+/VREF- pins are used when external voltage reference for the ADC module is implemented

**Note:** The AVDD and AVSS pins must be connected, independent of the ADC voltage reference source.

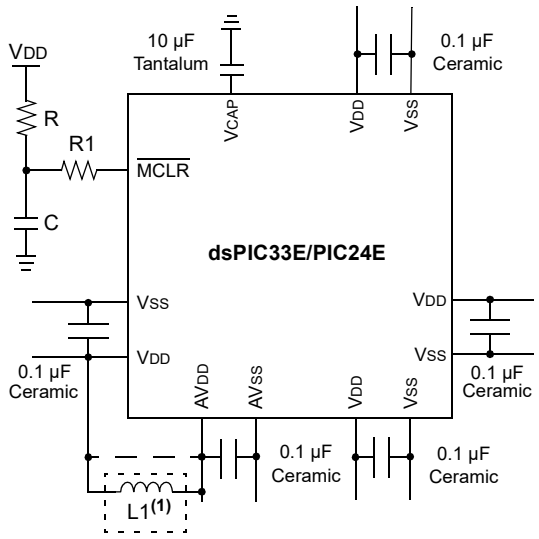
## 2.2 Decoupling Capacitors

The use of decoupling capacitors on every pair of power supply pins, such as VDD, VSS, AVDD and AVSS is required.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** Recommendation of 0.1 µF (100 nF), 10-20V. This capacitor should be a low-ESR and have resonance frequency in the range of 20 MHz and higher. It is recommended to use ceramic capacitors.
- **Placement on the Printed Circuit Board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended to place the capacitors on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, above tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

**FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION**




**Note 1:** As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{F_{CNV}}{2}$$ (i.e., ADC conversion rate/2)

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

### 2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

## 2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohm) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD and must have a capacitor greater than 4.7 µF (10 µF is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 30.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 27.3 "On-Chip Voltage Regulator"** for details.

## 2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

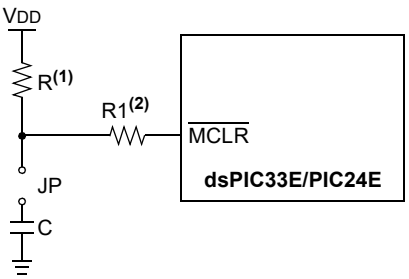
- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

**FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS**




**Note 1:** R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

**2:** R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor, C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.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## 2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes, and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High ($V_{IH}$) and Voltage Input Low ($V_{IL}$) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3 or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip website.

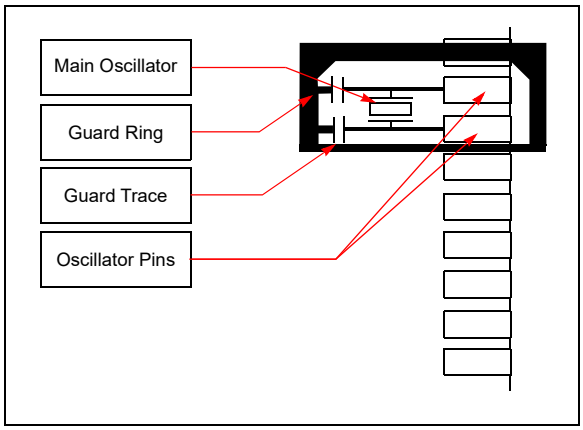
- *"Using MPLAB® ICD 3"* (poster) DS51765
- *"MPLAB® ICD 3 Design Advisory"* DS51764
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* DS51616
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) DS51749

## 2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator. For details, see **Section 9.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

**FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT**



## 2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to a certain frequency (see **Section 9.0 "Oscillator Configuration"**) to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLFBD, to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

## 2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between VSS and unused pins, and drive the output to logic low.

## 2.9 Application Examples

- Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- Compressor motor control
- Washing machine 3-phase motor control
- BLDC motor control
- Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- Audio and fluid sensor monitoring
- Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- Smart cards and smart card readers

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.

**FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION**

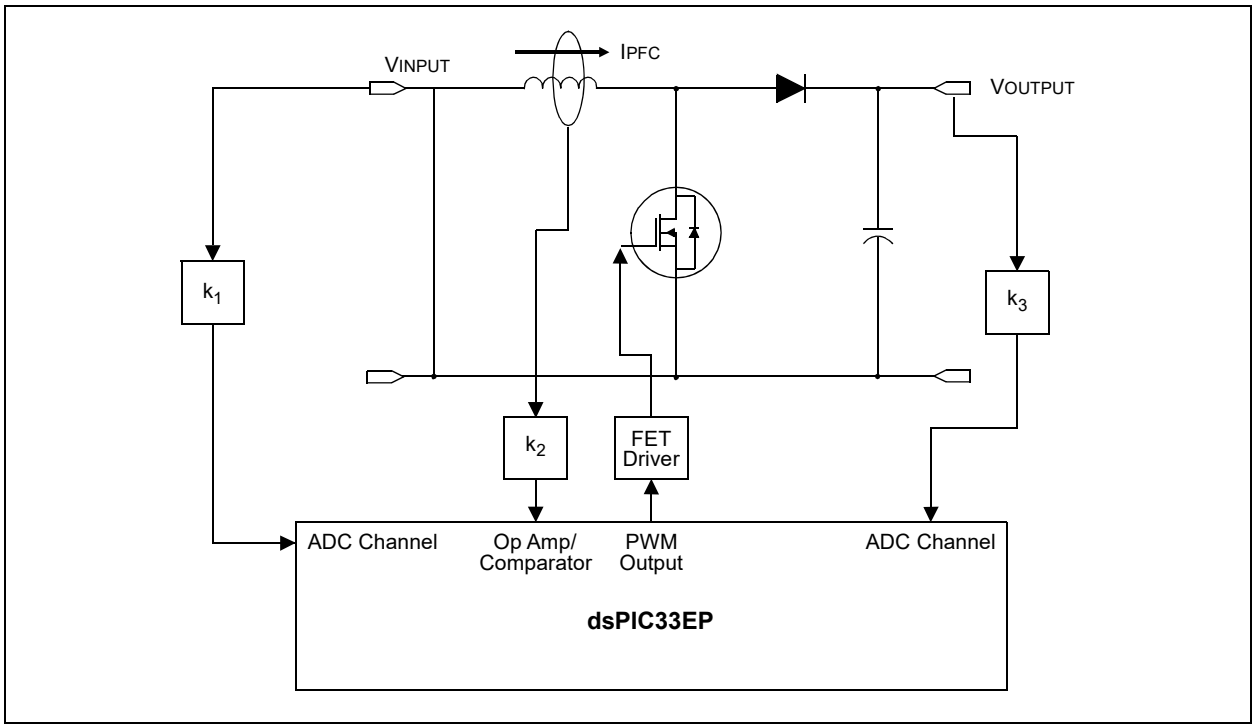




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**FIGURE 2-5: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER**

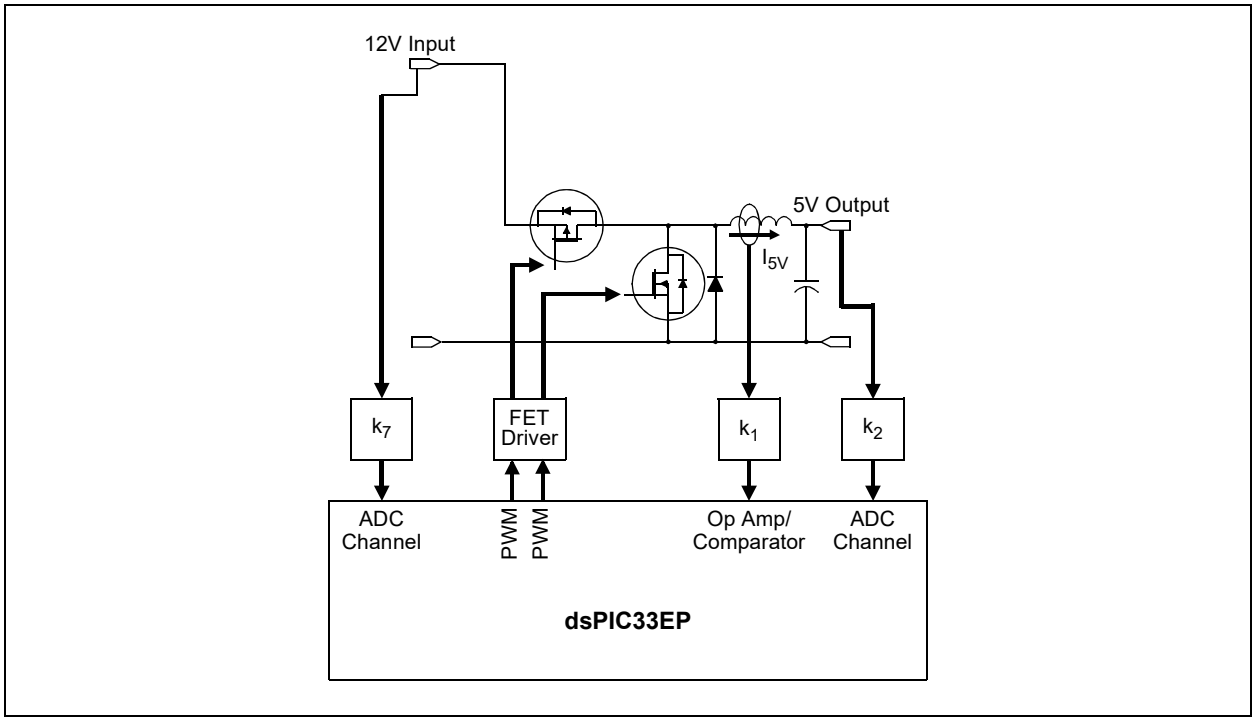



**FIGURE 2-6: MULTIPHASE SYNCHRONOUS BUCK CONVERTER**

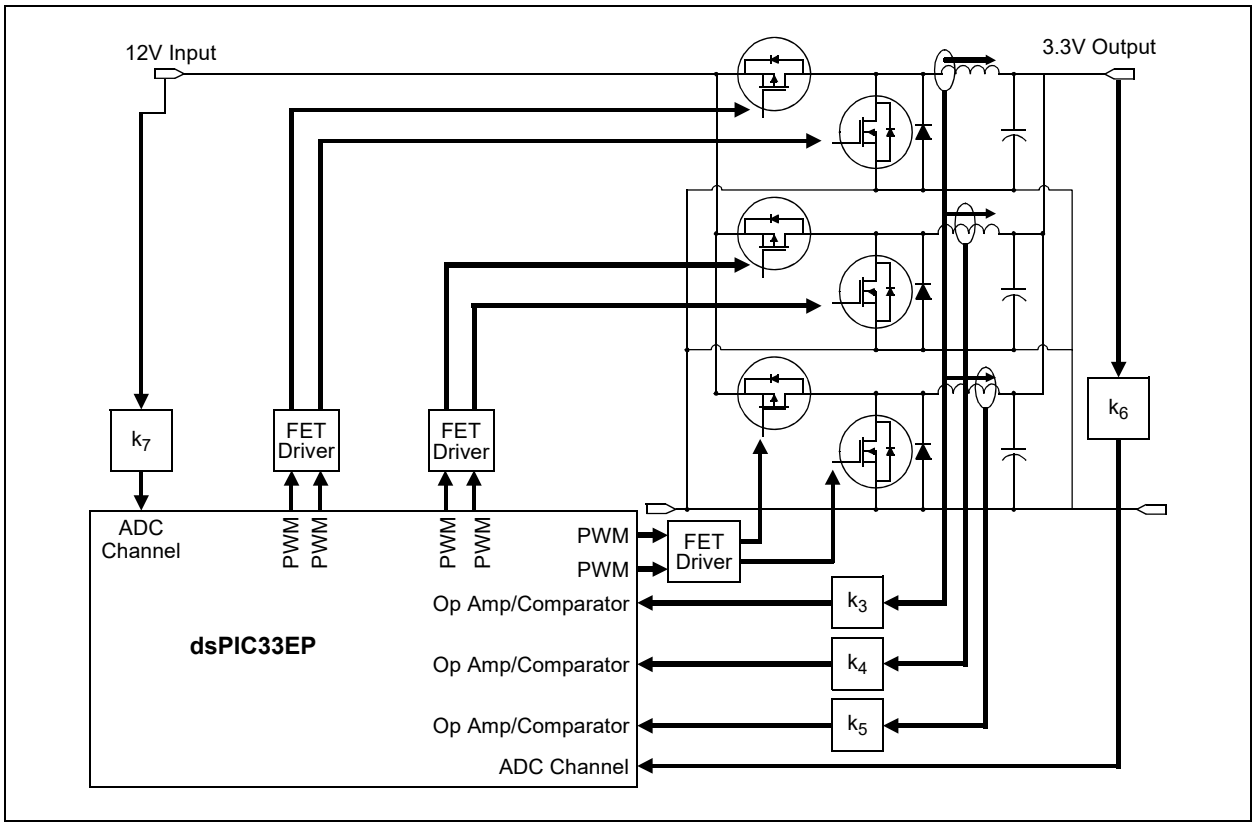


**FIGURE 2-7: INTERLEAVED PFC**

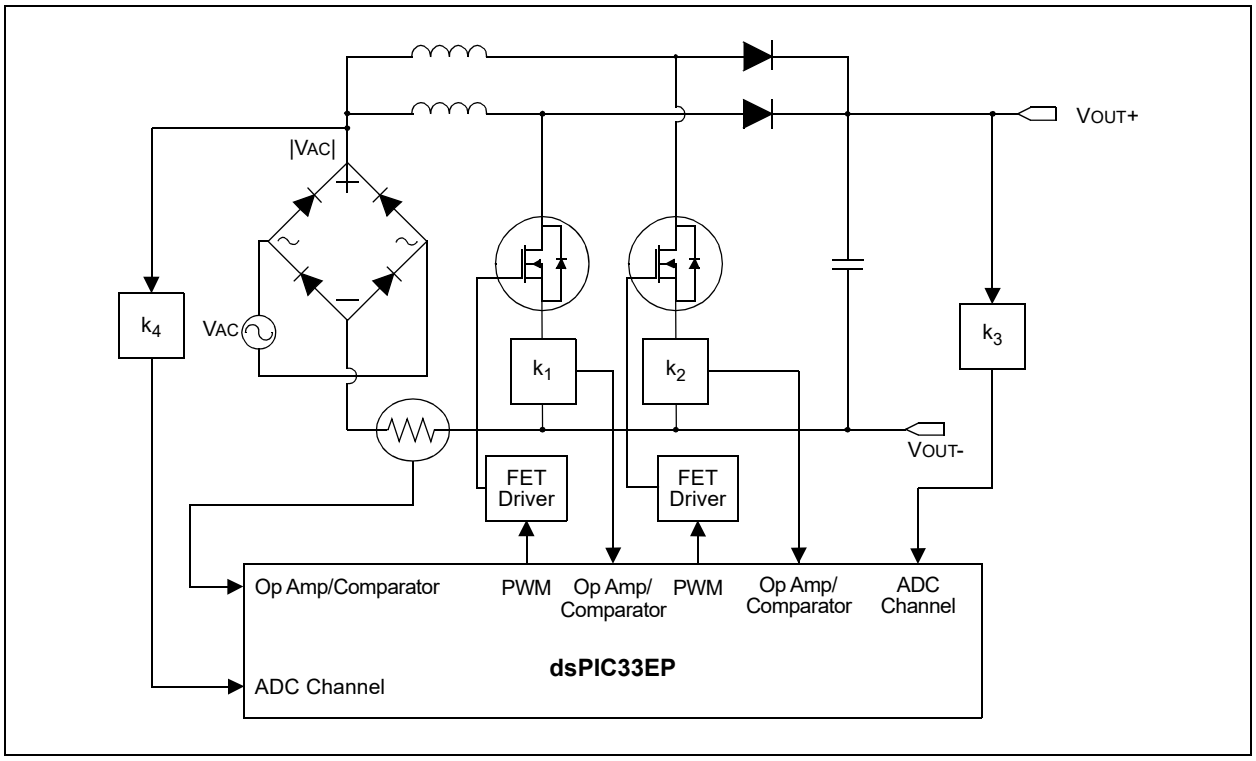
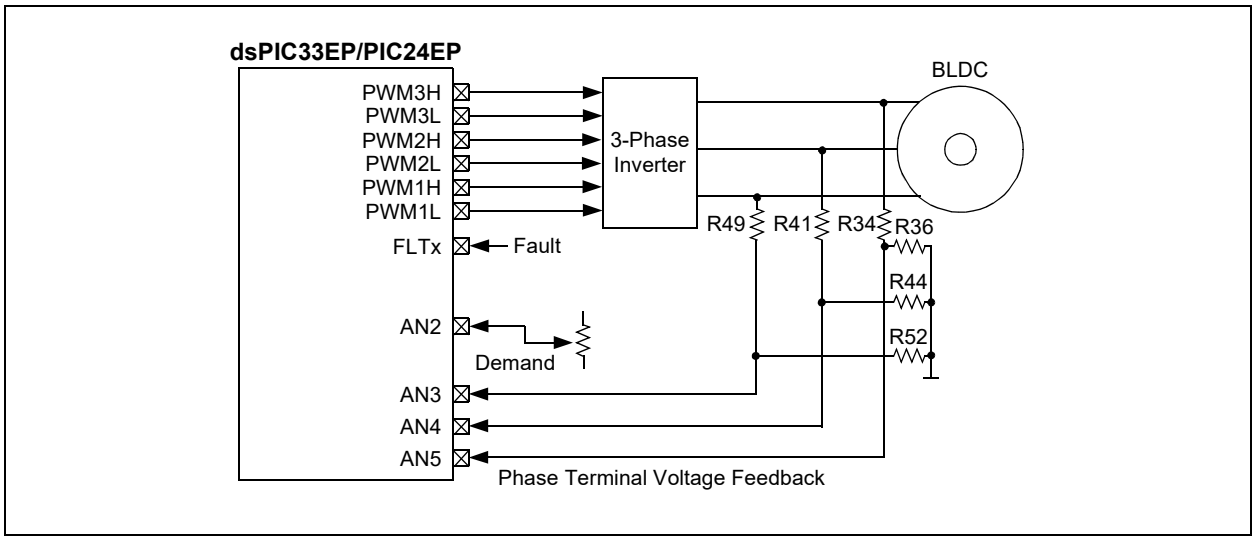



**FIGURE 2-8: BEMF VOLTAGE MEASURED USING THE ADC MODULE**





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# 3.0 CPU

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"CPU"** (www.microchip.com/DS70359) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle effective execution rate, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

## 3.1 Registers

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices have sixteen, 16-bit Working registers in the programmer's model. Each of the Working registers can act as a data, address or address offset register. The 16th Working register (W15) operates as a Software Stack Pointer (SSP) for interrupts and calls.

## 3.2 Instruction Set

The instruction set for dsPIC33EPXXXGP50X and dsPIC33EPXXXMC20X/50X devices has two classes of instructions: the MCU class of instructions and the DSP class of instructions. The instruction set for PIC24EPXXXGP/MC20X devices has the MCU class of instructions only and does not support DSP instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

## 3.3 Data Space Addressing

The base Data Space can be addressed as 64 Kbytes (32K words).

The Data Space includes two ranges of memory, referred to as X and Y data memory. Each memory range is accessible through its own independent Address Generation Unit (AGU). The MCU class of instructions operates solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Spaces have memory locations that are device-specific, and are described further in the data memory maps in **Section 4.2 "Data Address Space"**.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space (PS) at any 32-Kbyte aligned program word boundary. The Program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to the **"Data Memory"** (www.microchip.com/DS70595) and **"dsPIC33/PIC24 Program Memory"** (www.microchip.com/DS70000613) sections in the *"dsPIC33/PIC24 Family Reference Manual"* for more details on EDS, PSV and table accesses.

On the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU Circular Addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data re-ordering for radix-2 FFT algorithms. PIC24EPXXXGP/MC20X devices do not support Modulo and Bit-Reversed Addressing.

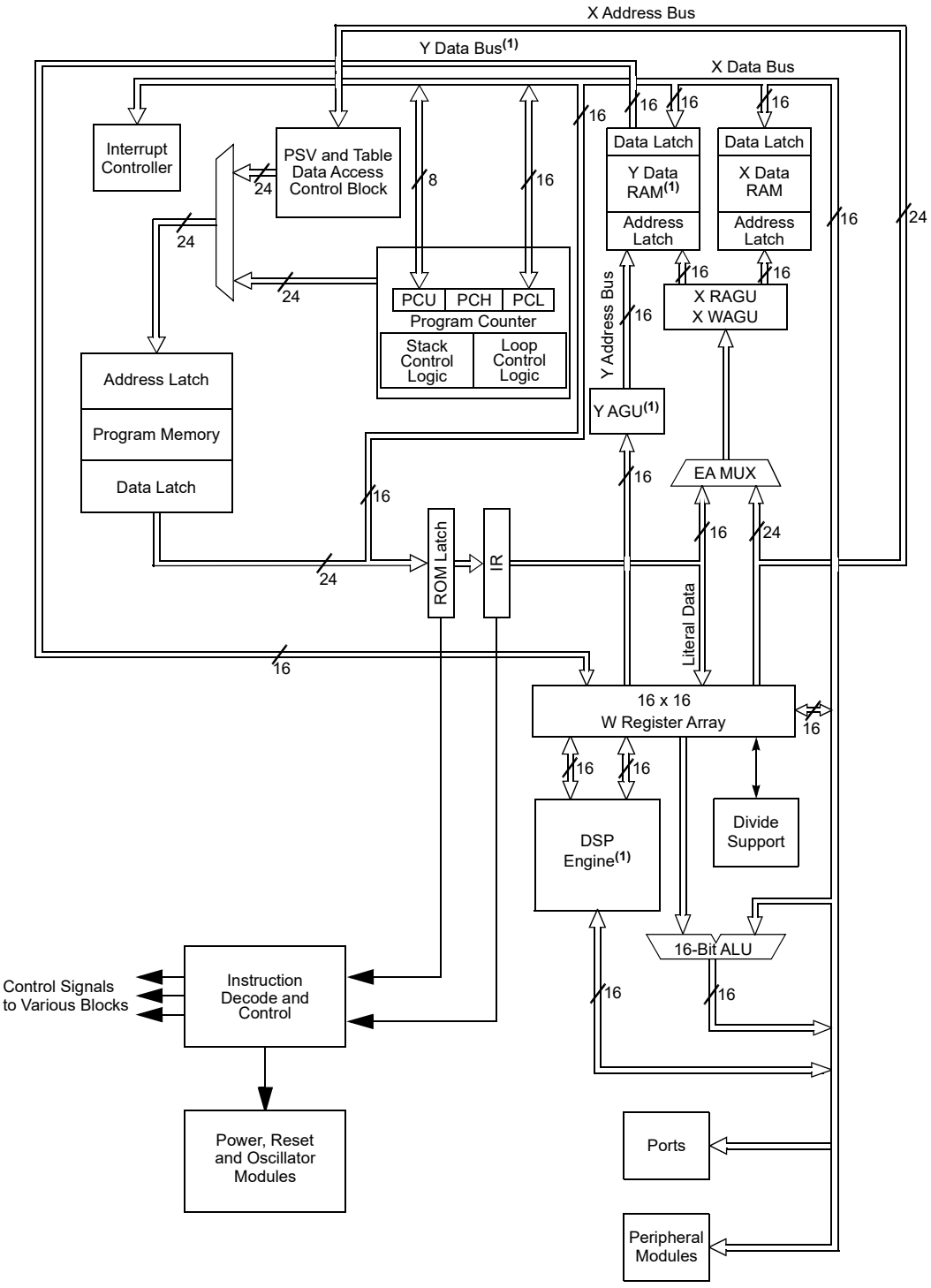
## 3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

**FIGURE 3-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X CPU BLOCK DIAGRAM**




**Note 1:** This feature is not available on PIC24EPXXXGP/MC20X devices.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## 3.5 Programmer's Model

The programmer's model for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X is shown in Figure 3-2. All registers in the programmer's model are memory-mapped and can be manipulated directly by instructions. Table 3-1 lists a description of each register.

In addition to the registers contained in the programmer's model, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain control registers for Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only), Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only) and interrupts. These registers are described in subsequent sections of this document.

All registers associated with the programmer's model are memory-mapped, as shown in Table 4-1.

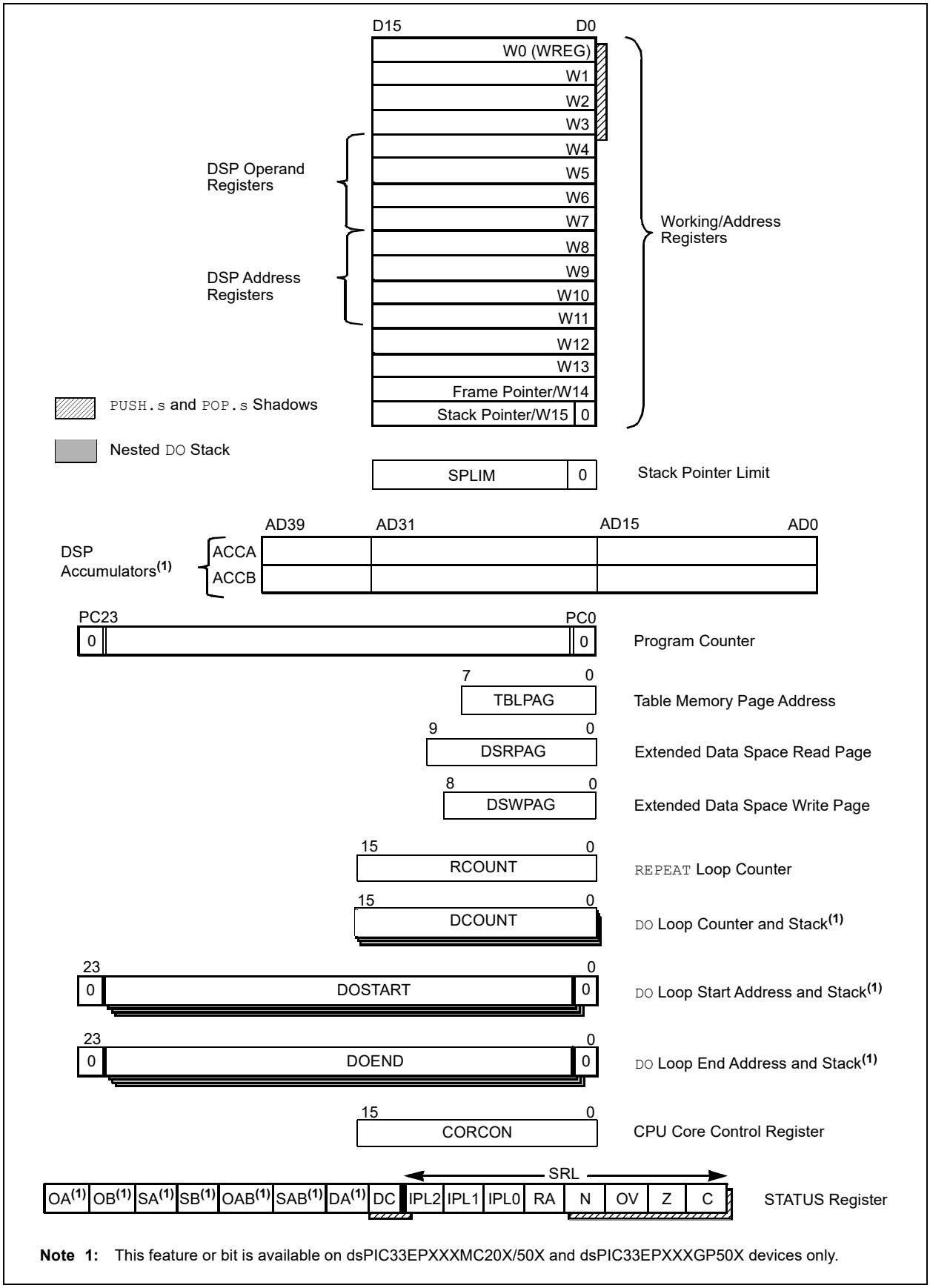
**TABLE 3-1: PROGRAMMER'S MODEL REGISTER DESCRIPTIONS**

| Register(s) Name | Description |
|---|---|
| W0 through W15 | Working Register Array |
| ACCA, ACCB | 40-Bit DSP Accumulators |
| PC | 23-Bit Program Counter |
| SR | ALU and DSP Engine STATUS Register |
| SPLIM | Stack Pointer Limit Value Register |
| TBLPAG | Table Memory Page Address Register |
| DSRPAG | Extended Data Space (EDS) Read Page Register |
| DSWPAG | Extended Data Space (EDS) Write Page Register |
| RCOUNT | REPEAT Loop Counter Register |
| DCOUNT(1) | DO Loop Counter Register |
| DOSTARTH(1,2), DOSTARTL(1,2) | DO Loop Start Address Register (High and Low) |
| DOENDH(1), DOENDL(1) | DO Loop End Address Register (High and Low) |
| CORCON | Contains DSP Engine, DO Loop Control and Trap Status bits |

**Note 1:** This register is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

**2:** The DOSTARTH and DOSTARTL registers are read-only.

**FIGURE 3-2: PROGRAMMER'S MODEL**




**Note 1:** This feature or bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.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## 3.6 CPU Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 3.6.1 KEY RESOURCES

- **"CPU"** (www.microchip.com/DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 3.7 CPU Control Registers

**REGISTER 3-1: SR: CPU STATUS REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/C-0 | R/C-0 | R-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OA(1) | OB(1) | SA(1,4) | SB(1,4) | OAB(1) | SAB(1) | DA(1) | DC |
| bit 15 | | | | | | | bit 8 |

| R/W-0(2,3) | R/W-0(2,3) | R/W-0(2,3) | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IPL2 | IPL1 | IPL0 | RA | N | OV | Z | C |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1'= Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **OA:** Accumulator A Overflow Status bit(1)
1 = Accumulator A has overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit(1)
1 = Accumulator B has overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit(1,4)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit(1,4)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit(1)
1 = Accumulators A or B have overflowed
0 = Neither Accumulators A or B have overflowed

bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit(1)
1 = Accumulators A or B are saturated or have been saturated at some time
0 = Neither Accumulators A or B are saturated

bit 9 **DA:** DO Loop Active bit(1)
1 = DO loop is in progress
0 = DO loop is not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

**Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

**2:** The IPL[2:0] bits are concatenated with the IPL[3] bit (CORCON[3]) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL[3] = 1. User interrupts are disabled when IPL[3] = 1.

**3:** The IPL[2:0] Status bits are read-only when the NSTDIS bit (INTCON1[15]) = 1.

**4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.


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**REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)**

bit 7-5 **IPL[2:0]:** CPU Interrupt Priority Level Status bits(2,3)
111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit
1 = REPEAT loop in progress
0 = REPEAT loop not in progress

bit 3 **N:** MCU ALU Negative bit
1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2 **OV:** MCU ALU Overflow bit
This bit is used for signed arithmetic (two's complement). It indicates an overflow of the magnitude that causes the sign bit to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = No overflow occurred

bit 1 **Z:** MCU ALU Zero bit
1 = An operation that affects the Z bit has set it at some time in the past
0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)

bit 0 **C:** MCU ALU Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

**Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

**2:** The IPL[2:0] bits are concatenated with the IPL[3] bit (CORCON[3]) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL[3] = 1. User interrupts are disabled when IPL[3] = 1.

**3:** The IPL[2:0] Status bits are read-only when the NSTDIS bit (INTCON1[15]) = 1.

**4:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

**REGISTER 3-2: CORCON: CORE CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VAR | — | US1(1) | US0(1) | EDT(1,2) | DL2(1) | DL1(1) | DL0(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SATA(1) | SATB(1) | SATDW(1) | ACCSAT(1) | IPL3(3) | SFA | RND(1) | IF(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing latency is enabled
0 = Fixed exception processing latency is enabled

bit 14 **Unimplemented:** Read as '0'

bit 13-12 **US[1:0]:** DSP Multiply Unsigned/Signed Control bits(1)
11 = Reserved
10 = DSP engine multiplies are mixed-sign
01 = DSP engine multiplies are unsigned
00 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit(1,2)
1 = Terminates executing DO loop at end of current loop iteration
0 = No effect

bit 10-8 **DL[2:0]:** DO Loop Nesting Level Status bits(1)
111 = Seven DO loops are active
•
•
•
001 = One DO loop is active
000 = Zero DO loops are active

bit 7 **SATA:** ACCA Saturation Enable bit(1)
1 = Accumulator A saturation is enabled
0 = Accumulator A saturation is disabled

bit 6 **SATB:** ACCB Saturation Enable bit(1)
1 = Accumulator B saturation is enabled
0 = Accumulator B saturation is disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit(1)
1 = Data Space write saturation is enabled
0 = Data Space write saturation is disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit(1)
1 = 9.31 saturation (super saturation)
0 = 1.31 saturation (normal saturation)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(3)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

**Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
**2:** This bit is always read as '0'.
**3:** The IPL3 bit is concatenated with the IPL[2:0] bits (SR[7:5]) to form the CPU Interrupt Priority Level.


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**REGISTER 3-2: CORCON: CORE CONTROL REGISTER (CONTINUED)**

bit 2 **SFA:** Stack Frame Active Status bit
1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1 **RND:** Rounding Mode Select bit(1)
1 = Biased (conventional) rounding is enabled
0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit(1)
1 = Integer mode is enabled for DSP multiply
0 = Fractional mode is enabled for DSP multiply

**Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.
**2:** This bit is always read as '0'.
**3:** The IPL3 bit is concatenated with the IPL[2:0] bits (SR[7:5]) to form the CPU Interrupt Priority Level.

## 3.8 Arithmetic Logic Unit (ALU)

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X ALU is 16 bits wide, and is capable of addition, subtraction, bit shifts and logic operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. Depending on the operation, the ALU can affect the values of the Carry (C), Zero (Z), Negative (N), Overflow (OV) and Digit Carry (DC) Status bits in the SR register. The C and DC Status bits operate as Borrow and Digit Borrow bits, respectively, for subtraction operations.

The ALU can perform 8-bit or 16-bit operations, depending on the mode of the instruction that is used. Data for the ALU operation can come from the W register array or data memory, depending on the addressing mode of the instruction. Likewise, output data from the ALU can be written to the W register array or a data memory location.

Refer to the *"16-Bit MCU and DSC Programmer's Reference Manual"* (DS70000157) for information on the SR bits affected by each instruction.

The core CPU incorporates hardware support for both multiplication and division. This includes a dedicated hardware multiplier and support hardware for 16-bit divisor division.

### 3.8.1 MULTIPLIER

Using the high-speed 17-bit x 17-bit multiplier, the ALU supports unsigned, signed, or mixed-sign operation in several MCU multiplication modes:

- 16-bit x 16-bit signed
- 16-bit x 16-bit unsigned
- 16-bit signed x 5-bit (literal) unsigned
- 16-bit signed x 16-bit unsigned
- 16-bit unsigned x 5-bit (literal) unsigned
- 16-bit unsigned x 16-bit signed
- 8-bit unsigned x 8-bit unsigned

### 3.8.2 DIVIDER

The divide block supports 32-bit/16-bit and 16-bit/16-bit signed and unsigned integer divide operations with the following data sizes:

- 32-bit signed/16-bit signed divide
- 32-bit unsigned/16-bit unsigned divide
- 16-bit signed/16-bit signed divide
- 16-bit unsigned/16-bit unsigned divide

The quotient for all divide instructions ends up in W0 and the remainder in W1. The 16-bit signed and unsigned `DIV` instructions can specify any W register for both the 16-bit divisor (Wn) and any W register (aligned) pair (W(m + 1):Wm) for the 32-bit dividend. The divide algorithm takes one cycle per bit of divisor, so both 32-bit/16-bit and 16-bit/16-bit instructions take the same number of cycles to execute.

## 3.9 DSP Engine (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

The DSP engine consists of a high-speed 17-bit x 17-bit multiplier, a 40-bit barrel shifter and a 40-bit adder/subtracter (with two target accumulators, round and saturation logic).

The DSP engine can also perform inherent accumulator-to-accumulator operations that require no additional data. These instructions are `ADD`, `SUB` and `NEG`.

The DSP engine has options selected through bits in the CPU Core Control register (CORCON), as listed below:

- Fractional or integer DSP multiply (IF)
- Signed, unsigned or mixed-sign DSP multiply (US)
- Conventional or convergent rounding (RND)
- Automatic saturation on/off for ACCA (SATA)
- Automatic saturation on/off for ACCB (SATB)
- Automatic saturation on/off for writes to data memory (SATDW)
- Accumulator Saturation mode selection (ACCSAT)

**TABLE 3-2: DSP INSTRUCTIONS SUMMARY**

| Instruction | Algebraic Operation | ACC Write Back |
|---|---|---|
| CLR | $A = 0$ | Yes |
| ED | $A = (x - y)^2$ | No |
| EDAC | $A = A + (x - y)^2$ | No |
| MAC | $A = A + (x \bullet y)$ | Yes |
| MAC | $A = A + x^2$ | No |
| MOVSAC | No change in A | Yes |
| MPY | $A = x \bullet y$ | No |
| MPY | $A = x^2$ | No |
| MPY.N | $A = -x \bullet y$ | No |
| MSC | $A = A - x \bullet y$ | Yes |


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# 4.0 MEMORY ORGANIZATION

**Note:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"dsPIC33/PIC24 Program Memory"** (www.microchip.com/DS70000613) in the "*dsPIC33/PIC24 Family Reference Manual*".

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture features separate program and data memory spaces, and buses. This architecture also allows the direct access of program memory from the Data Space (DS) during code execution.

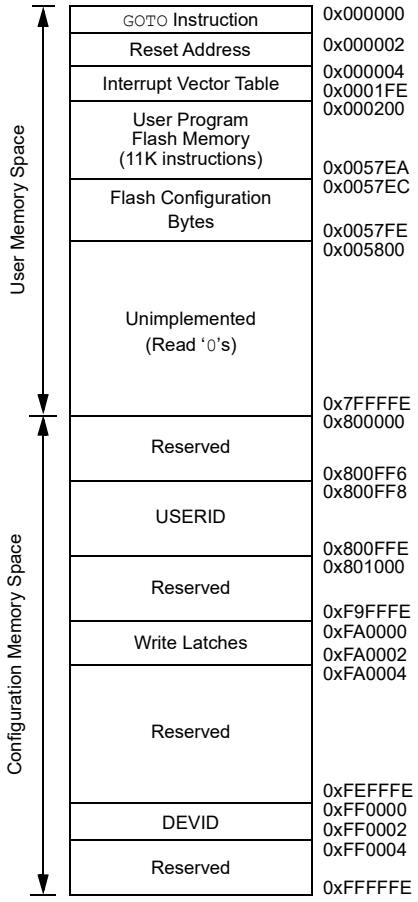
## 4.1 Program Address Space

The program address memory space of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices is 4M instructions. The space is addressable by a 24-bit value derived either from the 23-bit PC during program execution, or from table operation or Data Space remapping, as described in **Section 4.8 "Interfacing Program and Data Memory Spaces"**.

User application access to the program memory space is restricted to the lower half of the address range (0x000000 to 0x7FFFFF). The exception is the use of TBLRD operations, which use TBLPAG[7] to read Device ID sections of the configuration memory space.

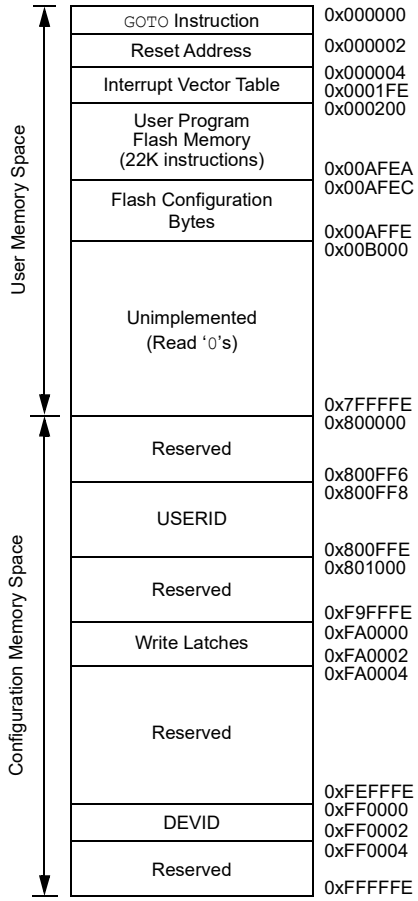
The program memory maps, which are presented by device family and memory size, are shown in Figure 4-1 through Figure 4-5.

**FIGURE 4-1: PROGRAM MEMORY MAP FOR dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X AND PIC24EP32GP/MC20X DEVICES**




**Note:** Memory areas are not shown to scale.

**FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X AND PIC24EP64GP/MC20X DEVICES**




**Note:** Memory areas are not shown to scale.


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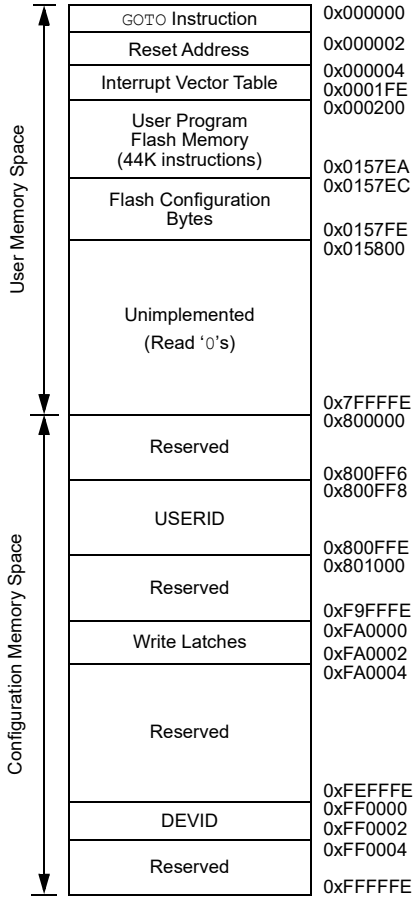
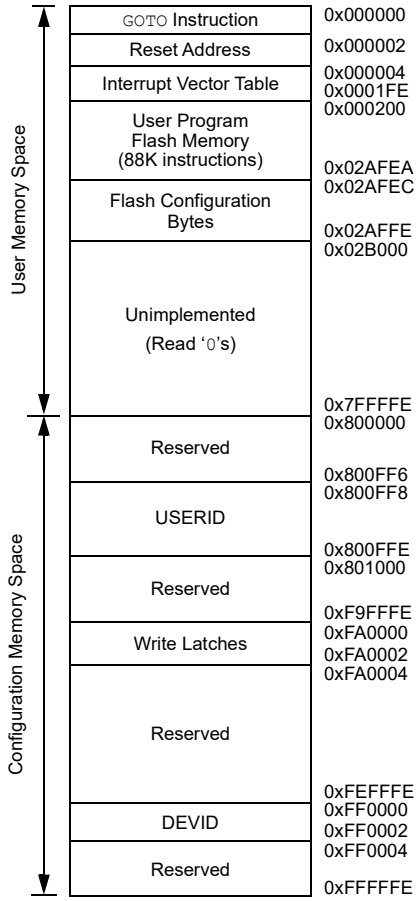
**FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EP128GP50X, dsPIC33EP128MC20X/50X AND PIC24EP128GP/MC20X DEVICES**




**Note:** Memory areas are not shown to scale.

**FIGURE 4-4: PROGRAM MEMORY MAP FOR dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X AND PIC24EP256GP/MC20X DEVICES**




**Note:** Memory areas are not shown to scale.


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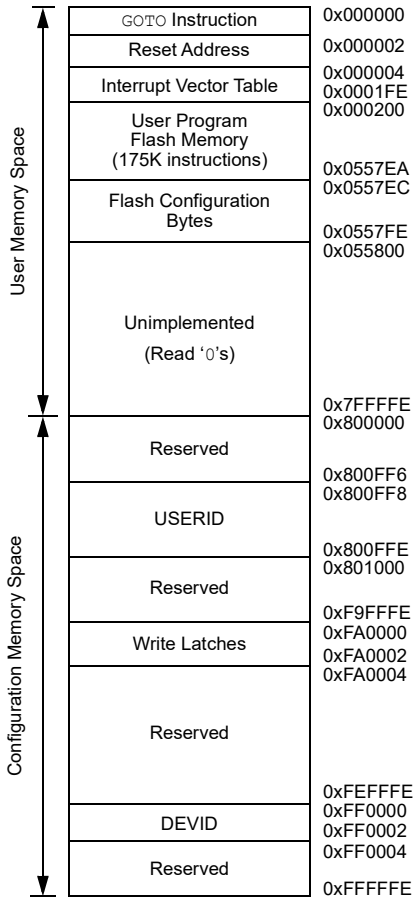
**FIGURE 4-5: PROGRAM MEMORY MAP FOR dsPIC33EP512GP50X, dsPIC33EP512MC20X/50X AND PIC24EP512GP/MC20X DEVICES**




**Note:** Memory areas are not shown to scale.

### 4.1.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in word-addressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-6).

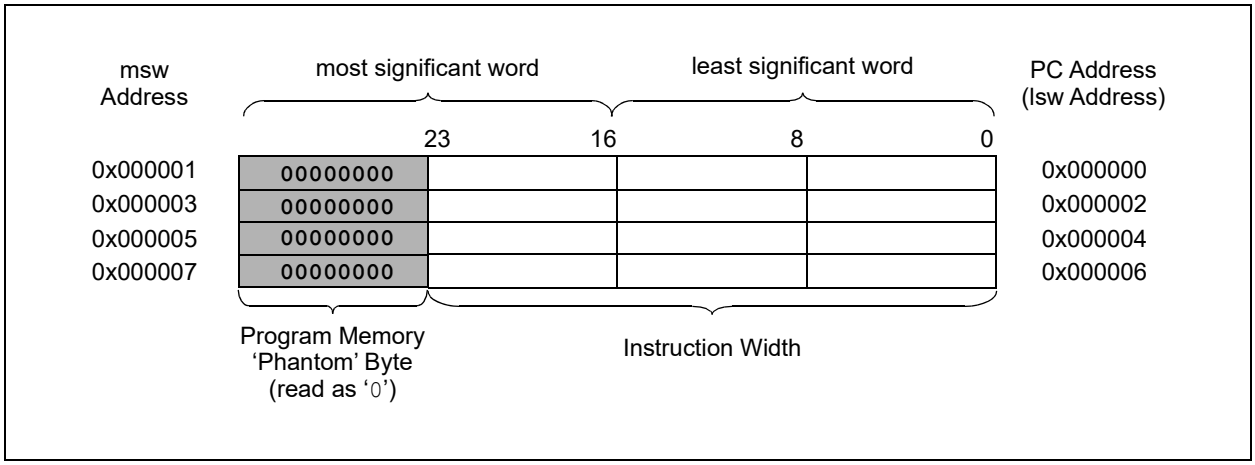
Program memory addresses are always word-aligned on the lower word and addresses are incremented, or decremented by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

### 4.1.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A `GOTO` instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 7.1 "Interrupt Vector Table"**.

**FIGURE 4-6: PROGRAM MEMORY ORGANIZATION**





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## 4.2 Data Address Space

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU has a separate 16-bit wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps, which are presented by device family and memory size, are shown in Figure 4-7 through Figure 4-16.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a base Data Space address range of 64 Kbytes (32K words).

The base Data Space address is used in conjunction with a Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space, which has a total address range of 16 Mbytes.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement up to 52 Kbytes of data memory (4 Kbytes of data memory for Special Function Registers and up to 48 Kbytes of data memory for RAM). If an EA points to a location outside of this area, an all-zero word or byte is returned.

### 4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit wide blocks. Data are aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

### 4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCU devices and improve Data Space memory usage efficiency, the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB. The MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

### 4.2.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X core and peripheral modules for controlling the operation of the device.

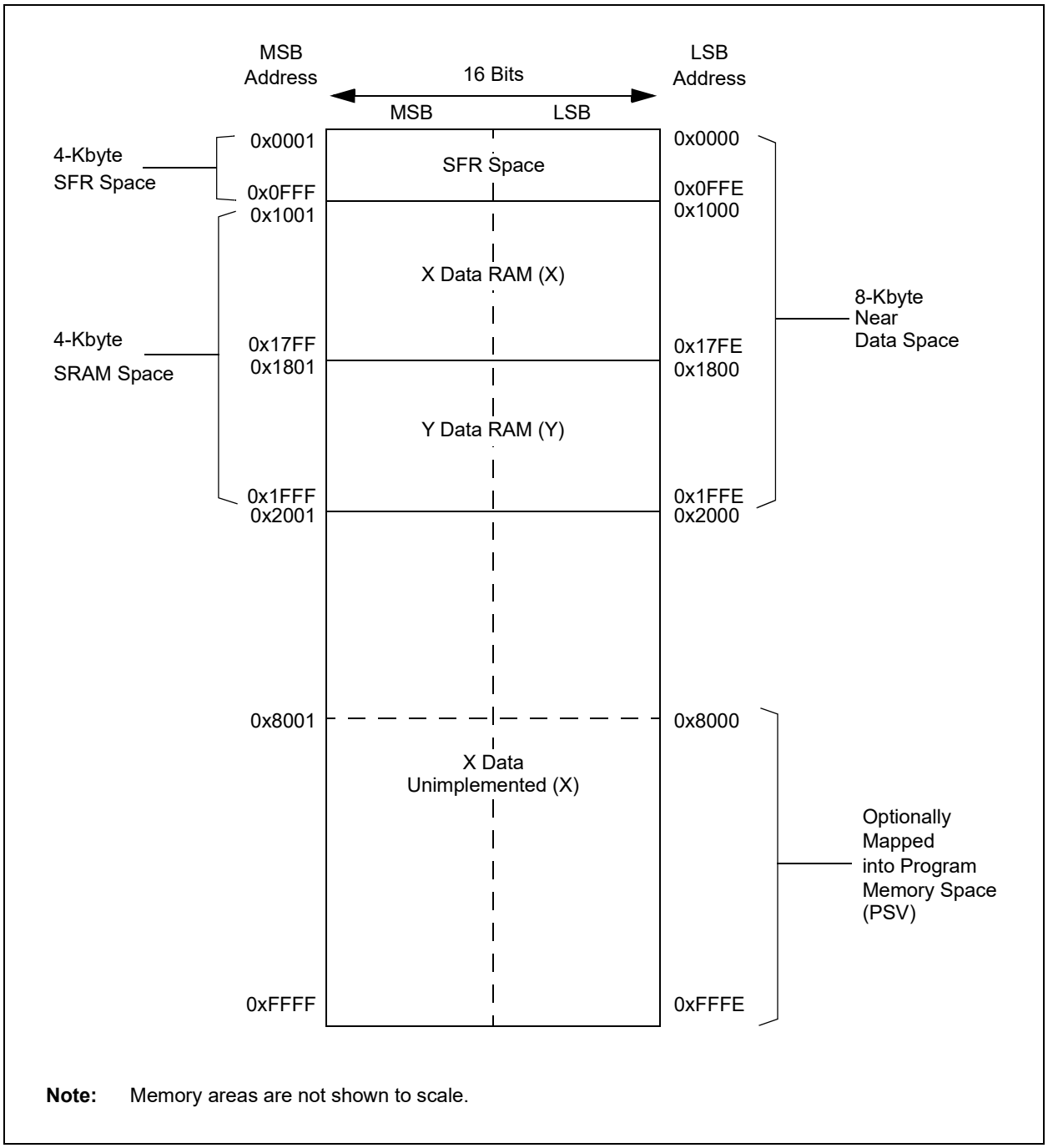
SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

| **Note:** | The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information. |
|---|---|

### 4.2.4 NEAR DATA SPACE

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a Working register as an Address Pointer.

**FIGURE 4-7: DATA MEMORY MAP FOR dsPIC33EP32MC20X/50X AND dsPIC33EP32GP50X DEVICES**




**Note:** Memory areas are not shown to scale.


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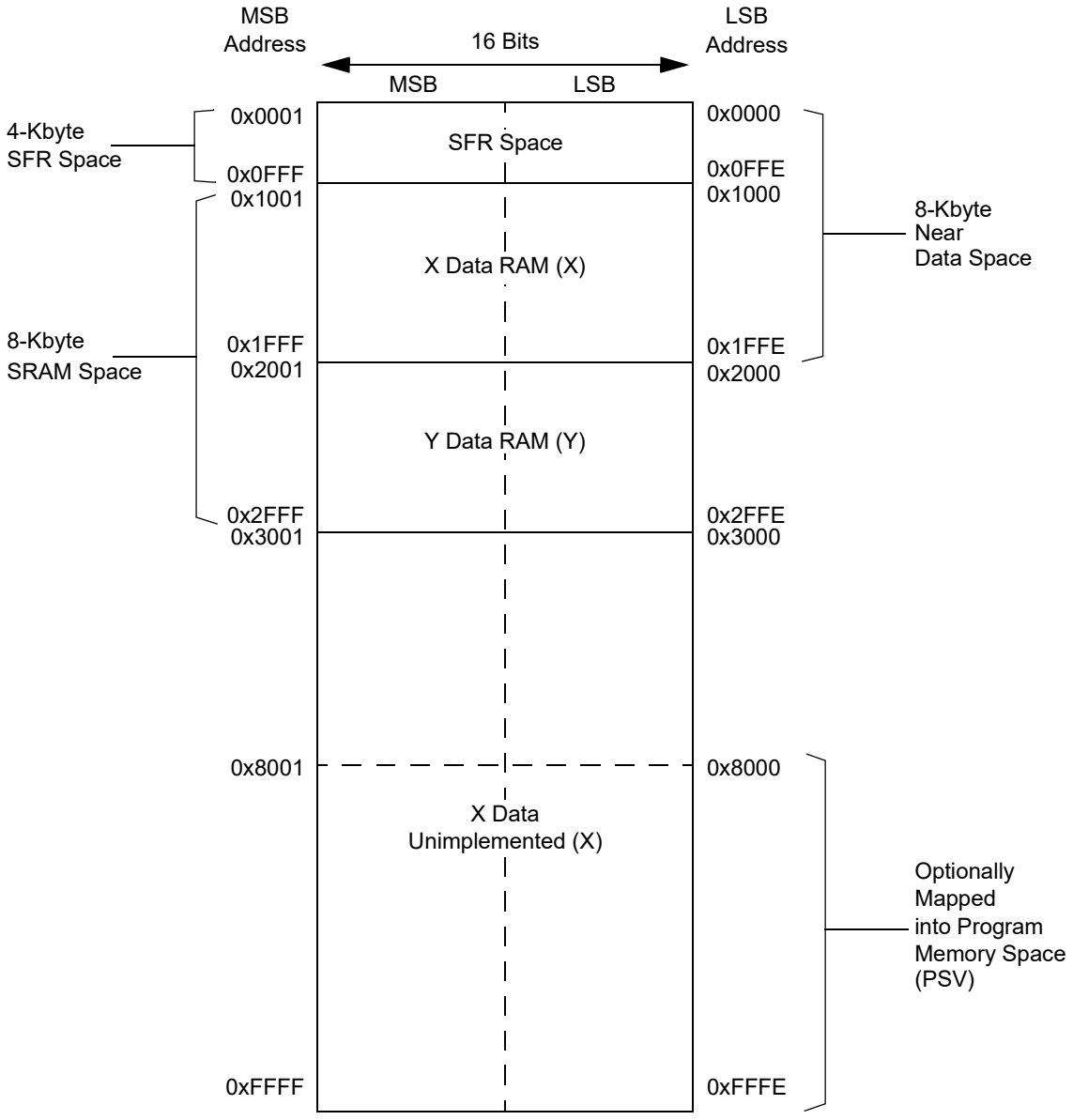
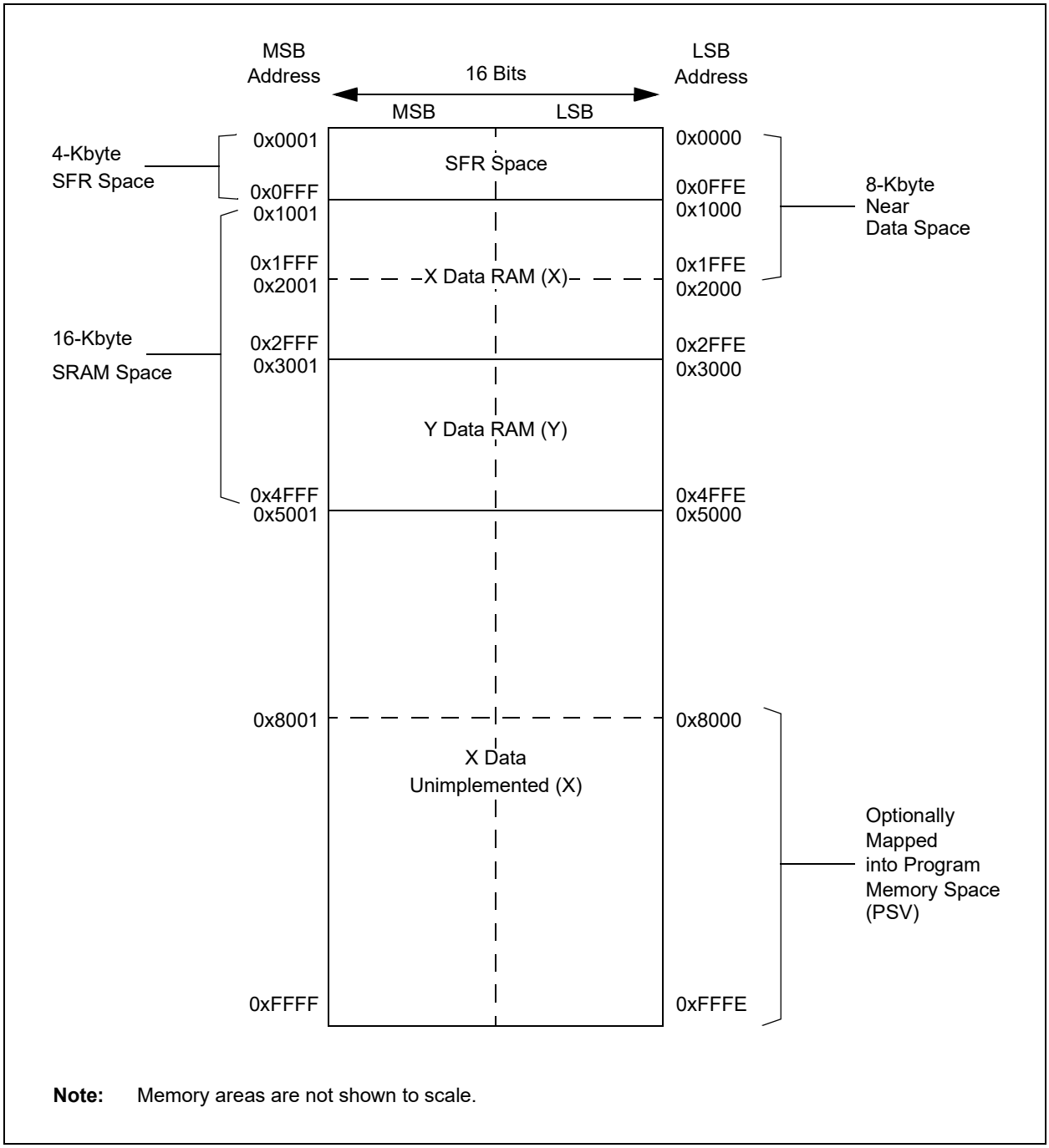
**FIGURE 4-8: DATA MEMORY MAP FOR dsPIC33EP64MC20X/50X AND dsPIC33EP64GP50X DEVICES**




**Note:** Memory areas are not shown to scale.

**FIGURE 4-9: DATA MEMORY MAP FOR dsPIC33EP128MC20X/50X AND dsPIC33EP128GP50X DEVICES**




**Note:** Memory areas are not shown to scale.


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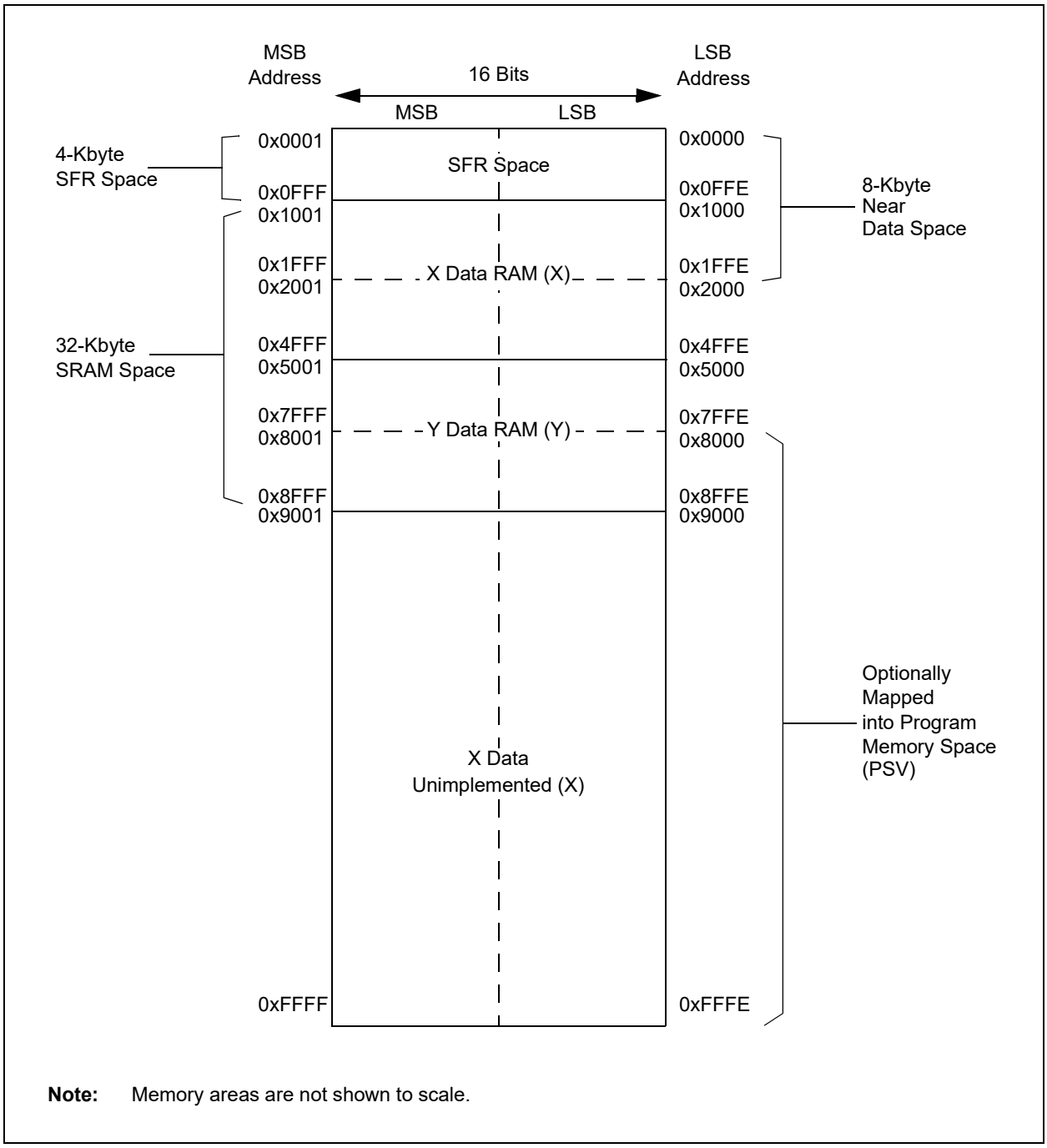
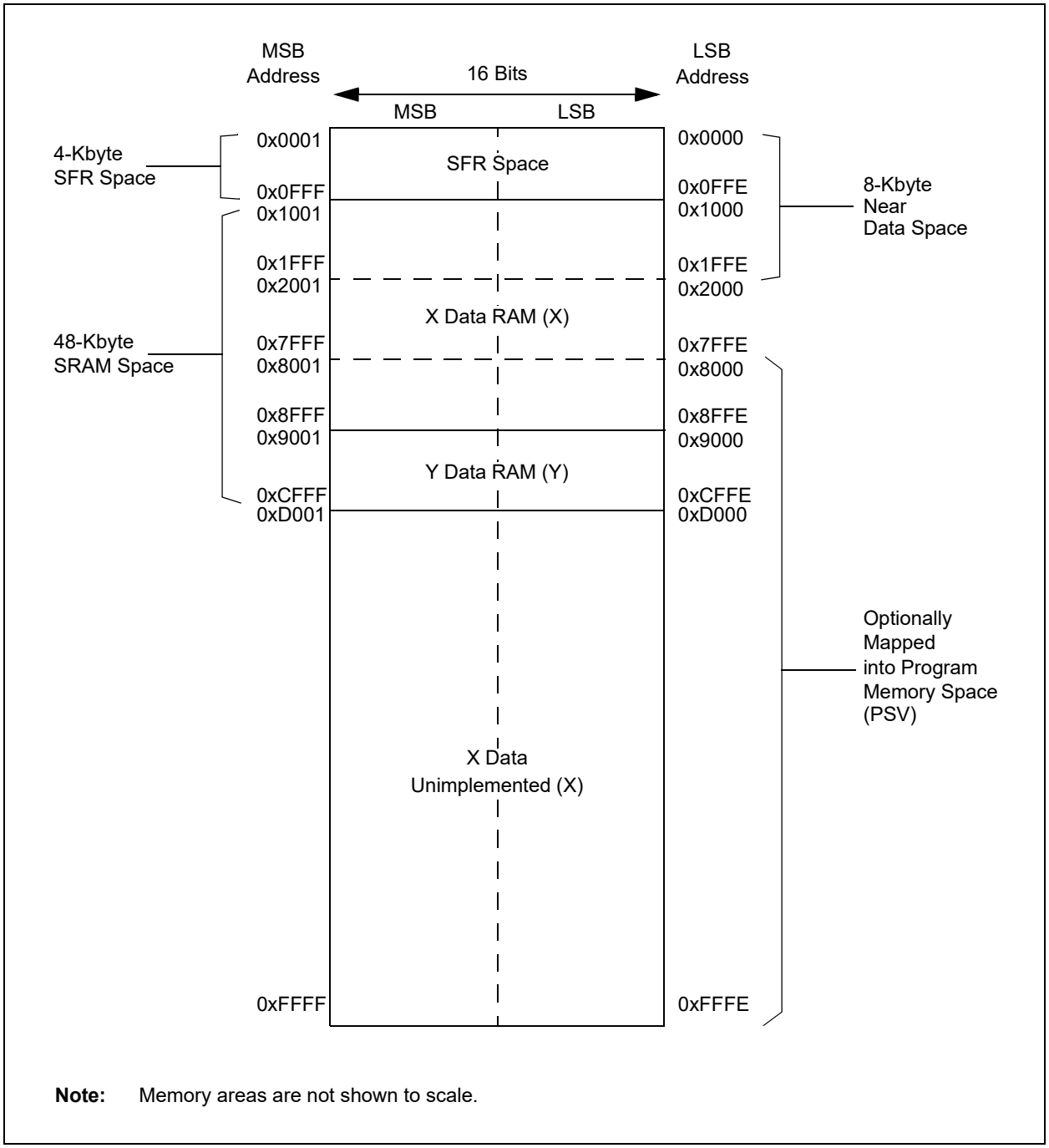
**FIGURE 4-10: DATA MEMORY MAP FOR dsPIC33EP256MC20X/50X AND dsPIC33EP256GP50X DEVICES**




**Note:** Memory areas are not shown to scale.

**FIGURE 4-11: DATA MEMORY MAP FOR dsPIC33EP512MC20X/50X AND dsPIC33EP512GP50X DEVICES**




**Note:** Memory areas are not shown to scale.


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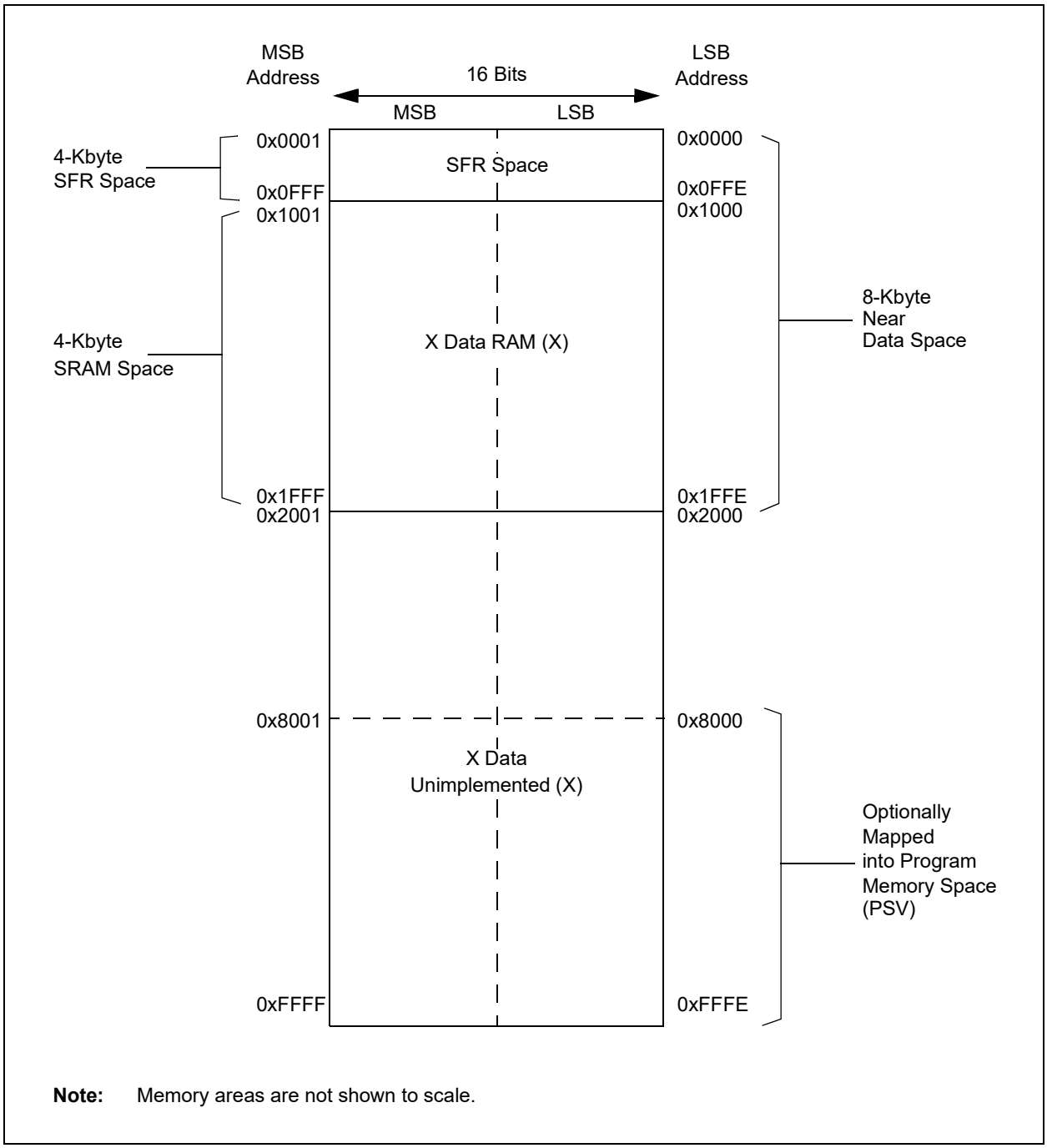
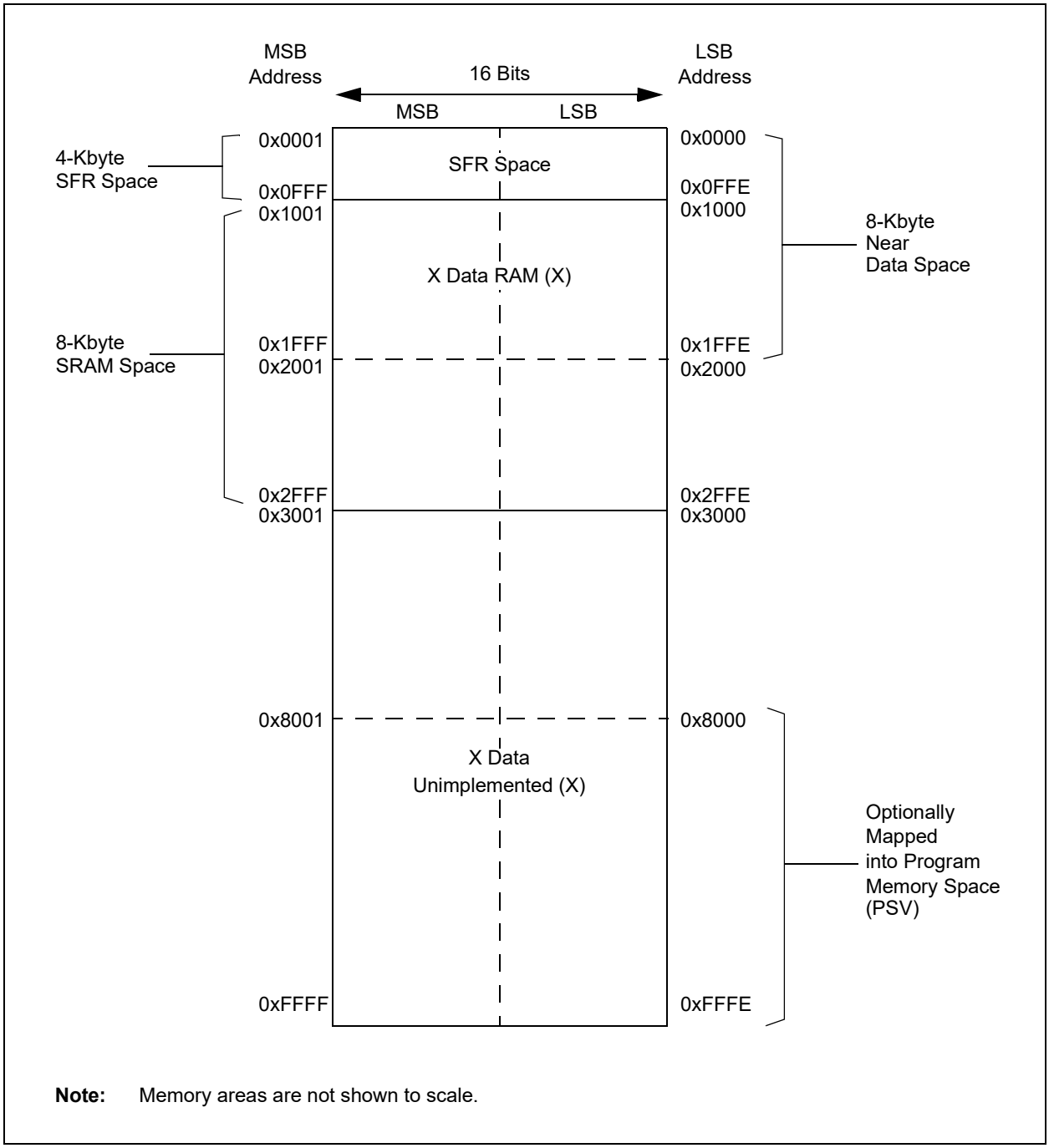
**FIGURE 4-12: DATA MEMORY MAP FOR PIC24EP32GP/MC20X/50X DEVICES**




**Note:** Memory areas are not shown to scale.

**FIGURE 4-13: DATA MEMORY MAP FOR PIC24EP64GP/MC20X/50X DEVICES**




**Note:** Memory areas are not shown to scale.


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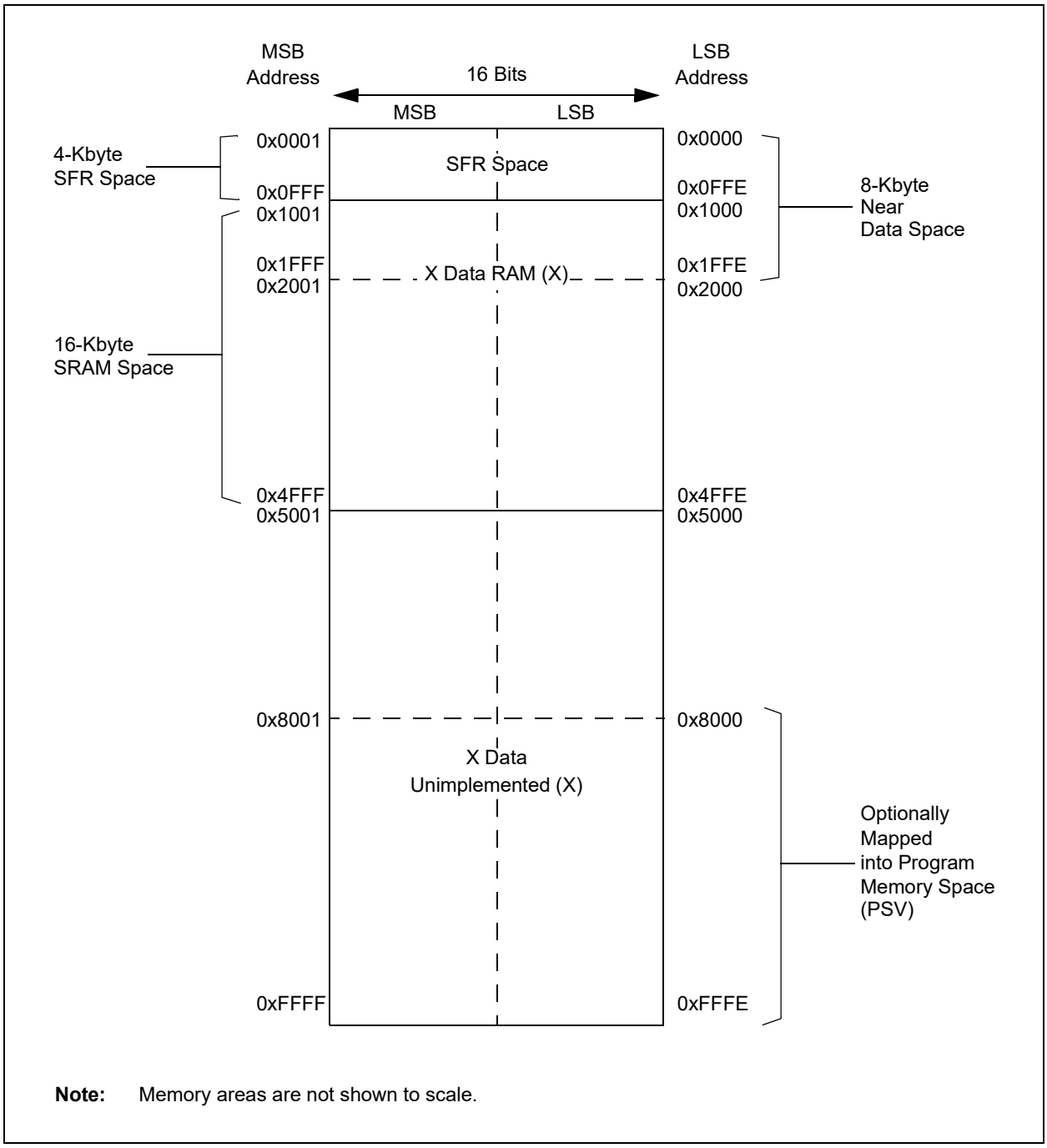
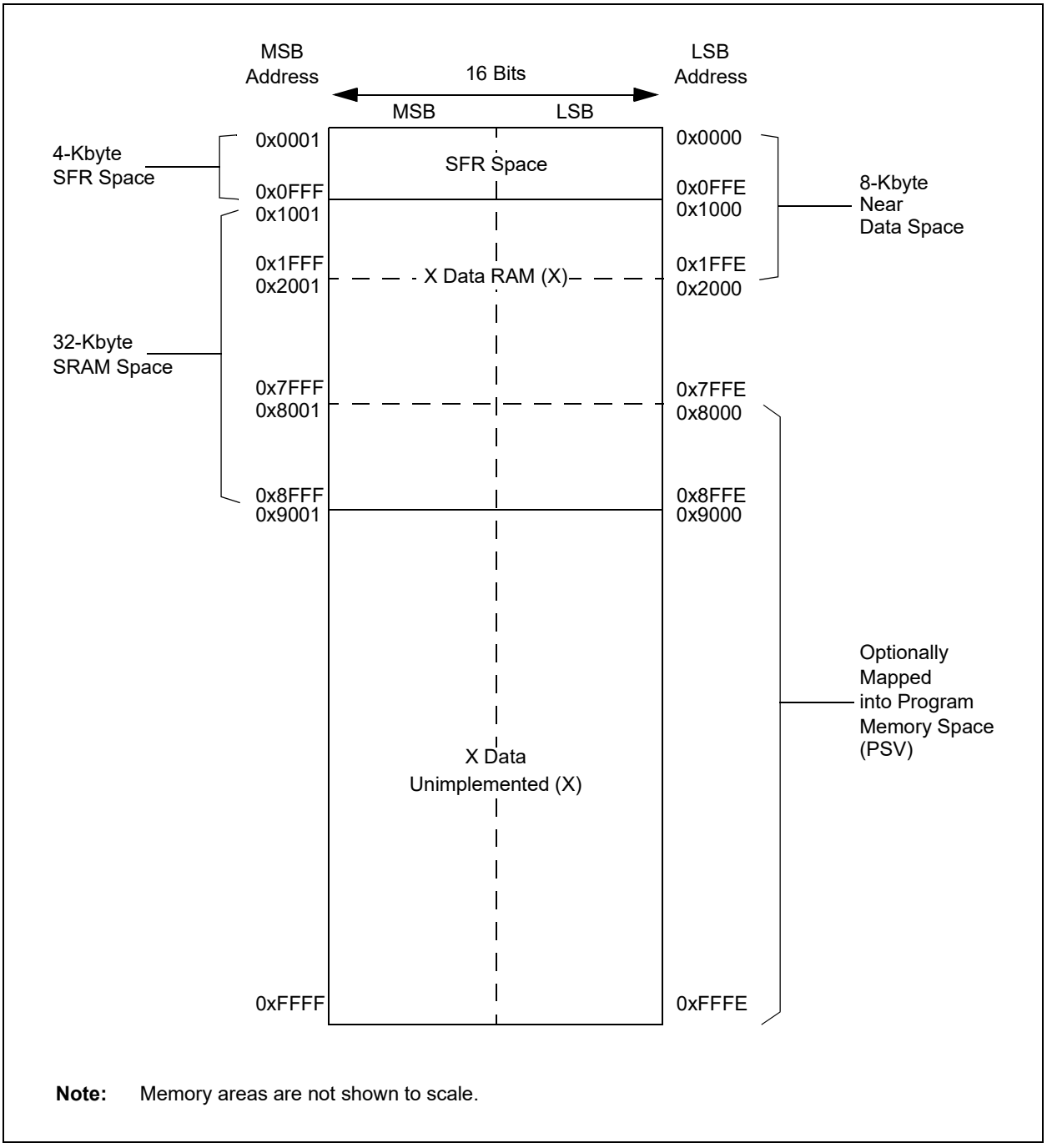
**FIGURE 4-14: DATA MEMORY MAP FOR PIC24EP128GP/MC20X/50X DEVICES**




**Note:** Memory areas are not shown to scale.

**FIGURE 4-15: DATA MEMORY MAP FOR PIC24EP256GP/MC20X/50X DEVICES**




**Note:** Memory areas are not shown to scale.


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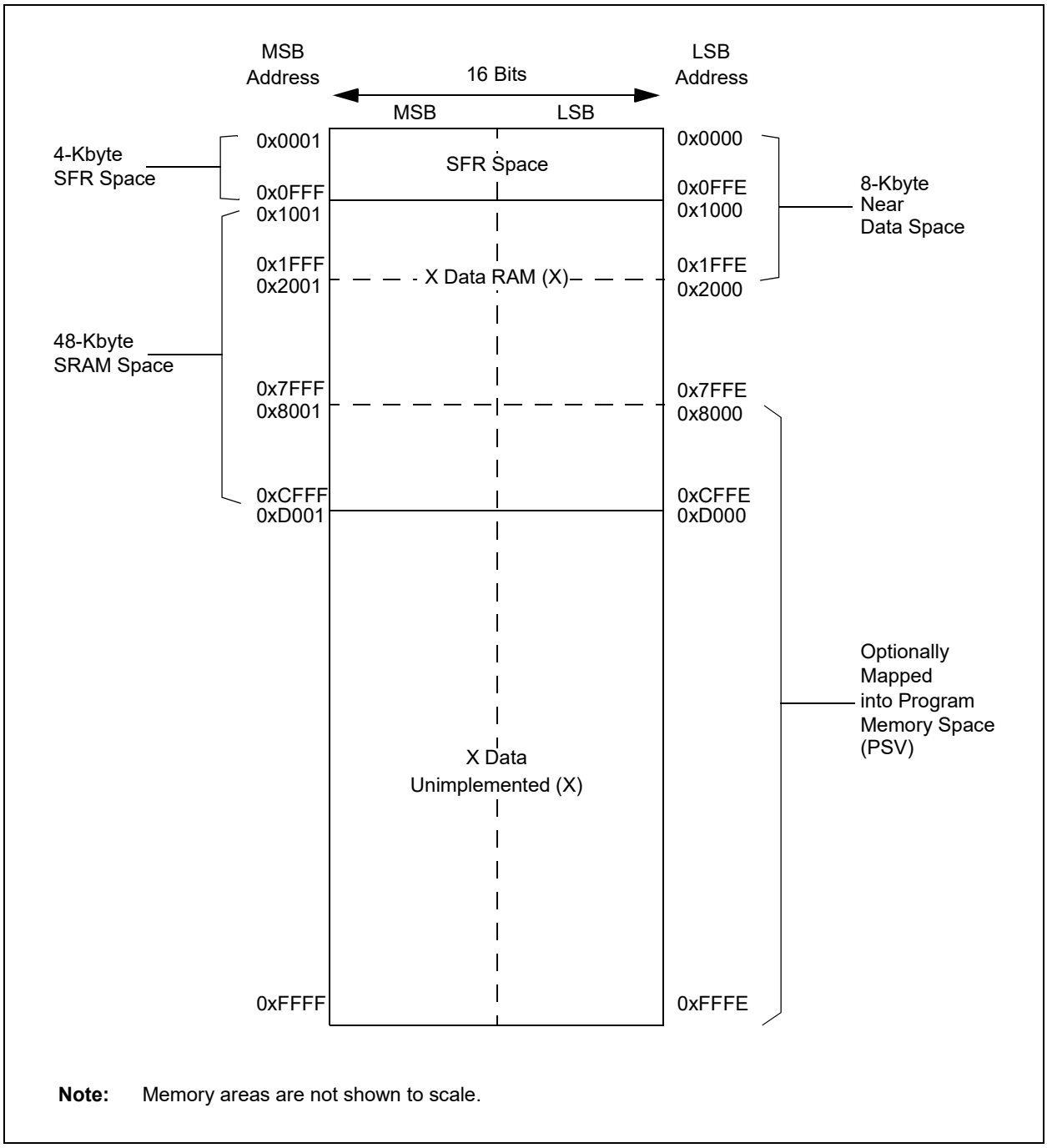
**FIGURE 4-16: DATA MEMORY MAP FOR PIC24EP512GP/MC20X/50X DEVICES**




**Note:** Memory areas are not shown to scale.

### 4.2.5 X AND Y DATA SPACES

The dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X core has two Data Spaces, X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (`MAC` class).

The Y Data Space is used in concert with the X Data Space by the `MAC` class of instructions (`CLR`, `ED`, `EDAC`, `MAC`, `MOVSAC`, `MPY`, `MPY.N` and `MSC`) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space. Modulo Addressing and Bit-Reversed Addressing are not present in PIC24EPXXXGP/MC20X devices.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

## 4.3 Memory Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 4.3.1 KEY RESOURCES

- **"dsPIC33/PIC24 Program Memory"** (www.microchip.com/DS70000613) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools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## 4.4 Special Function Register Maps

**TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W0 | 0000 | W0 (WREG) | | | | | | | | | | | | | | | | xxxx |
| W1 | 0002 | W1 | | | | | | | | | | | | | | | | xxxx |
| W2 | 0004 | W2 | | | | | | | | | | | | | | | | xxxx |
| W3 | 0006 | W3 | | | | | | | | | | | | | | | | xxxx |
| W4 | 0008 | W4 | | | | | | | | | | | | | | | | xxxx |
| W5 | 000A | W5 | | | | | | | | | | | | | | | | xxxx |
| W6 | 000C | W6 | | | | | | | | | | | | | | | | xxxx |
| W7 | 000E | W7 | | | | | | | | | | | | | | | | xxxx |
| W8 | 0010 | W8 | | | | | | | | | | | | | | | | xxxx |
| W9 | 0012 | W9 | | | | | | | | | | | | | | | | xxxx |
| W10 | 0014 | W10 | | | | | | | | | | | | | | | | xxxx |
| W11 | 0016 | W11 | | | | | | | | | | | | | | | | xxxx |
| W12 | 0018 | W12 | | | | | | | | | | | | | | | | xxxx |
| W13 | 001A | W13 | | | | | | | | | | | | | | | | xxxx |
| W14 | 001C | W14 | | | | | | | | | | | | | | | | xxxx |
| W15 | 001E | W15 | | | | | | | | | | | | | | | | xxxx |
| SPLIM | 0020 | SPLIM | | | | | | | | | | | | | | | | 0000 |
| ACCAL | 0022 | ACCAL | | | | | | | | | | | | | | | | 0000 |
| ACCAH | 0024 | ACCAH | | | | | | | | | | | | | | | | 0000 |
| ACCAU | 0026 | Sign Extension of ACCA[39] | | | | | | | | ACCAU | | | | | | | | 0000 |
| ACCBL | 0028 | ACCBL | | | | | | | | | | | | | | | | 0000 |
| ACCBH | 002A | ACCBH | | | | | | | | | | | | | | | | 0000 |
| ACCBU | 002C | Sign Extension of ACCB[39] | | | | | | | | ACCBU | | | | | | | | 0000 |
| PCL | 002E | PCL[15:0] | | | | | | | | | | | | | | | — | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | — | PCH[6:0] | | | | | | | 0000 |
| DSRPAG | 0032 | — | — | — | — | — | — | DSRPAG[9:0] | | | | | | | | | | 0001 |
| DSWPAG | 0034 | — | — | — | — | — | — | — | DSWPAG[8:0] | | | | | | | | | 0001 |
| RCOUNT | 0036 | RCOUNT[15:0] | | | | | | | | | | | | | | | | 0000 |
| DCOUNT | 0038 | DCOUNT[15:0] | | | | | | | | | | | | | | | | 0000 |
| DOSTARTL | 003A | DOSTARTL[15:1] | | | | | | | | | | | | | | | — | 0000 |
| DOSTARTH | 003C | — | — | — | — | — | — | — | — | — | — | DOSTARTH[5:0] | | | | | | 0000 |
| DOENDL | 003E | DOENDL[15:1] | | | | | | | | | | | | | | | — | 0000 |
| DOENDH | 0040 | — | — | — | — | — | — | — | — | — | — | DOENDH[5:0] | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-1: CPU CORE REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SR | 0042 | OA | OB | SA | SB | OAB | SAB | DA | DC | IPL[2:0] | | | RA | N | OV | Z | C | 0000 |
| CORCON | 0044 | VAR | — | US[1:0] | | EDT | DL[2:0] | | | SATA | SATB | SATDW | ACCSAT | IPL3 | SFA | RND | IF | 0020 |
| MODCON | 0046 | XMODEN | YMODEN | — | — | BWM[3:0] | | | | YWM[3:0] | | | | XWM[3:0] | | | | 0000 |
| XMODSRT | 0048 | XMODSRT[15:0] | | | | | | | | | | | | | | | — | 0000 |
| XMODEND | 004A | XMODEND[15:0] | | | | | | | | | | | | | | | — | 0001 |
| YMODSRT | 004C | YMODSRT[15:0] | | | | | | | | | | | | | | | — | 0000 |
| YMODEND | 004E | YMODEND[15:0] | | | | | | | | | | | | | | | — | 0001 |
| XBREV | 0050 | BREN | XBREV[14:0] | | | | | | | | | | | | | | | 0000 |
| DISICNT | 0052 | — | — | DISICNT[13:0] | | | | | | | | | | | | | | 0000 |
| TBLPAG | 0054 | — | — | — | — | — | — | — | — | TBLPAG[7:0] | | | | | | | | 0000 |
| MSTRPR | 0058 | MSTRPR[15:0] | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-2: CPU CORE REGISTER MAP FOR PIC24EPXXXGP/MC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W0 | 0000 | W0 (WREG) | | | | | | | | | | | | | | | | xxxx |
| W1 | 0002 | W1 | | | | | | | | | | | | | | | | xxxx |
| W2 | 0004 | W2 | | | | | | | | | | | | | | | | xxxx |
| W3 | 0006 | W3 | | | | | | | | | | | | | | | | xxxx |
| W4 | 0008 | W4 | | | | | | | | | | | | | | | | xxxx |
| W5 | 000A | W5 | | | | | | | | | | | | | | | | xxxx |
| W6 | 000C | W6 | | | | | | | | | | | | | | | | xxxx |
| W7 | 000E | W7 | | | | | | | | | | | | | | | | xxxx |
| W8 | 0010 | W8 | | | | | | | | | | | | | | | | xxxx |
| W9 | 0012 | W9 | | | | | | | | | | | | | | | | xxxx |
| W10 | 0014 | W10 | | | | | | | | | | | | | | | | xxxx |
| W11 | 0016 | W11 | | | | | | | | | | | | | | | | xxxx |
| W12 | 0018 | W12 | | | | | | | | | | | | | | | | xxxx |
| W13 | 001A | W13 | | | | | | | | | | | | | | | | xxxx |
| W14 | 001C | W14 | | | | | | | | | | | | | | | | xxxx |
| W15 | 001E | W15 | | | | | | | | | | | | | | | | xxxx |
| SPLIM | 0020 | SPLIM[15:0] | | | | | | | | | | | | | | | | 0000 |
| PCL | 002E | PCL[15:1] | | | | | | | | | | | | | | | — | 0000 |
| PCH | 0030 | — | — | — | — | — | — | — | — | — | PCH[6:0] | | | | | | | 0000 |
| DSRPAG | 0032 | — | — | — | — | — | — | DSRPAG[9:0] | | | | | | | | | | 0001 |
| DSWPAG | 0034 | — | — | — | — | — | — | — | DSWPAG[8:0] | | | | | | | | | 0001 |
| RCOUNT | 0036 | RCOUNT[15:0] | | | | | | | | | | | | | | | | 0000 |
| SR | 0042 | — | — | — | — | — | — | — | DC | IPL[2:0] | | | RA | N | OV | Z | C | 0000 |
| CORCON | 0044 | VAR | — | — | — | — | — | — | — | — | — | — | — | IPL3 | SFA | — | — | 0020 |
| DISICNT | 0052 | — | — | DISICNT[13:0] | | | | | | | | | | | | | | 0000 |
| TBLPAG | 0054 | — | — | — | — | — | — | — | — | TBLPAG[7:0] | | | | | | | | 0000 |
| MSTRPR | 0058 | MSTRPR[15:0] | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | — | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | — | — | — | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | — | — | — | — | — | — | — | — | — | IC4IF | IC3IF | DMA3IF | — | — | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | — | — | — | — | — | — | — | — | — | — | — | — | MI2C2IF | SI2C2IF | — | 0000 |
| IFS4 | 0808 | — | — | CTMUIF | — | — | — | — | — | — | — | — | — | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS8 | 0810 | JTAGIF | ICDIF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS9 | 0812 | — | — | — | — | — | — | — | — | — | PTG3IF | PTG2IF | PTG1IF | PTG0IF | PTGWDTIF | PTGSTEPIF | — | 0000 |
| IEC0 | 0820 | — | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | — | — | — | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | — | — | — | — | — | — | — | — | — | IC4IE | IC3IE | DMA3IE | — | — | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | — | — | — | — | — | — | — | — | — | — | — | — | MI2C2IE | SI2C2IE | — | 0000 |
| IEC4 | 0828 | — | — | CTMUIE | — | — | — | — | — | — | — | — | — | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC8 | 0830 | JTAGIE | ICDIE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC9 | 0832 | — | — | — | — | — | — | — | — | — | PTG3IE | PTG2IE | PTG1IE | PTG0IE | PTGWDTIE | PTGSTEPIE | — | 0000 |
| IPC0 | 0840 | — | T1IP[2:0] | | | — | OC1IP[2:0] | | | — | IC1IP[2:0] | | | — | INT0IP[2:0] | | | 4444 |
| IPC1 | 0842 | — | T2IP[2:0] | | | — | OC2IP[2:0] | | | — | IC2IP[2:0] | | | — | DMA0IP[2:0] | | | 4444 |
| IPC2 | 0844 | — | U1RXIP[2:0] | | | — | SPI1IP[2:0] | | | — | SPI1EIP[2:0] | | | — | T3IP[2:0] | | | 4444 |
| IPC3 | 0846 | — | — | — | — | — | DMA1IP[2:0] | | | — | AD1IP[2:0] | | | — | U1TXIP[2:0] | | | 0444 |
| IPC4 | 0848 | — | CNIP[2:0] | | | — | CMIP[2:0] | | | — | MI2C1IP[2:0] | | | — | SI2C1IP[2:0] | | | 4444 |
| IPC5 | 084A | — | — | — | — | — | — | — | — | — | — | — | — | — | INT1IP[2:0] | | | 0004 |
| IPC6 | 084C | — | T4IP[2:0] | | | — | OC4IP[2:0] | | | — | OC3IP[2:0] | | | — | DMA2IP[2:0] | | | 4444 |
| IPC7 | 084E | — | U2TXIP[2:0] | | | — | U2RXIP[2:0] | | | — | INT2IP[2:0] | | | — | T5IP[2:0] | | | 4444 |
| IPC8 | 0850 | — | — | — | — | — | — | — | — | — | SPI2IP[2:0] | | | — | SPI2EIP[2:0] | | | 0044 |
| IPC9 | 0852 | — | — | — | — | — | IC4IP[2:0] | | | — | IC3IP[2:0] | | | — | DMA3IP[2:0] | | | 0444 |
| IPC12 | 0858 | — | — | — | — | — | MI2C2IP[2:0] | | | — | SI2C2IP[2:0] | | | — | — | — | — | 0440 |
| IPC16 | 0860 | — | CRCIP[2:0] | | | — | U2EIP[2:0] | | | — | U1EIP[2:0] | | | — | — | — | — | 4440 |
| IPC19 | 0866 | — | — | — | — | — | — | — | — | — | CTMUIP[2:0] | | | — | — | — | — | 0040 |
| IPC35 | 0886 | — | JTAGIP[2:0] | | | — | ICDIP[2:0] | | | — | — | — | — | — | — | — | — | 4400 |
| IPC36 | 0888 | — | PTG0IP[2:0] | | | — | PTGWDTIP[2:0] | | | — | PTGSTEPIP[2:0] | | | — | — | — | — | 4440 |
| IPC37 | 088A | — | — | — | — | — | PTG3IP[2:0] | | | — | PTG2IP[2:0] | | | — | PTG1IP[2:0] | | | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | — | — | — | — | — | — | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | — | — | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | — | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | ILR[3:0] | | | | VECNUM[7:0] | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | — | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | — | — | — | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | — | — | — | — | — | — | — | — | — | IC4IF | IC3IF | DMA3IF | — | — | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | — | — | — | — | QEI1IF | PSEMIF | — | — | — | — | — | — | MI2C2IF | SI2C2IF | — | 0000 |
| IFS4 | 0808 | — | — | CTMUIF | — | — | — | — | — | — | — | — | — | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS5 | 080A | PWM2IF | PWM1IF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IF | 0000 |
| IFS8 | 0810 | JTAGIF | ICDIF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS9 | 0812 | — | — | — | — | — | — | — | — | — | PTG3IF | PTG2IF | PTG1IF | PTG0IF | PTGWDTIF | PTGSTEPIF | — | 0000 |
| IEC0 | 0820 | — | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | — | — | — | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | — | — | — | — | — | — | — | — | — | IC4IE | IC3IE | DMA3IE | — | — | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | — | — | — | — | QEI1IE | PSEMIE | — | — | — | — | — | — | MI2C2IE | SI2C2IE | — | 0000 |
| IEC4 | 0828 | — | — | CTMUIE | — | — | — | — | — | — | — | — | — | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC5 | 082A | PWM2IE | PWM1IE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC6 | 082C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IE | 0000 |
| IEC8 | 0830 | JTAGIE | ICDIE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC9 | 0832 | — | — | — | — | — | — | — | — | — | PTG3IE | PTG2IE | PTG1IE | PTG0IE | PTGWDTIE | PTGSTEPIE | — | 0000 |
| IPC0 | 0840 | — | T1IP[2:0] | | | — | OC1IP[2:0] | | | — | IC1IP[2:0] | | | — | INT0IP[2:0] | | | 4444 |
| IPC1 | 0842 | — | T2IP[2:0] | | | — | OC2IP[2:0] | | | — | IC2IP[2:0] | | | — | DMA0IP[2:0] | | | 4444 |
| IPC2 | 0844 | — | U1RXIP[2:0] | | | — | SPI1IP[2:0] | | | — | SPI1EIP[2:0] | | | — | T3IP[2:0] | | | 4444 |
| IPC3 | 0846 | — | — | — | — | — | DMA1IP[2:0] | | | — | AD1IP[2:0] | | | — | U1TXIP[2:0] | | | 0444 |
| IPC4 | 0848 | — | CNIP[2:0] | | | — | CMIP[2:0] | | | — | MI2C1IP[2:0] | | | — | SI2C1IP[2:0] | | | 4444 |
| IPC5 | 084A | — | — | — | — | — | — | — | — | — | — | — | — | — | INT1IP[2:0] | | | 0004 |
| IPC6 | 084C | — | T4IP[2:0] | | | — | OC4IP[2:0] | | | — | OC3IP[2:0] | | | — | DMA2IP[2:0] | | | 4444 |
| IPC7 | 084E | — | U2TXIP[2:0] | | | — | U2RXIP[2:0] | | | — | INT2IP[2:0] | | | — | T5IP[2:0] | | | 4444 |
| IPC8 | 0850 | — | — | — | — | — | — | — | — | — | SPI2IP[2:0] | | | — | SPI2EIP[2:0] | | | 0044 |
| IPC9 | 0852 | — | — | — | — | — | IC4IP[2:0] | | | — | IC3IP[2:0] | | | — | DMA3IP[2:0] | | | 0444 |
| IPC12 | 0858 | — | — | — | — | — | MI2C2IP[2:0] | | | — | SI2C2IP[2:0] | | | — | — | — | — | 0440 |
| IPC14 | 085C | — | — | — | — | — | QEI1IP[2:0] | | | — | PSEMIP[2:0] | | | — | — | — | — | 0440 |
| IPC16 | 0860 | — | CRCIP[2:0] | | | — | U2EIP[2:0] | | | — | U1EIP[2:0] | | | — | — | — | — | 4440 |
| IPC19 | 0866 | — | — | — | — | — | — | — | — | — | CTMUIP[2:0] | | | — | — | — | — | 0040 |
| IPC23 | 086E | — | PWM2IP[2:0] | | | — | PWM1IP[2:0] | | | — | — | — | — | — | — | — | — | 4400 |
| IPC24 | 0870 | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IP[2:0] | | | 4004 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-4: INTERRUPT CONTROLLER REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC35 | 0886 | — | JTAGIP[2:0] | | | — | ICDIP[2:0] | | | — | — | — | — | — | — | — | — | 4400 |
| IPC36 | 0888 | — | PTG0IP[2:0] | | | — | PTGWDTIP[2:0] | | | — | PTGSTEPIP[2:0] | | | — | — | — | — | 4440 |
| IPC37 | 088A | — | — | — | — | — | PTG3IP[2:0] | | | — | PTG2IP[2:0] | | | — | PTG1IP[2:0] | | | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | — | — | — | — | — | — | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | — | — | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | — | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | ILR[3:0] | | | | VECNUM[7:0] | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | — | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | — | — | — | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | — | — | — | — | — | — | — | — | — | IC4IF | IC3IF | DMA3IF | C1IF | C1RXIF | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | — | — | — | — | — | — | — | — | — | — | — | — | MI2C2IF | SI2C2IF | — | 0000 |
| IFS4 | 0808 | — | — | CTMUIF | — | — | — | — | — | — | C1TXIF | — | — | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IF | 0000 |
| IFS8 | 0810 | JTAGIF | ICDIF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS9 | 0812 | — | — | — | — | — | — | — | — | — | PTG3IF | PTG2IF | PTG1IF | PTG0IF | PTGWDTIF | PTGSTEPIF | — | 0000 |
| IEC0 | 0820 | — | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | — | — | — | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | — | — | — | — | — | — | — | — | — | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | — | — | — | — | — | — | — | — | — | — | — | — | MI2C2IE | SI2C2IE | — | 0000 |
| IEC4 | 0828 | — | — | CTMUIE | — | — | — | — | — | — | C1TXIE | — | — | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC8 | 0830 | JTAGIE | ICDIE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC9 | 0832 | — | — | — | — | — | — | — | — | — | PTG3IE | PTG2IE | PTG1IE | PTG0IE | PTGWDTIE | PTGSTEPIE | — | 0000 |
| IPC0 | 0840 | — | T1IP[2:0] | | | — | OC1IP[2:0] | | | — | IC1IP[2:0] | | | — | INT0IP[2:0] | | | 4444 |
| IPC1 | 0842 | — | T2IP[2:0] | | | — | OC2IP[2:0] | | | — | IC2IP[2:0] | | | — | DMA0IP[2:0] | | | 4444 |
| IPC2 | 0844 | — | U1RXIP[2:0] | | | — | SPI1IP[2:0] | | | — | SPI1EIP[2:0] | | | — | T3IP[2:0] | | | 4444 |
| IPC3 | 0846 | — | — | — | — | — | DMA1IP[2:0] | | | — | AD1IP[2:0] | | | — | U1TXIP[2:0] | | | 0444 |
| IPC4 | 0848 | — | CNIP[2:0] | | | — | CMIP[2:0] | | | — | MI2C1IP[2:0] | | | — | SI2C1IP[2:0] | | | 4444 |
| IPC5 | 084A | — | — | — | — | — | — | — | — | — | — | — | — | — | INT1IP[2:0] | | | 0004 |
| IPC6 | 084C | — | T4IP[2:0] | | | — | OC4IP[2:0] | | | — | OC3IP[2:0] | | | — | DMA2IP[2:0] | | | 4444 |
| IPC7 | 084E | — | U2TXIP[2:0] | | | — | U2RXIP[2:0] | | | — | INT2IP[2:0] | | | — | T5IP[2:0] | | | 4444 |
| IPC8 | 0850 | — | C1IP[2:0] | | | — | C1RXIP[2:0] | | | — | SPI2IP[2:0] | | | — | SPI2EIP[2:0] | | | 4444 |
| IPC9 | 0852 | — | — | — | — | — | IC4IP[2:0] | | | — | IC3IP[2:0] | | | — | DMA3IP[2:0] | | | 0444 |
| IPC11 | 0856 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IPC12 | 0858 | — | — | — | — | — | MI2C2IP[2:0] | | | — | SI2C2IP[2:0] | | | — | — | — | — | 0440 |
| IPC16 | 0860 | — | CRCIP[2:0] | | | — | U2EIP[2:0] | | | — | U1EIP[2:0] | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | — | — | — | — | C1TXIP[2:0] | | | — | — | — | — | — | — | — | — | 0400 |
| IPC19 | 0866 | — | — | — | — | — | — | — | — | — | CTMUIP[2:0] | | | — | — | — | — | 0040 |
| IPC35 | 0886 | — | JTAGIP[2:0] | | | — | ICDIP[2:0] | | | — | — | — | — | — | — | — | — | 4400 |
| IPC36 | 0888 | — | PTG0IP[2:0] | | | — | PTGWDTIP[2:0] | | | — | PTGSTEPIP[2:0] | | | — | — | — | — | 4440 |
| IPC37 | 088A | — | — | — | — | — | PTG3IP[2:0] | | | — | PTG2IP[2:0] | | | — | PTG1IP[2:0] | | | 0444 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-5: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | — | — | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | — | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | ILR[3:0] | | | | VECNUM[7:0] | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | — | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | — | — | — | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | — | — | — | — | — | — | — | — | — | IC4IF | IC3IF | DMA3IF | — | — | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | — | — | — | — | QEI1IF | PSEMIF | — | — | — | — | — | — | MI2C2IF | SI2C2IF | — | 0000 |
| IFS4 | 0808 | — | — | CTMUIF | — | — | — | — | — | — | — | — | — | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS5 | 080A | PWM2IF | PWM1IF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IF | 0000 |
| IFS8 | 0810 | JTAGIF | ICDIF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS9 | 0812 | — | — | — | — | — | — | — | — | — | PTG3IF | PTG2IF | PTG1IF | PTG0IF | PTGWDTIF | PTGSTEPIF | — | 0000 |
| IEC0 | 0820 | — | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | — | — | — | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | — | — | — | — | — | — | — | — | — | IC4IE | IC3IE | DMA3IE | — | — | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | — | — | — | — | QEI1IE | PSEMIE | — | — | — | — | — | — | MI2C2IE | SI2C2IE | — | 0000 |
| IEC4 | 0828 | — | — | CTMUIE | — | — | — | — | — | — | — | — | — | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC5 | 082A | PWM2IE | PWM1IE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC6 | 082C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IE | 0000 |
| IEC8 | 0830 | JTAGIE | ICDIE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC9 | 0832 | — | — | — | — | — | — | — | — | — | PTG3IE | PTG2IE | PTG1IE | PTG0IE | PTGWDTIE | PTGSTEPIE | — | 0000 |
| IPC0 | 0840 | — | T1IP[2:0] | | | — | OC1IP[2:0] | | | — | IC1IP[2:0] | | | — | INT0IP[2:0] | | | 4444 |
| IPC1 | 0842 | — | T2IP[2:0] | | | — | OC2IP[2:0] | | | — | IC2IP[2:0] | | | — | DMA0IP[2:0] | | | 4444 |
| IPC2 | 0844 | — | U1RXIP[2:0] | | | — | SPI1IP[2:0] | | | — | SPI1EIP[2:0] | | | — | T3IP[2:0] | | | 4444 |
| IPC3 | 0846 | — | — | — | — | — | DMA1IP[2:0] | | | — | AD1IP[2:0] | | | — | U1TXIP[2:0] | | | 0444 |
| IPC4 | 0848 | — | CNIP[2:0] | | | — | CMIP[2:0] | | | — | MI2C1IP[2:0] | | | — | SI2C1IP[2:0] | | | 4444 |
| IPC5 | 084A | — | — | — | — | — | — | — | — | — | — | — | — | — | INT1IP[2:0] | | | 0004 |
| IPC6 | 084C | — | T4IP[2:0] | | | — | OC4IP[2:0] | | | — | OC3IP[2:0] | | | — | DMA2IP[2:0] | | | 4444 |
| IPC7 | 084E | — | U2TXIP[2:0] | | | — | U2RXIP[2:0] | | | — | INT2IP[2:0] | | | — | T5IP[2:0] | | | 4444 |
| IPC8 | 0850 | — | — | — | — | — | C1RXIP[2:0] | | | — | SPI2IP[2:0] | | | — | SPI2EIP[2:0] | | | 0444 |
| IPC9 | 0852 | — | — | — | — | — | IC4IP[2:0] | | | — | IC3IP[2:0] | | | — | DMA3IP[2:0] | | | 0444 |
| IPC12 | 0858 | — | — | — | — | — | MI2C2IP[2:0] | | | — | SI2C2IP[2:0] | | | — | — | — | — | 0440 |
| IPC14 | 085C | — | — | — | — | — | QEI1IP[2:0] | | | — | PSEMIP[2:0] | | | — | — | — | — | 0440 |
| IPC16 | 0860 | — | CRCIP[2:0] | | | — | U2EIP[2:0] | | | — | U1EIP[2:0] | | | — | — | — | — | 4440 |
| IPC19 | 0866 | — | — | — | — | — | — | — | — | — | CTMUIP[2:0] | | | — | — | — | — | 0040 |
| IPC23 | 086E | — | PWM2IP[2:0] | | | — | PWM1IP[2:0] | | | — | — | — | — | — | — | — | — | 4400 |
| IPC24 | 0870 | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IP[2:0] | | | 0004 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-6: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC35 | 0886 | — | JTAGIP[2:0] | | | — | ICDIP[2:0] | | | — | — | — | — | — | — | — | — | 4400 |
| IPC36 | 0888 | — | PTG0IP[2:0] | | | — | PTGWDTIP[2:0] | | | — | PTGSTEPIP[2:0] | | | — | — | — | — | 4440 |
| IPC37 | 088A | — | — | — | — | — | PTG3IP[2:0] | | | — | PTG2IP[2:0] | | | — | PTG1IP[2:0] | | | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | — | — | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | — | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | ILR[3:0] | | | | VECNUM[7:0] | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IFS0 | 0800 | — | DMA1IF | AD1IF | U1TXIF | U1RXIF | SPI1IF | SPI1EIF | T3IF | T2IF | OC2IF | IC2IF | DMA0IF | T1IF | OC1IF | IC1IF | INT0IF | 0000 |
| IFS1 | 0802 | U2TXIF | U2RXIF | INT2IF | T5IF | T4IF | OC4IF | OC3IF | DMA2IF | — | — | — | INT1IF | CNIF | CMIF | MI2C1IF | SI2C1IF | 0000 |
| IFS2 | 0804 | — | — | — | — | — | — | — | — | — | IC4IF | IC3IF | DMA3IF | C1IF | C1RXIF | SPI2IF | SPI2EIF | 0000 |
| IFS3 | 0806 | — | — | — | — | — | QEI1IF | PSEMIF | — | — | — | — | — | — | MI2C2IF | SI2C2IF | — | 0000 |
| IFS4 | 0808 | — | — | CTMUIF | — | — | — | — | — | — | C1TXIF | — | — | CRCIF | U2EIF | U1EIF | — | 0000 |
| IFS5 | 080A | PWM2IF | PWM1IF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS6 | 080C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IF | 0000 |
| IFS8 | 0810 | JTAGIF | ICDIF | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IFS9 | 0812 | — | — | — | — | — | — | — | — | — | PTG3IF | PTG2IF | PTG1IF | PTG0IF | PTGWDTIF | PTGSTEPIF | — | 0000 |
| IEC0 | 0820 | — | DMA1IE | AD1IE | U1TXIE | U1RXIE | SPI1IE | SPI1EIE | T3IE | T2IE | OC2IE | IC2IE | DMA0IE | T1IE | OC1IE | IC1IE | INT0IE | 0000 |
| IEC1 | 0822 | U2TXIE | U2RXIE | INT2IE | T5IE | T4IE | OC4IE | OC3IE | DMA2IE | — | — | — | INT1IE | CNIE | CMIE | MI2C1IE | SI2C1IE | 0000 |
| IEC2 | 0824 | — | — | — | — | — | — | — | — | — | IC4IE | IC3IE | DMA3IE | C1IE | C1RXIE | SPI2IE | SPI2EIE | 0000 |
| IEC3 | 0826 | — | — | — | — | — | QEI1IE | PSEMIE | — | — | — | — | — | — | MI2C2IE | SI2C2IE | — | 0000 |
| IEC4 | 0828 | — | — | CTMUIE | — | — | — | — | — | — | C1TXIE | — | — | CRCIE | U2EIE | U1EIE | — | 0000 |
| IEC5 | 082A | PWM2IE | PWM1IE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC6 | 082C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IE | 0000 |
| IEC7 | 082E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC8 | 0830 | JTAGIE | ICDIE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| IEC9 | 0832 | — | — | — | — | — | — | — | — | — | PTG3IE | PTG2IE | PTG1IE | PTG0IE | PTGWDTIE | PTGSTEPIE | — | 0000 |
| IPC0 | 0840 | — | T1IP[2:0] | | | — | OC1IP[2:0] | | | — | IC1IP[2:0] | | | — | INT0IP[2:0] | | | 4444 |
| IPC1 | 0842 | — | T2IP[2:0] | | | — | OC2IP[2:0] | | | — | IC2IP[2:0] | | | — | DMA0IP[2:0] | | | 4444 |
| IPC2 | 0844 | — | U1RXIP[2:0] | | | — | SPI1IP[2:0] | | | — | SPI1EIP[2:0] | | | — | T3IP[2:0] | | | 4444 |
| IPC3 | 0846 | — | — | — | — | — | DMA1IP[2:0] | | | — | AD1IP[2:0] | | | — | U1TXIP[2:0] | | | 0444 |
| IPC4 | 0848 | — | CNIP[2:0] | | | — | CMIP[2:0] | | | — | MI2C1IP[2:0] | | | — | SI2C1IP[2:0] | | | 4444 |
| IPC5 | 084A | — | — | — | — | — | — | — | — | — | — | — | — | — | INT1IP[2:0] | | | 0004 |
| IPC6 | 084C | — | T4IP[2:0] | | | — | OC4IP[2:0] | | | — | OC3IP[2:0] | | | — | DMA2IP[2:0] | | | 4444 |
| IPC7 | 084E | — | U2TXIP[2:0] | | | — | U2RXIP[2:0] | | | — | INT2IP[2:0] | | | — | T5IP[2:0] | | | 4444 |
| IPC8 | 0850 | — | C1IP[2:0] | | | — | C1RXIP[2:0] | | | — | SPI2IP[2:0] | | | — | SPI2EIP[2:0] | | | 4444 |
| IPC9 | 0852 | — | — | — | — | — | IC4IP[2:0] | | | — | IC3IP[2:0] | | | — | DMA3IP[2:0] | | | 0444 |
| IPC12 | 0858 | — | — | — | — | — | MI2C2IP[2:0] | | | — | SI2C2IP[2:0] | | | — | — | — | — | 0440 |
| IPC14 | 085C | — | — | — | — | — | QEI1IP[2:0] | | | — | PSEMIP[2:0] | | | — | — | — | — | 0440 |
| IPC16 | 0860 | — | CRCIP[2:0] | | | — | U2EIP[2:0] | | | — | U1EIP[2:0] | | | — | — | — | — | 4440 |
| IPC17 | 0862 | — | — | — | — | — | C1TXIP[2:0] | | | — | — | — | — | — | — | — | — | 0400 |
| IPC19 | 0866 | — | — | — | — | — | — | — | — | — | CTMUIP[2:0] | | | — | — | — | — | 0040 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-7: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY (CONTINUED)**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IPC23 | 086E | — | PWM2IP[2:0] | | | — | PWM1IP[2:0] | | | — | — | — | — | — | — | — | — | 4400 |
| IPC24 | 0870 | — | — | — | — | — | — | — | — | — | — | — | — | — | PWM3IP[2:0] | | | 0004 |
| IPC35 | 0886 | — | JTAGIP[2:0] | | | — | ICDIP[2:0] | | | — | — | — | — | — | — | — | — | 4400 |
| IPC36 | 0888 | — | PTG0IP[2:0] | | | — | PTGWDTIP[2:0] | | | — | PTGSTEPIP[2:0] | | | — | — | — | — | 4440 |
| IPC37 | 088A | — | — | — | — | — | PTG3IP[2:0] | | | — | PTG2IP[2:0] | | | — | PTG1IP[2:0] | | | 0444 |
| INTCON1 | 08C0 | NSTDIS | OVAERR | OVBERR | COVAERR | COVBERR | OVATE | OVBTE | COVTE | SFTACERR | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — | 0000 |
| INTCON2 | 08C2 | GIE | DISI | SWTRAP | — | — | — | — | — | — | — | — | — | — | INT2EP | INT1EP | INT0EP | 8000 |
| INTCON3 | 08C4 | — | — | — | — | — | — | — | — | — | — | DAE | DOOVR | — | — | — | — | 0000 |
| INTCON4 | 08C6 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | SGHT | 0000 |
| INTTREG | 08C8 | — | — | — | — | ILR[3:0] | | | | VECNUM[7:0] | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-8: TIMER1 THROUGH TIMER5 REGISTER MAP**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMR1 | 0100 | Timer1 Register | | | | | | | | | | | | | | | | xxxx |
| PR1 | 0102 | Period Register 1 | | | | | | | | | | | | | | | | FFFF |
| T1CON | 0104 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS[1:0] | | — | TSYNC | TCS | — | 0000 |
| TMR2 | 0106 | Timer2 Register | | | | | | | | | | | | | | | | xxxx |
| TMR3HLD | 0108 | Timer3 Holding Register (for 32-bit timer operations only) | | | | | | | | | | | | | | | | xxxx |
| TMR3 | 010A | Timer3 Register | | | | | | | | | | | | | | | | xxxx |
| PR2 | 010C | Period Register 2 | | | | | | | | | | | | | | | | FFFF |
| PR3 | 010E | Period Register 3 | | | | | | | | | | | | | | | | FFFF |
| T2CON | 0110 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS[1:0] | | T32 | — | TCS | — | 0000 |
| T3CON | 0112 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS[1:0] | | — | — | TCS | — | 0000 |
| TMR4 | 0114 | Timer4 Register | | | | | | | | | | | | | | | | xxxx |
| TMR5HLD | 0116 | Timer5 Holding Register (for 32-bit operations only) | | | | | | | | | | | | | | | | xxxx |
| TMR5 | 0118 | Timer5 Register | | | | | | | | | | | | | | | | xxxx |
| PR4 | 011A | Period Register 4 | | | | | | | | | | | | | | | | FFFF |
| PR5 | 011C | Period Register 5 | | | | | | | | | | | | | | | | FFFF |
| T4CON | 011E | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS[1:0] | | T32 | — | TCS | — | 0000 |
| T5CON | 0120 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS[1:0] | | — | — | TCS | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-9: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 4 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| IC1CON1 | 0140 | — | — | ICSIDL | ICTSEL[2:0] | | | — | — | — | ICI[1:0] | | ICOV | ICBNE | ICM[2:0] | | | 0000 |
| IC1CON2 | 0142 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL[4:0] | | | | | 000D |
| IC1BUF | 0144 | Input Capture 1 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC1TMR | 0146 | Input Capture 1 Timer Register | | | | | | | | | | | | | | | | 0000 |
| IC2CON1 | 0148 | — | — | ICSIDL | ICTSEL[2:0] | | | — | — | — | ICI[1:0] | | ICOV | ICBNE | ICM[2:0] | | | 0000 |
| IC2CON2 | 014A | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL[4:0] | | | | | 000D |
| IC2BUF | 014C | Input Capture 2 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC2TMR | 014E | Input Capture 2 Timer Register | | | | | | | | | | | | | | | | 0000 |
| IC3CON1 | 0150 | — | — | ICSIDL | ICTSEL[2:0] | | | — | — | — | ICI[1:0] | | ICOV | ICBNE | ICM[2:0] | | | 0000 |
| IC3CON2 | 0152 | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL[4:0] | | | | | 000D |
| IC3BUF | 0154 | Input Capture 3 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC3TMR | 0156 | Input Capture 3 Timer Register | | | | | | | | | | | | | | | | 0000 |
| IC4CON1 | 0158 | — | — | ICSIDL | ICTSEL[2:0] | | | — | — | — | ICI[1:0] | | ICOV | ICBNE | ICM[2:0] | | | 0000 |
| IC4CON2 | 015A | — | — | — | — | — | — | — | IC32 | ICTRIG | TRIGSTAT | — | SYNCSEL[4:0] | | | | | 000D |
| IC4BUF | 015C | Input Capture 4 Buffer Register | | | | | | | | | | | | | | | | xxxx |
| IC4TMR | 015E | Input Capture 4 Timer Register | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-10: OUTPUT COMPARE 1 THROUGH OUTPUT COMPARE 4 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OC1CON1 | 0900 | — | — | OCSIDL | OCTSEL[2:0] | | | — | ENFLTB | ENFLTA | — | OCFLTB | OCFLTA | TRIGMODE | OCM[2:0] | | | 0000 |
| OC1CON2 | 0902 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL[4:0] | | | | | 000C |
| OC1RS | 0904 | Output Compare 1 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC1R | 0906 | Output Compare 1 Register | | | | | | | | | | | | | | | | xxxx |
| OC1TMR | 0908 | Timer Value 1 Register | | | | | | | | | | | | | | | | xxxx |
| OC2CON1 | 090A | — | — | OCSIDL | OCTSEL[2:0] | | | — | ENFLTB | ENFLTA | — | OCFLTB | OCFLTA | TRIGMODE | OCM[2:0] | | | 0000 |
| OC2CON2 | 090C | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL[4:0] | | | | | 000C |
| OC2RS | 090E | Output Compare 2 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC2R | 0910 | Output Compare 2 Register | | | | | | | | | | | | | | | | xxxx |
| OC2TMR | 0912 | Timer Value 2 Register | | | | | | | | | | | | | | | | xxxx |
| OC3CON1 | 0914 | — | — | OCSIDL | OCTSEL[2:0] | | | — | ENFLTB | ENFLTA | — | OCFLTB | OCFLTA | TRIGMODE | OCM[2:0] | | | 0000 |
| OC3CON2 | 0916 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL[4:0] | | | | | 000C |
| OC3RS | 0918 | Output Compare 3 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC3R | 091A | Output Compare 3 Register | | | | | | | | | | | | | | | | xxxx |
| OC3TMR | 091C | Timer Value 3 Register | | | | | | | | | | | | | | | | xxxx |
| OC4CON1 | 091E | — | — | OCSIDL | OCTSEL[2:0] | | | — | ENFLTB | ENFLTA | — | OCFLTB | OCFLTA | TRIGMODE | OCM[2:0] | | | 0000 |
| OC4CON2 | 0920 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL[4:0] | | | | | 000C |
| OC4RS | 0922 | Output Compare 4 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC4R | 0924 | Output Compare 4 Register | | | | | | | | | | | | | | | | xxxx |
| OC4TMR | 0926 | Timer Value 4 Register | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-11: PTG REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTGCST | 0AC0 | PTGEN | — | PTGSIDL | PTGTOGL | — | PTGSWT | PTGSSEN | PTGIVIS | PTGSTRT | PTGWTO | — | — | — | — | PTGITM[1:0] | | 0000 |
| PTGCON | 0AC2 | PTGCLK[2:0] | | | PTGDIV[4:0] | | | | | PTGPWD[3:0] | | | | — | PTGWDT[2:0] | | | 0000 |
| PTGBTE | 0AC4 | ADCTS[4:1] | | | | IC4TSS | IC3TSS | IC2TSS | IC1TSS | OC4CS | OC3CS | OC2CS | OC1CS | OC4TSS | OC3TSS | OC2TSS | OC1TSS | 0000 |
| PTGHOLD | 0AC6 | PTGHOLD[15:0] | | | | | | | | | | | | | | | | 0000 |
| PTGT0LIM | 0AC8 | PTGT0LIM[15:0] | | | | | | | | | | | | | | | | 0000 |
| PTGT1LIM | 0ACA | PTGT1LIM[15:0] | | | | | | | | | | | | | | | | 0000 |
| PTGSDLIM | 0ACC | PTGSDLIM[15:0] | | | | | | | | | | | | | | | | 0000 |
| PTGC0LIM | 0ACE | PTGC0LIM[15:0] | | | | | | | | | | | | | | | | 0000 |
| PTGC1LIM | 0AD0 | PTGC1LIM[15:0] | | | | | | | | | | | | | | | | 0000 |
| PTGADJ | 0AD2 | PTGADJ[15:0] | | | | | | | | | | | | | | | | 0000 |
| PTGL0 | 0AD4 | PTGL0[15:0] | | | | | | | | | | | | | | | | 0000 |
| PTGQPTR | 0AD6 | — | — | — | — | — | — | — | — | — | — | — | PTGQPTR[4:0] | | | | | 0000 |
| PTGQUE0 | 0AD8 | STEP1[7:0] | | | | | | | | STEP0[7:0] | | | | | | | | 0000 |
| PTGQUE1 | 0ADA | STEP3[7:0] | | | | | | | | STEP2[7:0] | | | | | | | | 0000 |
| PTGQUE2 | 0ADC | STEP5[7:0] | | | | | | | | STEP4[7:0] | | | | | | | | 0000 |
| PTGQUE3 | 0ADE | STEP7[7:0] | | | | | | | | STEP6[7:0] | | | | | | | | 0000 |
| PTGQUE4 | 0AE0 | STEP9[7:0] | | | | | | | | STEP8[7:0] | | | | | | | | 0000 |
| PTGQUE5 | 0AE2 | STEP11[7:0] | | | | | | | | STEP10[7:0] | | | | | | | | 0000 |
| PTGQUE6 | 0AE4 | STEP13[7:0] | | | | | | | | STEP12[7:0] | | | | | | | | 0000 |
| PTGQUE7 | 0AE6 | STEP15[7:0] | | | | | | | | STEP14[7:0] | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-12: PWM REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PTCON | 0C00 | PTEN | — | PTSIDL | SESTAT | SEIEN | EIPU | SYNCPOL | SYNCOEN | SYNCEN | SYNCSRC[2:0] | | | SEVTPS[3:0] | | | | 0000 |
| PTCON2 | 0C02 | — | — | — | — | — | — | — | — | — | — | — | — | — | PCLKDIV[2:0] | | | 0000 |
| PTPER | 0C04 | PTPER[15:0] | | | | | | | | | | | | | | | | 00F8 |
| SEVTCMP | 0C06 | SEVTCMP[15:0] | | | | | | | | | | | | | | | | 0000 |
| MDC | 0C0A | MDC[15:0] | | | | | | | | | | | | | | | | 0000 |
| CHOP | 0C1A | CHPCLKEN | — | — | — | — | — | CHOPCLK[9:0] | | | | | | | | | | 0000 |
| PWMKEY | 0C1E | PWMKEY[15:0] | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-13: PWM GENERATOR 1 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON1 | 0C20 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC[1:0] | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON1 | 0C22 | PENH | PENL | POLH | POLL | PMOD[1:0] | | OVRENH | OVRENL | OVRDAT[1:0] | | FLTDAT[1:0] | | CLDAT[1:0] | | SWAP | OSYNC | C000 |
| FCLCON1 | 0C24 | — | CLSRC[4:0] | | | | | CLPOL | CLMOD | FLTSRC[4:0] | | | | | FLTPOL | FLTMOD[1:0] | | 0000 |
| PDC1 | 0C26 | PDC1[15:0] | | | | | | | | | | | | | | | | FFF8 |
| PHASE1 | 0C28 | PHASE1[15:0] | | | | | | | | | | | | | | | | 0000 |
| DTR1 | 0C2A | — | — | DTR1[13:0] | | | | | | | | | | | | | | 0000 |
| ALTDTR1 | 0C2C | — | — | ALTDTR1[13:0] | | | | | | | | | | | | | | 0000 |
| TRIG1 | 0C32 | TRGCMP[15:0] | | | | | | | | | | | | | | | | 0000 |
| TRGCON1 | 0C34 | TRGDIV[3:0] | | | | — | — | — | — | — | — | TRGSTRT[5:0] | | | | | | 0000 |
| LEBCON1 | 0C3A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY1 | 0C3C | — | — | — | — | LEB[11:0] | | | | | | | | | | | | 0000 |
| AUXCON1 | 0C3E | — | — | — | — | BLANKSEL[3:0] | | | | — | — | CHOPSEL[3:0] | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-14: PWM GENERATOR 2 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON2 | 0C40 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC[1:0] | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON2 | 0C42 | PENH | PENL | POLH | POLL | PMOD[1:0] | | OVRENH | OVRENL | OVRDAT[1:0] | | FLTDAT[1:0] | | CLDAT[1:0] | | SWAP | OSYNC | C000 |
| FCLCON2 | 0C44 | — | CLSRC[4:0] | | | | | CLPOL | CLMOD | FLTSRC[4:0] | | | | | FLTPOL | FLTMOD[1:0] | | 00F8 |
| PDC2 | 0C46 | PDC2[15:0] | | | | | | | | | | | | | | | | 0000 |
| PHASE2 | 0C48 | PHASE2[15:0] | | | | | | | | | | | | | | | | 0000 |
| DTR2 | 0C4A | — | — | DTR2[13:0] | | | | | | | | | | | | | | 0000 |
| ALTDTR2 | 0C4C | — | — | ALTDTR2[13:0] | | | | | | | | | | | | | | 0000 |
| TRIG2 | 0C52 | TRGCMP[15:0] | | | | | | | | | | | | | | | | 0000 |
| TRGCON2 | 0C54 | TRGDIV[3:0] | | | | — | — | — | — | — | — | TRGSTRT[5:0] | | | | | | 0000 |
| LEBCON2 | 0C5A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY2 | 0C5C | — | — | — | — | LEB[11:0] | | | | | | | | | | | | 0000 |
| AUXCON2 | 0C5E | — | — | — | — | BLANKSEL[3:0] | | | | — | — | CHOPSEL[3:0] | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-15: PWM GENERATOR 3 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PWMCON3 | 0C60 | FLTSTAT | CLSTAT | TRGSTAT | FLTIEN | CLIEN | TRGIEN | ITB | MDCS | DTC[1:0] | | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON3 | 0C62 | PENH | PENL | POLH | POLL | PMOD[1:0] | | OVRENH | OVRENL | OVRDAT[1:0] | | FLTDAT[1:0] | | CLDAT[1:0] | | SWAP | OSYNC | C000 |
| FCLCON3 | 0C64 | — | CLSRC[4:0] | | | | | CLPOL | CLMOD | FLTSRC[4:0] | | | | | FLTPOL | FLTMOD[1:0] | | 00F8 |
| PDC3 | 0C66 | PDC3[15:0] | | | | | | | | | | | | | | | | 0000 |
| PHASE3 | 0C68 | PHASE3[15:0] | | | | | | | | | | | | | | | | 0000 |
| DTR3 | 0C6A | — | — | DTR3[13:0] | | | | | | | | | | | | | | 0000 |
| ALTDTR3 | 0C6C | — | — | ALTDTR3[13:0] | | | | | | | | | | | | | | 0000 |
| TRIG3 | 0C72 | TRGCMP[15:0] | | | | | | | | | | | | | | | | 0000 |
| TRGCON3 | 0C74 | TRGDIV[3:0] | | | | — | — | — | — | — | — | TRGSTRT[5:0] | | | | | | 0000 |
| LEBCON3 | 0C7A | PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY3 | 0C7C | — | — | — | — | LEB[11:0] | | | | | | | | | | | | 0000 |
| AUXCON3 | 0C7E | — | — | — | — | BLANKSEL[3:0] | | | | — | — | CHOPSEL[3:0] | | | | CHOPHEN | CHOPLEN | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-16: QEI1 REGISTER MAP FOR dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| QEI1CON | 01C0 | QEIEN | — | QEISIDL | PIMOD[2:0] | | | IMV[1:0] | | — | INTDIV[2:0] | | | CNTPOL | GATEN | CCM[1:0] | | 0000 |
| QEI1IOC | 01C2 | QCAPEN | FLTREN | QFDIV[2:0] | | | OUTFNC[1:0] | | SWPAB | HOMPOL | IDXPOL | QEBPOL | QEAPOL | HOME | INDEX | QEB | QEA | 000x |
| QEI1STAT | 01C4 | — | — | PCHEQIRQ | PCHEQIEN | PCLEQIRQ | PCLEQIEN | POSOVIRQ | POSOVIEN | PCIIRQ | PCIIEN | VELOVIRQ | VELOVIEN | HOMIRQ | HOMIEN | IDXIRQ | IDXIEN | 0000 |
| POS1CNTL | 01C6 | POSCNT[15:0] | | | | | | | | | | | | | | | | 0000 |
| POS1CNTH | 01C8 | POSCNT[31:16] | | | | | | | | | | | | | | | | 0000 |
| POS1HLD | 01CA | POSHLD[15:0] | | | | | | | | | | | | | | | | 0000 |
| VEL1CNT | 01CC | VELCNT[15:0] | | | | | | | | | | | | | | | | 0000 |
| INT1TMRL | 01CE | INTTMR[15:0] | | | | | | | | | | | | | | | | 0000 |
| INT1TMRH | 01D0 | INTTMR[31:16] | | | | | | | | | | | | | | | | 0000 |
| INT1HLDL | 01D2 | INTHLD[15:0] | | | | | | | | | | | | | | | | 0000 |
| INT1HLDH | 01D4 | INTHLD[31:16] | | | | | | | | | | | | | | | | 0000 |
| INDX1CNTL | 01D6 | INDXCNT[15:0] | | | | | | | | | | | | | | | | 0000 |
| INDX1CNTH | 01D8 | INDXCNT[31:16] | | | | | | | | | | | | | | | | 0000 |
| INDX1HLD | 01DA | INDXHLD[15:0] | | | | | | | | | | | | | | | | 0000 |
| QEI1GECL | 01DC | QEIGEC[15:0] | | | | | | | | | | | | | | | | 0000 |
| QEI1ICL | 01DC | QEIIC[15:0] | | | | | | | | | | | | | | | | 0000 |
| QEI1GECH | 01DE | QEIGEC[31:16] | | | | | | | | | | | | | | | | 0000 |
| QEI1ICH | 01DE | QEIIC[31:16] | | | | | | | | | | | | | | | | 0000 |
| QEI1LECL | 01E0 | QEILEC[15:0] | | | | | | | | | | | | | | | | 0000 |
| QEI1LECH | 01E2 | QEILEC[31:16] | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-17: I2C1 AND I2C2 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| I2C1RCV | 0200 | — | — | — | — | — | — | — | — | I2C1 Receive Register | | | | | | | | 0000 |
| I2C1TRN | 0202 | — | — | — | — | — | — | — | — | I2C1 Transmit Register | | | | | | | | 00FF |
| I2C1BRG | 0204 | — | — | — | — | — | — | — | Baud Rate Generator | | | | | | | | | 0000 |
| I2C1CON | 0206 | I2CEN | — | I2CSIDL | SCLREL | IPMIEN | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| I2C1STAT | 0208 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| I2C1ADD | 020A | — | — | — | — | — | — | I2C1 Address Register | | | | | | | | | | 0000 |
| I2C1MSK | 020C | — | — | — | — | — | — | I2C1 Address Mask Register | | | | | | | | | | 0000 |
| I2C2RCV | 0210 | — | — | — | — | — | — | — | — | I2C2 Receive Register | | | | | | | | 0000 |
| I2C2TRN | 0212 | — | — | — | — | — | — | — | — | I2C2 Transmit Register | | | | | | | | 00FF |
| I2C2BRG | 0214 | — | — | — | — | — | — | — | Baud Rate Generator | | | | | | | | | 0000 |
| I2C2CON | 0216 | I2CEN | — | I2CSIDL | SCLREL | IPMIEN | A10M | DISSLW | SMEN | GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN | 1000 |
| I2C2STAT | 0218 | ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 | IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF | 0000 |
| I2C2ADD | 021A | — | — | — | — | — | — | I2C2 Address Register | | | | | | | | | | 0000 |
| I2C2MSK | 021C | — | — | — | — | — | — | I2C2 Address Mask Register | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-18: UART1 AND UART2 REGISTER MAP**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| U1MODE | 0220 | UARTEN | — | USIDL | IREN | RTSMD | — | UEN[1:0] | | WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL[1:0] | | STSEL | 0000 |
| U1STA | 0222 | UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL[1:0] | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| U1TXREG | 0224 | — | — | — | — | — | — | — | UART1 Transmit Register | | | | | | | | | xxxx |
| U1RXREG | 0226 | — | — | — | — | — | — | — | UART1 Receive Register | | | | | | | | | 0000 |
| U1BRG | 0228 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |
| U2MODE | 0230 | UARTEN | — | USIDL | IREN | RTSMD | — | UEN[1:0] | | WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL[1:0] | | STSEL | 0000 |
| U2STA | 0232 | UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN | UTXBF | TRMT | URXISEL[1:0] | | ADDEN | RIDLE | PERR | FERR | OERR | URXDA | 0110 |
| U2TXREG | 0234 | — | — | — | — | — | — | — | UART2 Transmit Register | | | | | | | | | xxxx |
| U2RXREG | 0236 | — | — | — | — | — | — | — | UART2 Receive Register | | | | | | | | | 0000 |
| U2BRG | 0238 | Baud Rate Generator Prescaler | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-19: SPI1 AND SPI2 REGISTER MAP**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SPI1STAT | 0240 | SPIEN | — | SPISIDL | — | — | SPIBEC[2:0] | | | SRMPT | SPIROV | SRXMPT | SISEL[2:0] | | | SPITBF | SPIRBF | 0000 |
| SPI1CON1 | 0242 | — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | SPRE[2:0] | | | PPRE[1:0] | | 0000 |
| SPI1CON2 | 0244 | FRMEN | SPIFSD | FRMPOL | — | — | — | — | — | — | — | — | — | — | — | FRMDLY | SPIBEN | 0000 |
| SPI1BUF | 0248 | SPI1 Transmit and Receive Buffer Register | | | | | | | | | | | | | | | | 0000 |
| SPI2STAT | 0260 | SPIEN | — | SPISIDL | — | — | SPIBEC[2:0] | | | SRMPT | SPIROV | SRXMPT | SISEL[2:0] | | | SPITBF | SPIRBF | 0000 |
| SPI2CON1 | 0262 | — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE | SSEN | CKP | MSTEN | SPRE[2:0] | | | PPRE[1:0] | | 0000 |
| SPI2CON2 | 0264 | FRMEN | SPIFSD | FRMPOL | — | — | — | — | — | — | — | — | — | — | — | FRMDLY | SPIBEN | 0000 |
| SPI2BUF | 0268 | SPI2 Transmit and Receive Buffer Register | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-20: ADC1 REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC1BUF0 | 0300 | ADC1 Data Buffer 0 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF1 | 0302 | ADC1 Data Buffer 1 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF2 | 0304 | ADC1 Data Buffer 2 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF3 | 0306 | ADC1 Data Buffer 3 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF4 | 0308 | ADC1 Data Buffer 4 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF5 | 030A | ADC1 Data Buffer 5 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF6 | 030C | ADC1 Data Buffer 6 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF7 | 030E | ADC1 Data Buffer 7 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF8 | 0310 | ADC1 Data Buffer 8 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUF9 | 0312 | ADC1 Data Buffer 9 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFA | 0314 | ADC1 Data Buffer 10 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFB | 0316 | ADC1 Data Buffer 11 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFC | 0318 | ADC1 Data Buffer 12 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFD | 031A | ADC1 Data Buffer 13 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFE | 031C | ADC1 Data Buffer 14 | | | | | | | | | | | | | | | | xxxx |
| ADC1BUFF | 031E | ADC1 Data Buffer 15 | | | | | | | | | | | | | | | | xxxx |
| AD1CON1 | 0320 | ADON | — | ADSIDL | ADDMABM | — | AD12B | FORM[1:0] | | SSRC[2:0] | | | SSRCG | SIMSAM | ASAM | SAMP | DONE | 0000 |
| AD1CON2 | 0322 | VCFG[2:0] | | | — | — | CSCNA | CHPS[1:0] | | BUFS | SMPI[4:0] | | | | | BUFM | ALTS | 0000 |
| AD1CON3 | 0324 | ADRC | — | — | SAMC[4:0] | | | | | ADCS[7:0] | | | | | | | | 0000 |
| AD1CHS123 | 0326 | — | — | — | — | — | CH123NB[1:0] | | CH123SB | — | — | — | — | — | CH123NA[1:0] | | CH123SA | 0000 |
| AD1CHS0 | 0328 | CH0NB | — | — | CH0SB[4:0] | | | | | CH0NA | — | — | CH0SA[4:0] | | | | | 0000 |
| AD1CSSH | 032E | CSS[31:30] | | — | — | — | CSS[26:24] | | | — | — | — | — | — | — | — | — | 0000 |
| AD1CSSL | 0330 | CSS[15:0] | | | | | | | | | | | | | | | | 0000 |
| AD1CON4 | 0332 | — | — | — | — | — | — | — | ADDMAEN | — | — | — | — | — | DMABL[2:0] | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-21: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1[0]) = 0 OR 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C1CTRL1 | 0400 | — | — | CSIDL | ABAT | CANCKS | REQOP[2:0] | | | OPMODE[2:0] | | | — | CANCAP | — | — | WIN | 0480 |
| C1CTRL2 | 0402 | — | — | — | — | — | — | — | — | — | — | — | DNCNT[4:0] | | | | | 0000 |
| C1VEC | 0404 | — | — | — | FILHIT[4:0] | | | | | — | ICODE[6:0] | | | | | | | 0040 |
| C1FCTRL | 0406 | DMABS[2:0] | | | — | — | — | — | — | — | — | — | FSA[4:0] | | | | | 0000 |
| C1FIFO | 0408 | — | — | FBP[5:0] | | | | | | — | — | FNRB[5:0] | | | | | | 0000 |
| C1INTF | 040A | — | — | TXBO | TXBP | RXBP | TXWAR | RXWAR | EWARN | IVRIF | WAKIF | ERRIF | — | FIFOIF | RBOVIF | RBIF | TBIF | 0000 |
| C1INTE | 040C | — | — | — | — | — | — | — | — | IVRIE | WAKIE | ERRIE | — | FIFOIE | RBOVIE | RBIE | TBIE | 0000 |
| C1EC | 040E | TERRCNT[7:0] | | | | | | | | RERRCNT[7:0] | | | | | | | | 0000 |
| C1CFG1 | 0410 | — | — | — | — | — | — | — | — | SJW[1:0] | | BRP[5:0] | | | | | | 0000 |
| C1CFG2 | 0412 | — | WAKFIL | — | — | — | SEG2PH[2:0] | | | SEG2PHTS | SAM | SEG1PH[2:0] | | | PRSEG[2:0] | | | 0000 |
| C1FEN1 | 0414 | FLTEN[15:0] | | | | | | | | | | | | | | | | FFFF |
| C1FMSKSEL1 | 0418 | F7MSK[1:0] | | F6MSK[1:0] | | F5MSK[1:0] | | F4MSK[1:0] | | F3MSK[1:0] | | F2MSK[1:0] | | F1MSK[1:0] | | F0MSK[1:0] | | 0000 |
| C1FMSKSEL2 | 041A | F15MSK[1:0] | | F14MSK[1:0] | | F13MSK[1:0] | | F12MSK[1:0] | | F11MSK[1:0] | | F10MSK[1:0] | | F9MSK[1:0] | | F8MSK[1:0] | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-22: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1[0]) = 0 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0400-041E | See definition when WIN = x | | | | | | | | | | | | | | | | |
| C1RXFUL1 | 0420 | RXFUL[15:0] | | | | | | | | | | | | | | | | 0000 |
| C1RXFUL2 | 0422 | RXFUL[31:16] | | | | | | | | | | | | | | | | 0000 |
| C1RXOVF1 | 0428 | RXOVF[15:0] | | | | | | | | | | | | | | | | 0000 |
| C1RXOVF2 | 042A | RXOVF[31:16] | | | | | | | | | | | | | | | | 0000 |
| C1TR01CON | 0430 | TXEN1 | TXABT1 | TXLARB1 | TXERR1 | TXREQ1 | RTREN1 | TX1PRI[1:0] | | TXEN0 | TXABAT0 | TXLARB0 | TXERR0 | TXREQ0 | RTREN0 | TX0PRI[1:0] | | 0000 |
| C1TR23CON | 0432 | TXEN3 | TXABT3 | TXLARB3 | TXERR3 | TXREQ3 | RTREN3 | TX3PRI[1:0] | | TXEN2 | TXABAT2 | TXLARB2 | TXERR2 | TXREQ2 | RTREN2 | TX2PRI[1:0] | | 0000 |
| C1TR45CON | 0434 | TXEN5 | TXABT5 | TXLARB5 | TXERR5 | TXREQ5 | RTREN5 | TX5PRI[1:0] | | TXEN4 | TXABAT4 | TXLARB4 | TXERR4 | TXREQ4 | RTREN4 | TX4PRI[1:0] | | 0000 |
| C1TR67CON | 0436 | TXEN7 | TXABT7 | TXLARB7 | TXERR7 | TXREQ7 | RTREN7 | TX7PRI[1:0] | | TXEN6 | TXABAT6 | TXLARB6 | TXERR6 | TXREQ6 | RTREN6 | TX6PRI[1:0] | | xxxx |
| C1RXD | 0440 | ECAN1 Receive Data Word | | | | | | | | | | | | | | | | xxxx |
| C1TXD | 0442 | ECAN1 Transmit Data Word | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-23: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1[0]) = 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0400-041E | See definition when WIN = x | | | | | | | | | | | | | | | | |
| C1BUFPNT1 | 0420 | F3BP[3:0] | | | | F2BP[3:0] | | | | F1BP[3:0] | | | | F0BP[3:0] | | | | 0000 |
| C1BUFPNT2 | 0422 | F7BP[3:0] | | | | F6BP[3:0] | | | | F5BP[3:0] | | | | F4BP[3:0] | | | | 0000 |
| C1BUFPNT3 | 0424 | F11BP[3:0] | | | | F10BP[3:0] | | | | F9BP[3:0] | | | | F8BP[3:0] | | | | 0000 |
| C1BUFPNT4 | 0426 | F15BP[3:0] | | | | F14BP[3:0] | | | | F13BP[3:0] | | | | F12BP[3:0] | | | | 0000 |
| C1RXM0SID | 0430 | SID[10:3] | | | | | | | | SID[2:0] | | | — | MIDE | — | EID[17:16] | | xxxx |
| C1RXM0EID | 0432 | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXM1SID | 0434 | SID[10:3] | | | | | | | | SID[2:0] | | | — | MIDE | — | EID[17:16] | | xxxx |
| C1RXM1EID | 0436 | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXM2SID | 0438 | SID[10:3] | | | | | | | | SID[2:0] | | | — | MIDE | — | EID[17:16] | | xxxx |
| C1RXM2EID | 043A | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF0SID | 0440 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF0EID | 0442 | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF1SID | 0444 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF1EID | 0446 | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF2SID | 0448 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF2EID | 044A | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF3SID | 044C | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF3EID | 044E | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF4SID | 0450 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF4EID | 0452 | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF5SID | 0454 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF5EID | 0456 | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF6SID | 0458 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF6EID | 045A | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF7SID | 045C | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF7EID | 045E | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF8SID | 0460 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF8EID | 0462 | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF9SID | 0464 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF9EID | 0466 | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF10SID | 0468 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF10EID | 046A | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF11SID | 046C | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-23: ECAN1 REGISTER MAP WHEN WIN (C1CTRL1[0]) = 1 FOR dsPIC33EPXXXMC/GP50X DEVICES ONLY (CONTINUED)**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C1RXF11EID | 046E | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF12SID | 0470 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF12EID | 0472 | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF13SID | 0474 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF13EID | 0476 | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF14SID | 0478 | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF14EID | 047A | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |
| C1RXF15SID | 047C | SID[10:3] | | | | | | | | SID[2:0] | | | — | EXIDE | — | EID[17:16] | | xxxx |
| C1RXF15EID | 047E | EID[15:8] | | | | | | | | EID[7:0] | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-24: CRC REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CRCCON1 | 0640 | CRCEN | — | CSIDL | VWORD[4:0] | | | | | CRCFUL | CRCMPT | CRCISEL | CRCGO | LENDIAN | — | — | — | 0000 |
| CRCCON2 | 0642 | — | — | — | DWIDTH[4:0] | | | | | — | — | — | PLEN[4:0] | | | | | 0000 |
| CRCXORL | 0644 | X[15:1] | | | | | | | | | | | | | | | — | 0000 |
| CRCXORH | 0646 | X[31:16] | | | | | | | | | | | | | | | | 0000 |
| CRCDATL | 0648 | CRC Data Input Low Word | | | | | | | | | | | | | | | | 0000 |
| CRCDATH | 064A | CRC Data Input High Word | | | | | | | | | | | | | | | | 0000 |
| CRCWDATL | 064C | CRC Result Low Word | | | | | | | | | | | | | | | | 0000 |
| CRCWDATH | 064E | CRC Result High Word | | | | | | | | | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Shaded bits are not used in the operation of the programmable CRC module.

**TABLE 4-25: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC202/502 AND PIC24EPXXXGP/MC202 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPOR0 | 0680 | — | — | RP35R[5:0] | | | | | | — | — | RP20R[5:0] | | | | | | 0000 |
| RPOR1 | 0682 | — | — | RP37R[5:0] | | | | | | — | — | RP36R[5:0] | | | | | | 0000 |
| RPOR2 | 0684 | — | — | RP39R[5:0] | | | | | | — | — | RP38R[5:0] | | | | | | 0000 |
| RPOR3 | 0686 | — | — | RP41R[5:0] | | | | | | — | — | RP40R[5:0] | | | | | | 0000 |
| RPOR4 | 0688 | — | — | RP43R[5:0] | | | | | | — | — | RP42R[5:0] | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-26: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC203/503 AND PIC24EPXXXGP/MC203 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPOR0 | 0680 | — | — | RP35R[5:0] | | | | | | — | — | RP20R[5:0] | | | | | | 0000 |
| RPOR1 | 0682 | — | — | RP37R[5:0] | | | | | | — | — | RP36R[5:0] | | | | | | 0000 |
| RPOR2 | 0684 | — | — | RP39R[5:0] | | | | | | — | — | RP38R[5:0] | | | | | | 0000 |
| RPOR3 | 0686 | — | — | RP41R[5:0] | | | | | | — | — | RP40R[5:0] | | | | | | 0000 |
| RPOR4 | 0688 | — | — | RP43R[5:0] | | | | | | — | — | RP42R[5:0] | | | | | | 0000 |
| RPOR5 | 068A | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| RPOR6 | 068C | — | — | — | — | — | — | — | — | — | — | RP56R[5:0] | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-27: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC204/504 AND PIC24EPXXXGP/MC204 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPOR0 | 0680 | — | — | RP35R[5:0] | | | | | | — | — | RP20R[5:0] | | | | | | 0000 |
| RPOR1 | 0682 | — | — | RP37R[5:0] | | | | | | — | — | RP36R[5:0] | | | | | | 0000 |
| RPOR2 | 0684 | — | — | RP39R[5:0] | | | | | | — | — | RP38R[5:0] | | | | | | 0000 |
| RPOR3 | 0686 | — | — | RP41R[5:0] | | | | | | — | — | RP40R[5:0] | | | | | | 0000 |
| RPOR4 | 0688 | — | — | RP43R[5:0] | | | | | | — | — | RP42R[5:0] | | | | | | 0000 |
| RPOR5 | 068A | — | — | RP55R[5:0] | | | | | | — | — | RP54R[5:0] | | | | | | 0000 |
| RPOR6 | 068C | — | — | RP57R[5:0] | | | | | | — | — | RP56R[5:0] | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-28: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGP/MC206/506 AND PIC24EPXXXGP/MC206 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPOR0 | 0680 | — | — | RP35R[5:0] | | | | | | — | — | RP20R[5:0] | | | | | | 0000 |
| RPOR1 | 0682 | — | — | RP37R[5:0] | | | | | | — | — | RP36R[5:0] | | | | | | 0000 |
| RPOR2 | 0684 | — | — | RP39R[5:0] | | | | | | — | — | RP38R[5:0] | | | | | | 0000 |
| RPOR3 | 0686 | — | — | RP41R[5:0] | | | | | | — | — | RP40R[5:0] | | | | | | 0000 |
| RPOR4 | 0688 | — | — | RP43R[5:0] | | | | | | — | — | RP42R[5:0] | | | | | | 0000 |
| RPOR5 | 068A | — | — | RP55R[5:0] | | | | | | — | — | RP54R[5:0] | | | | | | 0000 |
| RPOR6 | 068C | — | — | RP57R[5:0] | | | | | | — | — | RP56R[5:0] | | | | | | 0000 |
| RPOR7 | 068E | — | — | RP97R[5:0] | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPOR8 | 0690 | — | — | RP118R[5:0] | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPOR9 | 0692 | — | — | — | — | — | — | — | — | — | — | RP120R[5:0] | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-29: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R[6:0] | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R[6:0] | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR[6:0] | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R[6:0] | | | | | | | — | IC1R[6:0] | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R[6:0] | | | | | | | — | IC3R[6:0] | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR[6:0] | | | | | | | 0000 |
| RPINR12 | 06B8 | — | FLT2R[6:0] | | | | | | | — | FLT1R[6:0] | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R[6:0] | | | | | | | — | QEA1R[6:0] | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R[6:0] | | | | | | | — | INDX1R[6:0] | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR[6:0] | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR[6:0] | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2INR[6:0] | | | | | | | — | SDI2R[6:0] | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R[6:0] | | | | | | | 0000 |
| RPINR26 | 06D4 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| RPINR37 | 06EA | — | SYNCI1R[6:0] | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR38 | 06EC | — | DTCMP1R[6:0] | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR39 | 06EE | — | DTCMP3R[6:0] | | | | | | | — | DTCMP2R[6:0] | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-30: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R[6:0] | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R[6:0] | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR[6:0] | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R[6:0] | | | | | | | — | IC1R[6:0] | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R[6:0] | | | | | | | — | IC3R[6:0] | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR[6:0] | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR[6:0] | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR[6:0] | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2INR[6:0] | | | | | | | — | SDI2R[6:0] | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R[6:0] | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-31: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R[6:0] | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R[6:0] | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR[6:0] | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R[6:0] | | | | | | | — | IC1R[6:0] | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R[6:0] | | | | | | | — | IC3R[6:0] | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR[6:0] | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR[6:0] | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR[6:0] | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2INR[6:0] | | | | | | | — | SDI2R[6:0] | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R[6:0] | | | | | | | 0000 |
| RPINR26 | 06D4 | — | — | — | — | — | — | — | — | — | C1RXR[6:0] | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-32: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R[6:0] | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R[6:0] | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR[6:0] | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R[6:0] | | | | | | | — | IC1R[6:0] | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R[6:0] | | | | | | | — | IC3R[6:0] | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR[6:0] | | | | | | | 0000 |
| RPINR12 | 06B8 | — | FLT2R[6:0] | | | | | | | — | FLT1R[6:0] | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R[6:0] | | | | | | | — | QEA1R[6:0] | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R[6:0] | | | | | | | — | INDX1R[6:0] | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR[6:0] | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR[6:0] | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2INR[6:0] | | | | | | | — | SDI2R[6:0] | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R[6:0] | | | | | | | 0000 |
| RPINR26 | 06D4 | — | — | — | — | — | — | — | — | — | C1RXR[6:0] | | | | | | | 0000 |
| RPINR37 | 06EA | — | SYNCI1R[6:0] | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR38 | 06EC | — | DTCMP1R[6:0] | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR39 | 06EE | — | DTCMP3R[6:0] | | | | | | | — | DTCMP2R[6:0] | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-33: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R[6:0] | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R[6:0] | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR[6:0] | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R[6:0] | | | | | | | — | IC1R[6:0] | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R[6:0] | | | | | | | — | IC3R[6:0] | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR[6:0] | | | | | | | 0000 |
| RPINR12 | 06B8 | — | FLT2R[6:0] | | | | | | | — | FLT1R[6:0] | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R[6:0] | | | | | | | — | QEA1R[6:0] | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R[6:0] | | | | | | | — | INDX1R[6:0] | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR[6:0] | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR[6:0] | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2INR[6:0] | | | | | | | — | SDI2R[6:0] | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R[6:0] | | | | | | | 0000 |
| RPINR37 | 06EA | — | SYNCI1R[6:0] | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR38 | 06EC | — | DTCMP1R[6:0] | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR39 | 06EE | — | DTCMP3R[6:0] | | | | | | | — | DTCMP2R[6:0] | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-34: NVM REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NVMCON | 0728 | WR | WREN | WRERR | NVMSIDL | — | — | — | — | — | — | — | — | NVMOP[3:0] | | | | 0000 |
| NVMADRL | 072A | NVMADR[15:0] | | | | | | | | | | | | | | | | 0000 |
| NVMADRH | 072C | — | — | — | — | — | — | — | — | NVMADR[23:16] | | | | | | | | 0000 |
| NVMKEY | 072E | — | — | — | — | — | — | — | — | NVMKEY[7:0] | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-35: SYSTEM CONTROL REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RCON | 0740 | TRAPR | IOPUWR | — | — | VREGSF | — | CM | VREGS | EXTR | SWR | SWDTEN | WDTO | SLEEP | IDLE | BOR | POR | Note 1 |
| OSCCON | 0742 | — | COSC[2:0] | | | — | NOSC[2:0] | | | CLKLOCK | IOLOCK | LOCK | — | CF | — | — | OSWEN | Note 2 |
| CLKDIV | 0744 | ROI | DOZE[2:0] | | | DOZEN | FRCDIV[2:0] | | | PLLPOST[1:0] | | — | PLLPRE[4:0] | | | | | 3040 |
| PLLFBD | 0746 | — | — | — | — | — | — | — | PLLDIV[8:0] | | | | | | | | | 0030 |
| OSCTUN | 0748 | — | — | — | — | — | — | — | — | — | — | TUN[5:0] | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
**Note 1:** RCON register Reset values are dependent on the type of Reset.
**2:** OSCCON register Reset values are dependent on the Configuration Fuses.

**TABLE 4-36: REFERENCE CLOCK REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REFOCON | 074E | ROON | — | ROSSLP | ROSEL | RODIV[3:0] | | | | — | — | — | — | — | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-37: PMD REGISTER MAP FOR PIC24EPXXXGP20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | — | — | — | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | — | — | AD1MD | 0000 |
| PMD2 | 0762 | — | — | — | — | IC4MD | IC3MD | IC2MD | IC1MD | — | — | — | — | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | — | — | — | — | — | CMPMD | — | — | CRCMD | — | — | — | — | — | I2C2MD | — | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | — | — | REFOMD | CTMUMD | — | — | 0000 |
| PMD6 | 076A | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | — | — | — | DMA0MD<br>DMA1MD<br>DMA2MD<br>DMA3MD | PTGMD | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-38: PMD REGISTER MAP FOR PIC24EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | QEI1MD | PWMMD | — | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | — | — | AD1MD | 0000 |
| PMD2 | 0762 | — | — | — | — | IC4MD | IC3MD | IC2MD | IC1MD | — | — | — | — | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | — | — | — | — | — | CMPMD | — | — | CRCMD | — | — | — | — | — | I2C2MD | — | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | — | — | REFOMD | CTMUMD | — | — | 0000 |
| PMD6 | 076A | — | — | — | — | — | PWM3MD | PWM2MD | PWM1MD | — | — | — | — | — | — | — | — | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | — | — | — | DMA0MD<br>DMA1MD<br>DMA2MD<br>DMA3MD | PTGMD | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-39: PMD REGISTER MAP FOR dsPIC33EPXXXGP50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | — | — | — | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | — | C1MD | AD1MD | 0000 |
| PMD2 | 0762 | — | — | — | — | IC4MD | IC3MD | IC2MD | IC1MD | — | — | — | — | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | — | — | — | — | — | CMPMD | — | — | CRCMD | — | — | — | — | — | I2C2MD | — | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | — | — | REFOMD | CTMUMD | — | — | 0000 |
| PMD6 | 076A | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | — | — | — | DMA0MD<br>DMA1MD<br>DMA2MD<br>DMA3MD | PTGMD | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-40: PMD REGISTER MAP FOR dsPIC33EPXXXMC50X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | QEI1MD | PWMMD | — | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | — | C1MD | AD1MD | 0000 |
| PMD2 | 0762 | — | — | — | — | IC4MD | IC3MD | IC2MD | IC1MD | — | — | — | — | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | — | — | — | — | — | CMPMD | — | — | CRCMD | — | — | — | — | — | I2C2MD | — | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | — | — | REFOMD | CTMUMD | — | — | 0000 |
| PMD6 | 076A | — | — | — | — | — | PWM3MD | PWM2MD | PWM1MD | — | — | — | — | — | — | — | — | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | — | — | — | DMA0MD<br>DMA1MD<br>DMA2MD<br>DMA3MD | PTGMD | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-41: PMD REGISTER MAP FOR dsPIC33EPXXXMC20X DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0760 | T5MD | T4MD | T3MD | T2MD | T1MD | QEI1MD | PWMMD | — | I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | — | — | AD1MD | 0000 |
| PMD2 | 0762 | — | — | — | — | IC4MD | IC3MD | IC2MD | IC1MD | — | — | — | — | OC4MD | OC3MD | OC2MD | OC1MD | 0000 |
| PMD3 | 0764 | — | — | — | — | — | CMPMD | — | — | CRCMD | — | — | — | — | — | I2C2MD | — | 0000 |
| PMD4 | 0766 | — | — | — | — | — | — | — | — | — | — | — | — | REFOMD | CTMUMD | — | — | 0000 |
| PMD6 | 076A | — | — | — | — | — | PWM3MD | PWM2MD | PWM1MD | — | — | — | — | — | — | — | — | 0000 |
| PMD7 | 076C | — | — | — | — | — | — | — | — | — | — | — | DMA0MD<br>DMA1MD<br>DMA2MD<br>DMA3MD | PTGMD | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-42: OP AMP/COMPARATOR REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CMSTAT | 0A80 | PSIDL | — | — | — | C4EVT | C3EVT | C2EVT | C1EVT | — | — | — | — | C4OUT | C3OUT | C2OUT | C1OUT | 0000 |
| CVRCON | 0A82 | — | CVR2OE | — | — | — | VREFSEL | — | — | CVREN | CVR1OE | CVRR | CVRSS | CVR[3:0] | | | | 0000 |
| CM1CON | 0A84 | CON | COE | CPOL | — | — | OPMODE | CEVT | COUT | EVPOL[1:0] | | — | CREF | — | — | CCH[1:0] | | 0000 |
| CM1MSKSRC | 0A86 | — | — | — | — | SELSRCC[3:0] | | | | SELSRCB[3:0] | | | | SELSRCA[3:0] | | | | 0000 |
| CM1MSKCON | 0A88 | HLMS | — | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN | 0000 |
| CM1FLTR | 0A8A | — | — | — | — | — | — | — | — | — | CFSEL[2:0] | | | CFLTREN | CFDIV[2:0] | | | 0000 |
| CM2CON | 0A8C | CON | COE | CPOL | — | — | OPMODE | CEVT | COUT | EVPOL[1:0] | | — | CREF | — | — | CCH[1:0] | | 0000 |
| CM2MSKSRC | 0A8E | — | — | — | — | SELSRCC[3:0] | | | | SELSRCB[3:0] | | | | SELSRCA[3:0] | | | | 0000 |
| CM2MSKCON | 0A90 | HLMS | — | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN | 0000 |
| CM2FLTR | 0A92 | — | — | — | — | — | — | — | — | — | CFSEL[2:0] | | | CFLTREN | CFDIV[2:0] | | | 0000 |
| CM3CON(1) | 0A94 | CON | COE | CPOL | — | — | OPMODE | CEVT | COUT | EVPOL[1:0] | | — | CREF | — | — | CCH[1:0] | | 0000 |
| CM3MSKSRC(1) | 0A96 | — | — | — | — | SELSRCC[3:0] | | | | SELSRCB[3:0] | | | | SELSRCA[3:0] | | | | 0000 |
| CM3MSKCON(1) | 0A98 | HLMS | — | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN | 0000 |
| CM3FLTR(1) | 0A9A | — | — | — | — | — | — | — | — | — | CFSEL[2:0] | | | CFLTREN | CFDIV[2:0] | | | 0000 |
| CM4CON | 0A9C | CON | COE | CPOL | — | — | — | CEVT | COUT | EVPOL[1:0] | | — | CREF | — | — | CCH[1:0] | | 0000 |
| CM4MSKSRC | 0A9E | — | — | — | — | SELSRCC[3:0] | | | | SELSRCB[3:0] | | | | SELSRCA[3:0] | | | | 0000 |
| CM4MSKCON | 0AA0 | HLMS | — | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN | NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN | 0000 |
| CM4FLTR | 0AA2 | — | — | — | — | — | — | — | — | — | CFSEL[2:0] | | | CFLTREN | CFDIV[2:0] | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
**Note 1:** These registers are unavailable on dsPIC33EPXXXGP502/MC502/MC202 and PIC24EP256GP/MC202 (28-pin) devices.

**TABLE 4-43: CTMU REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CTMUCON1 | 033A | CTMUEN | — | CTMUSIDL | TGEN | EDGEN | EDGSEQEN | IDISSEN | CTTRIG | — | — | — | — | — | — | — | — | 0000 |
| CTMUCON2 | 033C | EDG1MOD | EDG1POL | EDG1SEL[3:0] | | | | EDG2STAT | EDG1STAT | EDG2MOD | EDG2POL | EDG2SEL[3:0] | | | | — | — | 0000 |
| CTMUICON | 033E | ITRIM[5:0] | | | | | | IRNG[1:0] | | — | — | — | — | — | — | — | — | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-44: JTAG INTERFACE REGISTER MAP**

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| JDATAH | 0FF0 | — | — | — | — | JDATAH[27:16] | | | | | | | | | | | | xxxx |
| JDATAL | 0FF2 | JDATAL[15:0] | | | | | | | | | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-45: DMAC REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DMA0CON | 0B00 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE[1:0] | | — | — | MODE[1:0] | | 0000 |
| DMA0REQ | 0B02 | FORCE | — | — | — | — | — | — | — | IRQSEL[7:0] | | | | | | | | 00FF |
| DMA0STAL | 0B04 | STA[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA0STAH | 0B06 | — | — | — | — | — | — | — | — | STA[23:16] | | | | | | | | 0000 |
| DMA0STBL | 0B08 | STB[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA0STBH | 0B0A | — | — | — | — | — | — | — | — | STB[23:16] | | | | | | | | 0000 |
| DMA0PAD | 0B0C | PAD[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA0CNT | 0B0E | — | — | CNT[13:0] | | | | | | | | | | | | | | 0000 |
| DMA1CON | 0B10 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE[1:0] | | — | — | MODE[1:0] | | 0000 |
| DMA1REQ | 0B12 | FORCE | — | — | — | — | — | — | — | IRQSEL[7:0] | | | | | | | | 00FF |
| DMA1STAL | 0B14 | STA[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA1STAH | 0B16 | — | — | — | — | — | — | — | — | STA[23:16] | | | | | | | | 0000 |
| DMA1STBL | 0B18 | STB[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA1STBH | 0B1A | — | — | — | — | — | — | — | — | STB[23:16] | | | | | | | | 0000 |
| DMA1PAD | 0B1C | PAD[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA1CNT | 0B1E | — | — | CNT[13:0] | | | | | | | | | | | | | | 0000 |
| DMA2CON | 0B20 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE[1:0] | | — | — | MODE[1:0] | | 0000 |
| DMA2REQ | 0B22 | FORCE | — | — | — | — | — | — | — | IRQSEL[7:0] | | | | | | | | 00FF |
| DMA2STAL | 0B24 | STA[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA2STAH | 0B26 | — | — | — | — | — | — | — | — | STA[23:16] | | | | | | | | 0000 |
| DMA2STBL | 0B28 | STB[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA2STBH | 0B2A | — | — | — | — | — | — | — | — | STB[23:16] | | | | | | | | 0000 |
| DMA2PAD | 0B2C | PAD[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA2CNT | 0B2E | — | — | CNT[13:0] | | | | | | | | | | | | | | 0000 |
| DMA3CON | 0B30 | CHEN | SIZE | DIR | HALF | NULLW | — | — | — | — | — | AMODE[1:0] | | — | — | MODE[1:0] | | 0000 |
| DMA3REQ | 0B32 | FORCE | — | — | — | — | — | — | — | IRQSEL[7:0] | | | | | | | | 00FF |
| DMA3STAL | 0B34 | STA[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA3STAH | 0B36 | — | — | — | — | — | — | — | — | STA[23:16] | | | | | | | | 0000 |
| DMA3STBL | 0B38 | STB[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA3STBH | 0B3A | — | — | — | — | — | — | — | — | STB[23:16] | | | | | | | | 0000 |
| DMA3PAD | 0B3C | PAD[15:0] | | | | | | | | | | | | | | | | 0000 |
| DMA3CNT | 0B3E | — | — | CNT[13:0] | | | | | | | | | | | | | | 0000 |
| DMAPWC | 0BF0 | — | — | — | — | — | — | — | — | — | — | — | — | PWCOL3 | PWCOL2 | PWCOL1 | PWCOL0 | 0000 |
| DMARQC | 0BF2 | — | — | — | — | — | — | — | — | — | — | — | — | RQCOL3 | RQCOL2 | RQCOL1 | RQCOL0 | 0000 |
| DMAPPS | 0BF4 | — | — | — | — | — | — | — | — | — | — | — | — | PPST3 | PPST2 | PPST1 | PPST0 | 0000 |
| DMALCA | 0BF6 | — | — | — | — | — | — | — | — | — | — | — | — | LSTCH[3:0] | | | | 000F |
| DSADRL | 0BF8 | DSADR[15:0] | | | | | | | | | | | | | | | | 0000 |
| DSADRH | 0BFA | — | — | — | — | — | — | — | — | DSADR[23:16] | | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-46: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 0E00 | — | — | — | TRISA[12:7] | | | | | | — | — | TRISA4 | — | — | TRISA[1:0] | | 1F93 |
| PORTA | 0E02 | — | — | — | RA[12:7] | | | | | | — | — | RA4 | — | — | RA[1:0] | | 0000 |
| LATA | 0E04 | — | — | — | LATA[12:7] | | | | | | — | — | LATA4 | — | — | LA1TA[1:0] | | 0000 |
| ODCA | 0E06 | — | — | — | ODCA[12:7] | | | | | | — | — | ODCA4 | — | — | ODCA[1:0] | | 0000 |
| CNENA | 0E08 | — | — | — | CNIEA[12:7] | | | | | | — | — | CNIEA4 | — | — | CNIEA[1:0] | | 0000 |
| CNPUA | 0E0A | — | — | — | CNPUA[12:7] | | | | | | — | — | CNPUA4 | — | — | CNPUA[1:0] | | 0000 |
| CNPDA | 0E0C | — | — | — | CNPDA[12:7] | | | | | | — | — | CNPDA4 | — | — | CNPDA[1:0] | | 0000 |
| ANSELA | 0E0E | — | — | — | ANSA[12:11] | | — | — | — | — | — | — | ANSA4 | — | — | ANSA[1:0] | | 1813 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-47: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 0E10 | TRISB[15:0] | | | | | | | | | | | | | | | | FFFF |
| PORTB | 0E12 | RB[15:0] | | | | | | | | | | | | | | | | xxxx |
| LATB | 0E14 | LATB[15:0] | | | | | | | | | | | | | | | | xxxx |
| ODCB | 0E16 | ODCB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNENB | 0E18 | CNIEB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNPUB | 0E1A | CNPUB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNPDB | 0E1C | CNPDB[15:0] | | | | | | | | | | | | | | | | 0000 |
| ANSELB | 0E1E | — | — | — | — | — | — | — | ANSB8 | — | — | — | — | ANSB[3:0] | | | | 010F |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-48: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISC | 0E20 | TRISC15 | — | TRISC[13:0] | | | | | | | | | | | | | | BFFF |
| PORTC | 0E22 | RC15 | — | RC[13:0] | | | | | | | | | | | | | | xxxx |
| LATC | 0E24 | LATC15 | — | LATC[13:0] | | | | | | | | | | | | | | xxxx |
| ODCC | 0E26 | ODCC15 | — | ODCC[13:0] | | | | | | | | | | | | | | 0000 |
| CNENC | 0E28 | CNIEC15 | — | CNIEC[13:0] | | | | | | | | | | | | | | 0000 |
| CNPUC | 0E2A | CNPUC15 | — | CNPUC[13:0] | | | | | | | | | | | | | | 0000 |
| CNPDC | 0E2C | CNPDC15 | — | CNPDC[13:0] | | | | | | | | | | | | | | 0000 |
| ANSELC | 0E2E | — | — | — | — | ANSC11 | — | — | — | — | — | — | — | — | ANSC[2:0] | | | 0807 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-49: PORTD REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISD | 0E30 | — | — | — | — | — | — | — | TRISD8 | — | TRISD[6:5] | | — | — | — | — | — | 0160 |
| PORTD | 0E32 | — | — | — | — | — | — | — | RD8 | — | RD[6:5] | | — | — | — | — | — | xxxx |
| LATD | 0E34 | — | — | — | — | — | — | — | LATD8 | — | LATD[6:5] | | — | — | — | — | — | xxxx |
| ODCD | 0E36 | — | — | — | — | — | — | — | ODCD8 | — | ODCD[6:5] | | — | — | — | — | — | 0000 |
| CNEND | 0E38 | — | — | — | — | — | — | — | CNIED8 | — | CNIED[6:5] | | — | — | — | — | — | 0000 |
| CNPUD | 0E3A | — | — | — | — | — | — | — | CNPUD8 | — | CNPUD[6:5] | | — | — | — | — | — | 0000 |
| CNPDD | 0E3C | — | — | — | — | — | — | — | CNPDD8 | — | CNPDD[6:5] | | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-50: PORTE REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISE | 0E40 | TRISE[15:12] | | | | — | — | — | — | — | — | — | — | — | — | — | — | F000 |
| PORTE | 0E42 | RE[15:12] | | | | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| LATE | 0E44 | LATE[15:12] | | | | — | — | — | — | — | — | — | — | — | — | — | — | xxxx |
| ODCE | 0E46 | ODCE[15:12] | | | | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNENE | 0E48 | CNIEE[15:12] | | | | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNPUE | 0E4A | CNPUE[15:12] | | | | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| CNPDE | 0E4C | CNPDE[15:12] | | | | — | — | — | — | — | — | — | — | — | — | — | — | 0000 |
| ANSELE | 0E4E | ANSE[15:12] | | | | — | — | — | — | — | — | — | — | — | — | — | — | F000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-51: PORTF REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISF | 0E50 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | TRISF[1:0] | | 0003 |
| PORTF | 0E52 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RF[1:0] | | xxxx |
| LATF | 0E54 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | LATF[1:0] | | xxxx |
| ODCF | 0E56 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ODCF[1:0] | | 0000 |
| CNENF | 0E58 | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CNIEF[1:0] | | 0000 |
| CNPUF | 0E5A | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CNPUF[1:0] | | 0000 |
| CNPDF | 0E5C | — | — | — | — | — | — | — | — | — | — | — | — | — | — | CNPDF[1:0] | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.


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**TABLE 4-52: PORTG REGISTER MAP FOR PIC24EPXXXGP/MC206 AND dsPIC33EPXXXGP/MC206/506 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISG | 0E60 | — | — | — | — | — | — | TRISG[9:6] | | | | — | — | — | — | — | — | 03C0 |
| PORTG | 0E62 | — | — | — | — | — | — | RG[9:6] | | | | — | — | — | — | — | — | xxxx |
| LATG | 0E64 | — | — | — | — | — | — | LATG[9:6] | | | | — | — | — | — | — | — | xxxx |
| ODCG | 0E66 | — | — | — | — | — | — | ODCG[9:6] | | | | — | — | — | — | — | — | 0000 |
| CNENG | 0E68 | — | — | — | — | — | — | CNIEG[9:6] | | | | — | — | — | — | — | — | 0000 |
| CNPUG | 0E6A | — | — | — | — | — | — | CNPUG[9:6] | | | | — | — | — | — | — | — | 0000 |
| CNPDG | 0E6C | — | — | — | — | — | — | CNPDG[9:6] | | | | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-53: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 0E00 | — | — | — | — | — | TRISA[10:7] | | | | — | — | TRISA[4:0] | | | | | 079F |
| PORTA | 0E02 | — | — | — | — | — | RA[10:7] | | | | — | — | RA[4:0] | | | | | 0000 |
| LATA | 0E04 | — | — | — | — | — | LATA[10:7] | | | | — | — | LATA[4:0] | | | | | 0000 |
| ODCA | 0E06 | — | — | — | — | — | ODCA[10:7] | | | | — | — | ODCA[4:0] | | | | | 0000 |
| CNENA | 0E08 | — | — | — | — | — | CNIEA[10:7] | | | | — | — | CNIEA[4:0] | | | | | 0000 |
| CNPUA | 0E0A | — | — | — | — | — | CNPUA[10:7] | | | | — | — | CNPUA[4:0] | | | | | 0000 |
| CNPDA | 0E0C | — | — | — | — | — | CNPDA[10:7] | | | | — | — | CNPDA[4:0] | | | | | 0000 |
| ANSELA | 0E0E | — | — | — | — | — | — | — | — | — | — | — | ANSA4 | — | — | ANSA[1:0] | | 0013 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-54: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 0E10 | TRISB[15:0] | | | | | | | | | | | | | | | | FFFF |
| PORTB | 0E12 | RB[15:0] | | | | | | | | | | | | | | | | xxxx |
| LATB | 0E14 | LATB[15:0] | | | | | | | | | | | | | | | | xxxx |
| ODCB | 0E16 | ODCB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNENB | 0E18 | CNIEB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNPUB | 0E1A | CNPUB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNPDB | 0E1C | CNPDB[15:0] | | | | | | | | | | | | | | | | 0000 |
| ANSELB | 0E1E | — | — | — | — | — | — | — | ANSB8 | — | — | — | — | ANSB[3:0] | | | | 010F |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-55: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC204 AND dsPIC33EPXXXGP/MC204/504 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISC | 0E20 | — | — | — | — | — | — | TRISC[9:0] | | | | | | | | | | 03FF |
| PORTC | 0E22 | — | — | — | — | — | — | RC[9:0] | | | | | | | | | | xxxx |
| LATC | 0E24 | — | — | — | — | — | — | LATC[9:0] | | | | | | | | | | xxxx |
| ODCC | 0E26 | — | — | — | — | — | — | ODCC[9:0] | | | | | | | | | | 0000 |
| CNENC | 0E28 | — | — | — | — | — | — | CNIEC[9:0] | | | | | | | | | | 0000 |
| CNPUC | 0E2A | — | — | — | — | — | — | CNPUC[9:0] | | | | | | | | | | 0000 |
| CNPDC | 0E2C | — | — | — | — | — | — | CNPDC[9:0] | | | | | | | | | | 0000 |
| ANSELC | 0E2E | — | — | — | — | — | — | — | — | — | — | — | — | — | ANSC[2:0] | | | 0007 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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**TABLE 4-56: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 0E00 | — | — | — | — | — | — | — | TRISA8 | — | — | — | TRISA[4:0] | | | | | 011F |
| PORTA | 0E02 | — | — | — | — | — | — | — | RA8 | — | — | — | RA[4:0] | | | | | 0000 |
| LATA | 0E04 | — | — | — | — | — | — | — | LATA8 | — | — | — | LATA[4:0] | | | | | 0000 |
| ODCA | 0E06 | — | — | — | — | — | — | — | ODCA8 | — | — | — | ODCA[4:0] | | | | | 0000 |
| CNENA | 0E08 | — | — | — | — | — | — | — | CNIEA8 | — | — | — | CNIEA[4:0] | | | | | 0000 |
| CNPUA | 0E0A | — | — | — | — | — | — | — | CNPUA8 | — | — | — | CNPUA[4:0] | | | | | 0000 |
| CNPDA | 0E0C | — | — | — | — | — | — | — | CNPDA8 | — | — | — | CNPDA[4:0] | | | | | 0000 |
| ANSELA | 0E0E | — | — | — | — | — | — | — | — | — | — | — | ANSA4 | — | — | ANSA[1:0] | | 0013 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-57: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 0E10 | TRISB[15:0] | | | | | | | | | | | | | | | | FFFF |
| PORTB | 0E12 | RB[15:0] | | | | | | | | | | | | | | | | xxxx |
| LATB | 0E14 | LATB[15:0] | | | | | | | | | | | | | | | | xxxx |
| ODCB | 0E16 | ODCB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNENB | 0E18 | CNIEB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNPUB | 0E1A | CNPUB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNPDB | 0E1C | CNPDB[15:0] | | | | | | | | | | | | | | | | 0000 |
| ANSELB | 0E1E | — | — | — | — | — | — | — | ANSB8 | — | — | — | — | ANSB[3:0] | | | | 010F |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-58: PORTC REGISTER MAP FOR PIC24EPXXXGP/MC203 AND dsPIC33EPXXXGP/MC203/503 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISC | 0E20 | — | — | — | — | — | — | — | TRISC8 | — | — | — | — | — | — | TRISC[1:0] | | 0103 |
| PORTC | 0E22 | — | — | — | — | — | — | — | RC8 | — | — | — | — | — | — | RC[1:0] | | xxxx |
| LATC | 0E24 | — | — | — | — | — | — | — | LATC8 | — | — | — | — | — | — | LATC[1:0] | | xxxx |
| ODCC | 0E26 | — | — | — | — | — | — | — | ODCC8 | — | — | — | — | — | — | ODCC[1:0] | | 0000 |
| CNENC | 0E28 | — | — | — | — | — | — | — | CNIEC8 | — | — | — | — | — | — | CNIEC[1:0] | | 0000 |
| CNPUC | 0E2A | — | — | — | — | — | — | — | CNPUC8 | — | — | — | — | — | — | CNPUC[1:0] | | 0000 |
| CNPDC | 0E2C | — | — | — | — | — | — | — | CNPDC8 | — | — | — | — | — | — | CNPDC[1:0] | | 0000 |
| ANSELC | 0E2E | — | — | — | — | — | — | — | — | — | — | — | — | — | — | ANSC[1:0] | | 0003 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

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**TABLE 4-59: PORTA REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 0E00 | — | — | — | — | — | — | — | — | — | — | — | TRISA[4:0] | | | | | 001F |
| PORTA | 0E02 | — | — | — | — | — | — | — | — | — | — | — | RA[4:0] | | | | | 0000 |
| LATA | 0E04 | — | — | — | — | — | — | — | — | — | — | — | LATA[4:0] | | | | | 0000 |
| ODCA | 0E06 | — | — | — | — | — | — | — | — | — | — | — | ODCA[4:0] | | | | | 0000 |
| CNENA | 0E08 | — | — | — | — | — | — | — | — | — | — | — | CNIEA[4:0] | | | | | 0000 |
| CNPUA | 0E0A | — | — | — | — | — | — | — | — | — | — | — | CNPUA[4:0] | | | | | 0000 |
| CNPDA | 0E0C | — | — | — | — | — | — | — | — | — | — | — | CNPDA[4:0] | | | | | 0000 |
| ANSELA | 0E0E | — | — | — | — | — | — | — | — | — | — | — | ANSA4 | — | — | ANSA[1:0] | | 0013 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-60: PORTB REGISTER MAP FOR PIC24EPXXXGP/MC202 AND dsPIC33EPXXXGP/MC202/502 DEVICES ONLY**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 0E10 | TRISB[15:0] | | | | | | | | | | | | | | | | FFFF |
| PORTB | 0E12 | RB[15:0] | | | | | | | | | | | | | | | | xxxx |
| LATB | 0E14 | LATB[15:0] | | | | | | | | | | | | | | | | xxxx |
| ODCB | 0E16 | ODCB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNENB | 0E18 | CNIEB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNPUB | 0E1A | CNPUB[15:0] | | | | | | | | | | | | | | | | 0000 |
| CNPDB | 0E1C | CNPDB[15:0] | | | | | | | | | | | | | | | | 0000 |
| ANSELB | 0E1E | — | — | — | — | — | — | — | ANSB8 | — | — | — | — | ANSB[3:0] | | | | 010F |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.



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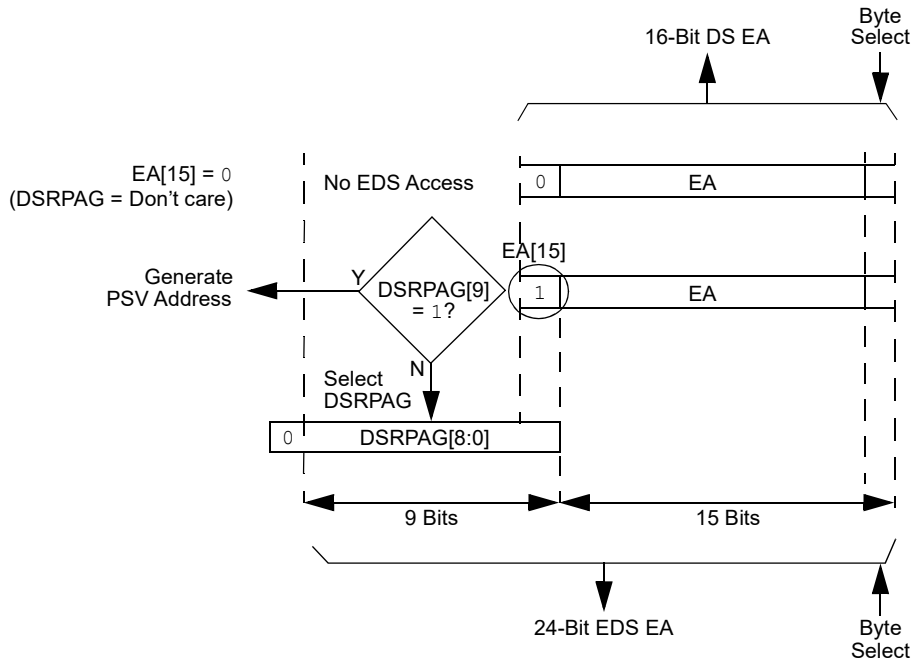
### 4.4.1 PAGED MEMORY SCHEME

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre-modified and post-modified Effective Addresses (EA). The upper half of the base Data Space address is used in conjunction with the Data Space Page registers, the 10-bit Read Page register (DSRPAG) or the 9-bit Write Page register (DSWPAG), to form an Extended Data Space (EDS) address or Program Space Visibility (PSV) address. The Data Space Page registers are located in the SFR space.

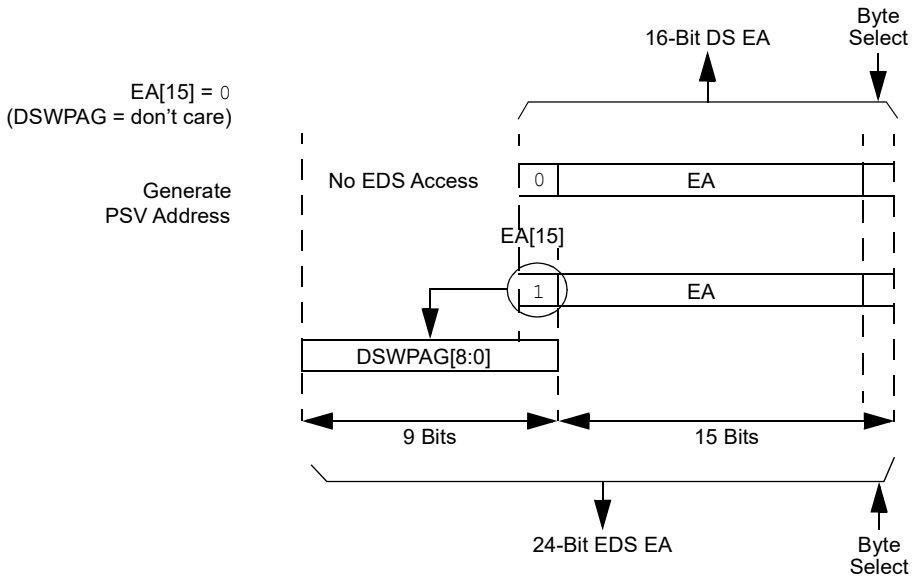
Construction of the EDS address is shown in Example 4-1. When DSRPAG[9] = 0 and the base address bit, EA[15] = 1, the DSRPAG[8:0] bits are concatenated onto EA[14:0] to form the 24-bit EDS read address. Similarly, when base address bit, EA[15] = 1, DSWPAG[8:0] are concatenated onto EA[14:0] to form the 24-bit EDS write address.

**EXAMPLE 4-1: EXTENDED DATA SPACE (EDS) READ ADDRESS GENERATION**




**Note:** DS read access when DSRPAG = 0x000 will force an address error trap.

**EXAMPLE 4-2: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION**




**Note:** DS read access when DSRPAG = 0x000 will force an address error trap.

The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Example 4-3.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.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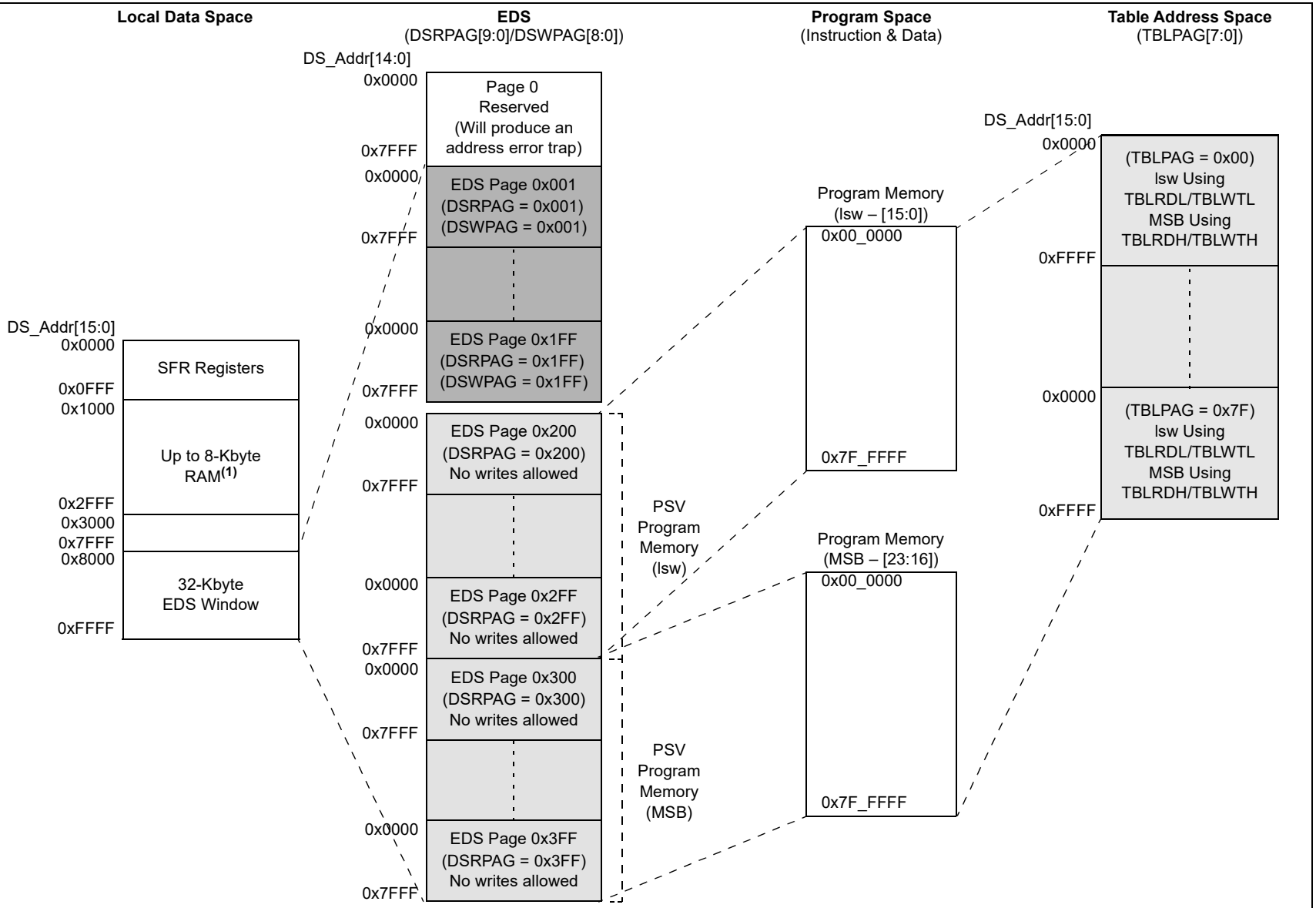
**EXAMPLE 4-3: PAGED DATA MEMORY SPACE**




**Note 1:** For 64K Flash devices. RAM size and end location is dependent on device; see **Section 4.2 "Data Address Space"** for more information.

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Allocating different Page registers for read and write access allows the architecture to support data movement between different pages in data memory. This is accomplished by setting the DSRPAG register value to the page from which you want to read, and configuring the DSWPAG register to the page to which it needs to be written. Data can also be moved from different PSV to EDS pages, by configuring the DSRPAG and DSWPAG registers to address PSV and EDS space, respectively. The data can be moved between pages by a single instruction.

When an EDS or PSV page overflow or underflow occurs, EA[15] is cleared as a result of the register indirect EA calculation. An overflow or underflow of the EA in the EDS or PSV pages can occur at the page boundaries when:

- The initial address prior to modification addresses an EDS or PSV page
- The EA calculation uses Pre-Modified or Post-Modified Register Indirect Addressing; however, this does not include Register Offset Addressing

In general, when an overflow is detected, the DSxPAG register is incremented and the EA[15] bit is set to keep the base address within the EDS or PSV window. When an underflow is detected, the DSxPAG register is decremented and the EA[15] bit is set to keep the base address within the EDS or PSV window. This creates a linear EDS and PSV address space, but only when using Register Indirect Addressing modes.

Exceptions to the operation described above arise when entering and exiting the boundaries of Page 0, EDS and PSV spaces. Table 4-61 lists the effects of overflow and underflow scenarios at different boundaries.

In the following cases, when overflow or underflow occurs, the EA[15] bit is set and the DSxPAG is not modified; therefore, the EA will wrap to the beginning of the current page:

- Register Indirect with Register Offset Addressing
- Modulo Addressing
- Bit-Reversed Addressing

**TABLE 4-61: OVERFLOW AND UNDERFLOW SCENARIOS AT PAGE 0, EDS and PSV SPACE BOUNDARIES(2,3,4)**

| O/U, R/W | Operation | Before | | | After | | |
|---|---|---|---|---|---|---|---|
| | | DSxPAG | DS EA[15] | Page Description | DSxPAG | DS EA[15] | Page Description |
| O, Read | [++Wn] or [Wn++] | DSRPAG = 0x1FF | 1 | EDS: Last page | DSRPAG = 0x1FF | 0 | See **Note 1** |
| O, Read | | DSRPAG = 0x2FF | 1 | PSV: Last lsw page | DSRPAG = 0x300 | 1 | PSV: First MSB page |
| O, Read | | DSRPAG = 0x3FF | 1 | PSV: Last MSB page | DSRPAG = 0x3FF | 0 | See **Note 1** |
| O, Write | | DSWPAG = 0x1FF | 1 | EDS: Last page | DSWPAG = 0x1FF | 0 | See **Note 1** |
| U, Read | [--Wn] or [Wn--] | DSRPAG = 0x001 | 1 | PSV page | DSRPAG = 0x001 | 0 | See **Note 1** |
| U, Read | | DSRPAG = 0x200 | 1 | PSV: First lsw page | DSRPAG = 0x200 | 0 | See **Note 1** |
| U, Read | | DSRPAG = 0x300 | 1 | PSV: First MSB page | DSRPAG = 0x2FF | 1 | PSV: Last lsw page |

**Legend:** O = Overflow, U = Underflow, R = Read, W = Write

**Note 1:** The Register Indirect Addressing now addresses a location in the base Data Space (0x0000-0x8000).

**2:** An EDS access with DSxPAG = 0x000 will generate an address error trap.

**3:** Only reads from PS are supported using DSRPAG. An attempt to write to PS using DSWPAG will generate an address error trap.

**4:** Pseudolinear Addressing is not supported for large offsets.


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### 4.4.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible regardless of the contents of the Data Space Page registers. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA[15] = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of base Data Space, in combination with DSRPAG = 0x000 or DSWPAG = 0x000. Consequently, DSRPAG and DSWPAG are initialized to 0x001 at Reset.

**Note 1:** DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.

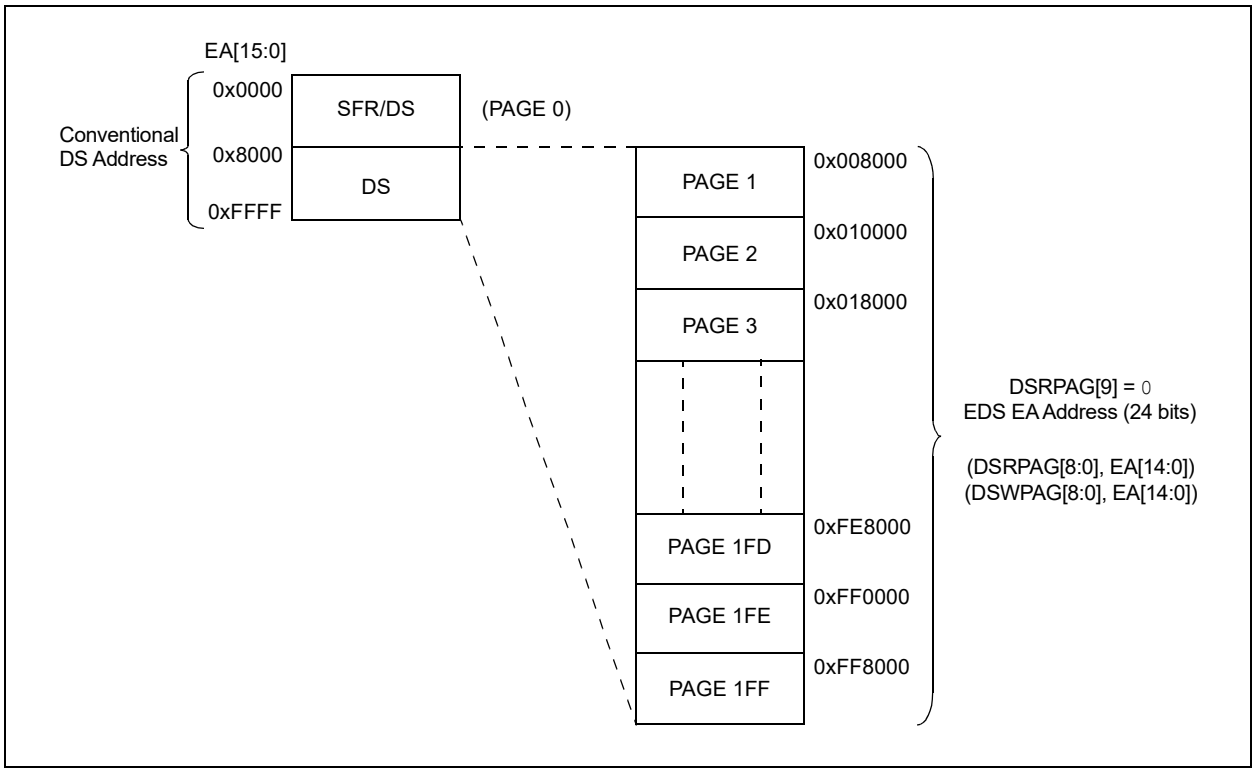
**2:** Clearing the DSxPAG in software has no effect.

The remaining pages, including both EDS and PSV pages, are only accessible using the DSRPAG or DSWPAG registers in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where base address bit, EA[15] = 1.

For example, when DSRPAG = 0x001 or DSWPAG = 0x001, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF, of the Data Space will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x002 or DSWPAG = 0x002, accesses to the upper 32 Kbytes of the Data Space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-17.

For more information on the PSV page access using Data Space Page registers, refer to the **"Program Space Visibility from Data Space"** section in **"dsPIC33/PIC24 Program Memory"** (www.microchip.com/DS70000613) of the *"dsPIC33/PIC24 Family Reference Manual"*.

**FIGURE 4-17: EDS MEMORY MAP**



### 4.4.3 DATA MEMORY ARBITRATION AND BUS MASTER PRIORITY

EDS accesses from bus masters in the system are arbitrated.

The arbiter for data memory (including EDS) arbitrates between the CPU, the DMA and the ICD module. In the event of coincidental access to a bus by the bus masters, the arbiter determines which bus master access has the highest priority. The other bus masters are suspended and processed after the access of the bus by the bus master with the highest priority.

By default, the CPU is Bus Master 0 (M0) with the highest priority and the ICD is Bus Master 4 (M4) with the lowest priority. The remaining bus master (DMA Controller) is allocated to M3 (M1 and M2 are reserved and cannot be used). The user application may raise or lower the priority of the DMA Controller to be above that of the CPU by setting the appropriate bits in the EDS Bus Master Priority Control (MSTRPR) register. All bus masters with raised priorities will maintain the same priority relationship relative to each other (i.e., M1 being highest and M3 being lowest, with M2 in between). Also, all the bus masters with priorities below that of the CPU maintain the same priority relationship relative to each other. The priority schemes for bus masters with different MSTRPR values are tabulated in Table 4-62.

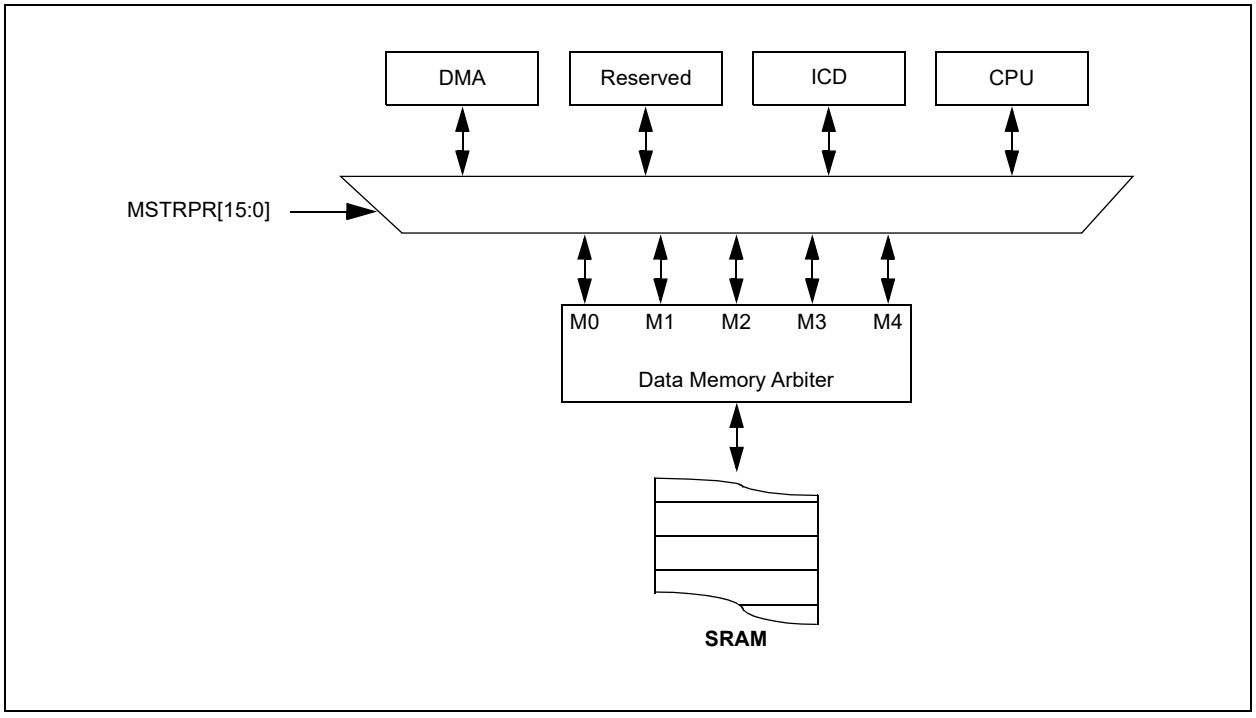
This bus master priority control allows the user application to manipulate the real-time response of the system, either statically during initialization or dynamically in response to real-time events.

**TABLE 4-62: DATA MEMORY BUS ARBITER PRIORITY**

| Priority | MSTRPR[15:0] Bits Setting(1) | |
|---|---|---|
| | 0x0000 | 0x0020 |
| M0 (highest) | CPU | DMA |
| M1 | Reserved | CPU |
| M2 | Reserved | Reserved |
| M3 | DMA | Reserved |
| M4 (lowest) | ICD | ICD |

**Note 1:** All other values of MSTRPR[15:0] are reserved.

**FIGURE 4-18: ARBITER ARCHITECTURE**





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### 4.4.4 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

**Note:** To protect against misaligned stack accesses, W15[0] is fixed to '0' by the hardware.

W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

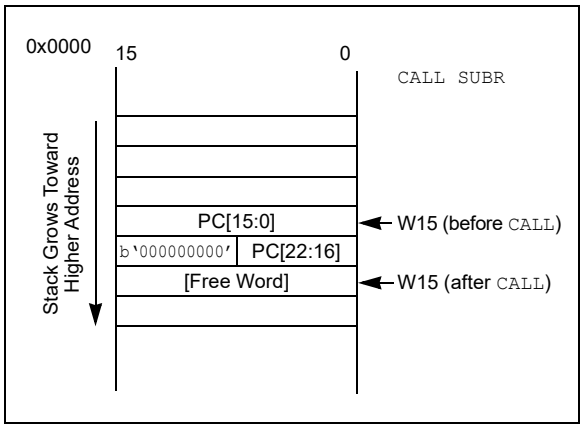
The Software Stack Pointer always points to the first available free word and fills the software stack working from lower toward higher addresses. Figure 4-19 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC[15:0] are pushed onto the first available stack word, then PC[22:16] are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-19. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

**Note 1:** To maintain system Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).

**2:** As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a C development environment

**FIGURE 4-19: CALL STACK FRAME**



## 4.5 Instruction Addressing Modes

The addressing modes shown in Table 4-63 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

### 4.5.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

### 4.5.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

```
Operand 3 = Operand 1 [function] Operand 2
```

where Operand 1 is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

**Note:** Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

**TABLE 4-63: FUNDAMENTAL ADDRESSING MODES SUPPORTED**

| Addressing Mode | Description |
|---|---|
| File Register Direct | The address of the file register is specified explicitly. |
| Register Direct | The contents of a register are accessed directly. |
| Register Indirect | The contents of Wn form the Effective Address (EA). |
| Register Indirect Post-Modified | The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value. |
| Register Indirect Pre-Modified | Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA. |
| Register Indirect with Register Offset (Register Indexed) | The sum of Wn and Wb forms the EA. |
| Register Indirect with Literal Offset | The sum of Wn and a literal forms the EA. |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### 4.5.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions, which apply to dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, and the DSP accumulator class of instructions, which apply to the dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

| | |
|---|---|
| **Note:** | For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one). |

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

| | |
|---|---|
| **Note:** | Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes. |

### 4.5.4 MAC INSTRUCTIONS (dsPIC33EPXXXMC20X/50X AND dsPIC33EPXXXGP50X DEVICES ONLY)

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The Two-Source Operand Prefetch registers must be members of the set: {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

| | |
|---|---|
| **Note:** | Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space). |

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

### 4.5.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

## 4.6 Modulo Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

| **Note:** | Modulo Addressing has address alignment restrictions for the buffer start or end address. See the **"Data Memory"** FRM (www.microchip.com/DS70595) for more information. |
|---|---|

### 4.6.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified, and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

| **Note:** | Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear). |
|---|---|

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

### 4.6.2 W ADDRESS REGISTER SELECTION

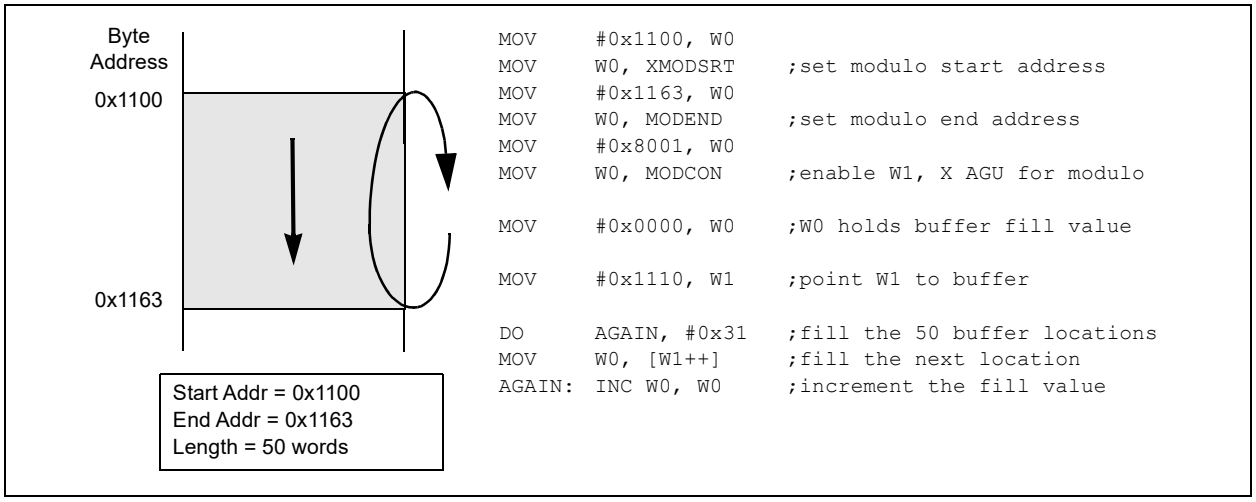
The Modulo and Bit-Reversed Addressing Control register, MODCON[15:0], contains enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = `1111`, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = `1111`, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM), to which Modulo Addressing is to be applied, is stored in MODCON[3:0] (see Table 4-1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '`1111`' and the XMODEN bit is set (MODCON[15]).

The Y Address Space Pointer W register (YWM), to which Modulo Addressing is to be applied, is stored in MODCON[7:4]. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '`1111`' and the YMODEN bit is set at MODCON[14].

**FIGURE 4-20: MODULO ADDRESSING OPERATION EXAMPLE**




```
MOV     #0x1100, W0
MOV     W0, XMODSRT     ;set modulo start address
MOV     #0x1163, W0
MOV     W0, MODEND      ;set modulo end address
MOV     #0x8001, W0
MOV     W0, MODCON      ;enable W1, X AGU for modulo

MOV     #0x0000, W0     ;W0 holds buffer fill value

MOV     #0x1110, W1     ;point W1 to buffer

DO      AGAIN, #0x31    ;fill the 50 buffer locations
MOV     W0, [W1++]      ;fill the next location
AGAIN:  INC W0, W0      ;increment the fill value
```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**Note:** Modulo Addressing has address alignment restrictions for the buffer start or end address. See the **"Data Memory"** FRM (www.microchip.com/DS70595) for more information.

**Note:** The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed but the contents of the register remain unchanged.

## 4.7 Bit-Reversed Addressing (dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X Devices Only)

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms. It is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

### 4.7.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when all these conditions are met:

- BWMx bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^N$ bytes, the last 'N' bits of the data buffer start address must be zeros.

XBREV[14:0] is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

**Note:** All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XBREVx value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XBREVx) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data are a requirement, the LSb of the EA is ignored (and always clear).

**Note:** Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV[15]) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

**FIGURE 4-21: BIT-REVERSED ADDRESSING EXAMPLE**

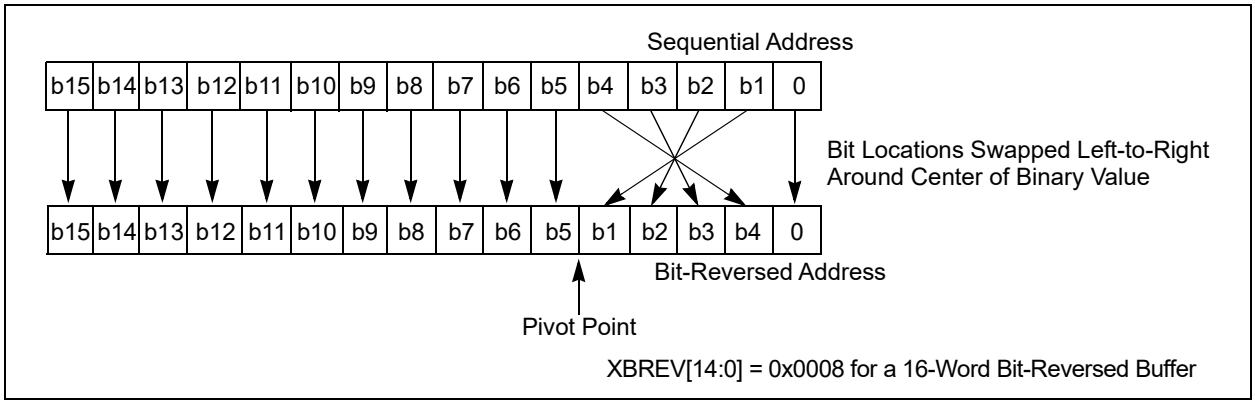

**TABLE 4-64: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)**

| Normal Address | | | | | Bit-Reversed Address | | | | |
|---|---|---|---|---|---|---|---|---|---|
| A3 | A2 | A1 | A0 | Decimal | A3 | A2 | A1 | A0 | Decimal |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 8 |
| 0 | 0 | 1 | 0 | 2 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 1 | 1 | 3 | 1 | 1 | 0 | 0 | 12 |
| 0 | 1 | 0 | 0 | 4 | 0 | 0 | 1 | 0 | 2 |
| 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | 0 | 10 |
| 0 | 1 | 1 | 0 | 6 | 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 | 1 | 1 | 1 | 0 | 14 |
| 1 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 9 | 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 | 0 | 1 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 11 | 1 | 1 | 0 | 1 | 13 |
| 1 | 1 | 0 | 0 | 12 | 0 | 0 | 1 | 1 | 3 |
| 1 | 1 | 0 | 1 | 13 | 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 1 | 0 | 14 | 0 | 1 | 1 | 1 | 7 |
| 1 | 1 | 1 | 1 | 15 | 1 | 1 | 1 | 1 | 15 |


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## 4.8 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X architecture uses a 24-bit wide Program Space (PS) and a 16-bit wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use these data successfully, they must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices provides two methods by which Program Space can be accessed during operation:

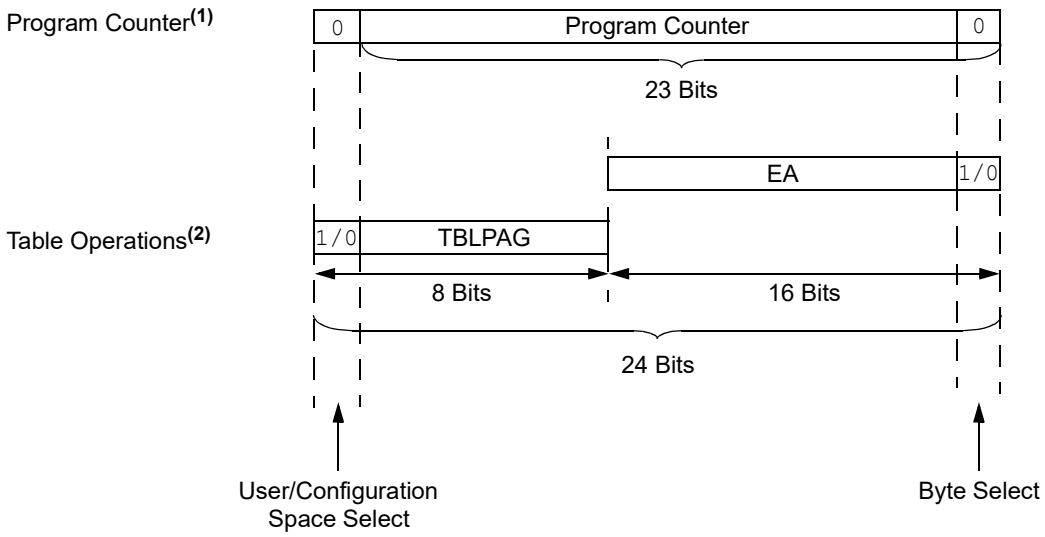
- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

**TABLE 4-65: PROGRAM SPACE ADDRESS CONSTRUCTION**

| Access Type | Access Space | Program Space Address | | | | |
|---|---|---|---|---|---|---|
| | | [23] | [22:16] | [15] | [14:1] | [0] |
| Instruction Access (Code Execution) | User | 0 | PC[22:1] | | | 0 |
| | | 0xx xxxx xxxx xxxx xxxx xxx0 | | | | |
| TBLRD/TBLWT (Byte/Word Read/Write) | User | TBLPAG[7:0] | | Data EA[15:0] | | |
| | | 0xxx xxxx | | xxxx xxxx xxxx xxxx | | |
| | Configuration | TBLPAG[7:0] | | Data EA[15:0] | | |
| | | 1xxx xxxx | | xxxx xxxx xxxx xxxx | | |

**FIGURE 4-22: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION**




**Note 1:** The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the Program and Data Spaces.

**2:** Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.

### 4.8.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

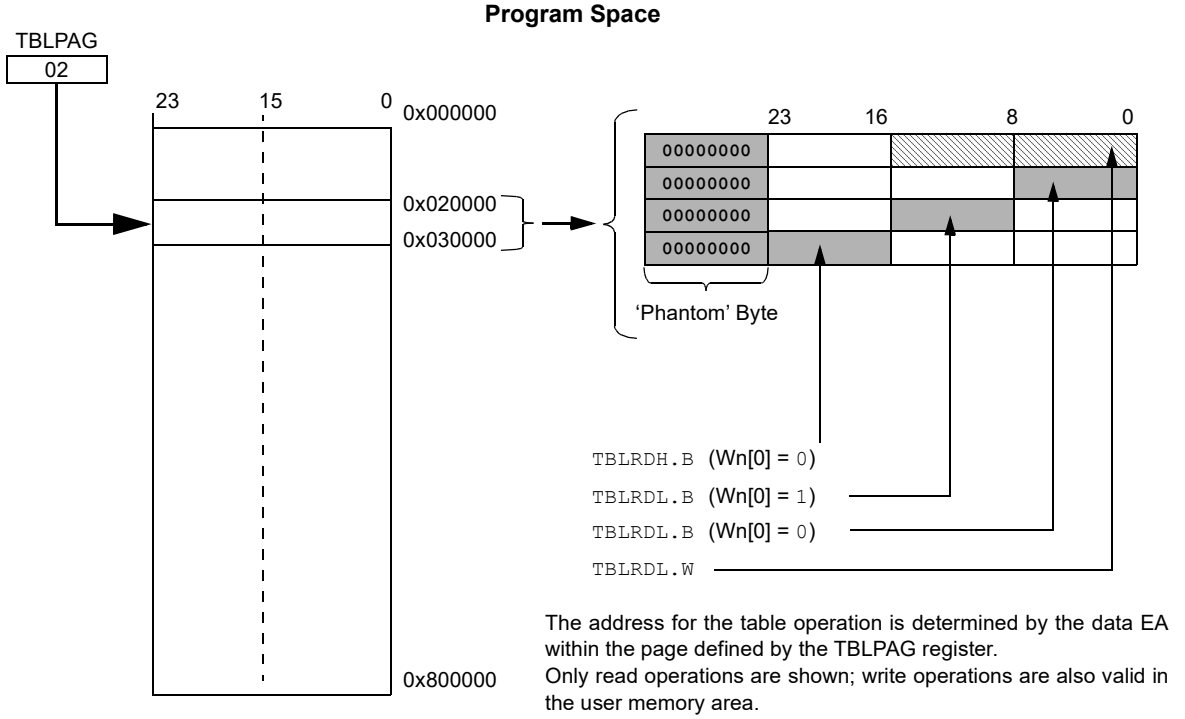
Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
  - In Word mode, this instruction maps the lower word of the Program Space location (P[15:0]) to a data address (D[15:0])
  - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.
- TBLRDH (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address (P[23:16]) to a data address. The 'phantom' byte (D[15:8]) is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to D[7:0] of the data address in the TBLRDL instruction. The data are always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG[7] = 0, the table page is located in the user memory space. When TBLPAG[7] = 1, the page is located in configuration space.

**FIGURE 4-23: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS**




The address for the table operation is determined by the data EA within the page defined by the TBLPAG register.
Only read operations are shown; write operations are also valid in the user memory area.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# 5.0 FLASH PROGRAM MEMORY

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Flash Programming"** (www.microchip.com/DS70000609) in the *"dsPIC33/PIC24 Family Reference Manual"*.

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data a single program memory word, and erase program memory in blocks or 'pages' of 1024 instructions (3072 bytes) at a time.

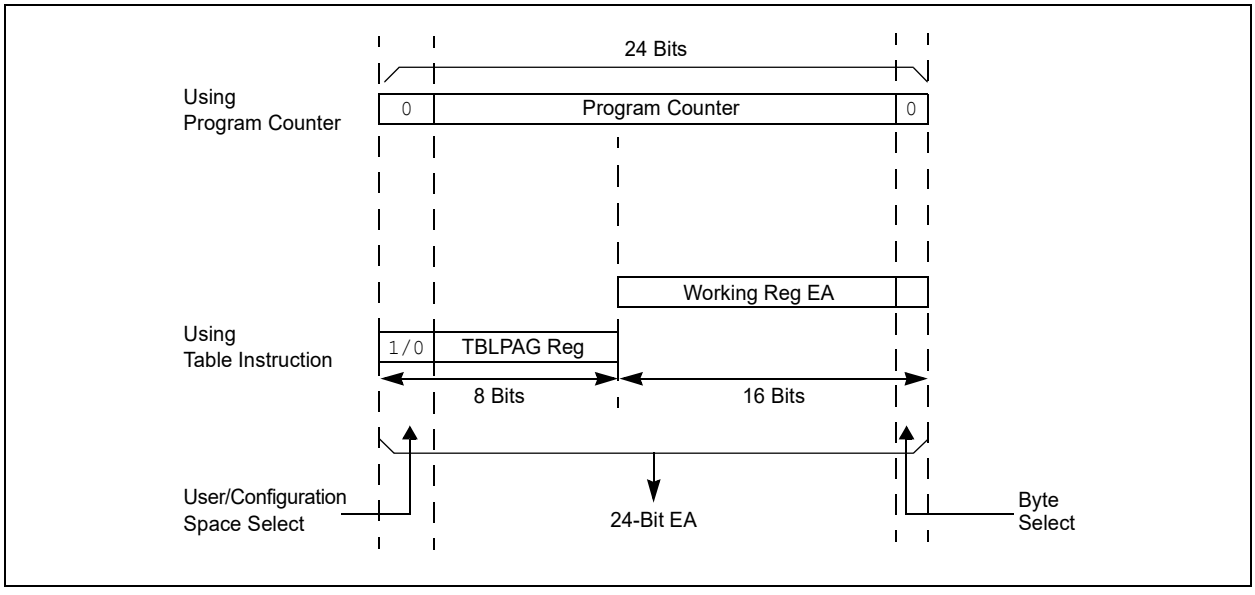
## 5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits[7:0] of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits[15:0] of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits[23:16] of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

**FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS**



## 5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory and to program two instruction words at a time. See the General Purpose and Motor Control Family tables (Table 1 and Table 2, respectively) for the page sizes of each device.

For more information on erasing and programming Flash memory, refer to **"Flash Programming"** (www.microchip.com/DS70000609) in the *"dsPIC33/PIC24 Family Reference Manual"*.

## 5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time) in Table 30-14 in **Section 30.0 "Electrical Characteristics"**.

Setting the WR bit (NVMCON[15]) starts the operation and the WR bit is automatically cleared when the operation is finished.

### 5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs.

Refer to **Flash Programming"** (www.microchip.com/DS70000609) in the "*dsPIC33/PIC24 Family Reference Manual"* for details and codes examples on programming using RTSP.

## 5.4 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 5.4.1 KEY RESOURCES

- **"Flash Programming"** (www.microchip.com/DS70000609) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 5.5 Control Registers

Four SFRs are used to erase and write the program Flash memory: NVMCON, NVMKEY, NVMADRH and NVMADRL.

The NVMCON register (Register 5-1) enables and initiates Flash memory erase and write operations.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRH and NVMADRL. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations or the selected page for erase operations.

The NVMADRH register is used to hold the upper eight bits of the EA, while the NVMADRL register is used to hold the lower 16 bits of the EA.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**REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER**

| R/SO-0(6) | R/W-0(1) | R/W-0(1) | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| WR | WREN | WRERR | NVMSIDL(2) | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R/W-0(1) | R/W-0(1) | R/W-0(1) | R/W-0(1) |
|---|---|---|---|---|---|---|---|
| — | — | — | — | NVMOP[3:0](3,4) | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | SO = Settable Only bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **WR:** Write Control bit(6)
- 1 = Initiates a Flash memory program or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
- 0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit(1)
- 1 = Enables Flash program/erase operations
- 0 = Inhibits Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit(1)
- 1 = An improper program or erase sequence attempt or termination has occurred (bit is set automatically on any set attempt of the WR bit)
- 0 = The program or erase operation completed normally

bit 12 **NVMSIDL:** NVM Stop in Idle Control bit(2)
- 1 = Flash voltage regulator goes into Standby mode during Idle mode
- 0 = Flash voltage regulator is active during Idle mode

bit 11-4 **Unimplemented:** Read as '0'

bit 3-0 **NVMOP[3:0]:** NVM Operation Select bits(1,3,4)
- 1111 = Reserved
- 1110 = Reserved
- 1101 = Reserved
- 1100 = Reserved
- 1011 = Reserved
- 1010 = Reserved
- 0011 = Memory page erase operation
- 0010 = Reserved
- 0001 = Memory double-word program operation(5)
- 0000 = Reserved

**Note 1:** These bits can only be reset on a POR.

**2:** If this bit is set, there will be minimal power savings (IIDLE) and upon exiting Idle mode, there is a delay (TVREG) before Flash memory becomes operational.

**3:** All other combinations of NVMOP[3:0] are unimplemented.

**4:** Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.

**5:** Two adjacent words on a 4-word boundary are programmed during execution of this operation.

**6:** This bit can only be reset on a POR or a BOR.

**REGISTER 5-2: NVMADRH: NONVOLATILE MEMORY ADDRESS REGISTER HIGH**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMADR[23:16]:** Nonvolatile Memory Write Address High bits

Selects the upper eight bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

**REGISTER 5-3: NVMADRL: NONVOLATILE MEMORY ADDRESS REGISTER LOW**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| NVMADR[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **NVMADR[15:0]:** Nonvolatile Memory Write Address Low bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written by the user application.

**REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
|---|---|---|---|---|---|---|---|
| NVMKEY[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **NVMKEY[7:0]:** Key Register (write-only) bits


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## 6.0 RESETS

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Reset"** (www.microchip.com/DS70602) in the *"dsPIC33/PIC24 Family Reference Manual"*.

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{SYSRST}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- $\overline{MCLR}$: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
  - Illegal Opcode Reset
  - Uninitialized W Register Reset
  - Security Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the $\overline{SYSRST}$ signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

**Note:** Refer to the specific peripheral section or **Section 4.0 "Memory Organization"** of this manual for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

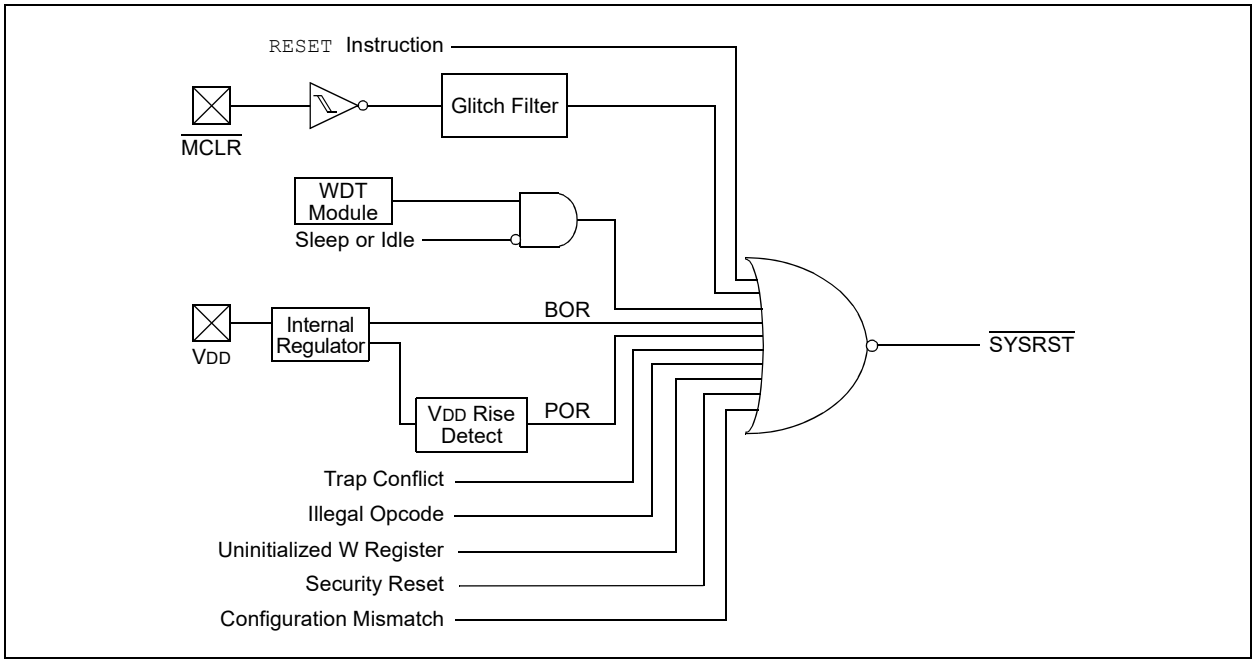
A POR clears all the bits, except for the POR and BOR bits (RCON[1:0]), that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

**Note:** The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

For all Resets, the default clock source is determined by the FNOSC[2:0] bits in the FOSCSEL Configuration register. The value of the FNOSC[2:0] bits is loaded into NOSC[2:0] (OSCCON[10:8]) on Reset, which in turn, initializes the system clock.

**FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM**



## 6.1 Reset Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 6.1.1 KEY RESOURCES

- **"Reset"** (www.microchip.com/DS70602) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools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**REGISTER 6-1: RCON: RESET CONTROL REGISTER(1)**

| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRAPR | IOPUWR | — | — | VREGSF | — | CM | VREGS |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| EXTR | SWR | SWDTEN(2) | WDTO | SLEEP | IDLE | BOR | POR |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or Uninitialized W register Reset has not occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **VREGSF:** Flash Voltage Regulator Standby During Sleep bit
1 = Flash voltage regulator is active during Sleep
0 = Flash voltage regulator goes into Standby mode during Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred.
0 = A Configuration Mismatch Reset has not occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset ($\overline{MCLR}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit(2)
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

**Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

**REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)**

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device has been in Sleep mode
0 = Device has not been in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

**Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.


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# 7.0 INTERRUPT CONTROLLER

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (www.microchip.com/DS70000600) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X CPU.

The interrupt controller has the following features:

- Up to Eight Processor Exceptions and Software Traps
- Eight User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for Each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies

## 7.1 Interrupt Vector Table

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 246 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

## 7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A `GOTO` instruction at the Reset address can redirect program execution to the appropriate start-up routine.

**Note:** Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a `RESET` instruction.

**FIGURE 7-1: dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X AND PIC24EPXXXGP/MC20X INTERRUPT VECTOR TABLE**

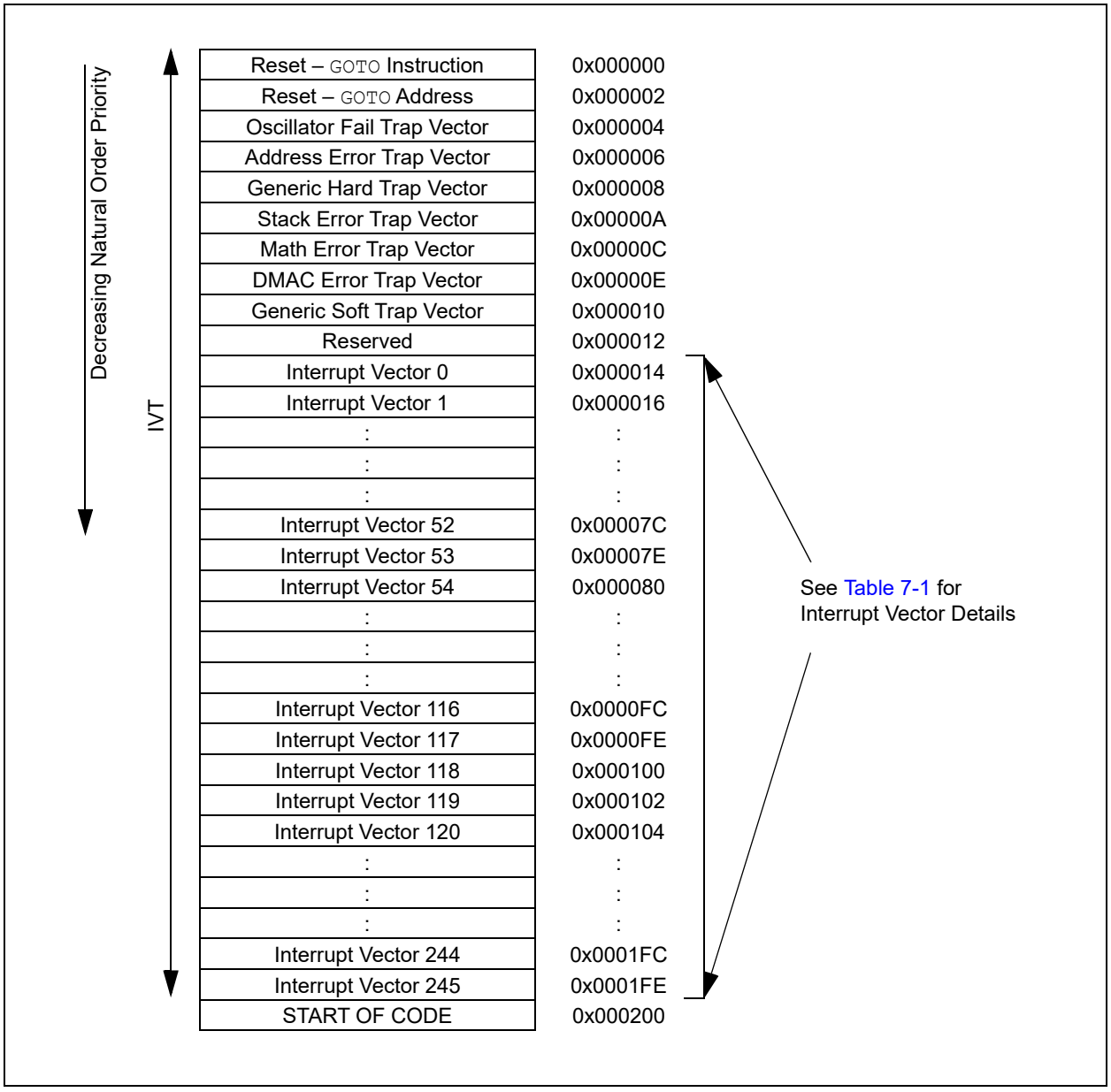



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**TABLE 7-1: INTERRUPT VECTOR DETAILS**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| Highest Natural Order Priority | | | | | | |
| INT0 – External Interrupt 0 | 8 | 0 | 0x000014 | IFS0[0] | IEC0[0] | IPC0[2:0] |
| IC1 – Input Capture 1 | 9 | 1 | 0x000016 | IFS0[1] | IEC0[1] | IPC0[6:4] |
| OC1 – Output Compare 1 | 10 | 2 | 0x000018 | IFS0[2] | IEC0[2] | IPC0[10:8] |
| T1 – Timer1 | 11 | 3 | 0x00001A | IFS0[3] | IEC0[3] | IPC0[14:12] |
| DMA0 – DMA Channel 0 | 12 | 4 | 0x00001C | IFS0[4] | IEC0[4] | IPC1[2:0] |
| IC2 – Input Capture 2 | 13 | 5 | 0x00001E | IFS0[5] | IEC0[5] | IPC1[6:4] |
| OC2 – Output Compare 2 | 14 | 6 | 0x000020 | IFS0[6] | IEC0[6] | IPC1[10:8] |
| T2 – Timer2 | 15 | 7 | 0x000022 | IFS0[7] | IEC0[7] | IPC1[14:12] |
| T3 – Timer3 | 16 | 8 | 0x000024 | IFS0[8] | IEC0[8] | IPC2[2:0] |
| SPI1E – SPI1 Error | 17 | 9 | 0x000026 | IFS0[9] | IEC0[9] | IPC2[6:4] |
| SPI1 – SPI1 Transfer Done | 18 | 10 | 0x000028 | IFS0[10] | IEC0[10] | IPC2[10:8] |
| U1RX – UART1 Receiver | 19 | 11 | 0x00002A | IFS0[11] | IEC0[11] | IPC2[14:12] |
| U1TX – UART1 Transmitter | 20 | 12 | 0x00002C | IFS0[12] | IEC0[12] | IPC3[2:0] |
| AD1 – ADC1 Convert Done | 21 | 13 | 0x00002E | IFS0[13] | IEC0[13] | IPC3[6:4] |
| DMA1 – DMA Channel 1 | 22 | 14 | 0x000030 | IFS0[14] | IEC0[14] | IPC3[10:8] |
| Reserved | 23 | 15 | 0x000032 | — | — | — |
| SI2C1 – I2C1 Slave Event | 24 | 16 | 0x000034 | IFS1[0] | IEC1[0] | IPC4[2:0] |
| MI2C1 – I2C1 Master Event | 25 | 17 | 0x000036 | IFS1[1] | IEC1[1] | IPC4[6:4] |
| CM – Comparator Combined Event | 26 | 18 | 0x000038 | IFS1[2] | IEC1[2] | IPC4[10:8] |
| CN – Input Change Interrupt | 27 | 19 | 0x00003A | IFS1[3] | IEC1[3] | IPC4[14:12] |
| INT1 – External Interrupt 1 | 28 | 20 | 0x00003C | IFS1[4] | IEC1[4] | IPC5[2:0] |
| Reserved | 29-31 | 21-23 | 0x00003E-0x000042 | — | — | — |
| DMA2 – DMA Channel 2 | 32 | 24 | 0x000044 | IFS1[8] | IEC1[8] | IPC6[2:0] |
| OC3 – Output Compare 3 | 33 | 25 | 0x000046 | IFS1[9] | IEC1[9] | IPC6[6:4] |
| OC4 – Output Compare 4 | 34 | 26 | 0x000048 | IFS1[10] | IEC1[10] | IPC6[10:8] |
| T4 – Timer4 | 35 | 27 | 0x00004A | IFS1[11] | IEC1[11] | IPC6[14:12] |
| T5 – Timer5 | 36 | 28 | 0x00004C | IFS1[12] | IEC1[12] | IPC7[2:0] |
| INT2 – External Interrupt 2 | 37 | 29 | 0x00004E | IFS1[13] | IEC1[13] | IPC7[6:4] |
| U2RX – UART2 Receiver | 38 | 30 | 0x000050 | IFS1[14] | IEC1[14] | IPC7[10:8] |
| U2TX – UART2 Transmitter | 39 | 31 | 0x000052 | IFS1[15] | IEC1[15] | IPC7[14:12] |
| SPI2E – SPI2 Error | 40 | 32 | 0x000054 | IFS2[0] | IEC2[0] | IPC8[2:0] |
| SPI2 – SPI2 Transfer Done | 41 | 33 | 0x000056 | IFS2[1] | IEC2[1] | IPC8[6:4] |
| C1RX – CAN1 RX Data Ready(1) | 42 | 34 | 0x000058 | IFS2[2] | IEC2[2] | IPC8[10:8] |
| C1 – CAN1 Event(1) | 43 | 35 | 0x00005A | IFS2[3] | IEC2[3] | IPC8[14:12] |
| DMA3 – DMA Channel 3 | 44 | 36 | 0x00005C | IFS2[4] | IEC2[4] | IPC9[2:0] |
| IC3 – Input Capture 3 | 45 | 37 | 0x00005E | IFS2[5] | IEC2[5] | IPC9[6:4] |
| IC4 – Input Capture 4 | 46 | 38 | 0x000060 | IFS2[6] | IEC2[6] | IPC9[10:8] |
| Reserved | 47-56 | 39-48 | 0x000062-0x000074 | — | — | — |
| SI2C2 – I2C2 Slave Event | 57 | 49 | 0x000076 | IFS3[1] | IEC3[1] | IPC12[6:4] |
| MI2C2 – I2C2 Master Event | 58 | 50 | 0x000078 | IFS3[2] | IEC3[2] | IPC12[10:8] |
| Reserved | 59-64 | 51-56 | 0x00007A-0x000084 | — | — | — |
| PWMSpEventMatch – PWM Special Event Match(2) | 65 | 57 | 0x000086 | IFS3[9] | IEC3[9] | IPC14[6:4] |

**Note 1:** This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

**2:** This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| QEI1 – QEI1 Position Counter Compare(2) | 66 | 58 | 0x000088 | IFS3[10] | IEC3[10] | IPC14[10:8] |
| Reserved | 67-72 | 59-64 | 0x00008A-0x000094 | — | — | — |
| U1E – UART1 Error Interrupt | 73 | 65 | 0x000096 | IFS4[1] | IEC4[1] | IPC16[6:4] |
| U2E – UART2 Error Interrupt | 74 | 66 | 0x000098 | IFS4[2] | IEC4[2] | IPC16[10:8] |
| CRC – CRC Generator Interrupt | 75 | 67 | 0x00009A | IFS4[3] | IEC4[3] | IPC16[14:12] |
| Reserved | 76-77 | 68-69 | 0x00009C-0x00009E | — | — | — |
| C1TX – CAN1 TX Data Request(1) | 78 | 70 | 0x000A0 | IFS4[6] | IEC4[6] | IPC17[10:8] |
| Reserved | 79-84 | 71-76 | 0x0000A2-0x0000AC | — | — | — |
| CTMU – CTMU Interrupt | 85 | 77 | 0x0000AE | IFS4[13] | IEC4[13] | IPC19[6:4] |
| Reserved | 86-101 | 78-93 | 0x0000B0-0x0000CE | — | — | — |
| PWM1 – PWM Generator 1(2) | 102 | 94 | 0x0000D0 | IFS5[14] | IEC5[14] | IPC23[10:8] |
| PWM2 – PWM Generator 2(2) | 103 | 95 | 0x0000D2 | IFS5[15] | IEC5[15] | IPC23[14:12] |
| PWM3 – PWM Generator 3(2) | 104 | 96 | 0x0000D4 | IFS6[0] | IEC6[0] | IPC24[2:0] |
| Reserved | 105-149 | 97-141 | 0x0001D6-0x00012E | — | — | — |
| ICD – ICD Application | 150 | 142 | 0x000142 | IFS8[14] | IEC8[14] | IPC35[10:8] |
| JTAG – JTAG Programming | 151 | 143 | 0x000130 | IFS8[15] | IEC8[15] | IPC35[14:12] |
| Reserved | 152 | 144 | 0x000134 | — | — | — |
| PTGSTEP – PTG Step | 153 | 145 | 0x000136 | IFS9[1] | IEC9[1] | IPC36[6:4] |
| PTGWDT – PTG Watchdog Time-out | 154 | 146 | 0x000138 | IFS9[2] | IEC9[2] | IPC36[10:8] |
| PTG0 – PTG Interrupt 0 | 155 | 147 | 0x00013A | IFS9[3] | IEC9[3] | IPC36[14:12] |
| PTG1 – PTG Interrupt 1 | 156 | 148 | 0x00013C | IFS9[4] | IEC9[4] | IPC37[2:0] |
| PTG2 – PTG Interrupt 2 | 157 | 149 | 0x00013E | IFS9[5] | IEC9[5] | IPC37[6:4] |
| PTG3 – PTG Interrupt 3 | 158 | 150 | 0x000140 | IFS9[6] | IEC9[6] | IPC37[10:8] |
| Reserved | 159-245 | 151-245 | 0x000142-0x0001FE | — | — | — |
| Lowest Natural Order Priority | | | | | | |

**Note 1:** This interrupt source is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

**2:** This interrupt source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.


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## 7.3 Interrupt Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 7.3.1 KEY RESOURCES

- **"Interrupts"** (www.microchip.com/DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 7.4 Interrupt Control and Status Registers

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement the following registers for the interrupt controller:

- INTCON1
- INTCON2
- INTCON3
- INTCON4
- INTTREG

### 7.4.1 INTCON1 THROUGH INTCON4

Global interrupt control functions are controlled from INTCON1, INTCON2, INTCON3 and INTCON4.

INTCON1 contains the Interrupt Nesting Disable (NSTDIS) bit, as well as the control and status flags for the processor trap sources.

The INTCON2 register controls external interrupt request signal behavior and also contains the Global Interrupt Enable (GIE) bit.

INTCON3 contains the status flags for the DMA and DO stack overflow status trap sources.

The INTCON4 register contains the Software-Generated Hard Trap (SGHT) status bit.

### 7.4.2 IFSx

The IFSx registers maintain all of the interrupt request flags. Each source of interrupt has a status bit, which is set by the respective peripherals or external signal and is cleared via software.

### 7.4.3 IECx

The IECx registers maintain all of the interrupt enable bits. These control bits are used to individually enable interrupts from the peripherals or external signals.

### 7.4.4 IPCx

The IPCx registers are used to set the Interrupt Priority Level (IPL) for each source of interrupt. Each user interrupt source can be assigned to one of eight priority levels.

### 7.4.5 INTTREG

The INTTREG register contains the associated interrupt vector number and the new CPU Interrupt Priority Level, which are latched into the Vector Number bits (VECNUM[7:0]) and Interrupt Priority Level bits (ILR[3:0]) fields in the INTTREG register. The new Interrupt Priority Level is the priority of the pending interrupt.

The interrupt sources are assigned to the IFSx, IECx and IPCx registers in the same sequence as they are listed in Table 7-1. For example, the INT0 (External Interrupt 0) is shown as having Vector Number 8 and a natural order priority of 0. Thus, the INT0IF bit is found in IFS0[0], the INT0IE bit in IEC0[0] and the INT0IP bits in the first position of IPC0 (IPC0[2:0]).

### 7.4.6 STATUS/CONTROL REGISTERS

Although these registers are not specifically part of the interrupt control hardware, two of the CPU Control registers contain bits that control interrupt functionality. For more information on these registers refer to **"CPU"** (www.microchip.com/DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*.

- The CPU STATUS Register, SR, contains the IPL[2:0] bits (SR[7:5]). These bits indicate the current CPU Interrupt Priority Level. The user software can change the current CPU Interrupt Priority Level by writing to the IPLx bits.
- The CORCON register contains the IPL3 bit which, together with IPL[2:0], also indicates the current CPU priority level. IPL3 is a read-only bit so that trap events cannot be masked by the user software.

All Interrupt registers are described in Register 7-3 through Register 7-7 in the following pages.

**REGISTER 7-1: SR: CPU STATUS REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/C-0 | R/C-0 | R-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OA | OB | SA | SB | OAB | SAB | DA | DC |
| bit 15 | | | | | | | bit 8 |

| R/W-0(3) | R/W-0(3) | R/W-0(3) | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IPL[2:0](2) | | | RA | N | OV | Z | C |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1'= Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-5 **IPL[2:0]:** CPU Interrupt Priority Level Status bits(2,3)

111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

**Note 1:** For complete register details, see Register 3-1.

**2:** The IPL[2:0] bits are concatenated with the IPL[3] bit (CORCON[3]) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL[3] = 1. User interrupts are disabled when IPL[3] = 1.

**3:** The IPL[2:0] Status bits are read-only when the NSTDIS bit (INTCON1[15]) = 1.


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**REGISTER 7-2: CORCON: CORE CONTROL REGISTER(1)**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| **VAR** | — | US1 | US0 | EDT | DL2 | DL1 | DL0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SATA | SATB | SATDW | ACCSAT | **IPL3(2)** | SFA | RND | IF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1'= Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **VAR:** Variable Exception Processing Latency Control bit
1 = Variable exception processing is enabled
0 = Fixed exception processing is enabled

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

**Note 1:** For complete register details, see Register 3-2.
**2:** The IPL3 bit is concatenated with the IPL[2:0] bits (SR[7:5]) to form the CPU Interrupt Priority Level.

**REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| NSTDIS | OVAERR(1) | OVBERR(1) | COVAERR(1) | COVBERR(1) | OVATE(1) | OVBTE(1) | COVTE(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| SFTACERR(1) | DIV0ERR | DMACERR | MATHERR | ADDRERR | STKERR | OSCFAIL | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14 **OVAERR:** Accumulator A Overflow Trap Flag bit(1)
1 = Trap was caused by overflow of Accumulator A
0 = Trap was not caused by overflow of Accumulator A

bit 13 **OVBERR:** Accumulator B Overflow Trap Flag bit(1)
1 = Trap was caused by overflow of Accumulator B
0 = Trap was not caused by overflow of Accumulator B

bit 12 **COVAERR:** Accumulator A Catastrophic Overflow Trap Flag bit(1)
1 = Trap was caused by catastrophic overflow of Accumulator A
0 = Trap was not caused by catastrophic overflow of Accumulator A

bit 11 **COVBERR:** Accumulator B Catastrophic Overflow Trap Flag bit(1)
1 = Trap was caused by catastrophic overflow of Accumulator B
0 = Trap was not caused by catastrophic overflow of Accumulator B

bit 10 **OVATE:** Accumulator A Overflow Trap Enable bit(1)
1 = Trap overflow of Accumulator A
0 = Trap is disabled

bit 9 **OVBTE:** Accumulator B Overflow Trap Enable bit(1)
1 = Trap overflow of Accumulator B
0 = Trap is disabled

bit 8 **COVTE:** Catastrophic Overflow Trap Enable bit(1)
1 = Trap on catastrophic overflow of Accumulator A or B is enabled
0 = Trap is disabled

bit 7 **SFTACERR:** Shift Accumulator Error Status bit(1)
1 = Math error trap was caused by an invalid accumulator shift
0 = Math error trap was not caused by an invalid accumulator shift

bit 6 **DIV0ERR:** Divide-by-Zero Error Status bit
1 = Math error trap was caused by a divide-by-zero
0 = Math error trap was not caused by a divide-by-zero

bit 5 **DMACERR:** DMAC Trap Flag bit
1 = DMAC trap has occurred
0 = DMAC trap has not occurred

**Note 1:** These bits are available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.


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**REGISTER 7-3: INTCON1: INTERRUPT CONTROL REGISTER 1 (CONTINUED)**

bit 4 **MATHERR:** Math Error Status bit
1 = Math error trap has occurred
0 = Math error trap has not occurred

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as '0'

**Note 1:** These bits are available on dsPIC33EPXXXMC20X/50X and dsPIC33EPXXXGP50X devices only.

**REGISTER 7-4: INTCON2: INTERRUPT CONTROL REGISTER 2**

| R/W-1 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| GIE | DISI | SWTRAP | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | INT2EP | INT1EP | INT0EP |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **GIE:** Global Interrupt Enable bit
1 = Interrupts and associated IE bits are enabled
0 = Interrupts are disabled, but traps are still enabled

bit 14 **DISI:** DISI Instruction Status bit
1 = DISI instruction is active
0 = DISI instruction is not active

bit 13 **SWTRAP:** Software Trap Status bit
1 = Software trap is enabled
0 = Software trap is disabled

bit 12-3 **Unimplemented:** Read as '0'

bit 2 **INT2EP:** External Interrupt 2 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 1 **INT1EP:** External Interrupt 1 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge

bit 0 **INT0EP:** External Interrupt 0 Edge Detect Polarity Select bit
1 = Interrupt on negative edge
0 = Interrupt on positive edge


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**REGISTER 7-5: INTCON3: INTERRUPT CONTROL REGISTER 3**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | DAE | DOOVR | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5 **DAE:** DMA Address Error Soft Trap Status bit
1 = DMA address error soft trap has occurred
0 = DMA address error soft trap has not occurred

bit 4 **DOOVR:** DO Stack Overflow Soft Trap Status bit
1 = DO stack overflow soft trap has occurred
0 = DO stack overflow soft trap has not occurred

bit 3-0 **Unimplemented:** Read as ‘0’

**REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | SGHT |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-1 **Unimplemented:** Read as ‘0’

bit 0 **SGHT:** Software-Generated Hard Trap Status bit
1 = Software-generated hard trap has occurred
0 = Software-generated hard trap has not occurred

**REGISTER 7-7: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | ILR[3:0] | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| VECNUM[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **ILR[3:0]:** New CPU Interrupt Priority Level bits
1111 = CPU Interrupt Priority Level is 15]
•
•
•
0001 = CPU Interrupt Priority Level is 1
0000 = CPU Interrupt Priority Level is 0

bit 7-0 **VECNUM[7:0]:** Vector Number of Pending Interrupt bits
11111111 = 255, Reserved; do not use
•
•
•
00001001 = 9, IC1 – Input Capture 1
00001000 = 8, INT0 – External Interrupt 0
00000111 = 7, Reserved; do not use
00000110 = 6, Generic soft error trap
00000101 = 5, DMAC error trap
00000100 = 4, Math error trap
00000011 = 3, Stack error trap
00000010 = 2, Generic hard trap
00000001 = 1, Address error trap
00000000 = 0, Oscillator fail trap


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# 8.0 DIRECT MEMORY ACCESS (DMA)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Direct Memory Access (DMA)"** (www.microchip.com/DS70348) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The DMA Controller transfers data between Peripheral Data registers and Data Space SRAM.

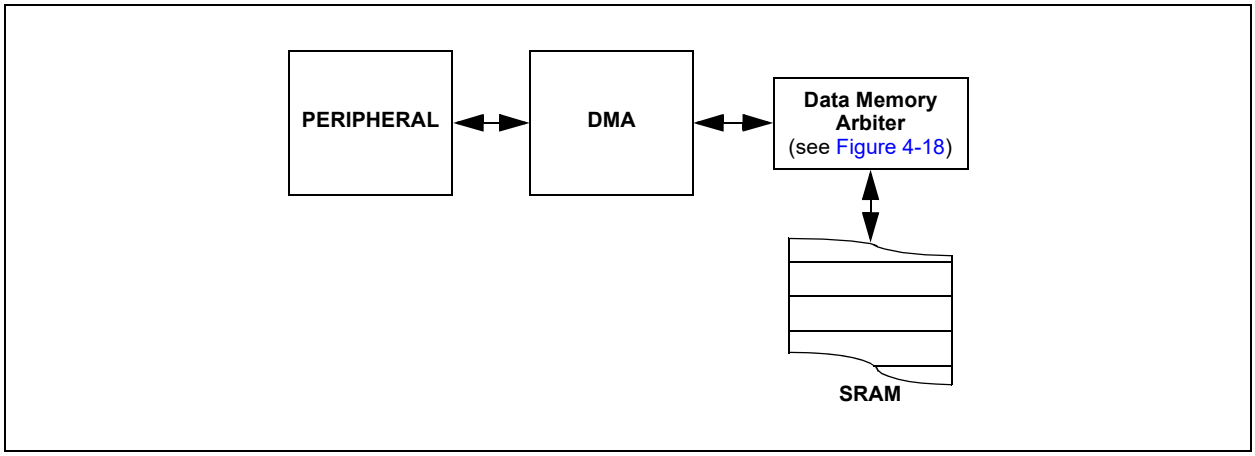
In addition, DMA can access the entire data memory space. The Data Memory Bus Arbiter is utilized when either the CPU or DMA attempts to access SRAM, resulting in potential DMA or CPU stalls.

The DMA Controller supports four independent channels. Each channel can be configured for transfers to or from selected peripherals. Some of the peripherals supported by the DMA Controller include:

- ECAN™
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI)
- UART
- Input Capture
- Output Compare

Refer to Table 8-1 for a complete list of supported peripherals.

**FIGURE 8-1: DMA CONTROLLER MODULE**



In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode
- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU interrupt after half or full block transfer complete
- Byte or word transfers
- Fixed priority channel arbitration
- Manual (software) or automatic (peripheral DMA requests) transfer initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM start addresses after each block transfer is complete)
- DMA request for each channel can be selected from any supported interrupt source
- Debug support features

The peripherals that can utilize DMA are listed in Table 8-1.

**TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS**

| Peripheral to DMA Association | DMAxREQ Register IRQSEL[7:0] Bits | DMAxPAD Register (Values to Read from Peripheral) | DMAxPAD Register (Values to Write to Peripheral) |
|---|---|---|---|
| INT0 – External Interrupt 0 | 00000000 | — | — |
| IC1 – Input Capture 1 | 00000001 | 0x0144 (IC1BUF) | — |
| IC2 – Input Capture 2 | 00000101 | 0x014C (IC2BUF) | — |
| IC3 – Input Capture 3 | 00100101 | 0x0154 (IC3BUF) | — |
| IC4 – Input Capture 4 | 00100110 | 0x015C (IC4BUF) | — |
| OC1 – Output Compare 1 | 00000010 | — | 0x0906 (OC1R)<br>0x0904 (OC1RS) |
| OC2 – Output Compare 2 | 00000110 | — | 0x0910 (OC2R)<br>0x090E (OC2RS) |
| OC3 – Output Compare 3 | 00011001 | — | 0x091A (OC3R)<br>0x0918 (OC3RS) |
| OC4 – Output Compare 4 | 00011010 | — | 0x0924 (OC4R)<br>0x0922 (OC4RS) |
| TMR2 – Timer2 | 00000111 | — | — |
| TMR3 – Timer3 | 00001000 | — | — |
| TMR4 – Timer4 | 00011011 | — | — |
| TMR5 – Timer5 | 00011100 | — | — |
| SPI1 Transfer Done | 00001010 | 0x0248 (SPI1BUF) | 0x0248 (SPI1BUF) |
| SPI2 Transfer Done | 00100001 | 0x0268 (SPI2BUF) | 0x0268 (SPI2BUF) |
| UART1RX – UART1 Receiver | 00001011 | 0x0226 (U1RXREG) | — |
| UART1TX – UART1 Transmitter | 00001100 | — | 0x0224 (U1TXREG) |
| UART2RX – UART2 Receiver | 00011110 | 0x0236 (U2RXREG) | — |
| UART2TX – UART2 Transmitter | 00011111 | — | 0x0234 (U2TXREG) |
| ECAN1 – RX Data Ready | 00100010 | 0x0440 (C1RXD) | — |
| ECAN1 – TX Data Request | 01000110 | — | 0x0442 (C1TXD) |
| ADC1 – ADC1 Convert Done | 00001101 | 0x0300 (ADC1BUF0) | — |


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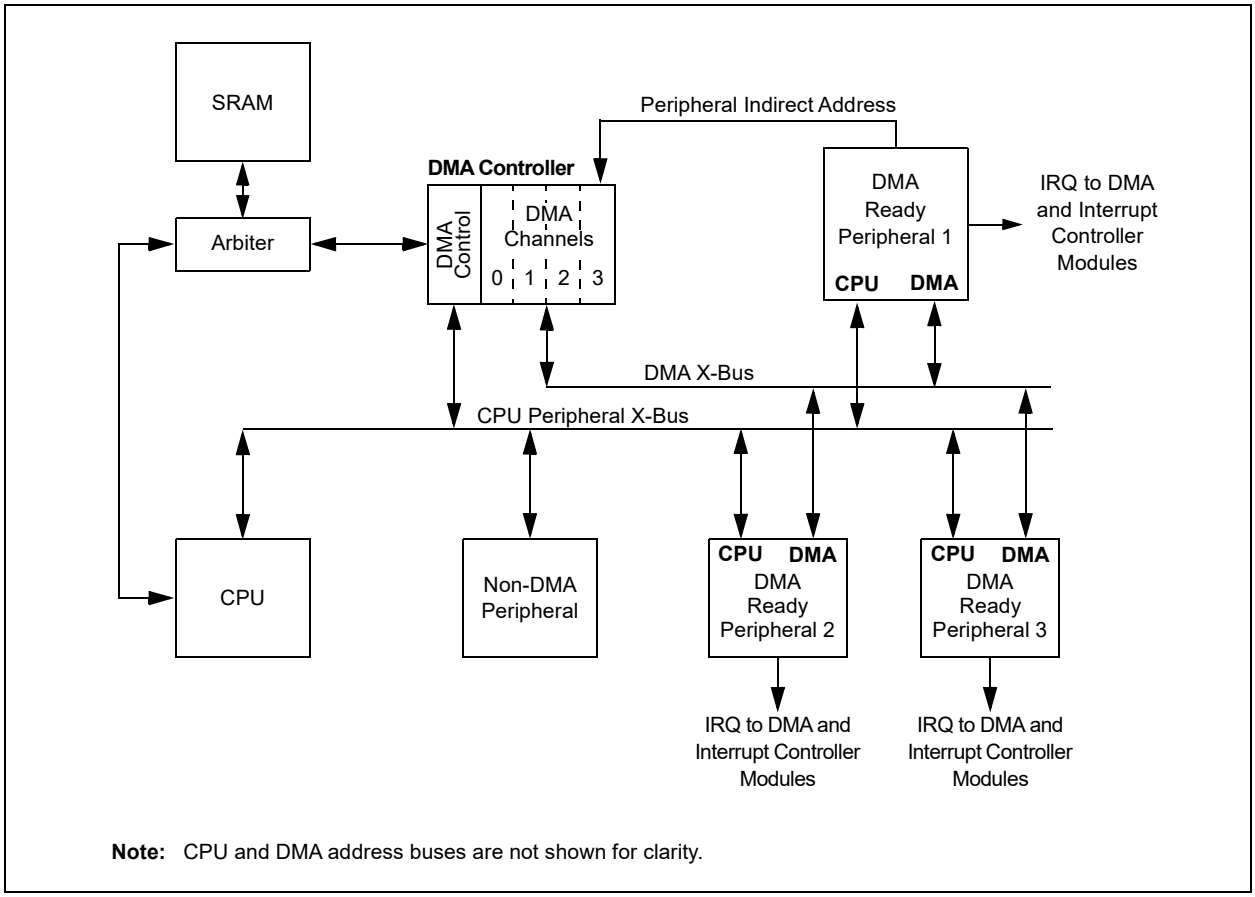
**FIGURE 8-2: DMA CONTROLLER BLOCK DIAGRAM**




**Note:** CPU and DMA address buses are not shown for clarity.

## 8.1 DMA Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 8.1.1 KEY RESOURCES

- **"Direct Memory Access (DMA)"** (www.microchip.com/DS70348) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 8.2 DMAC Registers

Each DMAC Channel x (where x = 0 through 3) contains the following registers:

- 16-Bit DMA Channel Control register (DMAxCON)
- 16-Bit DMA Channel IRQ Select register (DMAxREQ)
- 32-Bit DMA RAM Primary Start Address register (DMAxSTA)
- 32-Bit DMA RAM Secondary Start Address register (DMAxSTB)
- 16-Bit DMA Peripheral Address register (DMAxPAD)
- 14-Bit DMA Transfer Count register (DMAxCNT)

Additional status registers (DMAPWC, DMARQC, DMAPPS, DMALCA and DSADR) are common to all DMAC channels. These status registers provide information on write and request collisions, as well as on last address and channel access information.

The interrupt flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding interrupt enable control bits (DMAxIE) are located in an IECx register in the interrupt controller, and the corresponding interrupt priority control bits (DMAxIP) are located in an IPCx register in the interrupt controller.

**REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CHEN | SIZE | DIR | HALF | NULLW | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | AMODE1 | AMODE0 | — | — | MODE1 | MODE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CHEN:** DMA Channel Enable bit
1 = Channel is enabled
0 = Channel is disabled

bit 14 **SIZE:** DMA Data Transfer Size bit
1 = Byte
0 = Word

bit 13 **DIR:** DMA Transfer Direction bit (source/destination bus select)
1 = Reads from RAM address, writes to peripheral address
0 = Reads from peripheral address, writes to RAM address

bit 12 **HALF:** DMA Block Transfer Interrupt Select bit
1 = Initiates interrupt when half of the data have been moved
0 = Initiates interrupt when all of the data have been moved

bit 11 **NULLW:** Null Data Peripheral Write Mode Select bit
1 = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)
0 = Normal operation

bit 10-6 **Unimplemented:** Read as '0'

bit 5-4 **AMODE[1:0]:** DMA Channel Addressing Mode Select bits
11 = Reserved
10 = Peripheral Indirect Addressing mode
01 = Register Indirect without Post-Increment mode
00 = Register Indirect with Post-Increment mode

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **MODE[1:0]:** DMA Channel Operating Mode Select bits
11 = One-Shot, Ping-Pong modes are enabled (one block transfer from/to each DMA buffer)
10 = Continuous, Ping-Pong modes are enabled
01 = One-Shot, Ping-Pong modes are disabled
00 = Continuous, Ping-Pong modes are disabled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**REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER**

| R/S-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| FORCE(1) | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IRQSEL[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | S = Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FORCE:** Force DMA Transfer bit(1)
1 = Forces a single DMA transfer (Manual mode)
0 = Automatic DMA transfer initiation by DMA request

bit 14-8 **Unimplemented:** Read as '0'

bit 7-0 **IRQSEL[7:0]:** DMA Peripheral IRQ Number Select bits
01000110 = ECAN1 – TX Data Request(2)
00100110 = IC4 – Input Capture 4
00100101 = IC3 – Input Capture 3
00100010 = ECAN1 – RX Data Ready(2)
00100001 = SPI2 Transfer Done
00011111 = UART2TX – UART2 Transmitter
00011110 = UART2RX – UART2 Receiver
00011100 = TMR5 – Timer5
00011011 = TMR4 – Timer4
00011010 = OC4 – Output Compare 4
00011001 = OC3 – Output Compare 3
00001101 = ADC1 – ADC1 Convert done
00001100 = UART1TX – UART1 Transmitter
00001011 = UART1RX – UART1 Receiver
00001010 = SPI1 – Transfer Done
00001000 = TMR3 – Timer3
00000111 = TMR2 – Timer2
00000110 = OC2 – Output Compare 2
00000101 = IC2 – Input Capture 2
00000010 = OC1 – Output Compare 1
00000001 = IC1 – Input Capture 1
00000000 = INT0 – External Interrupt 0

**Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).

**2:** This selection is available in dsPIC33EPXXXGP/MC50X devices only.

**REGISTER 8-3: DMAxSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STA[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STA[23:16]:** Primary Start Address bits (source or destination)

**REGISTER 8-4: DMAxSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STA[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STA[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **STA[15:0]:** Primary Start Address bits (source or destination)


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**REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STB[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **STB[23:16]:** Secondary Start Address bits (source or destination)

**REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STB[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STB[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **STB[15:0]:** Secondary Start Address bits (source or destination)

**REGISTER 8-7: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PAD[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PAD[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PAD[15:0]:** Peripheral Address Register bits

**Note 1:** If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

**REGISTER 8-8: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER(1)**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CNT[13:8](2) | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CNT[7:0](2) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-0 **CNT[13:0]:** DMA Transfer Count Register bits(2)

**Note 1:** If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

**2:** The number of DMA transfers = CNT[13:0] + 1.


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**REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DSADR[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **DSADR[23:16]:** Most Recent DMA Address Accessed by DMA bits

**REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DSADR[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DSADR[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **DSADR[15:0]:** Most Recent DMA Address Accessed by DMA bits

**REGISTER 8-11: DMAPWC: DMA PERIPHERAL WRITE COLLISION STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | PWCOL3 | PWCOL2 | PWCOL1 | PWCOL0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **PWCOL3:** DMA Channel 3 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = No write collision is detected

bit 2 **PWCOL2:** DMA Channel 2 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = No write collision is detected

bit 1 **PWCOL1:** DMA Channel 1 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = No write collision is detected

bit 0 **PWCOL0:** DMA Channel 0 Peripheral Write Collision Flag bit
1 = Write collision is detected
0 = No write collision is detected


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**REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | RQCOL3 | RQCOL2 | RQCOL1 | RQCOL0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **RQCOL3:** DMA Channel 3 Transfer Request Collision Flag bit
1 = User force and interrupt-based request collision is detected
0 = No request collision is detected

bit 2 **RQCOL2:** DMA Channel 2 Transfer Request Collision Flag bit
1 = User force and interrupt-based request collision is detected
0 = No request collision is detected

bit 1 **RQCOL1:** DMA Channel 1 Transfer Request Collision Flag bit
1 = User force and interrupt-based request collision is detected
0 = No request collision is detected

bit 0 **RQCOL0:** DMA Channel 0 Transfer Request Collision Flag bit
1 = User force and interrupt-based request collision is detected
0 = No request collision is detected

**REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R-1 | R-1 | R-1 | R-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | LSTCH[3:0] | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3-0 **LSTCH[3:0]:** Last DMAC Channel Active Status bits

1111 = No DMA transfer has occurred since system Reset
1110 = Reserved
•
•
•
0100 = Reserved
0011 = Last data transfer was handled by Channel 3
0010 = Last data transfer was handled by Channel 2
0001 = Last data transfer was handled by Channel 1
0000 = Last data transfer was handled by Channel 0


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**REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | PPST3 | PPST2 | PPST1 | PPST0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **PPST3:** DMA Channel 3 Ping-Pong Mode Status Flag bit
1 = DMASTB3 register is selected
0 = DMASTA3 register is selected

bit 2 **PPST2:** DMA Channel 2 Ping-Pong Mode Status Flag bit
1 = DMASTB2 register is selected
0 = DMASTA2 register is selected

bit 1 **PPST1:** DMA Channel 1 Ping-Pong Mode Status Flag bit
1 = DMASTB1 register is selected
0 = DMASTA1 register is selected

bit 0 **PPST0:** DMA Channel 0 Ping-Pong Mode Status Flag bit
1 = DMASTB0 register is selected
0 = DMASTA0 register is selected

**NOTES:**


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## 9.0 OSCILLATOR CONFIGURATION

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Oscillator"** (www.microchip.com/DS70580) in the "*dsPIC33/PIC24 Family Reference Manual*".

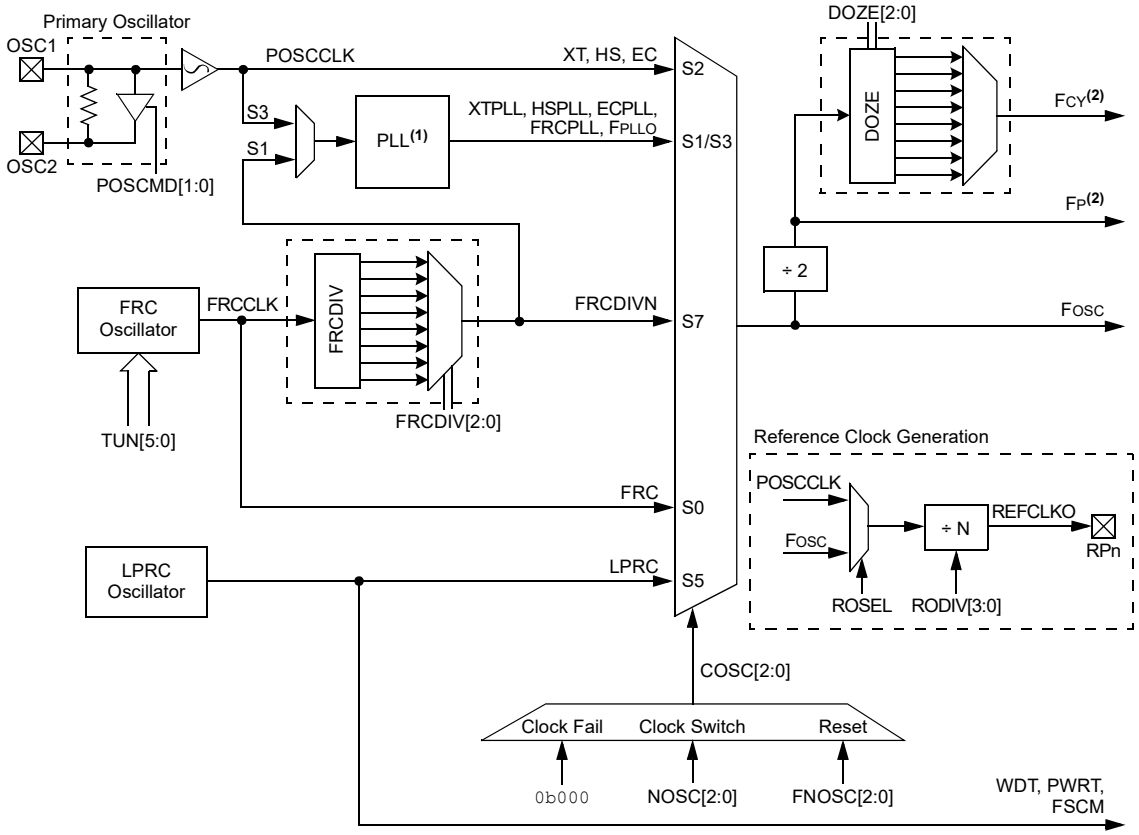
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X oscillator system provides:

- On-Chip Phase-Locked Loop (PLL) to Boost Internal Operating Frequency on Select Internal and External Oscillator Sources
- On-the-Fly Clock Switching between Various Clock Sources
- Doze mode for System Power Savings
- Fail-Safe Clock Monitor (FSCM) that Detects Clock Failure and Permits Safe Application Recovery or Shutdown
- Configuration Bits for Clock Source Selection

A simplified diagram of the oscillator system is shown in Figure 9-1.

**FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM**




**Note 1:** See Figure 9-2 for PLL details.

**2:** The term, FP, refers to the clock source for all peripherals, while FCY refers to the clock source for the CPU. Throughout this document, FCY and FP are used interchangeably, except in the case of Doze mode. FP and FCY will be different when Doze mode is used with a doze ratio of 1:2 or lower.

## 9.1 CPU Clocking System

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices provides six system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator

Instruction execution speed or device operating frequency, FCY, is given by Equation 9-1.

**EQUATION 9-1: DEVICE OPERATING FREQUENCY**

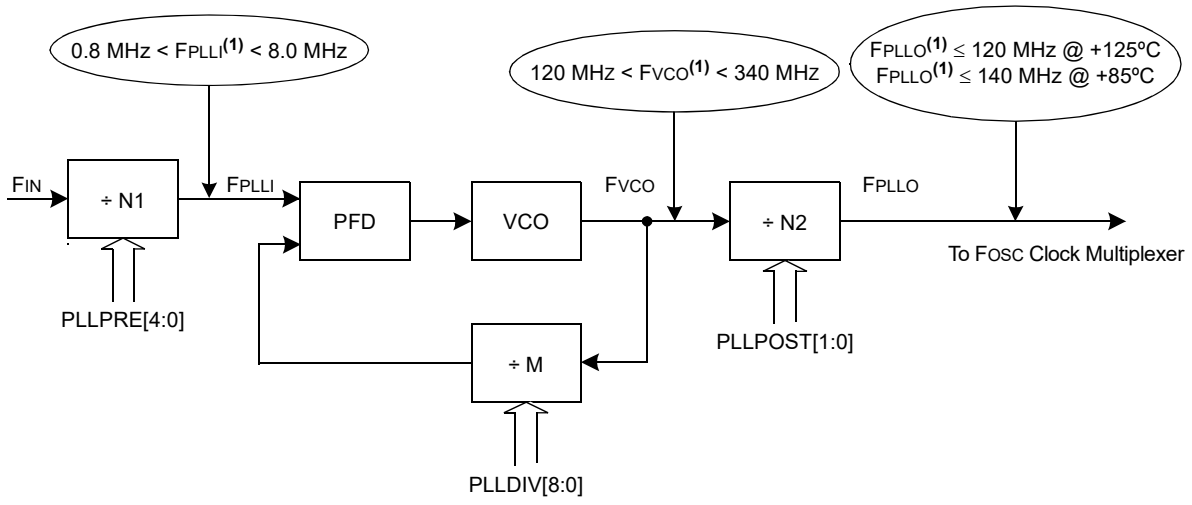
$$FCY = FOSC/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (FIN) and output frequency (FPLLO). In clock modes S1 and S3, when the PLL output is selected, FOSC = FPLLO.

Equation 9-3 provides the relationship between input frequency (FIN) and VCO frequency (FVCO).

**FIGURE 9-2: PLL BLOCK DIAGRAM**




**Note 1:** This frequency range must be met at all times.

**EQUATION 9-2: FPLLO CALCULATION**

$$FPLLO = FIN \times \left(\frac{M}{N1 \times N2}\right) = FIN \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2) \times 2(PLLPOST + 1)}\right)$$

Where:

$N1 = PLLPRE + 2$

$N2 = 2 \times (PLLPOST + 1)$

$M = PLLDIV + 2$

**EQUATION 9-3: FVCO CALCULATION**

$$Fvco = FIN \times \left(\frac{M}{N1}\right) = FIN \times \left(\frac{(PLLDIV + 2)}{(PLLPRE + 2)}\right)$$


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**TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION**

| Oscillator Mode | Oscillator Source | POSCMD[1:0] | FNOSC[2:0] | See Notes |
|---|---|---|---|---|
| Fast RC Oscillator with Divide-by-N (FRCDIVN) | Internal | xx | 111 | 1, 2 |
| Low-Power RC Oscillator (LPRC) | Internal | xx | 101 | 1 |
| Primary Oscillator (HS) with PLL (HSPLL) | Primary | 10 | 011 | |
| Primary Oscillator (XT) with PLL (XTPLL) | Primary | 01 | 011 | |
| Primary Oscillator (EC) with PLL (ECPLL) | Primary | 00 | 011 | 1 |
| Primary Oscillator (HS) | Primary | 10 | 010 | |
| Primary Oscillator (XT) | Primary | 01 | 010 | |
| Primary Oscillator (EC) | Primary | 00 | 010 | 1 |
| Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL) | Internal | xx | 001 | 1 |
| Fast RC Oscillator (FRC) | Internal | xx | 000 | 1 |

**Note 1:** OSC2 pin function is determined by the OSCIOFNC Configuration bit.

**2:** This is the default oscillator mode for an unprogrammed (erased) device.

## 9.2 Oscillator Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 9.2.1 KEY RESOURCES

- **"Oscillator"** (www.microchip.com/DS70580) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 9.3 Oscillator Control Registers

**REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1)**

| U-0 | R-0 | R-0 | R-0 | U-0 | R/W-y | R/W-y | R/W-y |
|---|---|---|---|---|---|---|---|
| — | COSC2 | COSC1 | COSC0 | — | NOSC2(2) | NOSC1(2) | NOSC0(2) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CLKLOCK | IOLOCK | LOCK | — | CF(3) | — | — | OSWEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | y = Value set from Configuration bits on POR | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-12 **COSC[2:0]:** Current Oscillator Selection bits (read-only)
111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Reserved
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 11 **Unimplemented:** Read as '0'

bit 10-8 **NOSC[2:0]:** New Oscillator Selection bits(2)
111 = Fast RC Oscillator (FRC) with Divide-by-n
110 = Fast RC Oscillator (FRC) with Divide-by-16
101 = Low-Power RC Oscillator (LPRC)
100 = Reserved
011 = Primary Oscillator (XT, HS, EC) with PLL
010 = Primary Oscillator (XT, HS, EC)
001 = Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)
000 = Fast RC Oscillator (FRC)

bit 7 **CLKLOCK:** Clock Lock Enable bit
1 = If (FCKSM0 = 1), then clock and PLL configurations are locked; if (FCKSM0 = 0), then clock and PLL configurations may be modified
0 = Clock and PLL selections are not locked, configurations may be modified

bit 6 **IOLOCK:** I/O Lock Enable bit
1 = I/O lock is active
0 = I/O lock is not active

bit 5 **LOCK:** PLL Lock Status bit (read-only)
1 = Indicates that PLL is in lock or PLL start-up timer is satisfied
0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled

**Note 1:** Writes to this register require an unlock sequence. Refer to **"Oscillator"** (www.microchip.com/DS70580) in the *"dsPIC33/PIC24 Family Reference Manual"* (available from the Microchip website) for details.

**2:** Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

**3:** This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.


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**REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER(1) (CONTINUED)**

bit 4 **Unimplemented:** Read as '0'

bit 3 **CF:** Clock Fail Detect bit(3)
- 1 = FSCM has detected clock failure
- 0 = FSCM has not detected clock failure

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **OSWEN:** Oscillator Switch Enable bit
- 1 = Requests oscillator switch to selection specified by the NOSC[2:0] bits
- 0 = Oscillator switch is complete

**Note 1:** Writes to this register require an unlock sequence. Refer to **"Oscillator"** (www.microchip.com/DS70580) in the *"dsPIC33/PIC24 Family Reference Manual"* (available from the Microchip website) for details.

**2:** Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

**3:** This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and trigger an oscillator failure trap.

**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER**

| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ROI | DOZE2(1) | DOZE1(1) | DOZE0(1) | DOZEN(2,3) | FRCDIV2 | FRCDIV1 | FRCDIV0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-1 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PLLPOST1 | PLLPOST0 | — | PLLPRE4 | PLLPRE3 | PLLPRE2 | PLLPRE1 | PLLPRE0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts will clear the DOZEN bit
0 = Interrupts have no effect on the DOZEN bit

bit 14-12 **DOZE[2:0]:** Processor Clock Reduction Select bits(1)
111 = FCY divided by 128
110 = FCY divided by 64
101 = FCY divided by 32
100 = FCY divided by 16
011 = FCY divided by 8 (default)
010 = FCY divided by 4
001 = FCY divided by 2
000 = FCY divided by 1

bit 11 **DOZEN:** Doze Mode Enable bit(2,3)
1 = DOZE[2:0] field specifies the ratio between the peripheral clocks and the processor clocks
0 = Processor clock and peripheral clock ratio is forced to 1:1

bit 10-8 **FRCDIV[2:0]:** Internal Fast RC Oscillator Postscaler bits
111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2
000 = FRC divided by 1 (default)

bit 7-6 **PLLPOST[1:0]:** PLL VCO Output Divider Select bits (also denoted as 'N2', PLL postscaler)
11 = Output divided by 8
10 = Reserved
01 = Output divided by 4 (default)
00 = Output divided by 2

bit 5 **Unimplemented:** Read as '0'

**Note 1:** The DOZE[2:0] bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE[2:0] are ignored.

**2:** This bit is cleared when the ROI bit is set and an interrupt occurs.

**3:** The DOZEN bit cannot be set if DOZE[2:0] = 000. If DOZE[2:0] = 000, any attempt by user software to set the DOZEN bit is ignored.


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**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)**

bit 4-0 **PLLPRE[4:0]:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)
11111 = Input divided by 33
•
•
•
00001 = Input divided by 3
00000 = Input divided by 2 (default)

**Note 1:** The DOZE[2:0] bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE[2:0] are ignored.

**2:** This bit is cleared when the ROI bit is set and an interrupt occurs.

**3:** The DOZEN bit cannot be set if DOZE[2:0] = 000. If DOZE[2:0] = 000, any attempt by user software to set the DOZEN bit is ignored.

**REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | PLLDIV8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PLLDIV[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-9 **Unimplemented:** Read as ‘0’

bit 8-0 **PLLDIV[8:0]:** PLL Feedback Divisor bits (also denoted as ‘M’, PLL multiplier)

111111111 = 513
•
•
•
000110000 = 50 (default)
•
•
•
000000010 = 4
000000001 = 3
000000000 = 2


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**REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | TUN[5:0] | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN[5:0]:** FRC Oscillator Tuning bits

011111 = Maximum frequency deviation of 1.453% (7.477 MHz)
011110 = Center frequency + 1.406% (7.474 MHz)
•
•
•
000001 = Center frequency + 0.047% (7.373 MHz)
000000 = Center frequency (7.37 MHz nominal)
111111 = Center frequency – 0.047% (7.367 MHz)
•
•
•
100001 = Center frequency – 1.453% (7.263 MHz)
100000 = Minimum frequency deviation of -1.5% (7.259 MHz)

**REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ROON | — | ROSSLP | ROSEL | RODIV3(1) | RODIV2(1) | RODIV1(1) | RODIV0(1) |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ROON:** Reference Oscillator Output Enable bit
1 = Reference Oscillator output is enabled on the REFCLK pin(2)
0 = Reference Oscillator output is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit
1 = Reference Oscillator output continues to run in Sleep
0 = Reference Oscillator output is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Oscillator crystal is used as the reference clock
0 = System clock is used as the reference clock

bit 11-8 **RODIV[3:0]:** Reference Oscillator Divider bits(1)
1111 = Reference clock divided by 32,768
1110 = Reference clock divided by 16,384
1101 = Reference clock divided by 8,192
1100 = Reference clock divided by 4,096
1011 = Reference clock divided by 2,048
1010 = Reference clock divided by 1,024
1001 = Reference clock divided by 512
1000 = Reference clock divided by 256
0111 = Reference clock divided by 128
0110 = Reference clock divided by 64
0101 = Reference clock divided by 32
0100 = Reference clock divided by 16
0011 = Reference clock divided by 8
0010 = Reference clock divided by 4
0001 = Reference clock divided by 2
0000 = Reference clock

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** The Reference Oscillator output must be disabled (ROON = 0) before writing to these bits.
**2:** This pin is remappable. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information.


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# 10.0 POWER-SAVING FEATURES

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Watchdog Timer and Power-Saving Modes"** (www.microchip.com/DS70615) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- Software-Controlled Doze mode
- Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

## 10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON[10:8]). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

## 10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices have two special power-saving modes that are entered through the execution of a special `PWRSAV` instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the `PWRSAV` instruction is shown in Example 10-1.

**Note:** `SLEEP_MODE` and `IDLE_MODE` are constants defined in the assembler include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

**EXAMPLE 10-1: `PWRSAV` INSTRUCTION SYNTAX**

```
PWRSAV  #IDLE_MODE     ; Put the device into Idle mode
PWRSAV  #SLEEP_MODE    ; Put the device into Sleep mode(1)
```

**Note 1:** The use of `PWRSV #SLEEP_MODE` has limitations when the Flash Voltage Regulator bit, VREGSF (RCON[11]), is set to Standby mode. Refer to **Section 10.2.1 "Sleep Mode"** for more information.

### 10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification (ICN) on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of these events:

- Any interrupt source that is individually enabled
- Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into standby when Sleep mode is entered by clearing the VREGS (RCON[8]) and VREGSF (RCON[11]) bits (default configuration). However, putting the Flash voltage regulator in Standby mode (VREGSF = 0) when in Sleep has the effect of corrupting the prefetched instructions placed in the instruction queue. When the part wakes up, these instructions may cause undefined behavior. To remove this problem, the instruction queue must be flushed after the part wakes up. A way to flush the instruction queue is to perform a branch. Therefore, it is required to implement the SLEEP instruction in a function with 4-instruction word alignment. The 4-instruction word alignment will assure that the SLEEP instruction is always placed on the correct address to make sure the flushing will be effective. Example 10-2 shows how this is performed.

**EXAMPLE 10-2: SLEEP MODE PWRSAV INSTRUCTION SYNTAX (WITH FLASH VOLTAGE REGULATOR SET TO STANDBY MODE)**

```
.global     _GoToSleep
.section    .text
.align      4

_GoToSleep:

PWRSAV      #SLEEP_MODE
BRA         TO_FLUSH_QUEUE_LABEL
TO_FLUSH_QUEUE_LABEL:
RETURN
```


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If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON[8]) and VREGSF (RCON[11]) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

### 10.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.4 "Peripheral Module Disable"**).
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (two-four clock cycles later), starting with the instruction following the `PWRSAV` instruction or the first instruction in the Interrupt Service Routine (ISR).

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral; for example, the TSIDL bit in the Timer1 Control register (T1CON[13]).

### 10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a `PWRSAV` instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

## 10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV[11]). The ratio between peripheral and core clock speed is determined by the DOZE[2:0] bits (CLKDIV[14:12]). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV[15]). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the ECAN™ module has been configured for 500 kbps, based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the ECAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

## 10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

| | |
|---|---|
| **Note:** | If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation). |

## 10.5 Power-Saving Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 10.5.1 KEY RESOURCES

- **"Watchdog Timer and Power-Saving Modes"** (www.microchip.com/DS70615) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools


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**REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| T5MD | T4MD | T3MD | T2MD | T1MD | QEI1MD(1) | PWMMD(1) | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| I2C1MD | U2MD | U1MD | SPI2MD | SPI1MD | — | C1MD(2) | AD1MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **T5MD:** Timer5 Module Disable bit
1 = Timer5 module is disabled
0 = Timer5 module is enabled

bit 14 **T4MD:** Timer4 Module Disable bit
1 = Timer4 module is disabled
0 = Timer4 module is enabled

bit 13 **T3MD:** Timer3 Module Disable bit
1 = Timer3 module is disabled
0 = Timer3 module is enabled

bit 12 **T2MD:** Timer2 Module Disable bit
1 = Timer2 module is disabled
0 = Timer2 module is enabled

bit 11 **T1MD:** Timer1 Module Disable bit
1 = Timer1 module is disabled
0 = Timer1 module is enabled

bit 10 **QEI1MD:** QEI1 Module Disable bit(1)
1 = QEI1 module is disabled
0 = QEI1 module is enabled

bit 9 **PWMMD:** PWM Module Disable bit(1)
1 = PWM module is disabled
0 = PWM module is enabled

bit 8 **Unimplemented:** Read as '0'

bit 7 **I2C1MD:** I2C1 Module Disable bit
1 = I2C1 module is disabled
0 = I2C1 module is enabled

bit 6 **U2MD:** UART2 Module Disable bit
1 = UART2 module is disabled
0 = UART2 module is enabled

bit 5 **U1MD:** UART1 Module Disable bit
1 = UART1 module is disabled
0 = UART1 module is enabled

bit 4 **SPI2MD:** SPI2 Module Disable bit
1 = SPI2 module is disabled
0 = SPI2 module is enabled

**Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
**2:** This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.

**REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1 (CONTINUED)**

bit 3 **SPI1MD:** SPI1 Module Disable bit
1 = SPI1 module is disabled
0 = SPI1 module is enabled

bit 2 **Unimplemented:** Read as '0'

bit 1 **C1MD:** ECAN1 Module Disable bit(2)
1 = ECAN1 module is disabled
0 = ECAN1 module is enabled

bit 0 **AD1MD:** ADC1 Module Disable bit
1 = ADC1 module is disabled
0 = ADC1 module is enabled

**Note 1:** This bit is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
**2:** This bit is available on dsPIC33EPXXXGP50X and dsPIC33EPXXXMC50X devices only.


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**REGISTER 10-2: PMD2: PERIPHERAL MODULE DISABLE CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | IC4MD | IC3MD | IC2MD | IC1MD |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | OC4MD | OC3MD | OC2MD | OC1MD |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **IC4MD:** Input Capture 4 Module Disable bit
1 = Input Capture 4 module is disabled
0 = Input Capture 4 module is enabled

bit 10 **IC3MD:** Input Capture 3 Module Disable bit
1 = Input Capture 3 module is disabled
0 = Input Capture 3 module is enabled

bit 9 **IC2MD:** Input Capture 2 Module Disable bit
1 = Input Capture 2 module is disabled
0 = Input Capture 2 module is enabled

bit 8 **IC1MD:** Input Capture 1 Module Disable bit
1 = Input Capture 1 module is disabled
0 = Input Capture 1 module is enabled

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **OC4MD:** Output Compare 4 Module Disable bit
1 = Output Compare 4 module is disabled
0 = Output Compare 4 module is enabled

bit 2 **OC3MD:** Output Compare 3 Module Disable bit
1 = Output Compare 3 module is disabled
0 = Output Compare 3 module is enabled

bit 1 **OC2MD:** Output Compare 2 Module Disable bit
1 = Output Compare 2 module is disabled
0 = Output Compare 2 module is enabled

bit 0 **OC1MD:** Output Compare 1 Module Disable bit
1 = Output Compare 1 module is disabled
0 = Output Compare 1 module is enabled

**REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | CMPMD | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CRCMD | — | — | — | — | — | I2C2MD | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **CRCMD:** CRC Module Disable bit
1 = CRC module is disabled
0 = CRC module is enabled

bit 6-2 **Unimplemented:** Read as '0'

bit 1 **I2C2MD:** I2C2 Module Disable bit
1 = I2C2 module is disabled
0 = I2C2 module is enabled

bit 0 **Unimplemented:** Read as '0'

**REGISTER 10-4: PMD4: PERIPHERAL MODULE DISABLE CONTROL REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | REFOMD | CTMUMD | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **REFOMD:** Reference Clock Module Disable bit
1 = Reference clock module is disabled
0 = Reference clock module is enabled

bit 2 **CTMUMD:** CTMU Module Disable bit
1 = CTMU module is disabled
0 = CTMU module is enabled

bit 1-0 **Unimplemented:** Read as '0'


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**REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | PWM3MD(1) | PWM2MD(1) | PWM1MD(1) |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10 **PWM3MD:** PWM3 Module Disable bit(1)
1 = PWM3 module is disabled
0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit(1)
1 = PWM2 module is disabled
0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit(1)
1 = PWM1 module is disabled
0 = PWM1 module is enabled

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** This bit is available on dsPIC33EPXXXMC50X/20X and PIC24EPXXXMC20X devices only.

**REGISTER 10-6: PMD7: PERIPHERAL MODULE DISABLE CONTROL REGISTER 7**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DMA0MD(1)<br>DMA1MD(1)<br>DMA2MD(1)<br>DMA3MD(1) | PTGMD | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as '0'

bit 4 **DMA0MD:** DMA0 Module Disable bit(1)
1 = DMA0 module is disabled
0 = DMA0 module is enabled

**DMA1MD:** DMA1 Module Disable bit(1)
1 = DMA1 module is disabled
0 = DMA1 module is enabled

**DMA2MD:** DMA2 Module Disable bit(1)
1 = DMA2 module is disabled
0 = DMA2 module is enabled

**DMA3MD:** DMA3 Module Disable bit(1)
1 = DMA3 module is disabled
0 = DMA3 module is enabled

bit 3 **PTGMD:** PTG Module Disable bit
1 = PTG module is disabled
0 = PTG module is enabled

bit 2-0 **Unimplemented:** Read as '0'

**Note 1:** This single bit enables and disables all four DMA channels.


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## 11.0 I/O PORTS

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"I/O Ports"** (www.microchip.com/DS70000598) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

Many of the device pins are shared among the peripherals and the parallel I/O ports. All I/O input ports feature Schmitt Trigger inputs for improved noise immunity.

### 11.1 Parallel I/O (PIO) Ports

Generally, a parallel I/O port that shares a pin with a peripheral is subservient to the peripheral. The peripheral's output buffer data and control signals are provided to a pair of multiplexers. The multiplexers select whether the peripheral or the associated port has ownership of the output data and control signals of the I/O pin. The logic also prevents "loop through," in which a port's digital output can drive the input of a peripheral that shares the same pin. Figure 11-1 illustrates how ports are shared with other peripherals and the associated I/O pin to which they are connected.

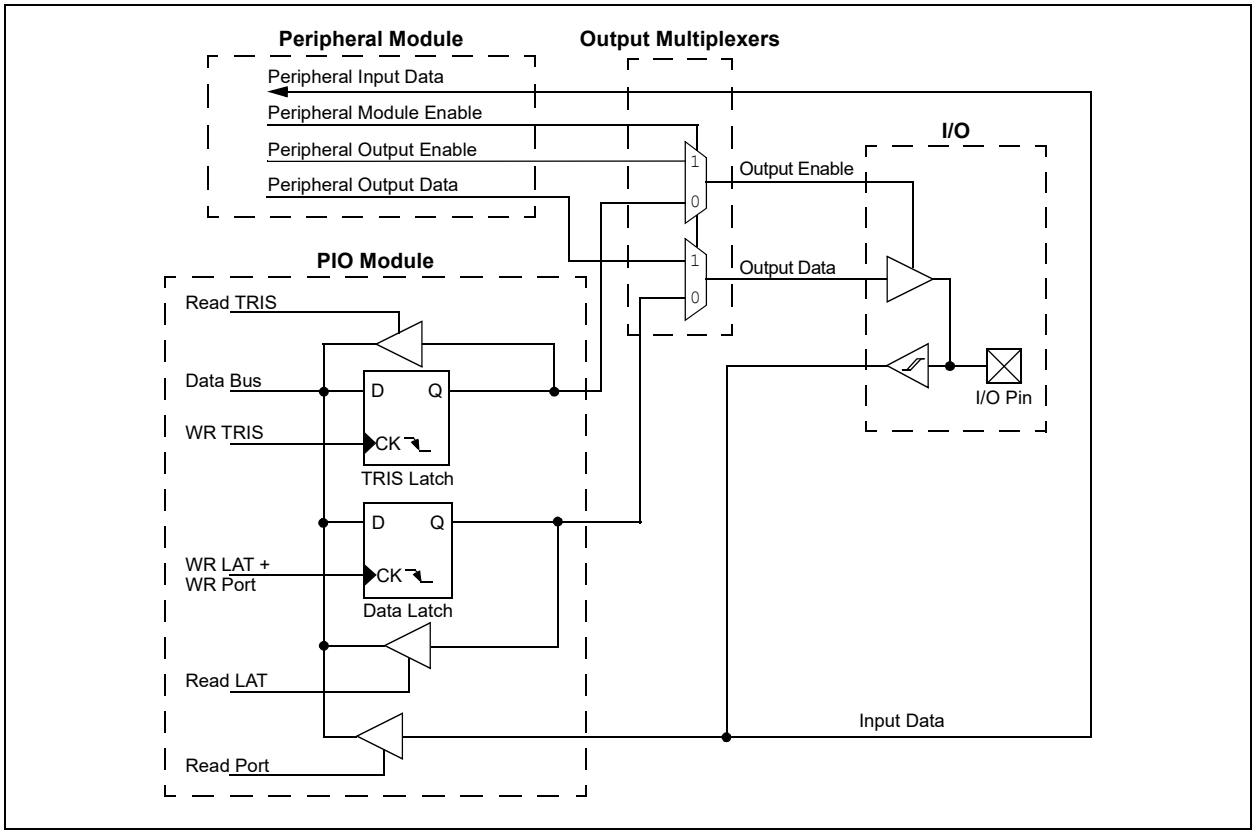
When a peripheral is enabled and the peripheral is actively driving an associated pin, the use of the pin as a general purpose output pin is disabled. The I/O pin can be read, but the output driver for the parallel port bit is disabled. If a peripheral is enabled, but the peripheral is not actively driving a pin, that pin can be driven by a port.

All port pins have eight registers directly associated with their operation as digital I/O. The Data Direction register (TRISx) determines whether the pin is an input or an output. If the data direction bit is a '1', then the pin is an input. All port pins are defined as inputs after a Reset. Reads from the Latch register (LATx) read the latch. Writes to the Latch write the latch. Reads from the port (PORTx) read the port pins, while writes to the port pins write the latch.

Any bit and its associated data and control registers that are not valid for a particular device is disabled. This means the corresponding LATx and TRISx registers and the port pin are read as zeros.

When a pin is shared with another peripheral or function that is defined as an input only, it is nevertheless regarded as a dedicated port because there is no other competing source of outputs.

**FIGURE 11-1: BLOCK DIAGRAM OF A TYPICAL SHARED PORT STRUCTURE**



### 11.1.1 OPEN-DRAIN CONFIGURATION

In addition to the PORTx, LATx and TRISx registers for data control, port pins can also be individually configured for either digital or open-drain output. This is controlled by the Open-Drain Control register, ODCx, associated with each port. Setting any of the bits configures the corresponding pin to act as an open-drain output.

The open-drain feature allows the generation of outputs other than VDD by using external pull-up resistors. The maximum open-drain voltage allowed on any pin is the same as the maximum VIH specification for that particular pin.

See the **"Pin Diagrams"** section for the available 5V tolerant pins and Table 30-11 for the maximum VIH specification for each pin.

## 11.2 Configuring Analog and Digital Port Pins

The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set. In order to use port pins for I/O functionality with digital modules, such as Timers, UARTs, etc., the corresponding ANSELx bit must be cleared. When ANSELx = 1 (the port is selected as analog) and TRISx = 1 (digital I/O enabled), the digital input value read by the port is always '0'.

The ANSELx register has a default value of 0xFFFF; therefore, all pins that share analog functions are analog (not digital) by default.

Pins with analog functions affected by the ANSELx registers are listed with a buffer type of analog in the Pinout I/O Descriptions (see Table 1-1).

If the TRISx bit is cleared (output) while the ANSELx bit is set, the digital output level (VOH or VOL) is converted by an analog peripheral, such as the ADC module or comparator module.

When the PORTx register is read, all pins configured as analog input channels are read as cleared (a low level).

Pins configured as digital inputs do not convert an analog input. Analog levels on any pin defined as a digital input (including the ANx pins) can cause the input buffer to consume current that exceeds the device specifications.

### 11.2.1 I/O PORT WRITE/READ TIMING

One instruction cycle is required between a port direction change or port write operation and a read operation of the same port. Typically this instruction would be a NOP, as shown in Example 11-1.

## 11.3 Input Change Notification (ICN)

The Input Change Notification function of the I/O ports allows devices to generate interrupt requests to the processor in response to a Change-of-State (COS) on selected input pins. This feature can detect input Change-of-States even in Sleep mode, when the clocks are disabled. Every I/O port pin can be selected (enabled) for generating an interrupt request on a Change-of-State.

Three control registers are associated with the Change Notification (CN) functionality of each I/O port. The CNENx registers contain the CN interrupt enable control bits for each of the input pins. Setting any of these bits enables a CN interrupt for the corresponding pins.

Each I/O pin also has a weak pull-up and a weak pull-down connected to it. The pull-ups and pull-downs act as a current source or sink source connected to the pin and eliminate the need for external resistors when push button, or keypad devices are connected. The pull-ups and pull-downs are enabled separately, using the CNPUx and the CNPDx registers, which contain the control bits for each of the pins. Setting any of the control bits enables the weak pull-ups and/or pull-downs for the corresponding pins.

| **Note:** | Pull-ups and pull-downs on Change Notification pins should always be disabled when the port pin is configured as a digital output. |
|---|---|

**EXAMPLE 11-1: PORT WRITE/READ EXAMPLE**

```
MOV   0xFF00, W0   ; Configure PORTB<15:8>
                   ; as inputs
MOV   W0, TRISB    ; and PORTB<7:0>
                   ; as outputs
NOP                ; Delay 1 cycle
BTSS  PORTB, #13   ; Next Instruction
```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## 11.4 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and their placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

### 11.4.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, “RPn” or “RPIn”, in their full pin designation, where “n” is the remappable pin number. “RP” is used to designate pins that support both remappable input and output functions, while “RPI” indicates pins that support remappable input functions only.

### 11.4.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital-only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital-only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral’s function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. These modules include $I^2C$ and the PWM. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/O and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

### 11.4.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral’s input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

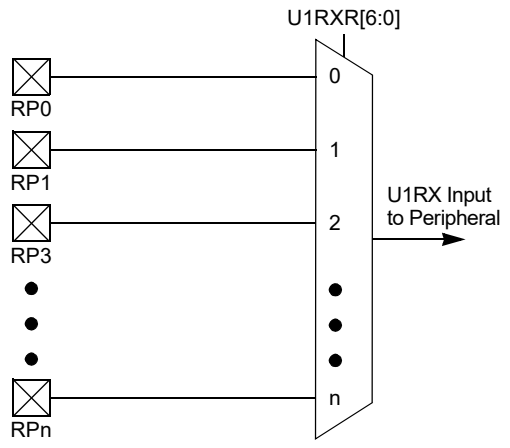
The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

### 11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-17). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

**FIGURE 11-2: REMAPPABLE INPUT FOR U1RX**




**Note:** For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

#### 11.4.4.1 Virtual Connections

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 25-1 in **Section 25.0 "Op Amp/Comparator Module"**) and the PTG module (see **Section 24.0 "Peripheral Trigger Generator (PTG) Module"**).

In addition, dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support virtual connections to the filtered QEI module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"**.

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R[6:0] bits of the RPINR12 register to the value of 'b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEI module allows peripherals to be connected to the QEI digital filter input. To utilize this filter, the QEI module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEI digital filter.

**EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43 OF THE dsPIC33EPXXXMC206 DEVICE**

```
RPINR15 = 0x2500;      /* Connect the QEI1 HOME1 input to RP37 (pin 43) */
RPINR7  = 0x009;       /* Connect the IC1 input to the digital filter on the FHOME1 input */

QEI1IOC = 0x4000;      /* Enable the QEI digital filter */
QEI1CON = 0x8000;      /* Enable the QEI module */
```


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**TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)**

| Input Name(1) | Function Name | Register | Configuration Bits |
|---|---|---|---|
| External Interrupt 1 | INT1 | RPINR0 | INT1R[6:0] |
| External Interrupt 2 | INT2 | RPINR1 | INT2R[6:0] |
| Timer2 External Clock | T2CK | RPINR3 | T2CKR[6:0] |
| Input Capture 1 | IC1 | RPINR7 | IC1R[6:0] |
| Input Capture 2 | IC2 | RPINR7 | IC2R[6:0] |
| Input Capture 3 | IC3 | RPINR8 | IC3R[6:0] |
| Input Capture 4 | IC4 | RPINR8 | IC4R[6:0] |
| Output Compare Fault A | OCFA | RPINR11 | OCFAR[6:0] |
| PWM Fault 1(3) | FLT1 | RPINR12 | FLT1R[6:0] |
| PWM Fault 2(3) | FLT2 | RPINR12 | FLT2R[6:0] |
| QEI1 Phase A(3) | QEA1 | RPINR14 | QEA1R[6:0] |
| QEI1 Phase B(3) | QEB1 | RPINR14 | QEB1R[6:0] |
| QEI1 Index(3) | INDX1 | RPINR15 | INDX1R[6:0] |
| QEI1 Home(3) | HOME1 | RPINR15 | HOM1R[6:0] |
| UART1 Receive | U1RX | RPINR18 | U1RXR[6:0] |
| UART2 Receive | U2RX | RPINR19 | U2RXR[6:0] |
| SPI2 Data Input | SDI2 | RPINR22 | SDI2R[6:0] |
| SPI2 Clock Input | SCK2 | RPINR22 | SCK2R[6:0] |
| SPI2 Slave Select | $\overline{SS2}$ | RPINR23 | SS2R[6:0] |
| CAN1 Receive(2) | C1RX | RPINR26 | C1RXR[6:0] |
| PWM Sync Input 1(3) | SYNCI1 | RPINR37 | SYNCI1R[6:0] |
| PWM Dead-Time Compensation 1(3) | DTCMP1 | RPINR38 | DTCMP1R[6:0] |
| PWM Dead-Time Compensation 2(3) | DTCMP2 | RPINR39 | DTCMP2R[6:0] |
| PWM Dead-Time Compensation 3(3) | DTCMP3 | RPINR39 | DTCMP3R[6:0] |

**Note 1:** Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

**2:** This input source is available on dsPIC33EPXXXGP/MC50X devices only.

**3:** This input source is available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES**

| Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment | Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment |
|---|---|---|---|---|---|
| 000 0000 | I | Vss | 010 1101 | I | RPI45 |
| 000 0001 | I | C1OUT(1) | 010 1110 | I | RPI46 |
| 000 0010 | I | C2OUT(1) | 010 1111 | I | RPI47 |
| 000 0011 | I | C3OUT(1) | 011 0000 | — | — |
| 000 0100 | I | C4OUT(1) | 011 0001 | — | — |
| 000 0101 | — | — | 011 0010 | — | — |
| 000 0110 | I | PTGO30(1) | 011 0011 | I | RPI51 |
| 000 0111 | I | PTGO31(1) | 011 0100 | I | RPI52 |
| 000 1000 | I | FINDX1(1,2) | 011 0101 | I | RPI53 |
| 000 1001 | I | FHOME1(1,2) | 011 0110 | I/O | RP54 |
| 000 1010 | — | — | 011 0111 | I/O | RP55 |
| 000 1011 | — | — | 011 1000 | I/O | RP56 |
| 000 1100 | — | — | 011 1001 | I/O | RP57 |
| 000 1101 | — | — | 011 1010 | I | RPI58 |
| 000 1110 | — | — | 011 1011 | — | — |
| 000 1111 | — | — | 011 1100 | — | — |
| 001 0000 | — | — | 011 1101 | — | — |
| 001 0001 | — | — | 011 1110 | — | — |
| 001 0010 | — | — | 011 1111 | — | — |
| 001 0011 | — | — | 100 0000 | — | — |
| 001 0100 | I/O | RP20 | 100 0001 | — | — |
| 001 0101 | — | — | 100 0010 | — | — |
| 001 0110 | — | — | 100 0011 | — | — |
| 001 0111 | — | — | 100 0100 | — | — |
| 001 1000 | I | RPI24 | 100 0101 | — | — |
| 001 1001 | I | RPI25 | 100 0110 | — | — |
| 001 1010 | — | — | 100 0111 | — | — |
| 001 1011 | I | RPI27 | 100 1000 | — | — |
| 001 1100 | I | RPI28 | 100 1001 | — | — |
| 001 1101 | — | — | 100 1010 | — | — |
| 001 1110 | — | — | 100 1011 | — | — |
| 001 1111 | — | — | 100 1100 | — | — |
| 010 0000 | I | RPI32 | 100 1101 | — | — |
| 010 0001 | I | RPI33 | 100 1110 | — | — |
| 010 0010 | I | RPI34 | 100 1111 | — | — |
| 010 0011 | I/O | RP35 | 101 0000 | — | — |
| 010 0100 | I/O | RP36 | 101 0001 | — | — |
| 010 0101 | I/O | RP37 | 101 0010 | — | — |
| 010 0110 | I/O | RP38 | 101 0011 | — | — |
| 010 0111 | I/O | RP39 | 101 0100 | — | — |

**Legend:** Shaded rows indicate PPS Input register values that are unimplemented.

**Note 1:** See **Section 11.4.4.1 "Virtual Connections"** for more information on selecting this pin assignment.

**2:** These inputs are available on dsPIC33EPXXXGP/MC50X devices only.


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**TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES (CONTINUED)**

| Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment | Peripheral Pin Select Input Register Value | Input/ Output | Pin Assignment |
|---|---|---|---|---|---|
| 010 1000 | I/O | RP40 | 101 0101 | — | — |
| 010 1001 | I/O | RP41 | 101 0110 | — | — |
| 010 1010 | I/O | RP42 | 101 0111 | — | — |
| 010 1011 | I/O | RP43 | 101 1000 | — | — |
| 010 1100 | I | RPI44 | 101 1001 | — | — |
| 101 1010 | — | — | 110 1101 | — | — |
| 101 1011 | — | — | 110 1110 | — | — |
| 101 1100 | — | — | 110 1111 | — | — |
| 101 1101 | — | — | 111 0000 | — | — |
| 101 1110 | I | RPI94 | 111 0001 | — | — |
| 101 1111 | I | RPI95 | 111 0010 | — | — |
| 110 0000 | I | RPI96 | 111 0011 | — | — |
| 110 0001 | I/O | RP97 | 111 0100 | — | — |
| 110 0010 | — | — | 111 0101 | — | — |
| 110 0011 | — | — | 111 0110 | I/O | RP118 |
| 110 0100 | — | — | 111 0111 | I | RPI119 |
| 110 0101 | — | — | 111 1000 | I/O | RP120 |
| 110 0110 | — | — | 111 1001 | I | RPI121 |
| 110 0111 | — | — | 111 1010 | — | — |
| 110 1000 | — | — | 111 1011 | — | — |
| 110 1001 | — | — | 111 1100 | — | — |
| 110 1010 | — | — | 111 1101 | — | — |
| 110 1011 | — | — | 111 1110 | — | — |
| 110 1100 | — | — | 111 1111 | — | — |

**Legend:** Shaded rows indicate PPS Input register values that are unimplemented.

**Note 1:** See **Section 11.4.4.1 "Virtual Connections"** for more information on selecting this pin assignment.

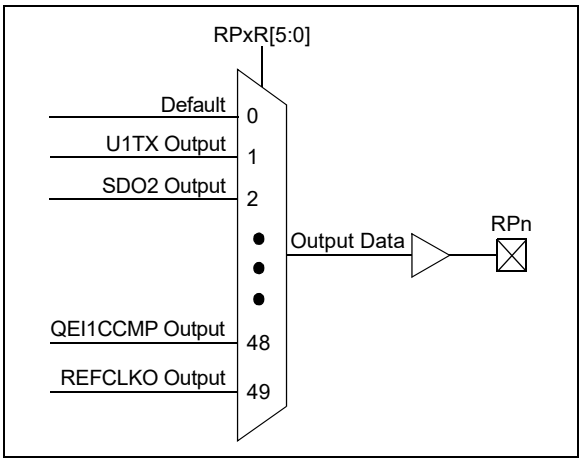
**2:** These inputs are available on dsPIC33EPXXXGP/MC50X devices only.

#### 11.4.4.2 Output Mapping

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 11-18 through Register 11-27). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

**FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUT FOR RPn**




#### 11.4.4.3 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

**TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)**

| Function | RPxR[5:0] | Output Name |
|---|---|---|
| Default PORT | 000000 | RPn tied to Default Pin |
| U1TX | 000001 | RPn tied to UART1 Transmit |
| U2TX | 000011 | RPn tied to UART2 Transmit |
| SDO2 | 001000 | RPn tied to SPI2 Data Output |
| SCK2 | 001001 | RPn tied to SPI2 Clock Output |
| $\overline{SS2}$ | 001010 | RPn tied to SPI2 Slave Select |
| C1TX(2) | 001110 | RPn tied to CAN1 Transmit |
| OC1 | 010000 | RPn tied to Output Compare 1 Output |
| OC2 | 010001 | RPn tied to Output Compare 2 Output |
| OC3 | 010010 | RPn tied to Output Compare 3 Output |
| OC4 | 010011 | RPn tied to Output Compare 4 Output |
| C1OUT | 011000 | RPn tied to Comparator Output 1 |
| C2OUT | 011001 | RPn tied to Comparator Output 2 |
| C3OUT | 011010 | RPn tied to Comparator Output 3 |
| SYNCO1(1) | 101101 | RPn tied to PWM Primary Time Base Sync Output |
| QEI1CCMP(1) | 101111 | RPn tied to QEI 1 Counter Comparator Output |
| REFCLKO | 110001 | RPn tied to Reference Clock Output |
| C4OUT | 110010 | RPn tied to Comparator Output 4 |

**Note 1:** This function is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** This function is available in dsPIC33EPXXXGP/MC50X devices only.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## 11.5 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 30-11, under “Injection Current”, have internal protection diodes to VDD and VSS. The term, “Injection Current”, is also referred to as “Clamp Current”. On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins by default after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a ‘0’, regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers in the I/O ports module (i.e., ANSELx) by setting the appropriate bit that corresponds to that I/O port pin to a ‘0’.

| **Note:** | Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver. |
|---|---|

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1. This indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPUx and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to ~(VDD – 0.8), not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristic specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the absolute maximum rating section of this data sheet. For example:

   VOH = 2.4V @ IOH = -8 mA and VDD = 3.3V

   The maximum output current sourced by any 8 mA I/O pin = 12 mA.

   LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in **Section 30.0 “Electrical Characteristics”** for additional information.
6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:
   a) Only one “output” function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
   b) It is possible to assign a “remappable output” function to multiple pins and externally short or tie them together for increased current drive.
   c) If any “dedicated output” function is enabled on a pin, it will take precedence over any remappable “output” function.
   d) If any “dedicated digital” (input or output) function is enabled on a pin, any number of “input” remappable functions can be mapped to the same pin.
   e) If any “dedicated analog” function(s) are enabled on a given pin, “digital input(s)” of any kind will all be disabled, although a single “digital output”, at the user’s cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input provided there is no external analog input, such as for a built-in self-test.
   f) Any number of “input” remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable “output”.

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g) The TRISx registers control *only* the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRIS setting. The TRISx register *does not* control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRIS settings, which means that the TRISx bit must be set to input for pins with only remappable input function(s) assigned

h) All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin has been disabled. Only the Analog Pin Select registers control the digital input buffer, *not* the TRISx register. The user must disable the analog function on a pin using the Analog Pin Select registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

## 11.6 I/O Ports Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 11.6.1 KEY RESOURCES

- **“I/O Ports”** (www.microchip.com/DS70000598) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools


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## 11.7 Peripheral Pin Select Registers

**REGISTER 11-1: RPINR0: PERIPHERAL PIN SELECT INPUT REGISTER 0**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | INT1R[6:0] | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **INT1R[6:0]:** Assign External Interrupt 1 (INT1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

**REGISTER 11-2: RPINR1: PERIPHERAL PIN SELECT INPUT REGISTER 1**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | INT2R[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **INT2R[6:0]:** Assign External Interrupt 2 (INT2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | T2CKR[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **T2CKR[6:0]:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-4: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC2R[6:0] | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC1R[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC2R[6:0]:** Assign Input Capture 2 (IC2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC1R[6:0]:** Assign Input Capture 1 (IC1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-5: RPINR8: PERIPHERAL PIN SELECT INPUT REGISTER 8**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC4R[6:0] | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC3R[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **IC4R[6:0]:** Assign Input Capture 4 (IC4) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **IC3R[6:0]:** Assign Input Capture 3 (IC3) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-6: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | OCFAR[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-0 **OCFAR[6:0]:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-7: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | FLT2R[6:0] | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | FLT1R[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **FLT2R[6:0]:** Assign PWM Fault 2 (FLT2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **FLT1R[6:0]:** Assign PWM Fault 1 (FLT1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-8: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | QEB1R[6:0] | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | QEA1R[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **QEB1R[6:0]:** Assign B (QEB) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **QEA1R[6:0]:** Assign A (QEA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-9: RPINR15: PERIPHERAL PIN SELECT INPUT REGISTER 15 (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | HOME1R[6:0] | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | INDX1R[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **HOME1R[6:0]:** Assign QEI1 HOME1 (HOME1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IND1XR[6:0]:** Assign QEI1 INDEX1 (INDX1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-10: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | U1RXR[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **U1RXR[6:0]:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-11: RPINR19: PERIPHERAL PIN SELECT INPUT REGISTER 19**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | U2RXR[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **U2RXR[6:0]:** Assign UART2 Receive (U2RX) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-12: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SCK2INR[6:0] | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SDI2R[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **SCK2INR[6:0]:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **SDI2R[6:0]:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-13: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SS2R[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **SS2R[6:0]:** Assign SPI2 Slave Select ($\overline{SS2}$) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-14: RPINR26: PERIPHERAL PIN SELECT INPUT REGISTER 26 (dsPIC33EPXXXGP/MC50X DEVICES ONLY)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | C1RXR[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as '0'

bit 6-0 **C1RXR[6:0]:** Assign CAN1 RX Input (CRX1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**REGISTER 11-15: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | SYNCI1R[6:0] | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **SYNCI1R[6:0]:** Assign PWM Synchronization Input 1 (SYNCI1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'


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**REGISTER 11-16: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38 (dsPIC33EPXXXMC20X AND PIC24EPXXXMC20X DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP1R[6:0] | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP1R[6:0]:** Assign PWM Dead-Time Compensation Input 1 (DTCMP1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

**REGISTER 11-17: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39 (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP3R[6:0] | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | DTCMP2R[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP3R[6:0]:** Assign PWM Dead-Time Compensation Input 3 (DTCMP3) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DTCMP2R[6:0]:** Assign PWM Dead-Time Compensation Input 2 (DTCMP2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111001 = Input tied to RPI121
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss


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**REGISTER 11-18: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP35R[5:0] | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP20R[5:0] | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP35R[5:0]:** Peripheral Output Function is Assigned to RP35 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP20R[5:0]:** Peripheral Output Function is Assigned to RP20 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-19: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP37R[5:0] | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP36R[5:0] | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP37R[5:0]:** Peripheral Output Function is Assigned to RP37 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP36R[5:0]:** Peripheral Output Function is Assigned to RP36 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-20: RPOR2: PERIPHERAL PIN SELECT OUTPUT REGISTER 2**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP39R[5:0] | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP38R[5:0] | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP39R[5:0]:** Peripheral Output Function is Assigned to RP39 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP38R[5:0]:** Peripheral Output Function is Assigned to RP38 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-21: RPOR3: PERIPHERAL PIN SELECT OUTPUT REGISTER 3**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP41R[5:0] | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP40R[5:0] | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP41R[5:0]:** Peripheral Output Function is Assigned to RP41 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP40R[5:0]:** Peripheral Output Function is Assigned to RP40 Output Pin bits (see Table 11-3 for peripheral function numbers)


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**REGISTER 11-22: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP43R[5:0] | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP42R[5:0] | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP43R[5:0]:** Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP42R[5:0]:** Peripheral Output Function is Assigned to RP42 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-23: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP55R[5:0] | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP54R[5:0] | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP55R[5:0]:** Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP54R[5:0]:** Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-24: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP57R[5:0] | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP56R[5:0] | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP57R[5:0]:** Peripheral Output Function is Assigned to RP57 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP56R[5:0]:** Peripheral Output Function is Assigned to RP56 Output Pin bits (see Table 11-3 for peripheral function numbers)

**REGISTER 11-25: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP97R[5:0] | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP97R[5:0]:** Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-0 **Unimplemented:** Read as '0'


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**REGISTER 11-26: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP118R[5:0] | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **RP118R[5:0]:** Peripheral Output Function is Assigned to RP118 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-0 **Unimplemented:** Read as ‘0’

**REGISTER 11-27: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | RP120R[5:0] | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **RP120R[5:0]:** Peripheral Output Function is Assigned to RP120 Output Pin bits (see Table 11-3 for peripheral function numbers)

**NOTES:**


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## 12.0 TIMER1

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (www.microchip.com/DS70362) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be Operated in Asynchronous Counter mode from an External Clock Source
- The External Clock Input (T1CK) can Optionally be Synchronized to the Internal Device Clock and the Clock Synchronization is Performed after the Prescaler

A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

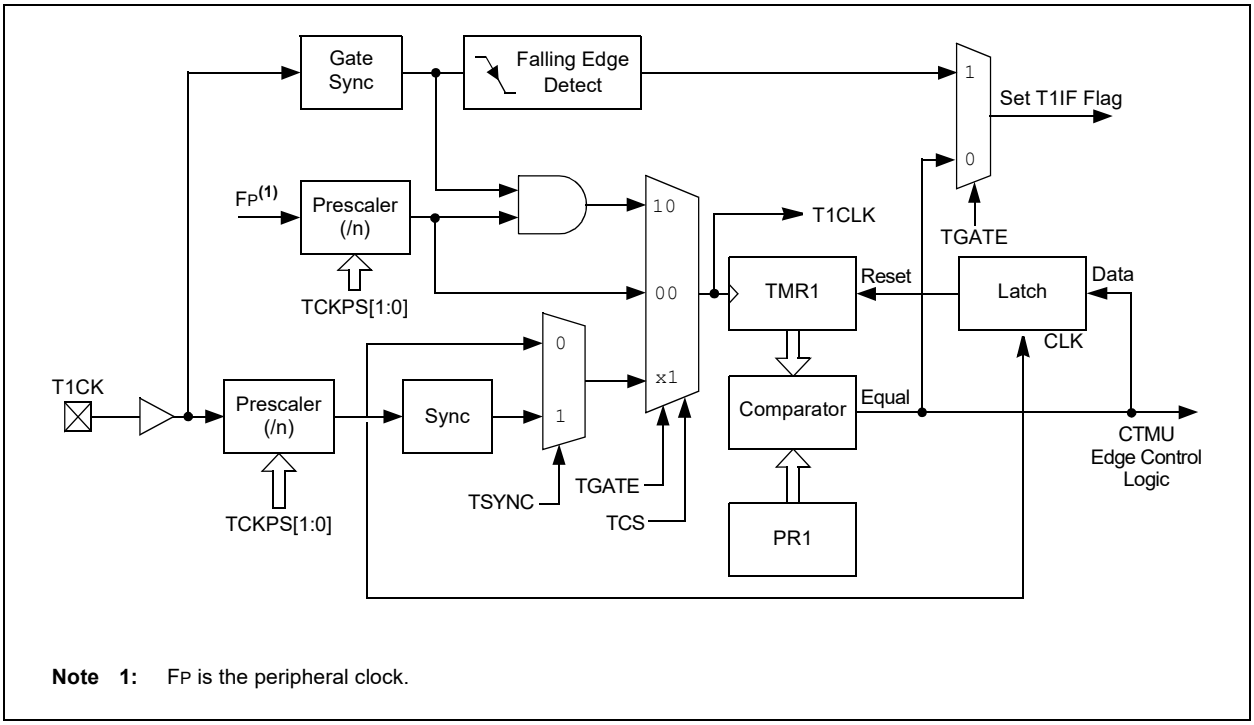
- Timer Clock Source Control bit (TCS): T1CON[1]
- Timer Synchronization Control bit (TSYNC): T1CON[2]
- Timer Gate Control bit (TGATE): T1CON[6]

Timer control bit setting for different operating modes are given in the Table 12-1.

**TABLE 12-1: TIMER MODE SETTINGS**

| Mode | TCS | TGATE | TSYNC |
|---|---|---|---|
| Timer | 0 | 0 | x |
| Gated Timer | 0 | 1 | x |
| Synchronous Counter | 1 | x | 1 |
| Asynchronous Counter | 1 | x | 0 |

**FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM**




**Note 1:** FP is the peripheral clock.

## 12.1 Timer1 Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 12.1.1 KEY RESOURCES

- **"Timers"** (www.microchip.com/DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools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## 12.2 Timer1 Control Register

**REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON(1) | — | TSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE | TCKPS1 | TCKPS0 | — | TSYNC(1) | TCS(1) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timer1 On bit(1)
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS[1:0]:** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit(1)
When TCS = 1:
1 = Synchronizes external clock input
0 = Does not synchronize external clock input
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit(1)
1 = External clock is from pin, T1CK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.

**NOTES:**


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## 13.0 TIMER2/3 AND TIMER4/5

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (www.microchip.com/DS70362) of the *"dsPIC33/PIC24 Family Reference Manual"*.

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare Modules (Timer2 and Timer3 only)
- ADC1 Event Trigger (32-bit timer pairs, and Timer3 and Timer5 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, and T4CON, T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

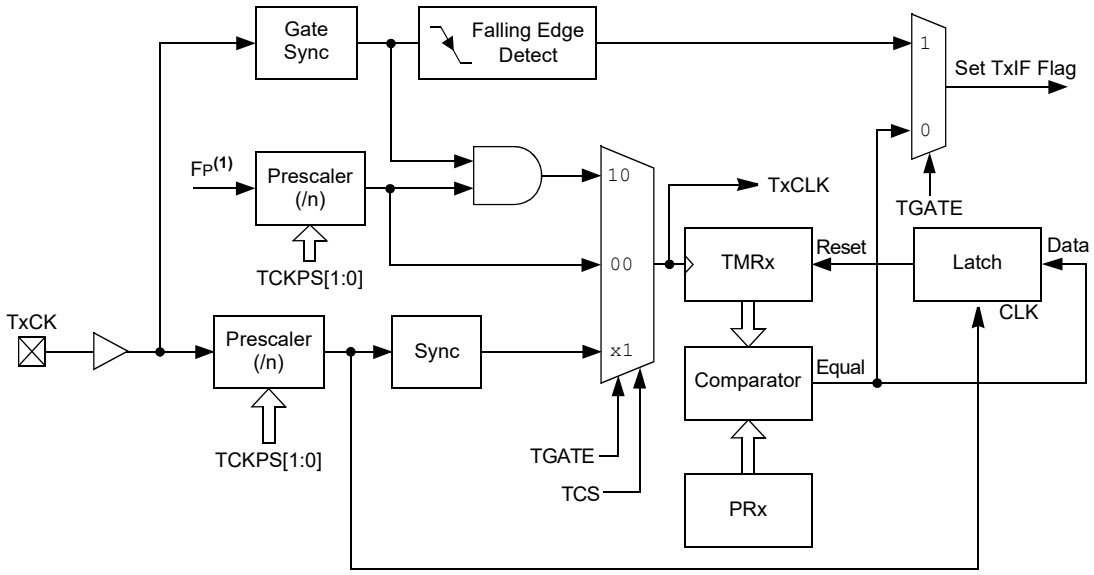
For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

**Note:** For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-3.

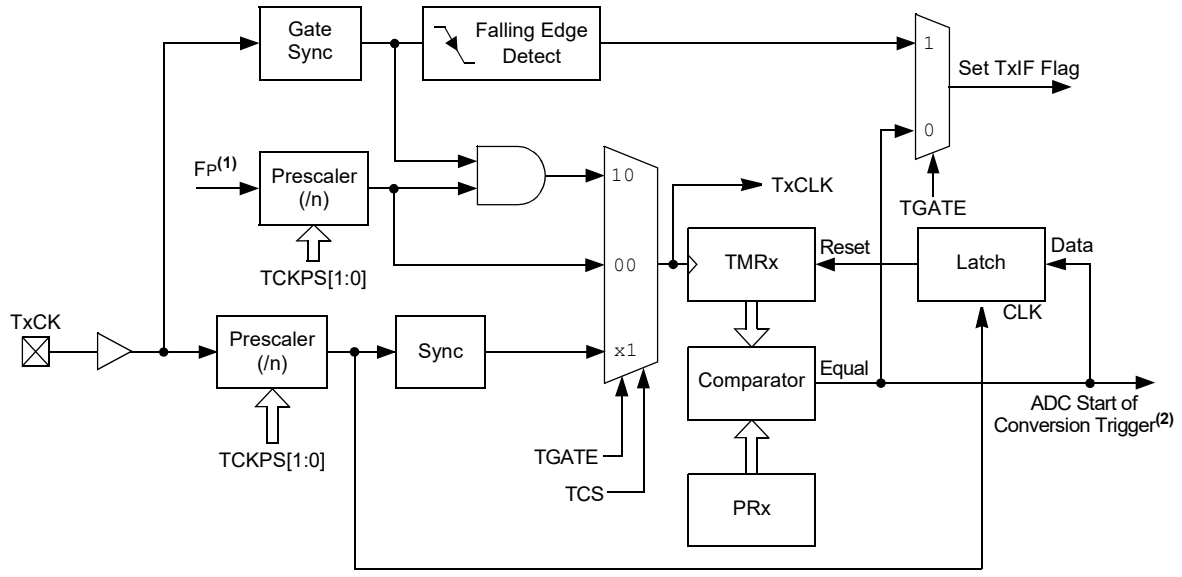
**Note:** Only Timer2, 3, 4 and 5 can trigger a DMA data transfer.

**FIGURE 13-1: TYPE B TIMER BLOCK DIAGRAM (x = 2 AND 4)**




**Note 1:** FP is the peripheral clock.

**FIGURE 13-2: TYPE C TIMER BLOCK DIAGRAM (x = 3 AND 5)**




**Note 1:** FP is the peripheral clock.
**2:** The ADC trigger is available on TMR3 and TMR5 only.


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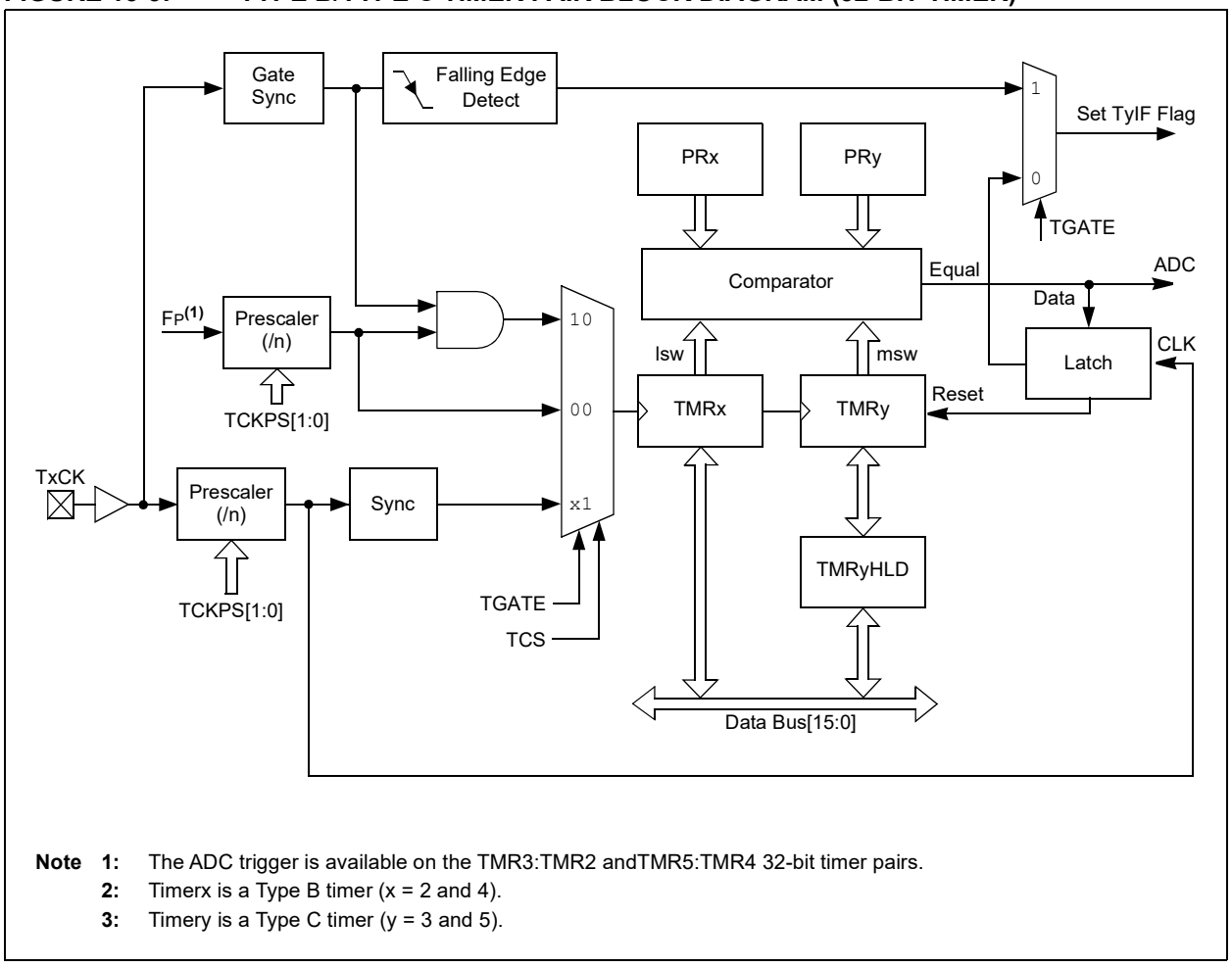
**FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)**




**Note 1:** The ADC trigger is available on the TMR3:TMR2 andTMR5:TMR4 32-bit timer pairs.
**2:** Timerx is a Type B timer (x = 2 and 4).
**3:** Timery is a Type C timer (y = 3 and 5).

## 13.1 Timerx/y Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 13.1.1 KEY RESOURCES

- **"Timers"** (www.microchip.com/DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 13.2 Timer Control Registers

**REGISTER 13-1: TxCON: (TIMER2 AND TIMER4) CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON | — | TSIDL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE | TCKPS1 | TCKPS0 | T32 | — | TCS(1) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timerx On bit
When T32 = 1:
1 = Starts 32-bit Timerx/y
0 = Stops 32-bit Timerx/y
When T32 = 0:
1 = Starts 16-bit Timerx
0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS[1:0]:** Timerx Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **T32:** 32-Bit Timer Mode Select bit
1 = Timerx and Timery form a single 32-bit timer
0 = Timerx and Timery act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit(1)
1 = External clock is from pin, TxCK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** The TxCK pin is not available on all devices. See the **"Pin Diagrams"** section for the available pins.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**REGISTER 13-2: TyCON: (TIMER3 AND TIMER5) CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON(1) | — | TSIDL(2) | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE(1) | TCKPS1(1) | TCKPS0(1) | — | — | TCS(1,3) | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timery On bit(1)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(2)
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(1)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS[1:0]:** Timery Input Clock Prescale Select bits(1)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(1,3)
1 = External clock is from pin, TyCK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

**Note 1:** When 32-bit operation is enabled (T2CON[3] = 1), these bits have no effect on Timery operation; all timer functions are set through TxCON.

**2:** When 32-bit timer operation is enabled (T32 = 1) in the Timerx Control register (TxCON[3]), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

**3:** The TyCK pin is not available on all devices. See the **"Pin Diagrams"** section for the available pins.

**NOTES:**


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## 14.0 INPUT CAPTURE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Input Capture with Dedicated Timer"** (www.microchip.com/DS70000352) in the "*dsPIC33/dsPIC24 Family Reference Manual*".

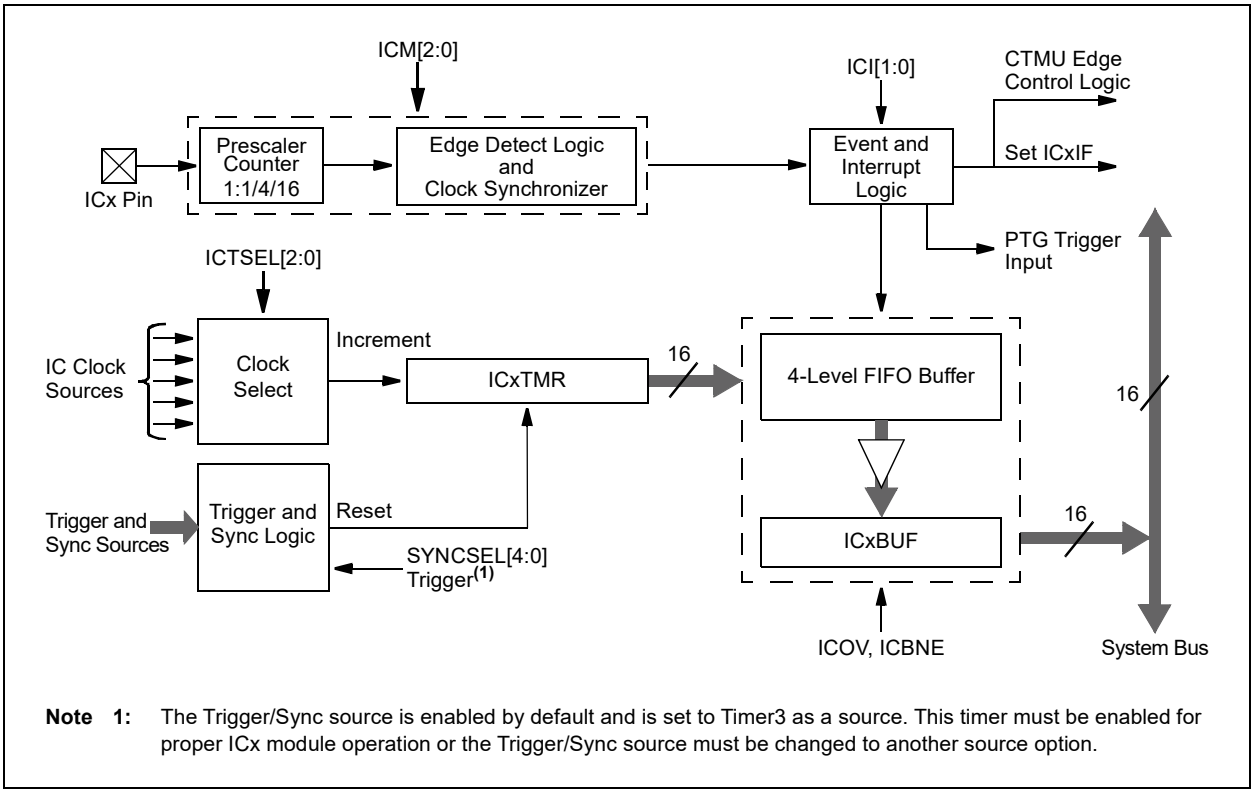
**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurement. The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices support four input capture channels.

Key features of the input capture module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 19 user-selectable Trigger/Sync sources available
- A 4-level FIFO buffer for capturing and holding timer values for several events
- Configurable interrupt generation
- Up to six clock sources available for each module, driving a separate internal 16-bit counter

**FIGURE 14-1: INPUT CAPTURE x MODULE BLOCK DIAGRAM**




**Note 1:** The Trigger/Sync source is enabled by default and is set to Timer3 as a source. This timer must be enabled for proper ICx module operation or the Trigger/Sync source must be changed to another source option.

## 14.1 Input Capture Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 14.1.1 KEY RESOURCES

- **"Input Capture with Dedicated Timer"** (www.microchip.com/DS70000352) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools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## 14.2 Input Capture Registers

**REGISTER 14-1: ICxCON1: INPUT CAPTURE x CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | ICSIDL | ICTSEL2 | ICTSEL1 | ICTSEL0 | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/HC/HS-0 | R/HC/HS-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | ICI1 | ICI0 | ICOV | ICBNE | ICM2 | ICM1 | ICM0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **ICSIDL:** Input Capture Stop in Idle Control bit
- 1 = Input capture will halt in CPU Idle mode
- 0 = Input capture will continue to operate in CPU Idle mode

bit 12-10 **ICTSEL[2:0]:** Input Capture Timer Select bits
- 111 = Peripheral clock (FP) is the clock source of the ICx
- 110 = Reserved
- 101 = Reserved
- 100 = T1CLK is the clock source of the ICx (only the synchronous clock is supported)
- 011 = T5CLK is the clock source of the ICx
- 010 = T4CLK is the clock source of the ICx
- 001 = T2CLK is the clock source of the ICx
- 000 = T3CLK is the clock source of the ICx

bit 9-7 **Unimplemented:** Read as '0'

bit 6-5 **ICI[1:0]:** Number of Captures per Interrupt Select bits (this field is not used if ICM[2:0] = 001 or 111)
- 11 = Interrupt on every fourth capture event
- 10 = Interrupt on every third capture event
- 01 = Interrupt on every second capture event
- 00 = Interrupt on every capture event

bit 4 **ICOV:** Input Capture Overflow Status Flag bit (read-only)
- 1 = Input capture buffer overflow occurred
- 0 = No input capture buffer overflow occurred

bit 3 **ICBNE:** Input Capture Buffer Not Empty Status bit (read-only)
- 1 = Input capture buffer is not empty, at least one more capture value can be read
- 0 = Input capture buffer is empty

bit 2-0 **ICM[2:0]:** Input Capture Mode Select bits
- 111 = Input capture functions as interrupt pin only in CPU Sleep and Idle modes (rising edge detect only, all other control bits are not applicable)
- 110 = Unused (module is disabled)
- 101 = Capture mode, every 16th rising edge (Prescaler Capture mode)
- 100 = Capture mode, every 4th rising edge (Prescaler Capture mode)
- 011 = Capture mode, every rising edge (Simple Capture mode)
- 010 = Capture mode, every falling edge (Simple Capture mode)
- 001 = Capture mode, every edge rising and falling (Edge Detect mode (ICI[1:0]) is not used in this mode)
- 000 = Input capture module is turned off

**REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | IC32 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W/HS-0 | U-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-1 |
|---|---|---|---|---|---|---|---|
| ICTRIG(2) | TRIGSTAT(3) | — | SYNCSEL4(4) | SYNCSEL3(4) | SYNCSEL2(4) | SYNCSEL1(4) | SYNCSEL0(4) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **IC32:** Input Capture 32-Bit Timer Mode Select bit (Cascade mode)
1 = Odd IC and Even IC form a single 32-bit input capture module(1)
0 = Cascade module operation is disabled

bit 7 **ICTRIG:** Input Capture Trigger Operation Select bit(2)
1 = Input source used to trigger the input capture timer (Trigger mode)
0 = Input source used to synchronize the input capture timer to a timer of another module (Synchronization mode)

bit 6 **TRIGSTAT:** Timer Trigger Status bit(3)
1 = ICxTMR has been triggered and is running
0 = ICxTMR has not been triggered and is being held clear

bit 5 **Unimplemented:** Read as '0'

**Note 1:** The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.
**2:** The input source is selected by the SYNCSEL[4:0] bits of the ICxCON2 register.
**3:** This bit is set by the selected input source (selected by SYNCSEL[4:0] bits). It can be read, set and cleared in software.
**4:** Do not use the ICx module as its own Sync or Trigger source.
**5:** This option should only be selected as a trigger source and not as a synchronization source.
**6:** Each Input Capture x (ICx) module has one PTG input source. See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO8 = IC1
PTGO9 = IC2
PTGO10 = IC3
PTGO11 = IC4


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**REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)**

bit 4-0 **SYNCSEL[4:0]:** Input Source Select for Synchronization and Trigger Operation bits(4)

11111 = No Sync or Trigger source for ICx
11110 = Reserved
11101 = Reserved
11100 = CTMU module synchronizes or triggers ICx(5)
11011 = ADC1 module synchronizes or triggers ICx(5)
11010 = CMP3 module synchronizes or triggers ICx(5)
11001 = CMP2 module synchronizes or triggers ICx(5)
11000 = CMP1 module synchronizes or triggers ICx(5)
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = Reserved
10011 = IC4 module synchronizes or triggers ICx
10010 = IC3 module synchronizes or triggers ICx
10001 = IC2 module synchronizes or triggers ICx
10000 = IC1 module synchronizes or triggers ICx
01111 = Timer5 synchronizes or triggers ICx
01110 = Timer4 synchronizes or triggers ICx
01101 = Timer3 synchronizes or triggers ICx **(default)**
01100 = Timer2 synchronizes or triggers ICx
01011 = Timer1 synchronizes or triggers ICx
01010 = PTGOx module synchronizes or triggers ICx(6)
01001 = Reserved
01000 = Reserved
00111 = Reserved
00110 = Reserved
00101 = Reserved
00100 = OC4 module synchronizes or triggers ICx
00011 = OC3 module synchronizes or triggers ICx
00010 = OC2 module synchronizes or triggers ICx
00001 = OC1 module synchronizes or triggers ICx
00000 = No Sync or Trigger source for ICx

**Note 1:** The IC32 bit in both the Odd and Even IC must be set to enable Cascade mode.

**2:** The input source is selected by the SYNCSEL[4:0] bits of the ICxCON2 register.

**3:** This bit is set by the selected input source (selected by SYNCSEL[4:0] bits). It can be read, set and cleared in software.

**4:** Do not use the ICx module as its own Sync or Trigger source.

**5:** This option should only be selected as a trigger source and not as a synchronization source.

**6:** Each Input Capture x (ICx) module has one PTG input source. See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO8 = IC1
PTGO9 = IC2
PTGO10 = IC3
PTGO11 = IC4

**NOTES:**


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## 15.0 OUTPUT COMPARE

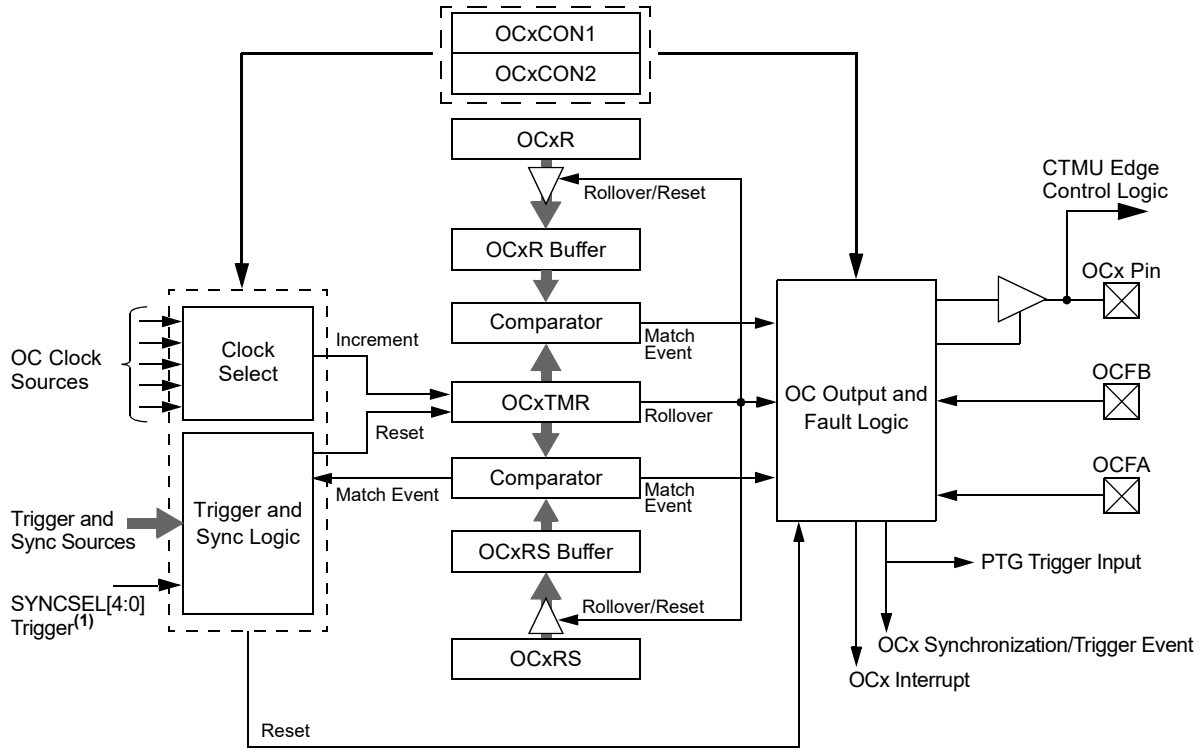
**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Output Compare"** (www.microchip.com/DS70000358) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The output compare module can select one of seven available clock sources for its time base. The module compares the value of the timer with the value of one or two compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the compare register value. The output compare module generates either a single output pulse or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

**Note:** Refer to **"Output Compare"** (www.microchip.com/DS70000358) in the *"dsPIC33/PIC24 Family Reference Manual"* for OCxR and OCxRS register restrictions.

**FIGURE 15-1: OUTPUT COMPARE x MODULE BLOCK DIAGRAM**




**Note 1:** The Trigger/Sync source is enabled by default and is set to Timer2 as a source. This timer must be enabled for proper OCx module operation or the Trigger/Sync source must be changed to another source option.

## 15.1 Output Compare Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 15.1.1 KEY RESOURCES

- **"Output Compare"** (www.microchip.com/DS70000358) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools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## 15.2 Output Compare Control Registers

**REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | ENFLTB |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | HSC/R/W-0 | HSC/R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ENFLTA | — | OCFLTB | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HSC = Hardware Settable/Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **OCSIDL:** Output Compare x Stop in Idle Mode Control bit
1 = Output Compare x halts in CPU Idle mode
0 = Output Compare x continues to operate in CPU Idle mode

bit 12-10 **OCTSEL[2:0]:** Output Compare x Clock Select bits
111 = Peripheral clock (FP)
110 = Reserved
101 = PTGOx clock(2)
100 = T1CLK is the clock source of the OCx (only the synchronous clock is supported)
011 = T5CLK is the clock source of the OCx
010 = T4CLK is the clock source of the OCx
001 = T3CLK is the clock source of the OCx
000 = T2CLK is the clock source of the OCx

bit 9 **Unimplemented:** Read as '0'

bit 8 **ENFLTB:** Fault B Input Enable bit
1 = Output Compare Fault B input (OCFB) is enabled
0 = Output Compare Fault B input (OCFB) is disabled

bit 7 **ENFLTA:** Fault A Input Enable bit
1 = Output Compare Fault A input (OCFA) is enabled
0 = Output Compare Fault A input (OCFA) is disabled

bit 6 **Unimplemented:** Read as '0'

bit 5 **OCFLTB:** PWM Fault B Condition Status bit
1 = PWM Fault B condition on OCFB pin has occurred
0 = No PWM Fault B condition on OCFB pin has occurred

bit 4 **OCFLTA:** PWM Fault A Condition Status bit
1 = PWM Fault A condition on OCFA pin has occurred
0 = No PWM Fault A condition on OCFA pin has occurred

**Note 1:** OCxR and OCxRS are double-buffered in PWM mode only.

**2:** Each Output Compare x module (OCx) has one PTG clock source. See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO4 = OC1
PTGO5 = OC2
PTGO6 = OC3
PTGO7 = OC4

**REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)**

bit 3 **TRIGMODE:** Trigger Status Mode Select bit
1 = TRIGSTAT (OCxCON2[6]) is cleared when OCxRS = OCxTMR or in software
0 = TRIGSTAT is cleared only by software

bit 2-0 **OCM[2:0]:** Output Compare x Mode Select bits
111 = Center-Aligned PWM mode: Output set high when OCxTMR = OCxR and set low when OCxTMR = OCxRS(1)
110 = Edge-Aligned PWM mode: Output set high when OCxTMR = 0 and set low when OCxTMR = OCxR(1)
101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS
100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle
011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin
010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low
001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high
000 = Output compare channel is disabled

**Note 1:** OCxR and OCxRS are double-buffered in PWM mode only.

**2:** Each Output Compare x module (OCx) has one PTG clock source. See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO4 = OC1
PTGO5 = OC2
PTGO6 = OC3
PTGO7 = OC4


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**REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | HS/R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FLTMD:** Fault Mode Select bit
1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit
1 = PWM output is driven high on a Fault
0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit
1 = OCx pin is tri-stated on a Fault condition
0 = OCx pin I/O state is defined by the FLTOUT bit on a Fault condition

bit 12 **OCINV:** Output Compare x Invert bit
1 = OCx output is inverted
0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)
1 = Cascade module operation is enabled
0 = Cascade module operation is disabled

bit 7 **OCTRIG:** Output Compare x Trigger/Sync Select bit
1 = Triggers OCx from the source designated by the SYNCSELx bits
0 = Synchronizes OCx with the source designated by the SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit
1 = Timer source has been triggered and is running
0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** Output Compare x Output Pin Direction Select bit
1 = OCx is tri-stated
0 = Output Compare x module drives the OCx pin

**Note 1:** Do not use the OCx module as its own Synchronization or Trigger source.

**2:** When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

**3:** Each Output Compare x module (OCx) has one PTG Trigger/Synchronization source. See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO0 = OC1
PTGO1 = OC2
PTGO2 = OC3
PTGO3 = OC4

**REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)**

bit 4-0 **SYNCSEL[4:0]:** Trigger/Synchronization Source Selection bits

11111 = OCxRS compare event is used for synchronization
11110 = INT2 pin synchronizes or triggers OCx
11101 = INT1 pin synchronizes or triggers OCx
11100 = CTMU module synchronizes or triggers OCx
11011 = ADC1 module synchronizes or triggers OCx
11010 = CMP3 module synchronizes or triggers OCx
11001 = CMP2 module synchronizes or triggers OCx
11000 = CMP1 module synchronizes or triggers OCx
10111 = Reserved
10110 = Reserved
10101 = Reserved
10100 = Reserved
10011 = IC4 input capture event synchronizes or triggers OCx
10010 = IC3 input capture event synchronizes or triggers OCx
10001 = IC2 input capture event synchronizes or triggers OCx
10000 = IC1 input capture event synchronizes or triggers OCx
01111 = Timer5 synchronizes or triggers OCx
01110 = Timer4 synchronizes or triggers OCx
01101 = Timer3 synchronizes or triggers OCx
01100 = Timer2 synchronizes or triggers OCx **(default)**
01011 = Timer1 synchronizes or triggers OCx
01010 = PTGOx synchronizes or triggers OCx(3)
01001 = Reserved
01000 = Reserved
00111 = Reserved
00110 = Reserved
00101 = Reserved
00100 = OC4 module synchronizes or triggers OCx(1,2)
00011 = OC3 module synchronizes or triggers OCx(1,2)
00010 = OC2 module synchronizes or triggers OCx(1,2)
00001 = OC1 module synchronizes or triggers OCx(1,2)
00000 = No Sync or Trigger source for OCx

**Note 1:** Do not use the OCx module as its own Synchronization or Trigger source.

**2:** When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a Trigger source, the OCy module must be unselected as a Trigger source prior to disabling it.

**3:** Each Output Compare x module (OCx) has one PTG Trigger/Synchronization source. See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO0 = OC1
PTGO1 = OC2
PTGO2 = OC3
PTGO3 = OC4


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# 16.0 HIGH-SPEED PWM MODULE (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"High-Speed PWM"** (www.microchip.com/DS70645) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices support a dedicated Pulse-Width Modulation (PWM) module with up to six outputs.

The high-speed PWMx module consists of the following major features:

- Three PWM Generators
- Two PWM Outputs per PWM Generator
- Individual Period and Duty Cycle for Each PWM Pair
- Duty Cycle, Dead Time, Phase Shift and Frequency Resolution of TCY/2 (7.14 ns at FCY = 70 MHz)
- Independent Fault and Current-Limit Inputs for Six PWM Outputs
- Redundant Output
- Center-Aligned PWM mode
- Output Override Control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for Input Clock
- PWMxL and PWMxH Output Pin Swapping
- Independent PWM Frequency, Duty Cycle and Phase-Shift Changes for Each PWM Generator
- Dead-Time Compensation
- Enhanced Leading-Edge Blanking (LEB) Functionality
- Frequency Resolution Enhancement
- PWM Capture Functionality

**Note:** In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 7.14 ns.

The high-speed PWMx module contains up to three PWM generators. Each PWM generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWMx can generate a trigger to the ADC module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADC module based on either of the two master time bases.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 input pin that utilizes PPS, can synchronize the high-speed PWMx module with an external signal. The SYNCO1 pin is an output pin that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

## 16.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs to include FLT1 and FLT2 which are re-mappable using the PPS feature, FLT3 and FLT4 which are available only on the larger 44-pin and 64-pin packages, and FLT32 which has been implemented with Class B safety features, and is available on a fixed pin on all dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

### 16.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the high-speed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled low externally or the internal pull-down resistor in the CNPDx register can be enabled.

**Note:** The Fault mode may be changed using the FLTMOD[1:0] bits (FCLCON[1:0]), regardless of the state of FLT32.

### 16.1.2 WRITE-PROTECTED REGISTERS

On dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FOSCSEL[6]). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring, PWMLOCK = 0.

To gain write access to these locked registers, the user application must write two consecutive values of (0xABCD and 0x4321) to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in Example 16-1.

**EXAMPLE 16-1: PWMx WRITE-PROTECTED REGISTER UNLOCK SEQUENCE**

```
; FLT32 pin must be pulled low externally in order to clear and disable the fault
; Writing to FCLCON1 register requires unlock sequence

mov #0xabcd,w10        ; Load first unlock key to w10 register
mov #0x4321,w11        ; Load second unlock key to w11 register
mov #0x0000,w0         ; Load desired value of FCLCON1 register in w0
mov w10, PWMKEY        ; Write first unlock key to PWMKEY register
mov w11, PWMKEY        ; Write second unlock key to PWMKEY register
mov w0,FCLCON1         ; Write desired value to FCLCON1 register

; Set PWM ownership and polarity using the IOCON1 register
; Writing to IOCON1 register requires unlock sequence

mov #0xabcd,w10        ; Load first unlock key to w10 register
mov #0x4321,w11        ; Load second unlock key to w11 register
mov #0xF000,w0         ; Load desired value of IOCON1 register in w0
mov w10, PWMKEY        ; Write first unlock key to PWMKEY register
mov w11, PWMKEY        ; Write second unlock key to PWMKEY register
mov w0,IOCON1          ; Write desired value to IOCON1 register
```


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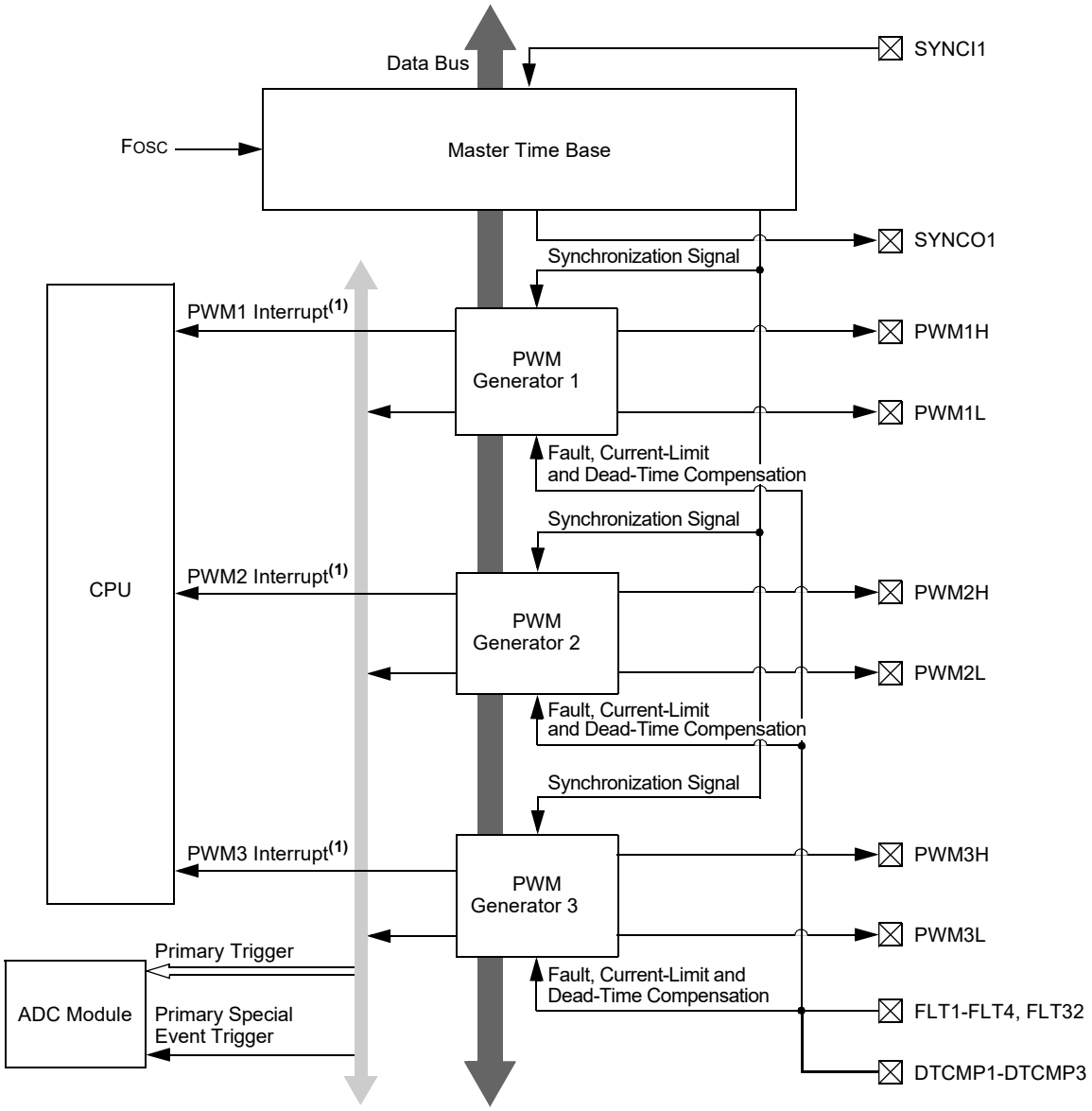
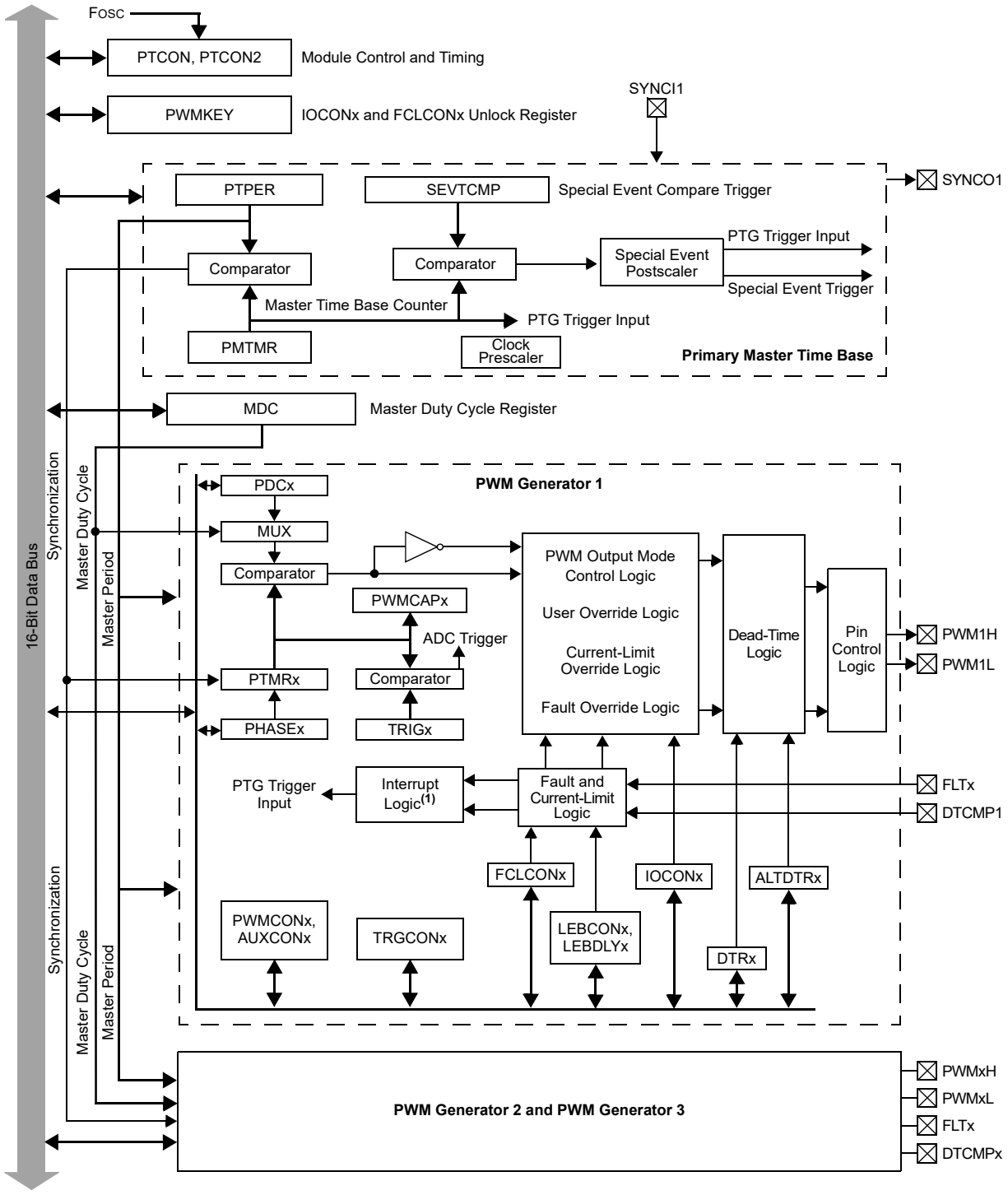
**FIGURE 16-1: HIGH-SPEED PWMx MODULE ARCHITECTURAL OVERVIEW**




**Note 1:** The PWM interrupts are generated by logically ORing the FLTSTAT, CLSTAT and TRGSTAT status bits for the given PWM generator. Refer to **"High-Speed PWM"** (www.microchip.com/DS70645) in the *"dsPIC33/PIC24 Family Reference Manual"* for more information.

**FIGURE 16-2: HIGH-SPEED PWMx MODULE REGISTER INTERCONNECTION DIAGRAM**




**Note 1:** The PWM interrupts are generated by logically ORing the FLTSTAT, CLSTAT and TRGSTAT status bits for the given PWM generator. Refer to **"High-Speed PWM"** (www.microchip.com/DS70645) in the *"dsPIC33/PIC24 Family Reference Manual"* for more information.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## 16.2 PWM Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 16.2.1 KEY RESOURCES

- **"High-Speed PWM"** (www.microchip.com/DS70645) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 16.3 PWMx Control Registers

**REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | HS/HC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTEN | — | PTSIDL | SESTAT | SEIEN | EIPU(1) | SYNCPOL(1) | SYNCOEN(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SYNCEN(1) | SYNCSRC2(1) | SYNCSRC1(1) | SYNCSRC0(1) | SEVTPS3(1) | SEVTPS2(1) | SEVTPS1(1) | SEVTPS0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PTEN:** PWMx Module Enable bit
1 = PWMx module is enabled
0 = PWMx module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTSIDL:** PWMx Time Base Stop in Idle Mode bit
1 = PWMx time base halts in CPU Idle mode
0 = PWMx time base runs in CPU Idle mode

bit 12 **SESTAT:** Special Event Interrupt Status bit
1 = Special event interrupt is pending
0 = Special event interrupt is not pending

bit 11 **SEIEN:** Special Event Interrupt Enable bit
1 = Special event interrupt is enabled
0 = Special event interrupt is disabled

bit 10 **EIPU:** Enable Immediate Period Updates bit(1)
1 = Active Period register is updated immediately
0 = Active Period register updates occur on PWMx cycle boundaries

bit 9 **SYNCPOL:** Synchronize Input and Output Polarity bit(1)
1 = SYNCI1/SYNCO1 polarity is inverted (active-low)
0 = SYNCI1/SYNCO1 is active-high

bit 8 **SYNCOEN:** Primary Time Base Sync Enable bit(1)
1 = SYNCO1 output is enabled
0 = SYNCO1 output is disabled

bit 7 **SYNCEN:** External Time Base Synchronization Enable bit(1)
1 = External synchronization of primary time base is enabled
0 = External synchronization of primary time base is disabled

**Note 1:** These bits should only be changed when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.

**2:** See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.


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**REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)**

bit 6-4 **SYNCSRC[2:0]:** Synchronous Source Selection bits(1)
111 = Reserved
•
•
•
100 = Reserved
011 = PTGO17(2)
010 = PTGO16(2)
001 = Reserved
000 = SYNCI1 input from PPS

bit 3-0 **SEVTPS[3:0]:** PWMx Special Event Trigger Output Postscaler Select bits(1)
1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event
•
•
•
0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event
0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

**Note 1:** These bits should only be changed when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the period register with a value that is slightly larger than the expected period of the external synchronization input signal.

**2:** See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.

**REGISTER 16-2: PTCON2: PWMx PRIMARY MASTER CLOCK DIVIDER SELECT REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | PCLKDIV[2:0](1) | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **PCLKDIV[2:0]:** PWMx Input Clock Prescaler (Divider) Select bits(1)

111 = Reserved
110 = Divide-by-64
101 = Divide-by-32
100 = Divide-by-16
011 = Divide-by-8
010 = Divide-by-4
001 = Divide-by-2
000 = Divide-by-1, maximum PWMx timing resolution (power-on default)

**Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.


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**REGISTER 16-3: PTPER: PWMx PRIMARY MASTER TIME BASE PERIOD REGISTER**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| PTPER[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTPER[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTPER[15:0]:** Primary Master Time Base (PMTMR) Period Value bits

**REGISTER 16-4: SEVTCMP: PWMx PRIMARY SPECIAL EVENT COMPARE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SEVTCMP[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SEVTCMP[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **SEVTCMP[15:0]:** Special Event Compare Count Value bits

**REGISTER 16-5: CHOP: PWMx CHOP CLOCK GENERATOR REGISTER**

| R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CHPCLKEN | — | — | — | — | — | CHOPCLK[9:8] | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CHOPCLK[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **CHPCLKEN:** Enable Chop Clock Generator bit
1 = Chop clock generator is enabled
0 = Chop clock generator is disabled

bit 14-10 **Unimplemented:** Read as ‘0’

bit 9-0 **CHOPCLK[9:0]:** Chop Clock Divider bits
The frequency of the chop clock signal is given by the following expression:
Chop Frequency = (FP/PCLKDIV[2:0])/(CHOPCLK[9:0] + 1)

**REGISTER 16-6: MDC: PWMx MASTER DUTY CYCLE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MDC[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| MDC[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **MDC[15:0]:** PWMx Master Duty Cycle Value bits


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**REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER**

| HS/HC-0 | HS/HC-0 | HS/HC-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTSTAT(1) | CLSTAT(1) | TRGSTAT(6) | FLTIEN | CLIEN | TRGIEN(6) | ITB(2) | MDCS(2) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DTC1 | DTC0 | DTCP(3) | — | MTBS | CAM(2,4) | XPRES(5) | IUE(2) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | HS = Hardware Settable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = No Fault interrupt is pending
This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = No current-limit interrupt is pending
This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit(6)
1 = Trigger interrupt is pending
0 = No trigger interrupt is pending
This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled and the FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt is enabled
0 = Current-limit interrupt is disabled and the CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit(6)
1 = A trigger event generates an interrupt request
0 = Trigger event interrupts are disabled and the TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(2)
1 = PHASEx register provides time base period for this PWM generator
0 = PTPER register provides timing for this PWM generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(2)
1 = MDC register provides duty cycle information for this PWM generator
0 = PDCx register provides duty cycle information for this PWM generator

**Note 1:** Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
**2:** These bits should not be changed after the PWMx is enabled (PTEN = 1).
**3:** DTC[1:0] = 11 for DTCP to be effective; otherwise, DTCP is ignored.
**4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
**5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.
**6:** When the local time base counter matches the value specified by the user in the TRIGx register, an ADC trigger signal is generated. Also, see the TRIGx register description.

**REGISTER 16-7: PWMCONx: PWMx CONTROL REGISTER (CONTINUED)**

bit 7-6 **DTC[1:0]:** Dead-Time Control bits
11 = Dead-Time Compensation mode
10 = Dead-time function is disabled
01 = Negative dead time is actively applied for Complementary Output mode
00 = Positive dead time is actively applied except for Push-Pull mode

bit 5 **DTCP:** Dead-Time Compensation Polarity bit(3)
When Set to '1':
If DTCMPx = 0, PWMxL is shortened and PWMxH is lengthened.
If DTCMPx = 1, PWMxH is shortened and PWMxL is lengthened.
When Set to '0':
If DTCMPx = 0, PWMxH is shortened and PWMxL is lengthened.
If DTCMPx = 1, PWMxL is shortened and PWMxH is lengthened.

bit 4 **Unimplemented:** Read as '0'

bit 3 **MTBS:** Master Time Base Select bit
1 = PWM generator uses the secondary master time base for synchronization and as the clock source for the PWM generation logic (if secondary time base is available)
0 = PWM generator uses the primary master time base for synchronization and as the clock source for the PWM generation logic

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,4)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled

bit 1 **XPRES:** External PWMx Reset Control bit(5)
1 = Current-limit source resets the time base for this PWM generator if it is in Independent Time Base mode
0 = External pins do not affect PWMx time base

bit 0 **IUE:** Immediate Update Enable bit(2)
1 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are immediate
0 = Updates to the active MDC/PDCx/DTRx/ALTDTRx/PHASEx registers are synchronized to the PWMx period boundary

**Note 1:** Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
**2:** These bits should not be changed after the PWMx is enabled (PTEN = 1).
**3:** DTC[1:0] = 11 for DTCP to be effective; otherwise, DTCP is ignored.
**4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
**5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.
**6:** When the local time base counter matches the value specified by the user in the TRIGx register, an ADC trigger signal is generated. Also, see the TRIGx register description.


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**REGISTER 16-8: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PDCx[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PDCx[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **PDCx[15:0]:** PWMx Generator # Duty Cycle Value bits

**REGISTER 16-9: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PHASEx[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PHASEx[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **PHASEx[15:0]:** PWMx Phase-Shift Value or Independent Time Base Period for the PWM Generator bits

**Note 1:** If ITB (PWMCONx[9]) = 0, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output mode (PMOD[1:0] (IOCON[11:10]) = 00, 01 or 10),
PHASEx[15:0] = Phase-shift value for PWMxH and PWMxL outputs

**2:** If ITB (PWMCONx[9]) = 1, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output mode (PMOD[1:0] (IOCONx[11:10]) = 00, 01 or 10),
PHASEx[15:0] = Independent time base period value for PWMxH and PWMxL

**REGISTER 16-10: DTRx: PWMx DEAD-TIME REGISTER**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | DTRx[13:8] | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| DTRx[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **DTRx[13:0]:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits

**REGISTER 16-11: ALTDTRx: PWMx ALTERNATE DEAD-TIME REGISTER**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | ALTDTRx[13:8] | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ALTDTRx[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **ALTDTRx[13:0]:** Unsigned 14-Bit Dead-Time Value for PWMx Dead-Time Unit bits


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**REGISTER 16-12: TRGCONx: PWMx TRIGGER CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TRGDIV[3:0] | | | | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | TRGSTRT[5:0](1) | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **TRGDIV[3:0]:** Trigger # Output Divider bits

1111 = Trigger output for every 16th trigger event
1110 = Trigger output for every 15th trigger event
1101 = Trigger output for every 14th trigger event
1100 = Trigger output for every 13th trigger event
1011 = Trigger output for every 12th trigger event
1010 = Trigger output for every 11th trigger event
1001 = Trigger output for every 10th trigger event
1000 = Trigger output for every 9th trigger event
0111 = Trigger output for every 8th trigger event
0110 = Trigger output for every 7th trigger event
0101 = Trigger output for every 6th trigger event
0100 = Trigger output for every 5th trigger event
0011 = Trigger output for every 4th trigger event
0010 = Trigger output for every 3rd trigger event
0001 = Trigger output for every 2nd trigger event
0000 = Trigger output for every trigger event

bit 11-6 **Unimplemented:** Read as '0'

bit 5-0 **TRGSTRT[5:0]:** Trigger Postscaler Start Enable Select bits(1)

111111 = Waits 63 PWM cycles before generating the first trigger event after the module is enabled
•
•
•
000010 = Waits 2 PWM cycles before generating the first trigger event after the module is enabled
000001 = Waits 1 PWM cycle before generating the first trigger event after the module is enabled
000000 = Waits 0 PWM cycles before generating the first trigger event after the module is enabled

**Note 1:** The secondary PWM generator cannot generate PWMx trigger interrupts.

**REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER(2,3)**

| R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PENH | PENL | POLH | POLL | PMOD1(1) | PMOD0(1) | OVRENH | OVRENL |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OVRDAT1 | OVRDAT0 | FLTDAT1 | FLTDAT0 | CLDAT1 | CLDAT0 | SWAP | OSYNC |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PENH:** PWMxH Output Pin Ownership bit
1 = PWMx module controls PWMxH pin
0 = GPIO module controls PWMxH pin

bit 14 **PENL:** PWMxL Output Pin Ownership bit
1 = PWMx module controls PWMxL pin
0 = GPIO module controls PWMxL pin

bit 13 **POLH:** PWMxH Output Pin Polarity bit
1 = PWMxH pin is active-low
0 = PWMxH pin is active-high

bit 12 **POLL:** PWMxL Output Pin Polarity bit
1 = PWMxL pin is active-low
0 = PWMxL pin is active-high

bit 11-10 **PMOD[1:0]:** PWMx # I/O Pin Mode bits(1)
11 = Reserved; do not use
10 = PWMx I/O pin pair is in the Push-Pull Output mode
01 = PWMx I/O pin pair is in the Redundant Output mode
00 = PWMx I/O pin pair is in the Complementary Output mode

bit 9 **OVRENH:** Override Enable for PWMxH Pin bit
1 = OVRDAT[1] controls output on PWMxH pin
0 = PWMx generator controls PWMxH pin

bit 8 **OVRENL:** Override Enable for PWMxL Pin bit
1 = OVRDAT[0] controls output on PWMxL pin
0 = PWMx generator controls PWMxL pin

bit 7-6 **OVRDAT[1:0]:** Data for PWMxH, PWMxL Pins if Override is Enabled bits
If OVERENH = 1, PWMxH is driven to the state specified by OVRDAT[1].
If OVERENL = 1, PWMxL is driven to the state specified by OVRDAT[0].

bit 5-4 **FLTDAT[1:0]:** Data for PWMxH and PWMxL Pins if FLTMOD is Enabled bits
If Fault is active, PWMxH is driven to the state specified by FLTDAT[1].
If Fault is active, PWMxL is driven to the state specified by FLTDAT[0].

bit 3-2 **CLDAT[1:0]:** Data for PWMxH and PWMxL Pins if CLMOD is Enabled bits
If current-limit is active, PWMxH is driven to the state specified by CLDAT[1].
If current-limit is active, PWMxL is driven to the state specified by CLDAT[0].

**Note 1:** These bits should not be changed after the PWMx module is enabled (PTEN = 1).

**2:** If the PWMLOCK Configuration bit (FOSCSEL[6]) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

**3:** The OSYNC bit (IOCON[0]) must be set to '1' prior to changing the state of the SWAP bit (IOCON[1]), else the SWAP function will attempt to occur in the middle of the PWM cycle and unpredictable results may occur.


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**REGISTER 16-13: IOCONx: PWMx I/O CONTROL REGISTER(2,3) (CONTINUED)**

bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
1 = PWMxH output signal is connected to PWMxL pins; PWMxL output signal is connected to PWMxH pins
0 = PWMxH and PWMxL pins are mapped to their respective pins

bit 0 **OSYNC:** Output Override Synchronization bit
1 = Output overrides via the OVRDAT[1:0] bits are synchronized to the PWMx time base. In Edge-Aligned mode, output overrides are updated when the local time base equals zero. In Center-Aligned mode, output overrides are updated when the local time base matches the PHASEx register.
0 = Output overrides via the OVDDAT[1:0] bits occur on the next CPU clock boundary

**Note 1:** These bits should not be changed after the PWMx module is enabled (PTEN = 1).

**2:** If the PWMLOCK Configuration bit (FOSCSEL[6]) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

**3:** The OSYNC bit (IOCON[0]) must be set to '1' prior to changing the state of the SWAP bit (IOCON[1]), else the SWAP function will attempt to occur in the middle of the PWM cycle and unpredictable results may occur.

**REGISTER 16-14: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRGCMP[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRGCMP[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **TRGCMP[15:0]:** Trigger Control Value bits

When the primary PWMx functions in local time base, this register contains the compare values that can trigger the ADC module.


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**REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER(1)**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL(2) | CLMOD |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRC0 | FLTPOL(2) | FLTMOD1 | FLTMOD0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-10 **CLSRC[4:0]:** Current-Limit Control Signal Source Select for PWM Generator # bits
11111 = Fault 32
11110 = Reserved
•
•
•
01100 = Reserved
01011 = Comparator 4
01010 = Op Amp/Comparator 3
01001 = Op Amp/Comparator 2
01000 = Op Amp/Comparator 1
00111 = Reserved
00110 = Reserved
00101 = Reserved
00100 = Reserved
00011 = Fault 4
00010 = Fault 3
00001 = Fault 2
00000 = Fault 1 **(default)**

bit 9 **CLPOL:** Current-Limit Polarity for PWM Generator # bit(2)
1 = The selected current-limit source is active-low
0 = The selected current-limit source is active-high

bit 8 **CLMOD:** Current-Limit Mode Enable for PWM Generator # bit
1 = Current-Limit mode is enabled
0 = Current-Limit mode is disabled

**Note 1:** If the PWMLOCK Configuration bit (FOSCSEL[6]) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

**2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

**REGISTER 16-15: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER(1)**

bit 7-3 **FLTSRC[4:0]:** Fault Control Signal Source Select for PWM Generator # bits
11111 = Fault 32 **(default)**
11110 = Reserved
•
•
•
01100 = Reserved
01011 = Comparator 4
01010 = Op Amp/Comparator 3
01001 = Op Amp/Comparator 2
01000 = Op Amp/Comparator 1
00111 = Reserved
00110 = Reserved
00101 = Reserved
00100 = Reserved
00011 = Fault 4
00010 = Fault 3
00001 = Fault 2
00000 = Fault 1

bit 2 **FLTPOL:** Fault Polarity for PWM Generator # bit(2)
1 = The selected Fault source is active-low
0 = The selected Fault source is active-high

bit 1-0 **FLTMOD[1:0]:** Fault Mode for PWM Generator # bits
11 = Fault input is disabled
10 = Reserved
01 = The selected Fault source forces PWMxH, PWMxL pins to FLTDATx values (cycle)
00 = The selected Fault source forces PWMxH, PWMxL pins to FLTDATx values (latched condition)

**Note 1:** If the PWMLOCK Configuration bit (FOSCSEL[6]) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

**2:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.


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**REGISTER 16-16: LEBCONx: PWMx LEADING-EDGE BLANKING CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| PHR | PHF | PLR | PLF | FLTLEBEN | CLLEBEN | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | BCH(1) | BCL(1) | BPHH | BPHL | BPLH | BPLL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores rising edge of PWMxH

bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores falling edge of PWMxH

bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores rising edge of PWMxL

bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores falling edge of PWMxL

bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected Fault input
0 = Leading-Edge Blanking is not applied to selected Fault input

bit 10 **CLLEBEN:** Current-Limit Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to selected current-limit input
0 = Leading-Edge Blanking is not applied to selected current-limit input

bit 9-6 **Unimplemented:** Read as '0'

bit 5 **BCH:** Blanking in Selected Blanking Signal High Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high
0 = No blanking when selected blanking signal is high

bit 4 **BCL:** Blanking in Selected Blanking Signal Low Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low
0 = No blanking when selected blanking signal is low

bit 3 **BPHH:** Blanking in PWMxH High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high
0 = No blanking when PWMxH output is high

bit 2 **BPHL:** Blanking in PWMxH Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low
0 = No blanking when PWMxH output is low

bit 1 **BPLH:** Blanking in PWMxL High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high
0 = No blanking when PWMxL output is high

bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low
0 = No blanking when PWMxL output is low

**Note 1:** The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

**REGISTER 16-17: LEBDLYx: PWMx LEADING-EDGE BLANKING DELAY REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | LEB[11:8] | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| LEB[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **LEB[11:0]:** Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits


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**REGISTER 16-18: AUXCONx: PWMx AUXILIARY CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | BLANKSEL[3:0] | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSEL0 | CHOPHEN | CHOPLEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **BLANKSEL[3:0]:** PWMx State Blank Source Select bits

The selected state blank signal will block the current-limit and/or Fault input signals (if enabled via the BCH and BCL bits in the LEBCONx register).

1001 = Reserved
•
•
•
0100 = Reserved
0011 = PWM3H selected as state blank source
0010 = PWM2H selected as state blank source
0001 = PWM1H selected as state blank source
0000 = No state blanking

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHOPSEL[3:0]:** PWMx Chop Clock Source Select bits

The selected signal will enable and disable (CHOP) the selected PWMx outputs.

1001 = Reserved
•
•
•
0100 = Reserved
0011 = PWM3H selected as CHOP clock source
0010 = PWM2H selected as CHOP clock source
0001 = PWM1H selected as CHOP clock source
0000 = Chop clock generator selected as CHOP clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit

1 = PWMxH chopping function is enabled
0 = PWMxH chopping function is disabled

bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit

1 = PWMxL chopping function is enabled
0 = PWMxL chopping function is disabled

**NOTES:**


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# 17.0 QUADRATURE ENCODER INTERFACE (QEI) MODULE (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Quadrature Encoder Interface (QEI)"** (www.microchip.com/DS70000601) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

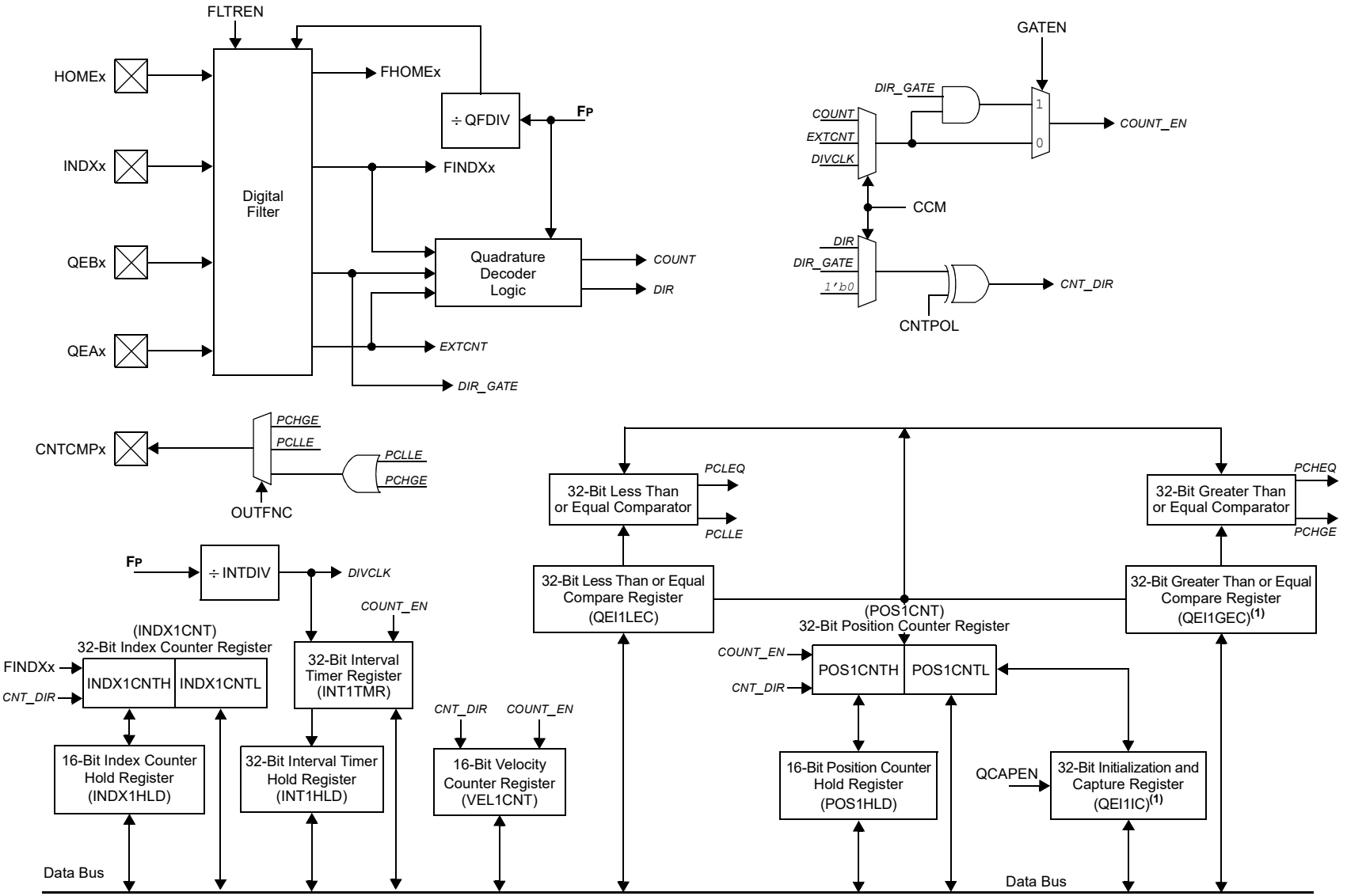
This chapter describes the Quadrature Encoder Interface (QEI) module and associated operational modes. The QEI module provides the interface to incremental encoders for obtaining mechanical position data.

The operational features of the QEI module include:

- 32-Bit Position Counter
- 32-Bit Index Pulse Counter
- 32-Bit Interval Timer
- 16-Bit Velocity Counter
- 32-Bit Position Initialization/Capture/Compare High register
- 32-Bit Position Compare Low register
- x4 Quadrature Count mode
- External Up/Down Count mode
- External Gated Count mode
- External Gated Timer mode
- Internal Timer mode

Figure 17-1 illustrates the QEI block diagram.

**FIGURE 17-1: QEI BLOCK DIAGRAM**




**Note 1:** These registers map to the same memory location.



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## 17.1 QEI Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 17.1.1 KEY RESOURCES

- **"Quadrature Encoder Interface"** (www.microchip.com/DS70000601) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 17.2 QEI Control Registers

**REGISTER 17-1: QEI1CON: QEI1 CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIEN | — | QEISIDL | PIMOD2(1) | PIMOD1(1) | PIMOD0(1) | IMV1(2) | IMV0(2) |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | INTDIV2(3) | INTDIV1(3) | INTDIV0(3) | CNTPOL | GATEN | CCM1 | CCM0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **QEIEN:** Quadrature Encoder Interface Module Counter Enable bit
1 = Module counters are enabled
0 = Module counters are disabled, but SFRs can be read or written to

bit 14 **Unimplemented:** Read as '0'

bit 13 **QEISIDL:** QEI Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **PIMOD[2:0]:** Position Counter Initialization Mode Select bits(1)
111 = Reserved
110 = Modulo Count mode for position counter
101 = Resets the position counter when the position counter equals QEI1GEC register
100 = Second index event after home event initializes position counter with contents of QEI1IC register
011 = First index event after home event initializes position counter with contents of QEI1IC register
010 = Next index input event initializes the position counter with contents of QEI1IC register
001 = Every index input event resets the position counter
000 = Index input event does not affect position counter

bit 9 **IMV1:** Index Match Value for Phase B bit(2)
1 = Phase B match occurs when QEB = 1
0 = Phase B match occurs when QEB = 0

bit 8 **IMV0:** Index Match Value for Phase A bit(2)
1 = Phase A match occurs when QEA = 1
0 = Phase A match occurs when QEA = 0

bit 7 **Unimplemented:** Read as '0'

**Note 1:** When CCM[1:0] = 10 or 11, all of the QEI counters operate as timers and the PIMOD[2:0] bits are ignored.
**2:** When CCM[1:0] = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.
**3:** The selected clock rate should be at least twice the expected maximum quadrature count rate.


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**REGISTER 17-1: QEI1CON: QEI1 CONTROL REGISTER (CONTINUED)**

bit 6-4 **INTDIV[2:0]:** Timer Input Clock Prescale Select bits (interval timer, main timer (position counter), velocity counter and index counter internal clock divider select)(3)

111 = 1:128 prescale value
110 = 1:64 prescale value
101 = 1:32 prescale value
100 = 1:16 prescale value
011 = 1:8 prescale value
010 = 1:4 prescale value
001 = 1:2 prescale value
000 = 1:1 prescale value

bit 3 **CNTPOL:** Position and Index Counter/Timer Direction Select bit

1 = Counter direction is negative unless modified by external up/down signal
0 = Counter direction is positive unless modified by external up/down signal

bit 2 **GATEN:** External Count Gate Enable bit

1 = External gate signal controls position counter operation
0 = External gate signal does not affect position counter/timer operation

bit 1-0 **CCM[1:0]:** Counter Control Mode Selection bits

11 = Internal Timer mode with optional external count is selected
10 = External clock count with optional external count is selected
01 = External clock count with external up/down direction is selected
00 = Quadrature Encoder Interface (x4 mode) Count mode is selected

**Note 1:** When CCM[1:0] = 10 or 11, all of the QEI counters operate as timers and the PIMOD[2:0] bits are ignored.

**2:** When CCM[1:0] = 00, and QEA and QEB values match the Index Match Value (IMV), the POSCNTH and POSCNTL registers are reset. QEA/QEB signals used for the index match have swap and polarity values applied, as determined by the SWPAB and QEAPOL/QEBPOL bits.

**3:** The selected clock rate should be at least twice the expected maximum quadrature count rate.

**REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QCAPEN | FLTREN | QFDIV2 | QFDIV1 | QFDIV0 | OUTFNC1 | OUTFNC0 | SWPAB |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R-x | R-x | R-x | R-x |
|---|---|---|---|---|---|---|---|
| HOMPOL | IDXPOL | QEBPOL | QEAPOL | HOME | INDEX | QEB | QEA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **QCAPEN:** QEI Position Counter Input Capture Enable bit
1 = Index match event triggers a position capture event
0 = Index match event does not trigger a position capture event

bit 14 **FLTREN:** QEAx/QEBx/INDXx/HOMEx Digital Filter Enable bit
1 = Input pin digital filter is enabled
0 = Input pin digital filter is disabled (bypassed)

bit 13-11 **QFDIV[2:0]:** QEAx/QEBx/INDXx/HOMEx Digital Input Filter Clock Divide Select bits
111 = 1:128 clock divide
110 = 1:64 clock divide
101 = 1:32 clock divide
100 = 1:16 clock divide
011 = 1:8 clock divide
010 = 1:4 clock divide
001 = 1:2 clock divide
000 = 1:1 clock divide

bit 10-9 **OUTFNC[1:0]:** QEI Module Output Function Mode Select bits
11 = The CTNCMPx pin goes high when QEI1LEC ≥ POS1CNT ≥ QEI1GEC
10 = The CTNCMPx pin goes high when POS1CNT ≤ QEI1LEC
01 = The CTNCMPx pin goes high when POS1CNT ≥ QEI1GEC
00 = Output is disabled

bit 8 **SWPAB:** Swap QEA and QEB Inputs bit
1 = QEAx and QEBx are swapped prior to quadrature decoder logic
0 = QEAx and QEBx are not swapped

bit 7 **HOMPOL:** HOMEx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 6 **IDXPOL:** INDXx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 5 **QEBPOL:** QEBx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 4 **QEAPOL:** QEAx Input Polarity Select bit
1 = Input is inverted
0 = Input is not inverted

bit 3 **HOME:** Status of HOMEx Input Pin After Polarity Control bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'


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**REGISTER 17-2: QEI1IOC: QEI1 I/O CONTROL REGISTER (CONTINUED)**

bit 2 **INDEX:** Status of INDXx Input Pin After Polarity Control bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 1 **QEB:** Status of QEBx Input Pin After Polarity Control And SWPAB Pin Swapping bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control And SWPAB Pin Swapping bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

**REGISTER 17-3: QEI1STAT: QEI1 STATUS REGISTER**

| U-0 | U-0 | HS/R/C-0 | R/W-0 | HS/R/C-0 | R/W-0 | HS/R/C-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | PCHEQIRQ | PCHEQIEN | PCLEQIRQ | PCLEQIEN | POSOVIRQ | POSOVIEN |
| bit 15 | | | | | | | bit 8 |

| HS/R/C-0 | R/W-0 | HS/R/C-0 | R/W-0 | HS/R/C-0 | R/W-0 | HS/R/C-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PCIIRQ(1) | PCIIEN | VELOVIRQ | VELOVIEN | HOMIRQ | HOMIEN | IDXIRQ | IDXIEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | C = Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **PCHEQIRQ:** Position Counter Greater Than or Equal Compare Status bit
1 = POS1CNT ≥ QEI1GEC
0 = POS1CNT < QEI1GEC

bit 12 **PCHEQIEN:** Position Counter Greater Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 11 **PCLEQIRQ:** Position Counter Less Than or Equal Compare Status bit
1 = POS1CNT ≤ QEI1LEC
0 = POS1CNT > QEI1LEC

bit 10 **PCLEQIEN:** Position Counter Less Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 9 **POSOVIRQ:** Position Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred

bit 8 **POSOVIEN:** Position Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 7 **PCIIRQ:** Position Counter (Homing) Initialization Process Complete Status bit(1)
1 = POS1CNT was reinitialized
0 = POS1CNT was not reinitialized

bit 6 **PCIIEN:** Position Counter (Homing) Initialization Process Complete interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **VELOVIRQ:** Velocity Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has not occurred

bit 4 **VELOVIEN:** Velocity Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **HOMIRQ:** Status Flag for Home Event Status bit
1 = Home event has occurred
0 = No Home event has occurred

**Note 1:** This status bit is only applicable to PIMOD[2:0] modes, '011' and '100'.


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**REGISTER 17-3: QEI1STAT: QEI1 STATUS REGISTER (CONTINUED)**

bit 2 **HOMIEN:** Home Input Event Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 1 **IDXIRQ:** Status Flag for Index Event Status bit
1 = Index event has occurred
0 = No Index event has occurred

bit 0 **IDXIEN:** Index Input Event Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

**Note 1:** This status bit is only applicable to PIMOD[2:0] modes, '011' and '100'.

**REGISTER 17-4: POS1CNTH: POSITION COUNTER 1 HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSCNT[31:24] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSCNT[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **POSCNT[31:16]:** High Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

**REGISTER 17-5: POS1CNTL: POSITION COUNTER 1 LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSCNT[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSCNT[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **POSCNT[15:0]:** Low Word Used to Form 32-Bit Position Counter Register (POS1CNT) bits

**REGISTER 17-6: POS1HLD: POSITION COUNTER 1 HOLD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSHLD[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| POSHLD[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **POSHLD[15:0]:** Hold Register for Reading and Writing POS1CNTH bits


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**REGISTER 17-7: VEL1CNT: VELOCITY COUNTER 1 REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| VELCNT[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| VELCNT[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **VELCNT[15:0]:** Velocity Counter bits

**REGISTER 17-8: INDX1CNTH: INDEX COUNTER 1 HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXCNT[31:24] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXCNT[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **INDXCNT[31:16]:** High Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits

**REGISTER 17-9: INDX1CNTL: INDEX COUNTER 1 LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXCNT[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXCNT[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **INDXCNT[15:0]:** Low Word Used to Form 32-Bit Index Counter Register (INDX1CNT) bits

**REGISTER 17-10: INDX1HLD: INDEX COUNTER 1 HOLD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXHLD[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INDXHLD[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **INDXHLD[15:0]:** Hold Register for Reading and Writing INDX1CNTH bits

**REGISTER 17-11: QEI1ICH: QEI1 INITIALIZATION/CAPTURE HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIIC[31:24] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIIC[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEIIC[31:16]:** High Word Used to Form 32-Bit Initialization/Capture Register (QEI1IC) bits

**REGISTER 17-12: QEI1ICL: QEI1 INITIALIZATION/CAPTURE LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIIC[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIIC[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEIIC[15:0]:** Low Word Used to Form 32-Bit Initialization/Capture Register (QEI1IC) bits


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**REGISTER 17-13: QEI1LECH: QEI1 LESS THAN OR EQUAL COMPARE HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEILEC[31:24] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEILEC[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEILEC[31:16]:** High Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

**REGISTER 17-14: QEI1LECL: QEI1 LESS THAN OR EQUAL COMPARE LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEILEC[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEILEC[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEILEC[15:0]:** Low Word Used to Form 32-Bit Less Than or Equal Compare Register (QEI1LEC) bits

**REGISTER 17-15: QEI1GECH: QEI1 GREATER THAN OR EQUAL COMPARE HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC[31:24] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEIGEC[31:16]:** High Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits

**REGISTER 17-16: QEI1GECL: QEI1 GREATER THAN OR EQUAL COMPARE LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| QEIGEC[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **QEIGEC[15:0]:** Low Word Used to Form 32-Bit Greater Than or Equal Compare Register (QEI1GEC) bits


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**REGISTER 17-17: INT1TMRH: INTERVAL 1 TIMER HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTTMR[31:24] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTTMR[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **INTTMR[31:16]:** High Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

**REGISTER 17-18: INT1TMRL: INTERVAL 1 TIMER LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTTMR[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTTMR[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **INTTMR[15:0]:** Low Word Used to Form 32-Bit Interval Timer Register (INT1TMR) bits

**REGISTER 17-19: INT1HLDH: INTERVAL 1 TIMER HOLD HIGH WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTHLD[31:24] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTHLD[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **INTHLD[31:16]:** Hold Register for Reading and Writing INT1TMRH bits

**REGISTER 17-20: INT1HLDL: INTERVAL 1 TIMER HOLD LOW WORD REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTHLD[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| INTHLD[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **INTHLD[15:0]:** Hold Register for Reading and Writing INT1TMRL bits


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## 18.0 SERIAL PERIPHERAL INTERFACE (SPI)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Serial Peripheral Interface (SPI)"** (www.microchip.com/DS70005185) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, ADC Converters, etc. The SPI module is compatible with Motorola® SPI and SIOP interfaces.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device family offers two SPI modules on a single device. These modules, which are designated as SPI1 and SPI2, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

**Note:** In this section, the SPI modules are referred to together as SPIx, or separately as SPI1 and SPI2. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1 and SPI2 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 module takes advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of the SPI2 module, but results in a lower maximum speed for SPI2. See **Section 30.0 "Electrical Characteristics"** for more information.

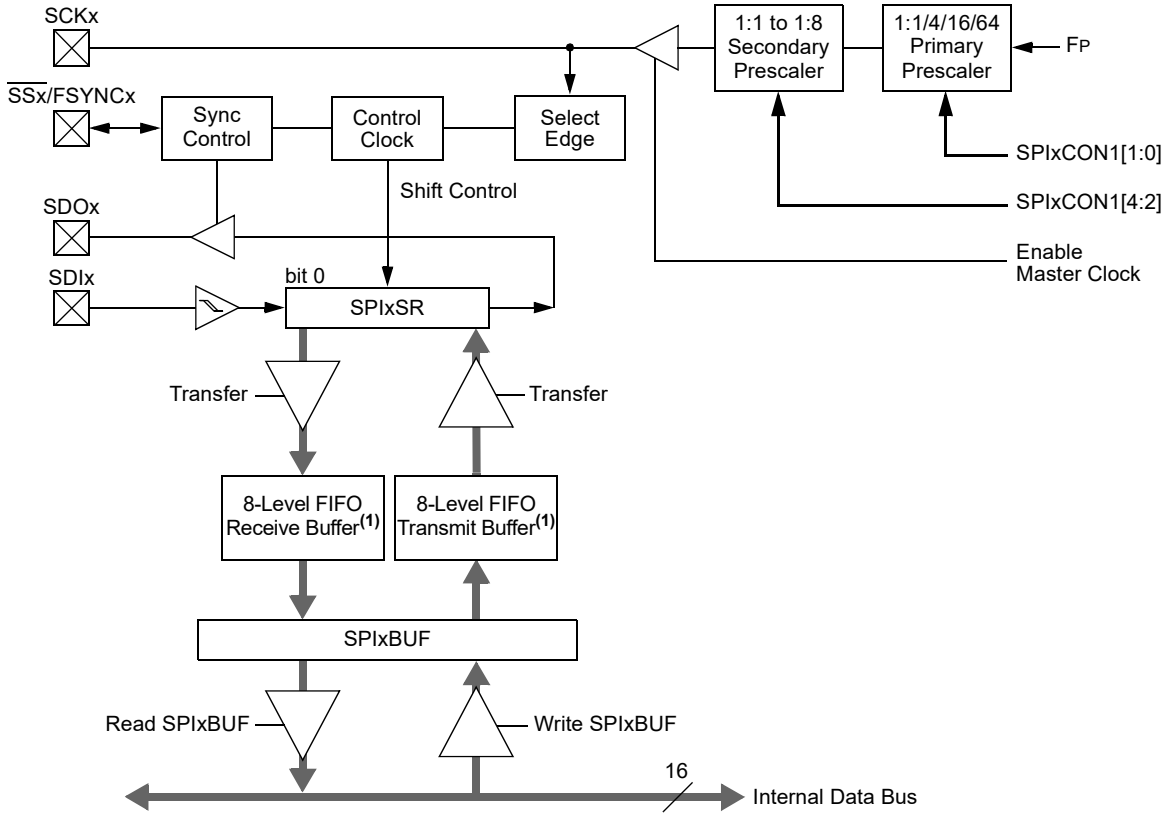
The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- $\overline{SS}$x/FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, $\overline{SS}$x is not used. In 2-pin mode, neither SDOx nor $\overline{SS}$x is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

**FIGURE 18-1: SPIx MODULE BLOCK DIAGRAM**




**Note 1:** In Standard mode, the FIFO is only one level deep.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## 18.1 SPI Helpful Tips

1. In Frame mode, if there is a possibility that the master may not be initialized before the slave:
   a) If FRMPOL (SPIxCON2[13]) = 1, use a pull-down resistor on SSx.
   b) If FRMPOL = 0, use a pull-up resistor on SSx.

| **Note:** | This insures that the first frame transmission after initialization is not shifted or corrupted. |
|---|---|

2. In Non-Framed Three-Wire mode, (i.e., not using SSx from a master):
   a) If CKP (SPIxCON1[6]) = 1, always place a pull-up resistor on SSx.
   b) If CKP = 0, always place a pull-down resistor on SSx.

| **Note:** | This will insure that during power-up and initialization the master/slave will not lose Sync due to an errant SCKx transition that would cause the slave to accumulate data shift errors for both transmit and receive appearing as corrupted data. |
|---|---|

3. FRMEN (SPIxCON2[15]) = 1 and SSEN (SPIxCON1[7]) = 1 are exclusive and invalid. In Frame mode, SCKx is continuous and the Frame Sync pulse is active on the SSx pin, which indicates the start of a data frame.

| **Note:** | Not all third-party devices support Frame mode timing. Refer to the SPIx specifications in **Section 30.0 "Electrical Characteristics"** for details. |
|---|---|

4. In Master mode only, set the SMP bit (SPIxCON1[9]) to a '1' for the fastest SPIx data rate possible. The SMP bit can only be set at the same time or after the MSTEN bit (SPIxCON1[5]) is set.

To avoid invalid slave read data to the master, the user's master software must ensure enough time for slave software to fill its write buffer before the user application initiates a master write/read cycle. It is always advisable to preload the SPIxBUF Transmit register in advance of the next master transaction cycle. SPIxBUF is transferred to the SPIx Shift register and is empty once the data transmission begins.

## 18.2 SPI Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |
|---|---|

### 18.2.1 KEY RESOURCES

- **"Serial Peripheral Interface (SPI)"** (www.microchip.com/DS70005185) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 18.3 SPIx Control Registers

**REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SPIEN | — | SPISIDL | — | — | SPIBEC2 | SPIBEC1 | SPIBEC0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | HS/R/C-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | HS/HC/R-0 | HS/HC/R-0 |
|---|---|---|---|---|---|---|---|
| SRMPT | SPIROV | SRXMPT | SISEL2 | SISEL1 | SISEL0 | SPITBF | SPIRBF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | HS = Hardware Settable bit | HC = Hardware Clearable bit |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **SPIEN:** SPIx Enable bit
1 = Enables the module and configures SCKx, SDOx, SDIx and $\overline{SSx}$ as serial port pins
0 = Disables the module

bit 14 **Unimplemented:** Read as '0'

bit 13 **SPISIDL:** SPIx Stop in Idle Mode bit
1 = Discontinues the module operation when device enters Idle mode
0 = Continues the module operation in Idle mode

bit 12-11 **Unimplemented:** Read as '0'

bit 10-8 **SPIBEC[2:0]:** SPIx Buffer Element Count bits (valid in Enhanced Buffer mode)
Master mode:
Number of SPIx transfers that are pending.
Slave mode:
Number of SPIx transfers that are unread.

bit 7 **SRMPT:** SPIx Shift Register (SPIxSR) Empty bit (valid in Enhanced Buffer mode)
1 = SPIx Shift register is empty and Ready-to-Send or receive the data
0 = SPIx Shift register is not empty

bit 6 **SPIROV:** SPIx Receive Overflow Flag bit
1 = A new byte/word is completely received and discarded; the user application has not read the previous data in the SPIxBUF register
0 = No overflow has occurred

bit 5 **SRXMPT:** SPIx Receive FIFO Empty bit (valid in Enhanced Buffer mode)
1 = RX FIFO is empty
0 = RX FIFO is not empty

bit 4-2 **SISEL[2:0]:** SPIx Buffer Interrupt Mode bits (valid in Enhanced Buffer mode)
111 = Interrupt when the SPIx transmit buffer is full (SPITBF bit is set)
110 = Interrupt when last bit is shifted into SPIxSR and as a result, the TX FIFO is empty
101 = Interrupt when the last bit is shifted out of SPIxSR and the transmit is complete
100 = Interrupt when one data are shifted into the SPIxSR and as a result, the TX FIFO has one open memory location
011 = Interrupt when the SPIx receive buffer is full (SPIRBF bit is set)
010 = Interrupt when the SPIx receive buffer is 3/4 or more full
001 = Interrupt when data are available in the receive buffer (SRMPT bit is set)
000 = Interrupt when the last data in the receive buffer are read and as a result, the buffer is empty (SRXMPT bit is set)


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**REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit

1 = Transmit not yet started, SPIxTXB is full
0 = Transmit started, SPIxTXB is empty

Standard Buffer mode:
Automatically set in hardware when core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when SPIx module transfers data from SPIxTXB to SPIxSR.

Enhanced Buffer mode:
Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit

1 = Receive is complete, SPIxRXB is full
0 = Receive is incomplete, SPIxRXB is empty

Standard Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.

Enhanced Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

**REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DISSCK | DISSDO | MODE16 | SMP | CKE(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SSEN(2) | CKP | MSTEN | SPRE2(3) | SPRE1(3) | SPRE0(3) | PPRE1(3) | PPRE0(3) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **DISSCK:** Disable SCKx Pin bit (SPIx Master modes only)
1 = Internal SPIx clock is disabled, pin functions as I/O
0 = Internal SPIx clock is enabled

bit 11 **DISSDO:** Disable SDOx Pin bit
1 = SDOx pin is not used by the module; pin functions as I/O
0 = SDOx pin is controlled by the module

bit 10 **MODE16:** Word/Byte Communication Select bit
1 = Communication is word-wide (16 bits)
0 = Communication is byte-wide (8 bits)

bit 9 **SMP:** SPIx Data Input Sample Phase bit
Master mode:
1 = Input data are sampled at end of data output time
0 = Input data are sampled at middle of data output time
Slave mode:
SMP must be cleared when SPIx is used in Slave mode.

bit 8 **CKE:** SPIx Clock Edge Select bit(1)
1 = Serial output data change on transition from Active Clock state to Idle Clock state (refer to bit 6)
0 = Serial output data change on transition from Idle Clock state to Active Clock state (refer to bit 6)

bit 7 **SSEN:** Slave Select Enable bit (Slave mode)(2)
1 = $\overline{SSx}$ pin is used for Slave mode
0 = $\overline{SSx}$ pin is not used by the module; pin is controlled by port function

bit 6 **CKP:** Clock Polarity Select bit
1 = Idle state for clock is a high level; active state is a low level
0 = Idle state for clock is a low level; active state is a high level

bit 5 **MSTEN:** Master Mode Enable bit
1 = Master mode
0 = Slave mode

**Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
**2:** This bit must be cleared when FRMEN = 1.
**3:** Do not set both primary and secondary prescalers to the value of 1:1.


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**REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)**

bit 4-2 **SPRE[2:0]:** Secondary Prescale bits (Master mode)(3)
111 = Secondary prescale 1:1
110 = Secondary prescale 2:1
•
•
•
000 = Secondary prescale 8:1

bit 1-0 **PPRE[1:0]:** Primary Prescale bits (Master mode)(3)
11 = Primary prescale 1:1
10 = Primary prescale 4:1
01 = Primary prescale 16:1
00 = Primary prescale 64:1

**Note 1:** The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
**2:** This bit must be cleared when FRMEN = 1.
**3:** Do not set both primary and secondary prescalers to the value of 1:1.

**REGISTER 18-3: SPIxCON2: SPIx CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| FRMEN | SPIFSD | FRMPOL | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | FRMDLY | SPIBEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FRMEN:** Framed SPIx Support bit
1 = Framed SPIx support is enabled ($\overline{SS}$x pin is used as Frame Sync pulse input/output)
0 = Framed SPIx support is disabled

bit 14 **SPIFSD:** Frame Sync Pulse Direction Control bit
1 = Frame Sync pulse input (slave)
0 = Frame Sync pulse output (master)

bit 13 **FRMPOL:** Frame Sync Pulse Polarity bit
1 = Frame Sync pulse is active-high
0 = Frame Sync pulse is active-low

bit 12-2 **Unimplemented:** Read as '0'

bit 1 **FRMDLY:** Frame Sync Pulse Edge Select bit
1 = Frame Sync pulse coincides with first bit clock
0 = Frame Sync pulse precedes first bit clock

bit 0 **SPIBEN:** Enhanced Buffer Enable bit
1 = Enhanced buffer is enabled
0 = Enhanced buffer is disabled (Standard mode)


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# 19.0 INTER-INTEGRATED CIRCUIT ($I^2C$)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Inter-Integrated Circuit ($I^2C$)"** (www.microchip.com/DS70000195) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

**3:** There are minimum bit rates of approximately FCY/512. As a result, high processor speeds may not support 100 Kbit/second operation. See timing specifications, IM10 and IM11, and the **"Baud Rate Generator"** in the "*dsPIC33/PIC24 Family Reference Manual*".

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices contains two Inter-Integrated Circuit ($I^2C$) modules: I2C1 and I2C2.

The $I^2C$ module provides complete hardware support for both Slave and Multi-Master modes of the $I^2C$ serial communication standard, with a 16-bit interface.

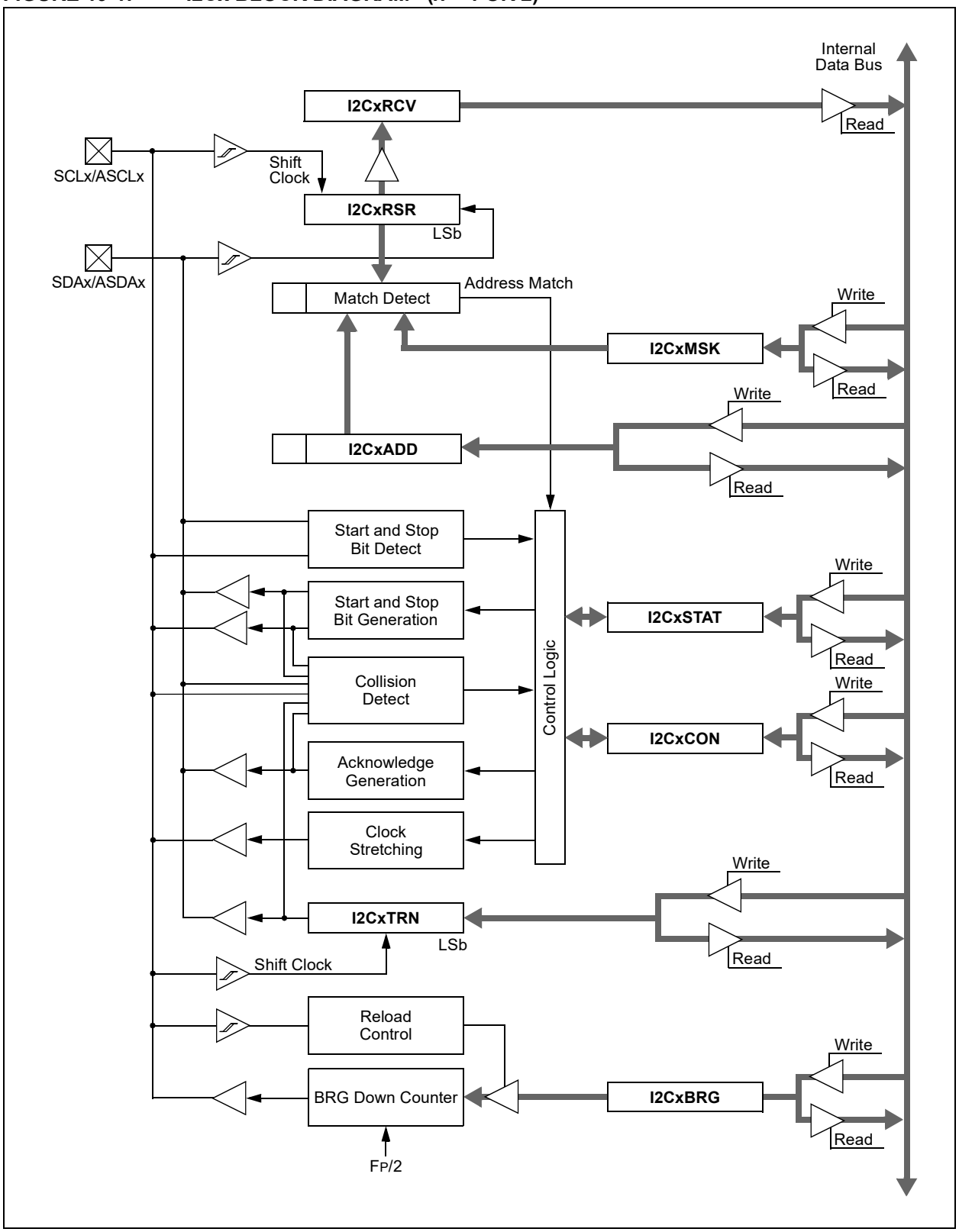
The $I^2C$ module has a 2-pin interface:

- The SCLx pin is clock
- The SDAx pin is data

The $I^2C$ module offers the following key features:

- $I^2C$ Interface Supporting both Master and Slave modes of Operation
- $I^2C$ Slave mode Supports 7 and 10-Bit Addressing
- $I^2C$ Master mode Supports 7 and 10-Bit Addressing
- $I^2C$ Port allows Bidirectional Transfers between Master and Slaves
- Serial Clock Synchronization for $I^2C$ Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control)
- $I^2C$ Supports Multi-Master Operation, Detects Bus Collision and Arbitrates Accordingly
- Intelligent Platform Management Interface (IPMI) Support
- System Management Bus (SMBus) Support

**FIGURE 19-1: I2Cx BLOCK DIAGRAM (x = 1 OR 2)**





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## 19.1 I²C Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 19.1.1 KEY RESOURCES

- **"Inter-Integrated Circuit (I²C)"** (www.microchip.com/DS70000195) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 19.2 I²C Control Registers

**REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | HC/R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| I2CEN | — | I2CSIDL | SCLREL | IPMIEN(1) | A10M | DISSLW | SMEN |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | HC/R/W-0 | HC/R/W-0 | HC/R/W-0 | HC/R/W-0 | HC/R/W-0 |
|---|---|---|---|---|---|---|---|
| GCEN | STREN | ACKDT | ACKEN | RCEN | PEN | RSEN | SEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **I2CEN:** I2Cx Enable bit
1 = Enables the I2Cx module and configures the SDAx and SCLx pins as serial port pins
0 = Disables the I2Cx module; all I²C pins are controlled by port functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **I2CSIDL:** I2Cx Stop in Idle Mode bit
1 = Discontinues module operation when device enters an Idle mode
0 = Continues module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (when operating as I²C slave)
1 = Releases SCLx clock
0 = Holds SCLx clock low (clock stretch)
If STREN = 1:
Bit is R/W (i.e., software can write '0' to initiate stretch and write '1' to release clock). Hardware is clear at the beginning of every slave data byte transmission. Hardware is clear at the end of every slave address byte reception. Hardware is clear at the end of every slave data byte reception.
If STREN = 0:
Bit is R/S (i.e., software can only write '1' to release clock). Hardware is clear at the beginning of every slave data byte transmission. Hardware is clear at the end of every slave address byte reception.

bit 11 **IPMIEN:** Intelligent Peripheral Management Interface (IPMI) Enable bit(1)
1 = IPMI mode is enabled; all addresses are Acknowledged
0 = IPMI mode disabled

bit 10 **A10M:** 10-Bit Slave Address bit
1 = I2CxADD is a 10-bit slave address
0 = I2CxADD is a 7-bit slave address

bit 9 **DISSLW:** Disable Slew Rate Control bit
1 = Slew rate control is disabled
0 = Slew rate control is enabled

bit 8 **SMEN:** SMBus Input Levels bit
1 = Enables I/O pin thresholds compliant with SMBus specification
0 = Disables SMBus input thresholds

bit 7 **GCEN:** General Call Enable bit (when operating as I²C slave)
1 = Enables interrupt when a general call address is received in I2CxRSR (module is enabled for reception)
0 = General call address disabled

**Note 1:** When performing master operations, ensure that the IPMIEN bit is set to '0'.


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**REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)**

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as $I^2C$ slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as $I^2C$ master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as $I^2C$ master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit. Hardware is clear at the end of the master Acknowledge sequence.
0 = Acknowledge sequence is not in progress

bit 3 **RCEN:** Receive Enable bit (when operating as $I^2C$ master)
1 = Enables Receive mode for $I^2C$. Hardware is clear at the end of the eighth bit of the master receive data byte.
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as $I^2C$ master)
1 = Initiates Stop condition on SDAx and SCLx pins. Hardware is clear at the end of the master Stop sequence.
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as $I^2C$ master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Repeated Start sequence.
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as $I^2C$ master)
1 = Initiates Start condition on SDAx and SCLx pins. Hardware is clear at the end of the master Start sequence.
0 = Start condition is not in progress

**Note 1:** When performing master operations, ensure that the IPMIEN bit is set to '0'.

**REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER**

| HSC/R-0 | HSC/R-0 | U-0 | U-0 | U-0 | HS/R/C-0 | HSC/R-0 | HSC/R-0 |
|---|---|---|---|---|---|---|---|
| ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 |
| bit 15 | | | | | | | bit 8 |

| HS/R/C-0 | HS/R/C-0 | HSC/R-0 | HSC/R/C-0 | HSC/R/C-0 | HSC/R-0 | HSC/R-0 | HSC/R-0 |
|---|---|---|---|---|---|---|---|
| IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Clearable bit | HS = Hardware Settable bit | HSC = Hardware Settable/Clearable bit |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ACKSTAT:** Acknowledge Status bit (when operating as $I^2C$ master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware is set or clear at the end of slave Acknowledge.

bit 14 **TRSTAT:** Transmit Status bit (when operating as $I^2C$ master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge.

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No bus collision detected
Hardware is set at detection of a bus collision.

bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware is set when address matches general call address. Hardware is clear at Stop detection.

bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection.

bit 7 **IWCOL:** I2Cx Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the $I^2C$ module is busy
0 = No collision
Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software).

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register was still holding the previous byte
0 = No overflow
Hardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).

bit 5 **D_A:** Data/Address bit (when operating as $I^2C$ slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.


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**REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)**

bit 3 **S:** Start bit
1 = Indicates that a Start (or Repeated Start) bit has been detected last
0 = Start bit was not detected last
Hardware is set or clear when a Start, Repeated Start or Stop is detected.

bit 2 **R_W:** Read/Write Information bit (when operating as $I^2C$ slave)
1 = Read – Indicates data transfer is output from the slave
0 = Write – Indicates data transfer is input to the slave
Hardware is set or clear after reception of an $I^2C$ device address byte.

bit 1 **RBF:** Receive Buffer Full Status bit
1 = Receive is complete, I2CxRCV is full
0 = Receive is not complete, I2CxRCV is empty
Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads I2CxRCV.

bit 0 **TBF:** Transmit Buffer Full Status bit
1 = Transmit in progress, I2CxTRN is full
0 = Transmit is complete, I2CxTRN is empty
Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of a data transmission.

**REGISTER 19-3: I2CxMSK: I2Cx SLAVE MODE ADDRESS MASK REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | AMSK[9:8] | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| AMSK[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-10 **Unimplemented:** Read as '0'

bit 9-0 **AMSK[9:0]:** Address Mask Select bits

For 10-Bit Address:

1 = Enables masking for bit Ax of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax; bit match is required in this position

For 7-Bit Address (I2CxMSK[6:0] only):

1 = Enables masking for bit Ax + 1 of incoming message address; bit match is not required in this position

0 = Disables masking for bit Ax + 1; bit match is required in this position


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## 20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"*.

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices contains two UART modules.

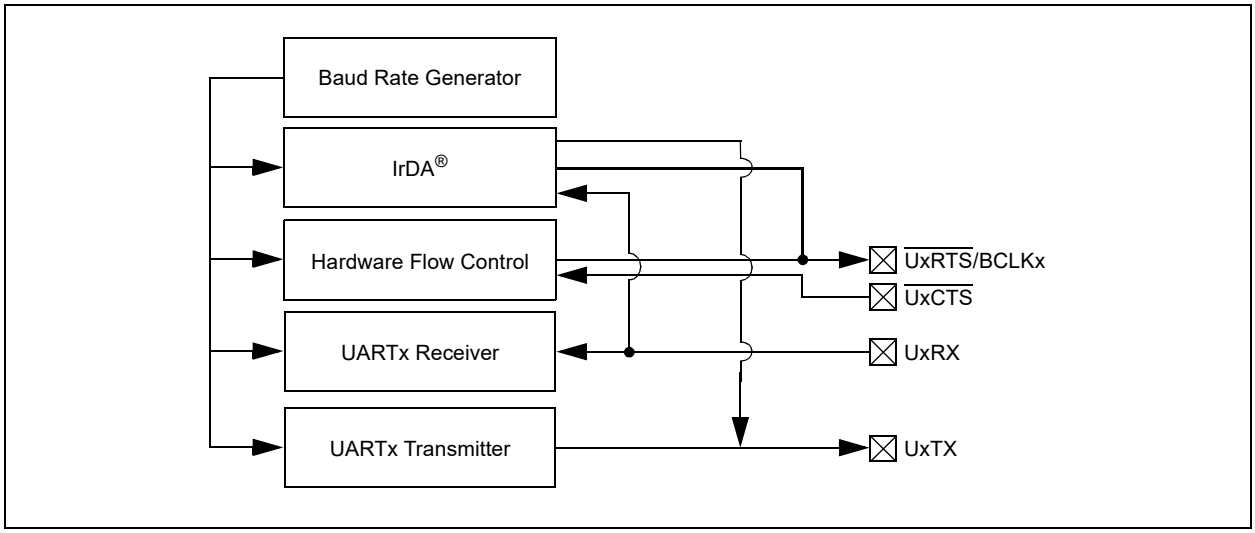
The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

**Note:** Hardware flow control using $\overline{\text{UxRTS}}$ and $\overline{\text{UxCTS}}$ is not available on all pin count devices. See the **"Pin Diagrams"** section for availability.

The primary features of the UARTx module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for all UARTx Error Conditions
- Loopback mode for Diagnostic Support

**FIGURE 20-1: UARTx SIMPLIFIED BLOCK DIAGRAM**



## 20.1 UART Helpful Tips

1. In multinode, direct-connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE[4]), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
   a) If URXINV = 0, use a pull-up resistor on the RX pin.
   b) If URXINV = 1, use a pull-down resistor on the RX pin.
2. The first character received on a wake-up from Sleep mode caused by activity on the UxRX pin of the UARTx module will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

## 20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 20.2.1 KEY RESOURCES

- **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools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## 20.3 UARTx Control Registers

**REGISTER 20-1: UxMODE: UARTx MODE REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| UARTEN(1) | — | USIDL | IREN(2) | RTSMD | — | UEN1 | UEN0 |
| bit 15 | | | | | | | bit 8 |

| HC/R/W-0 | R/W-0 | HC/R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL1 | PDSEL0 | STSEL |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **UARTEN:** UARTx Enable bit(1)
- 1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN[1:0]
- 0 = UARTx is disabled; all UARTx pins are controlled by PORT latches; UARTx power consumption is minimal

bit 14 **Unimplemented:** Read as '0'

bit 13 **USIDL:** UARTx Stop in Idle Mode bit
- 1 = Discontinues module operation when device enters Idle mode
- 0 = Continues module operation in Idle mode

bit 12 **IREN:** IrDA® Encoder and Decoder Enable bit(2)
- 1 = IrDA encoder and decoder are enabled
- 0 = IrDA encoder and decoder are disabled

bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
- 1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
- 0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode

bit 10 **Unimplemented:** Read as '0'

bit 9-8 **UEN[1:0]:** UARTx Pin Enable bits
- 11 = UxTX, UxRX and BCLKx pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches(3)
- 10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used(4)
- 01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches(4)
- 00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$/BCLKx pins are controlled by PORT latches

bit 7 **WAKE:** Wake-up on Start bit Detect During Sleep Mode Enable bit
- 1 = UARTx continues to sample the UxRX pin; interrupt is generated on the falling edge; bit is cleared in hardware on the following rising edge
- 0 = No wake-up is enabled

bit 6 **LPBACK:** UARTx Loopback Mode Select bit
- 1 = Enables Loopback mode
- 0 = Loopback mode is disabled

**Note 1:** Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for receive or transmit operation.

**2:** This feature is only available for the 16x BRG mode (BRGH = 0).

**3:** This feature is only available on 44-pin and 64-pin devices.

**4:** This feature is only available on 64-pin devices.

**REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)**

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
0 = Baud rate measurement is disabled or completed

bit 4 **URXINV:** UARTx Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates four clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)

bit 2-1 **PDSEL[1:0]:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

**Note 1:** Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for receive or transmit operation.
**2:** This feature is only available for the 16x BRG mode (BRGH = 0).
**3:** This feature is only available on 44-pin and 64-pin devices.
**4:** This feature is only available on 64-pin devices.


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**REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | HC/R/W-0 | R/W-0 | R-0 | R-1 |
|---|---|---|---|---|---|---|---|
| UTXISEL1 | UTXINV | UTXISEL0 | — | UTXBRK | UTXEN(1) | UTXBF | TRMT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R-1 | R-0 | R-0 | R/C-0 | R-0 |
|---|---|---|---|---|---|---|---|
| URXISEL1 | URXISEL0 | ADDEN | RIDLE | PERR | FERR | OERR | URXDA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | C = Clearable bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15,13 **UTXISEL[1:0]:** UARTx Transmission Interrupt Mode Selection bits
- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR) and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)

bit 14 **UTXINV:** UARTx Transmit Polarity Inversion bit

If IREN = 0:
- 1 = UxTX Idle state is '0'
- 0 = UxTX Idle state is '1'

If IREN = 1:
- 1 = IrDA encoded, UxTX Idle state is '1'
- 0 = IrDA encoded, UxTX Idle state is '0'

bit 12 **Unimplemented:** Read as '0'

bit 11 **UTXBRK:** UARTx Transmit Break bit
- 1 = Sends Sync Break on next transmission – Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
- 0 = Sync Break transmission is disabled or completed

bit 10 **UTXEN:** UARTx Transmit Enable bit(1)
- 1 = Transmit is enabled, UxTX pin is controlled by UARTx
- 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; UxTX pin is controlled by the PORT

bit 9 **UTXBF:** UARTx Transmit Buffer Full Status bit (read-only)
- 1 = Transmit buffer is full
- 0 = Transmit buffer is not full, at least one more character can be written

bit 8 **TRMT:** Transmit Shift Register Empty bit (read-only)
- 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
- 0 = Transmit Shift Register is not empty, a transmission is in progress or queued

bit 7-6 **URXISEL[1:0]:** UARTx Receive Interrupt Mode Selection bits
- 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has four data characters)
- 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has three data characters)
- 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters

**Note 1:** Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

**REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the UxRSR to the empty state

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

**Note 1:** Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (www.microchip.com/DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for transmit operation.


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# 21.0 ENHANCED CAN (ECAN™) MODULE (dsPIC33EPXXXGP/MC50X DEVICES ONLY)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Enhanced Controller Area Network (ECAN™)"** (www.microchip.com/DS70353) in the *"dsPIC33/PIC24 Family Reference Manual"*.

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

## 21.1 Overview

The Enhanced Controller Area Network (ECAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/protocol was designed to allow communications within noisy environments. The dsPIC33EPXXXGP/MC50X devices contain one ECAN module.

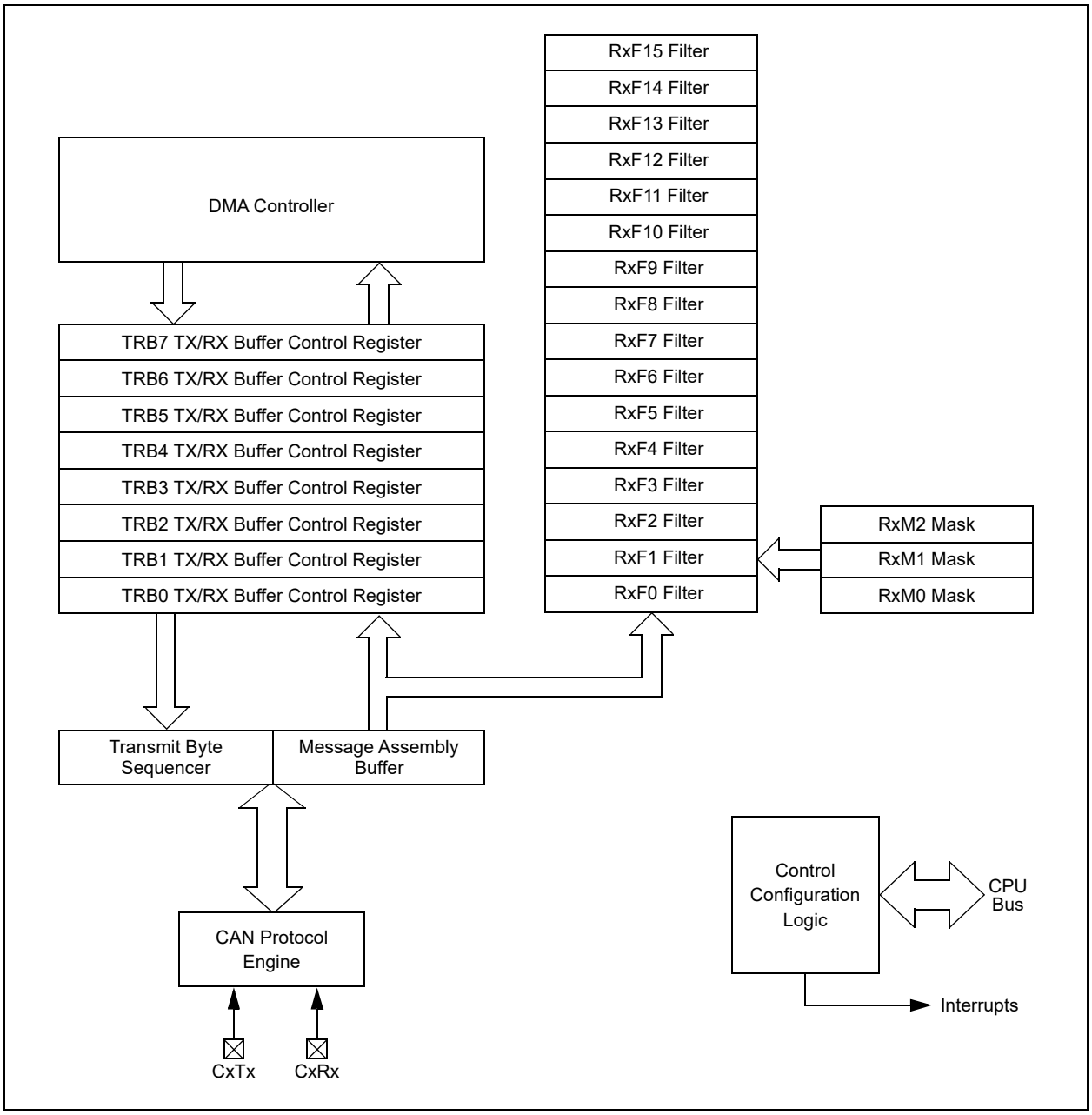
The ECAN module is a communication controller implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details.

The ECAN module features are as follows:

- Implementation of the CAN Protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and Extended Data Frames
- 0-8 Bytes Data Length
- Programmable Bit Rate Up to 1 Mbit/sec
- Automatic Response to Remote Transmission Requests
- Up to Eight Transmit Buffers with Application-Specified Prioritization and Abort Capability (each buffer can contain up to 8 bytes of data)
- Up to 32 Receive Buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 Full (Standard/Extended Identifier) Acceptance Filters
- Three Full Acceptance Filter Masks
- DeviceNet™ Addressing Support
- Programmable Wake-up Functionality with Integrated Low-Pass Filter
- Programmable Loopback mode supports Self-Test Operation
- Signaling via Interrupt Capabilities for All CAN Receiver and Transmitter Error States
- Programmable Clock Source
- Programmable Link to Input Capture (IC2) module for Timestamping and Network Synchronization
- Low-Power Sleep and Idle mode

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

**FIGURE 21-1: ECAN™ MODULE BLOCK DIAGRAM**





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## 21.2 Modes of Operation

The ECAN module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP[2:0] bits (CxCTRL1[10:8]). Entry into a mode is Acknowledged by monitoring the OPMODE[2:0] bits (CxCTRL1[7:5]). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

## 21.3 ECAN Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 21.3.1 KEY RESOURCES

- **"Enhanced Controller Area Network (ECAN™)"** (www.microchip.com/DS70353) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 21.4 ECAN Control Registers

**REGISTER 21-1: CxCTRL1: ECANx CONTROL REGISTER 1**

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | CSIDL | ABAT | CANCKS | REQOP2 | REQOP1 | REQOP0 |
| bit 15 | | | | | | | bit 8 |

| R-1 | R-0 | R-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OPMODE2 | OPMODE1 | OPMODE0 | — | CANCAP | — | — | WIN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** ECANx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signals all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted

bit 11 **CANCKS:** ECANx Module Clock (FCAN) Source Select bit
1 = FCAN is equal to 2 * FP
0 = FCAN is equal to FP

bit 10-8 **REQOP[2:0]:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 7-5 **OPMODE[2:0]**: Operation Mode bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 4 **Unimplemented:** Read as '0'

bit 3 **CANCAP:** CAN Message Receive Timer Capture Event Enable bit
1 = Enables input capture based on CAN message receive
0 = Disables CAN capture

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **WIN:** SFR Map Window Select bit
1 = Uses filter window
0 = Uses buffer window


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**REGISTER 21-2: CxCTRL2: ECANx CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DNCNT[4:0] | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **DNCNT[4:0]:** DeviceNet™ Filter Bit Number bits

10010-11111 = Invalid selection
10001 = Compares up to Data Byte 3, bit 6 with EID[17]
•
•
•
00001 = Compares up to Data Byte 1, bit 7 with EID[0]
00000 = Does not compare data bytes

**REGISTER 21-3: CxVEC: ECANx INTERRUPT CODE REGISTER**

| U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | FILHIT[4:0] | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R-1 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | ICODE[6:0] | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT[4:0]:** Filter Hit Number bits

10000-11111 = Reserved
01111 = Filter 15
•
•
•
00001 = Filter 1
00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE[6:0]:** Interrupt Flag Code bits

1000101-1111111 = Reserved
1000100 = FIFO almost full interrupt
1000011 = Receiver overflow interrupt
1000010 = Wake-up interrupt
1000001 = Error interrupt
1000000 = No interrupt
•
•
•
0010000-0111111 = Reserved
0001111 = RB15 buffer interrupt
•
•
•
0001001 = RB9 buffer interrupt
0001000 = RB8 buffer interrupt
0000111 = TRB7 buffer interrupt
0000110 = TRB6 buffer interrupt
0000101 = TRB5 buffer interrupt
0000100 = TRB4 buffer interrupt
0000011 = TRB3 buffer interrupt
0000010 = TRB2 buffer interrupt
0000001 = TRB1 buffer interrupt
0000000 = TRB0 buffer interrupt


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**REGISTER 21-4: CxFCTRL: ECANx FIFO CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| DMABS[2:0] | | | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | FSA[4:0] | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **DMABS[2:0]:** DMA Buffer Size bits
111 = Reserved
110 = 32 buffers in RAM
101 = 24 buffers in RAM
100 = 16 buffers in RAM
011 = 12 buffers in RAM
010 = 8 buffers in RAM
001 = 6 buffers in RAM
000 = 4 buffers in RAM

bit 12-5 **Unimplemented:** Read as '0'

bit 4-0 **FSA[4:0]:** FIFO Area Starts with Buffer bits
11111 = Read Buffer RB31
11110 = Read Buffer RB30
•
•
•
00001 = TX/RX Buffer TRB1
00000 = TX/RX Buffer TRB0

**REGISTER 21-5: CxFIFO: ECANx FIFO STATUS REGISTER**

| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | FBP[5:0] | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | FNRB[5:0] | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **FBP[5:0]:** FIFO Buffer Pointer bits
011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **FNRB[5:0]:** FIFO Next Read Buffer Pointer bits
011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer


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**REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER**

| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | TXBO | TXBP | RXBP | TXWAR | RXWAR | EWARN |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | U-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| IVRIF | WAKIF | ERRIF | — | FIFOIF | RBOVIF | RBIF | TBIF |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only ‘0’ can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **TXBO:** Transmitter in Error State Bus Off bit
1 = Transmitter is in Bus Off state
0 = Transmitter is not in Bus Off state

bit 12 **TXBP:** Transmitter in Error State Bus Passive bit
1 = Transmitter is in Bus Passive state
0 = Transmitter is not in Bus Passive state

bit 11 **RXBP:** Receiver in Error State Bus Passive bit
1 = Receiver is in Bus Passive state
0 = Receiver is not in Bus Passive state

bit 10 **TXWAR:** Transmitter in Error State Warning bit
1 = Transmitter is in Error Warning state
0 = Transmitter is not in Error Warning state

bit 9 **RXWAR:** Receiver in Error State Warning bit
1 = Receiver is in Error Warning state
0 = Receiver is not in Error Warning state

bit 8 **EWARN:** Transmitter or Receiver in Error State Warning bit
1 = Transmitter or receiver is in Error Warning state
0 = Transmitter or receiver is not in Error Warning state

bit 7 **IVRIF:** Invalid Message Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **WAKIF:** Bus Wake-up Activity Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **ERRIF:** Error Interrupt Flag bit (multiple sources in CxINTF[13:8])
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **FIFOIF:** FIFO Almost Full Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **RBOVIF:** RX Buffer Overflow Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

**REGISTER 21-6: CxINTF: ECANx INTERRUPT FLAG REGISTER (CONTINUED)**

bit 1 **RBIF:** RX Buffer Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 0 **TBIF:** TX Buffer Interrupt Flag bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred


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**REGISTER 21-7: CxINTE: ECANx INTERRUPT ENABLE REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IVRIE | WAKIE | ERRIE | — | FIFOIE | RBOVIE | RBIE | TBIE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7 **IVRIE:** Invalid Message Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **WAKIE:** Bus Wake-up Activity Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **ERRIE:** Error Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **FIFOIE:** FIFO Almost Full Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 2 **RBOVIE:** RX Buffer Overflow Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 1 **RBIE:** RX Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 0 **TBIE:** TX Buffer Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

**REGISTER 21-8: CxEC: ECANx TRANSMIT/RECEIVE ERROR COUNT REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| TERRCNT[7:0] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| RERRCNT[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **TERRCNT[7:0]:** Transmit Error Count bits

bit 7-0 **RERRCNT[7:0]:** Receive Error Count bits

**REGISTER 21-9: CxCFG1: ECANx BAUD RATE CONFIGURATION REGISTER 1**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-6 **SJW[1:0]:** Synchronization Jump Width bits
11 = Length is 4 x TQ
10 = Length is 3 x TQ
01 = Length is 2 x TQ
00 = Length is 1 x TQ

bit 5-0 **BRP[5:0]:** Baud Rate Prescaler bits
11 1111 = TQ = 2 x 64 x 1/FCAN
•
•
•
00 0010 = TQ = 2 x 3 x 1/FCAN
00 0001 = TQ = 2 x 2 x 1/FCAN
00 0000 = TQ = 2 x 1 x 1/FCAN


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**REGISTER 21-10: CxCFG2: ECANx BAUD RATE CONFIGURATION REGISTER 2**

| U-0 | R/W-x | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | WAKFIL | — | — | — | SEG2PH2 | SEG2PH1 | SEG2PH0 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SEG2PHTS | SAM | SEG1PH2 | SEG1PH1 | SEG1PH0 | PRSEG2 | PRSEG1 | PRSEG0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14 **WAKFIL:** Select CAN Bus Line Filter for Wake-up bit
1 = Uses CAN bus line filter for wake-up
0 = CAN bus line filter is not used for wake-up

bit 13-11 **Unimplemented:** Read as '0'

bit 10-8 **SEG2PH[2:0]:** Phase Segment 2 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 7 **SEG2PHTS:** Phase Segment 2 Time Select bit
1 = Freely programmable
0 = Maximum of SEG1PHx bits or Information Processing Time (IPT), whichever is greater

bit 6 **SAM:** Sample of the CAN Bus Line bit
1 = Bus line is sampled three times at the sample point
0 = Bus line is sampled once at the sample point

bit 5-3 **SEG1PH[2:0]:** Phase Segment 1 bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

bit 2-0 **PRSEG[2:0]:** Propagation Time Segment bits
111 = Length is 8 x TQ
•
•
•
000 = Length is 1 x TQ

**REGISTER 21-11: CxFEN1: ECANx ACCEPTANCE FILTER ENABLE REGISTER 1**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| FLTEN[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| FLTEN[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **FLTEN[15:0]:** Enable Filter n to Accept Messages bits
1 = Enables Filter n
0 = Disables Filter n

**REGISTER 21-12: CxBUFPNT1: ECANx FILTER 0-3 BUFFER POINTER REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F3BP[3:0] | | | | F2BP[3:0] | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F1BP[3:0] | | | | F0BP[3:0] | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **F3BP[3:0]:** RX Buffer Mask for Filter 3 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP[3:0]:** RX Buffer Mask for Filter 2 bits (same values as bits[15:12])

bit 7-4 **F1BP[3:0]:** RX Buffer Mask for Filter 1 bits (same values as bits[15:12])

bit 3-0 **F0BP[3:0]:** RX Buffer Mask for Filter 0 bits (same values as bits[15:12])


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**REGISTER 21-13: CxBUFPNT2: ECANx FILTER 4-7 BUFFER POINTER REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F7BP[3:0] | | | | F6BP[3:0] | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F5BP[3:0] | | | | F4BP[3:0] | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **F7BP[3:0]:** RX Buffer Mask for Filter 7 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F6BP[3:0]:** RX Buffer Mask for Filter 6 bits (same values as bits[15:12])

bit 7-4 **F5BP[3:0]:** RX Buffer Mask for Filter 5 bits (same values as bits[15:12])

bit 3-0 **F4BP[3:0]:** RX Buffer Mask for Filter 4 bits (same values as bits[15:12])

**REGISTER 21-14: CxBUFPNT3: ECANx FILTER 8-11 BUFFER POINTER REGISTER 3**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F11BP[3:0] | | | | F10BP[3:0] | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F9BP[3:0] | | | | F8BP[3:0] | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **F11BP[3:0]:** RX Buffer Mask for Filter 11 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F10BP[3:0]:** RX Buffer Mask for Filter 10 bits (same values as bits[15:12])

bit 7-4 **F9BP[3:0]:** RX Buffer Mask for Filter 9 bits (same values as bits[15:12])

bit 3-0 **F8BP[3:0]:** RX Buffer Mask for Filter 8 bits (same values as bits[15:12])

**REGISTER 21-15: CxBUFPNT4: ECANx FILTER 12-15 BUFFER POINTER REGISTER 4**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F15BP[3:0] | | | | F14BP[3:0] | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F13BP[3:0] | | | | F12BP[3:0] | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **F15BP[3:0]:** RX Buffer Mask for Filter 15 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP[3:0]:** RX Buffer Mask for Filter 14 bits (same values as bits[15:12])

bit 7-4 **F13BP[3:0]:** RX Buffer Mask for Filter 13 bits (same values as bits[15:12])

bit 3-0 **F12BP[3:0]:** RX Buffer Mask for Filter 12 bits (same values as bits[15:12])


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**REGISTER 21-16: CxRXFnSID: ECANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID[10:3] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | U-0 | R/W-x | U-0 | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID[2:0] | | | — | EXIDE | — | EID[17:16] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **SID[10:0]:** Standard Identifier bits
1 = Message address bit, SIDx, must be '1' to match filter
0 = Message address bit, SIDx, must be '0' to match filter

bit 4 **Unimplemented:** Read as '0'

bit 3 **EXIDE:** Extended Identifier Enable bit
If MIDE = 1:
1 = Matches only messages with Extended Identifier addresses
0 = Matches only messages with Standard Identifier addresses
If MIDE = 0:
Ignores EXIDE bit.

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID[17:16]:** Extended Identifier bits
1 = Message address bit, EIDx, must be '1' to match filter
0 = Message address bit, EIDx, must be '0' to match filter

**REGISTER 21-17: CxRXFnEID: ECANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **EID[15:0]:** Extended Identifier bits
1 = Message address bit, EIDx, must be ‘1’ to match filter
0 = Message address bit, EIDx, must be ‘0’ to match filter

**REGISTER 21-18: CxFMSKSEL1: ECANx FILTER 7-0 MASK SELECTION REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F7MSK[1:0] | | F6MSK[1:0] | | F5MSK[1:0] | | F4MSK[1:0] | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F3MSK[1:0] | | F2MSK[1:0] | | F1MSK[1:0] | | F0MSK[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **F7MSK[1:0]:** Mask Source for Filter 7 bits
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F6MSK[1:0]:** Mask Source for Filter 6 bits (same values as bits[15:14])

bit 11-10 **F5MSK[1:0]:** Mask Source for Filter 5 bits (same values as bits[15:14])

bit 9-8 **F4MSK[1:0]:** Mask Source for Filter 4 bits (same values as bits[15:14])

bit 7-6 **F3MSK[1:0]:** Mask Source for Filter 3 bits (same values as bits[15:14])

bit 5-4 **F2MSK[1:0]:** Mask Source for Filter 2 bits (same values as bits[15:14])

bit 3-2 **F1MSK[1:0]:** Mask Source for Filter 1 bits (same values as bits[15:14])

bit 1-0 **F0MSK[1:0]:** Mask Source for Filter 0 bits (same values as bits[15:14])


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**REGISTER 21-19: CxFMSKSEL2: ECANx FILTER 15-8 MASK SELECTION REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F15MSK[1:0] | | F14MSK[1:0] | | F13MSK[1:0] | | F12MSK[1:0] | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| F11MSK[1:0] | | F10MSK[1:0] | | F9MSK[1:0] | | F8MSK[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **F15MSK[1:0]:** Mask Source for Filter 15 bits
11 = Reserved
10 = Acceptance Mask 2 registers contain mask
01 = Acceptance Mask 1 registers contain mask
00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F14MSK[1:0]:** Mask Source for Filter 14 bits (same values as bits[15:14])

bit 11-10 **F13MSK[1:0]:** Mask Source for Filter 13 bits (same values as bits[15:14])

bit 9-8 **F12MSK[1:0]:** Mask Source for Filter 12 bits (same values as bits[15:14])

bit 7-6 **F11MSK[1:0]:** Mask Source for Filter 11 bits (same values as bits[15:14])

bit 5-4 **F10MSK[1:0]:** Mask Source for Filter 10 bits (same values as bits[15:14])

bit 3-2 **F9MSK[1:0]:** Mask Source for Filter 9 bits (same values as bits[15:14])

bit 1-0 **F8MSK[1:0]:** Mask Source for Filter 8 bits (same values as bits[15:14])

**REGISTER 21-20: CxRXMnSID: ECANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER (n = 0-2)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID[10:3] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | U-0 | R/W-x | U-0 | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID[2:0] | | | — | MIDE | — | EID[17:16] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **SID[10:0]:** Standard Identifier bits
1 = Includes bit, SIDx, in filter comparison
0 = SIDx bit is a don't care in filter comparison

bit 4 **Unimplemented:** Read as '0'

bit 3 **MIDE:** Identifier Receive Mode bit
1 = Matches only message types (standard or extended address) that correspond to EXIDE bit in the filter
0 = Matches either standard or extended address message if filters match (i.e., if (Filter SID) = (Message SID) or if (Filter SID/EID) = (Message SID/EID))

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID[17:16]:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = EIDx bit is a don't care in filter comparison

**REGISTER 21-21: CxRXMnEID: ECANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **EID[15:0]:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = EIDx bit is a don't care in filter comparison


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**REGISTER 21-22: CxRXFUL1: ECANx RECEIVE BUFFER FULL REGISTER 1**

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXFUL[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXFUL[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only '0' can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXFUL[15:0]:** Receive Buffer n Full bits
1 = Buffer is full (set by module)
0 = Buffer is empty (cleared by user software)

**REGISTER 21-23: CxRXFUL2: ECANx RECEIVE BUFFER FULL REGISTER 2**

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXFUL[31:24] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXFUL[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only '0' can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXFUL[31:16]:** Receive Buffer n Full bits
1 = Buffer is full (set by module)
0 = Buffer is empty (cleared by user software)

**REGISTER 21-24: CxRXOVF1: ECANx RECEIVE BUFFER OVERFLOW REGISTER 1**

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only ‘0’ can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXOVF[15:0]:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)

**REGISTER 21-25: CxRXOVF2: ECANx RECEIVE BUFFER OVERFLOW REGISTER 2**

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF[31:24] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 | R/C-0 |
|---|---|---|---|---|---|---|---|
| RXOVF[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | C = Writable bit, but only ‘0’ can be written to clear the bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **RXOVF[31:16]:** Receive Buffer n Overflow bits
1 = Module attempted to write to a full buffer (set by module)
0 = No overflow condition (cleared by user software)


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**REGISTER 21-26: CxTRmnCON: ECANx TX/RX BUFFER mn CONTROL REGISTER (m = 0,2,4,6; n = 1,3,5,7)**

| R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TXENn | TXABTn | TXLARBn | TXERRn | TXREQn | RTRENn | TXnPRI1 | TXnPRI0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R-0 | R-0 | R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TXENm | TXABTm(1) | TXLARBm(1) | TXERRm(1) | TXREQm | RTRENm | TXmPRI1 | TXmPRI0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 See Definition for bits[7:0], Controls Buffer n

bit 7 **TXENm:** TX/RX Buffer Selection bit
1 = Buffer TRBn is a transmit buffer
0 = Buffer TRBn is a receive buffer

bit 6 **TXABTm:** Message Aborted bit(1)
1 = Message was aborted
0 = Message completed transmission successfully

bit 5 **TXLARBm:** Message Lost Arbitration bit(1)
1 = Message lost arbitration while being sent
0 = Message did not lose arbitration while being sent

bit 4 **TXERRm:** Error Detected During Transmission bit(1)
1 = A bus error occurred while the message was being sent
0 = A bus error did not occur while the message was being sent

bit 3 **TXREQm:** Message Send Request bit
1 = Requests that a message be sent; the bit automatically clears when the message is successfully sent
0 = Clearing the bit to '0' while set requests a message abort

bit 2 **RTRENm:** Auto-Remote Transmit Enable bit
1 = When a remote transmit is received, TXREQ will be set
0 = When a remote transmit is received, TXREQ will be unaffected

bit 1-0 **TXmPRI[1:0]:** Message Transmission Priority bits
11 = Highest message priority
10 = High intermediate message priority
01 = Low intermediate message priority
00 = Lowest message priority

**Note 1:** This bit is cleared when TXREQ is set.

**Note:** The buffers, SID, EID, DLC, Data Field, and Receive Status registers are located in DMA RAM.

## 21.5 ECAN Message Buffers

ECAN Message Buffers are part of RAM memory. They are not ECAN Special Function Registers. The user application must directly write into the RAM area that is configured for ECAN Message Buffers. The location and size of the buffer area is defined by the user application.

**BUFFER 21-1: ECAN™ MESSAGE BUFFER WORD 0**

| U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | SID[10:6] | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID[5:0] | | | | | | SRR | IDE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-2 **SID[10:0]:** Standard Identifier bits

bit 1 **SRR:** Substitute Remote Request bit

When IDE = 0:
1 = Message will request remote transmission
0 = Normal message

When IDE = 1:
The SRR bit must be set to '1'.

bit 0 **IDE:** Extended Identifier bit

1 = Message will transmit Extended Identifier
0 = Message will transmit Standard Identifier

**BUFFER 21-2: ECAN™ MESSAGE BUFFER WORD 1**

| U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | — | EID[17:14] | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID[13:6] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **EID[17:6]:** Extended Identifier bits


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**BUFFER 21-3: ECAN™ MESSAGE BUFFER WORD 2**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID5 | EID4 | EID3 | EID2 | EID1 | EID0 | RTR | RB1 |
| bit 15 | | | | | | | bit 8 |

| U-x | U-x | U-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | RB0 | DLC3 | DLC2 | DLC1 | DLC0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 **EID[5:0]:** Extended Identifier bits

bit 9 **RTR:** Remote Transmission Request bit
When IDE = 1:
1 = Message will request remote transmission
0 = Normal message
When IDE = 0:
The RTR bit is ignored.

bit 8 **RB1:** Reserved Bit 1
User must set this bit to ‘0’ per CAN protocol.

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **RB0:** Reserved Bit 0
User must set this bit to ‘0’ per CAN protocol.

bit 3-0 **DLC[3:0]:** Data Length Code bits

**BUFFER 21-4: ECAN™ MESSAGE BUFFER WORD 3**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 1[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 0[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Byte 1[15:8]:** ECAN Message Byte 1 bits

bit 7-0 **Byte 0[7:0]:** ECAN Message Byte 0 bits

**BUFFER 21-5: ECAN™ MESSAGE BUFFER WORD 4**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 3[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 2[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Byte 3[15:8]:** ECAN Message Byte 3 bits

bit 7-0 **Byte 2[7:0]:** ECAN Message Byte 2 bits

**BUFFER 21-6: ECAN™ MESSAGE BUFFER WORD 5**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 5[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 4[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Byte 5[15:8]:** ECAN Message Byte 5 bits

bit 7-0 **Byte 4[7:0]:** ECAN Message Byte 4 bits


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**BUFFER 21-7: ECAN™ MESSAGE BUFFER WORD 6**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 7[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| Byte 6[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Byte 7[15:8]:** ECAN Message Byte 7 bits

bit 7-0 **Byte 6[7:0]:** ECAN Message Byte 6 bits

**BUFFER 21-8: ECAN™ MESSAGE BUFFER WORD 7**

| U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | FILHIT[4:0](1) | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT[4:0]:** Filter Hit Code bits(1)
Encodes number of filter that resulted in writing this buffer.

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** Only written by module for receive buffers, unused for transmit buffers.

**NOTES:**


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## 22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Charge Time Measurement Unit (CTMU)"** (www.microchip.com/DS70661) in the "*dsPIC33/PIC24 Family Reference Manual*".

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

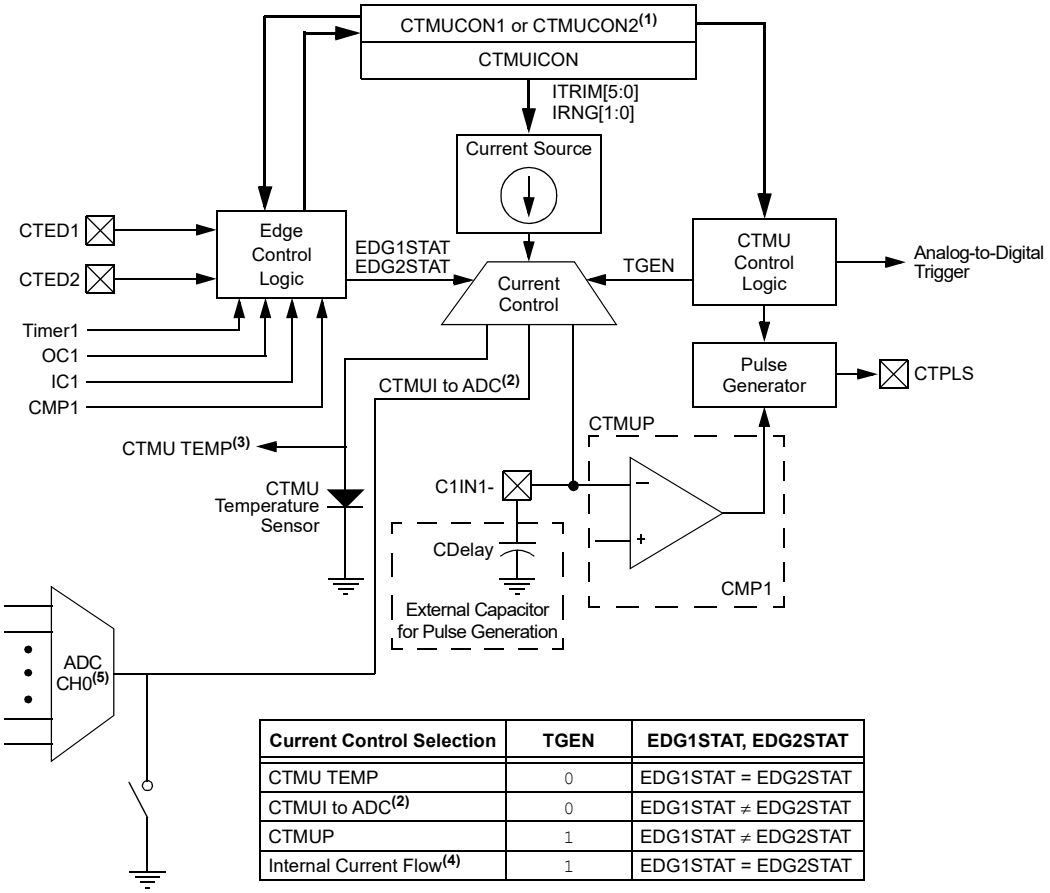
The Charge Time Measurement Unit is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Four Edge Input Trigger Sources
- Polarity Control for Each Edge Source
- Control of Edge Sequence
- Control of Response to Edges
- Precise Time Measurement Resolution of 1 ns
- Accurate Current Source Suitable for Capacitive Measurement
- On-Chip Temperature Measurement using a Built-in Diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors.The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

**FIGURE 22-1: CTMU BLOCK DIAGRAM**




| Current Control Selection | TGEN | EDG1STAT, EDG2STAT |
|---|---|---|
| CTMU TEMP | 0 | EDG1STAT = EDG2STAT |
| CTMUI to ADC(2) | 0 | EDG1STAT ≠ EDG2STAT |
| CTMUP | 1 | EDG1STAT ≠ EDG2STAT |
| Internal Current Flow(4) | 1 | EDG1STAT = EDG2STAT |

**Note 1:** When the CTMU is not actively used, set TGEN = 1, and ensure that EDG1STAT = EDG2STAT. All other settings allow current to flow into the ADC or the C1IN1- pin. If using the ADC for other purposes besides the CTMU, set IDISSEN = 0. If IDISSEN is set to '1', it will short the output of the ADC CH0 MUX to VSS.

**2:** CTMUI connects to the output of the ADC CH0 MUX. When CTMU current is steered into this node, the current will flow out through the selected ADC channel determined by the CH0 MUX (see the CH0Sx bits in the AD1CHS0 register).

**3:** CTMU TEMP connects to one of the ADC CH0 inputs; see CH0SA and CH0SB (AD1CHS0[12:8,4:0]).

**4:** If TGEN = 1 and EDG1STAT = EDG2STAT, CTMU current source is still enabled and may be shunted to VSS internally. This should be considered in low-power applications.

**5:** The switch connected to ADC CH0 is closed when IDISSEN (CTMUCON1[9]) = 1, and opened when IDISSEN = 0.

## 22.1 CTMU Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

### 22.1.1 KEY RESOURCES

- **"Charge Time Measurement Unit (CTMU)"** (www.microchip.com/DS70661) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools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## 22.2 CTMU Control Registers

**REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CTMUEN | — | CTMUSIDL | TGEN | EDGEN | EDGSEQEN | IDISSEN(1) | CTTRIG |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CTMUEN:** CTMU Enable bit
1 = Module is enabled
0 = Module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **TGEN:** Time Generation Enable bit
1 = Enables edge delay generation
0 = Disables edge delay generation

bit 11 **EDGEN:** Edge Enable bit
1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)
0 = Software is used to trigger edges (manual set of EDGxSTAT)

bit 10 **EDGSEQEN:** Edge Sequence Enable bit
1 = Edge 1 event must occur before Edge 2 event can occur
0 = No edge sequence is needed

bit 9 **IDISSEN:** Analog Current Source Control bit(1)
1 = Analog current source output is grounded
0 = Analog current source output is not grounded

bit 8 **CTTRIG:** ADC Trigger Control bit
1 = CTMU triggers ADC start of conversion
0 = CTMU does not trigger ADC start of conversion

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** The ADC module Sample-and-Hold capacitor is not automatically discharged between sample/conversion cycles. Software using the ADC as part of a capacitance measurement must discharge the ADC capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADC must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

**REGISTER 22-2: CTMUCON2: CTMU CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| EDG1MOD | EDG1POL | EDG1SEL3 | EDG1SEL2 | EDG1SEL1 | EDG1SEL0 | EDG2STAT | EDG1STAT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| EDG2MOD | EDG2POL | EDG2SEL3 | EDG2SEL2 | EDG2SEL1 | EDG2SEL0 | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **EDG1MOD:** Edge 1 Edge Sampling Mode Selection bit
1 = Edge 1 is edge-sensitive
0 = Edge 1 is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 is programmed for a positive edge response
0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL[3:0]:** Edge 1 Source Select bits
1xxx = Reserved
01xx = Reserved
0011 = CTED1 pin
0010 = CTED2 pin
0001 = OC1 module
0000 = Timer1 module

bit 9 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control the edge source.
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control the edge source.
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge Sampling Mode Selection bit
1 = Edge 2 is edge-sensitive
0 = Edge 2 is level-sensitive

bit 6 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 is programmed for a positive edge response
0 = Edge 2 is programmed for a negative edge response

bit 5-2 **EDG2SEL[3:0]:** Edge 2 Source Select bits
1111 = Reserved
01xx = Reserved
0100 = CMP1 module
0011 = CTED2 pin
0010 = CTED1 pin
0001 = OC1 module
0000 = IC1 module

bit 1-0 **Unimplemented:** Read as '0'


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**REGISTER 22-3: CTMUICON: CTMU CURRENT CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ITRIM5 | ITRIM4 | ITRIM3 | ITRIM2 | ITRIM1 | ITRIM0 | IRNG1 | IRNG0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-10 **ITRIM[5:0]:** Current Source Trim bits

011111 = Maximum positive change from nominal current + 62%
011110 = Maximum positive change from nominal current + 60%
•
•
•
000010 = Minimum positive change from nominal current + 4%
000001 = Minimum positive change from nominal current + 2%
000000 = Nominal current output specified by IRNG[1:0]
111111 = Minimum negative change from nominal current – 2%
111110 = Minimum negative change from nominal current – 4%
•
•
•
100010 = Maximum negative change from nominal current – 60%
100001 = Maximum negative change from nominal current – 62%

bit 9-8 **IRNG[1:0]:** Current Source Range Select bits

11 = 100 × Base Current(2)
10 = 10 × Base Current(2)
01 = Base Current Level(2)
00 = 1000 × Base Current(1,2)

bit 7-0 **Unimplemented:** Read as ‘0’

**Note 1:** This current range is not available to be used with the internal temperature measurement diode.

**2:** Refer to the CTMU Current Source Specifications (Table 30-56) in **Section 30.0 “Electrical Characteristics”** for the current range selection values.

**NOTES:**


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# 23.0 10-BIT/12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Analog-to-Digital Converter (ADC)"** (www.microchip.com/DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*.

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices have one ADC module. The ADC module supports up to 16 analog input channels.

On ADC1, the AD12B bit (AD1CON1[10]) allows the ADC module to be configured by the user as either a 10-bit, four Sample-and-Hold (S&H) ADC (default configuration) or a 12-bit, one S&H ADC.

**Note:** The ADC module needs to be disabled before modifying the AD12B bit.

## 23.1 Key Features

### 23.1.1 10-BIT ADC CONFIGURATION

The 10-bit ADC configuration has the following key features:

- Successive Approximation (SAR) Conversion
- Conversion Speeds of Up to 1.1 Msps
- Up to 16 Analog Input Pins
- Connections to Three Internal Op Amps
- Connections to the Charge Time Measurement Unit (CTMU) and Temperature Measurement Diode
- Channel Selection and Triggering can be Controlled by the Peripheral Trigger Generator (PTG)
- External Voltage Reference Input Pins
- Simultaneous Sampling of:
  - Up to four analog input pins
  - Three op amp outputs
  - Combinations of analog inputs and op amp outputs
- Automatic Channel Scan mode
- Selectable Conversion Trigger Source
- Selectable Buffer Fill modes
- Four Result Alignment Options (signed/unsigned, fractional/integer)
- Operation during CPU Sleep and Idle modes

### 23.1.2 12-BIT ADC CONFIGURATION

The 12-bit ADC configuration supports all the features listed above, with the exception of the following:

- In the 12-bit configuration, conversion speeds of up to 500 ksps are supported
- There is only one S&H amplifier in the 12-bit configuration; therefore, simultaneous sampling of multiple channels is not supported

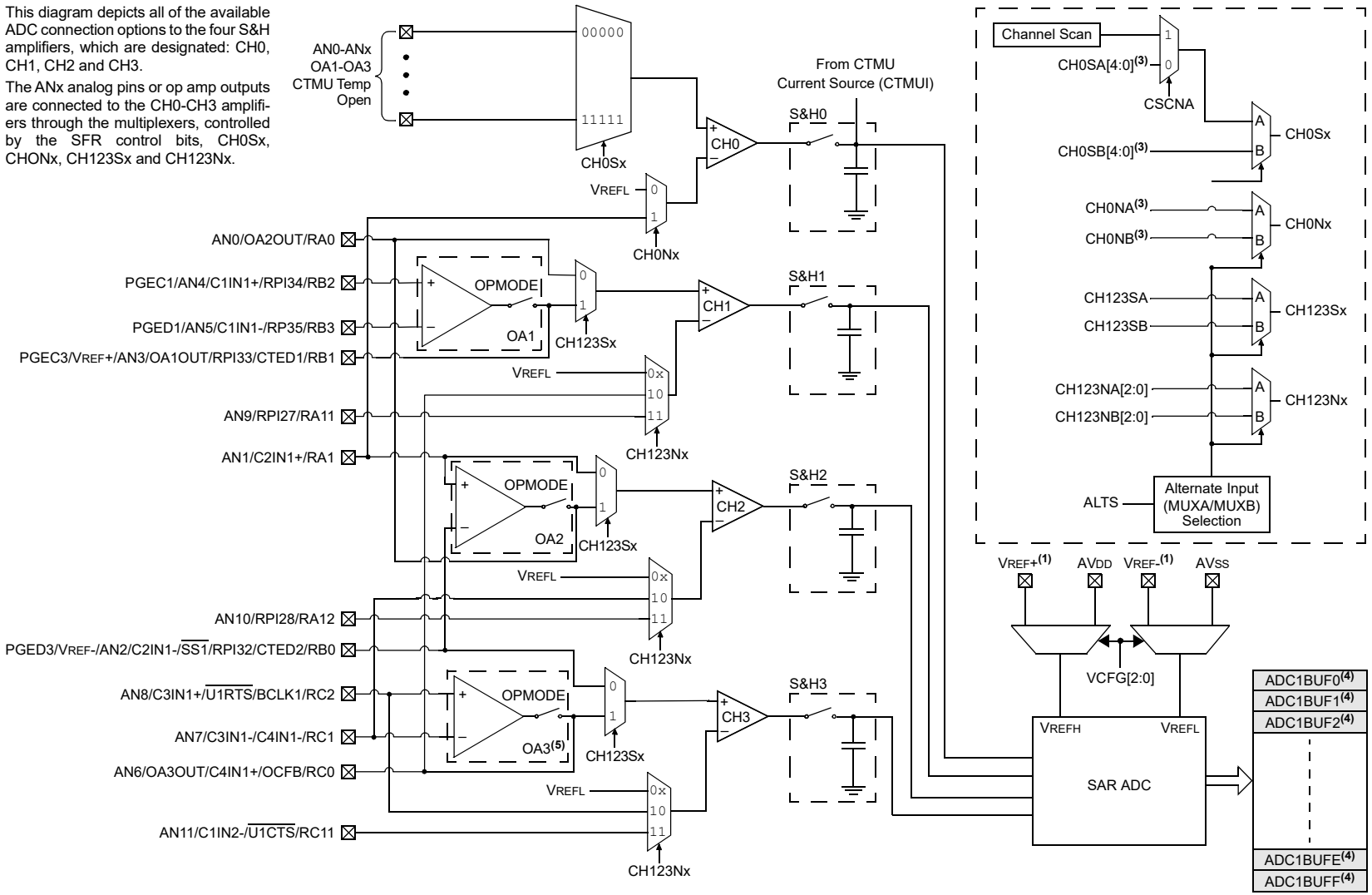
Depending on the particular device pinout, the ADC can have up to 16 analog input pins, designated AN0 through AN15. These analog inputs are shared with op amp inputs and outputs, comparator inputs, and external voltage references. When op amp/comparator functionality is enabled, or an external voltage reference is used, the analog input that shares that pin is no longer available. The actual number of analog input pins, op amps and external voltage reference input configuration depends on the specific device.

A block diagram of the ADC module is shown in Figure 23-1. Figure 23-2 provides a diagram of the ADC conversion clock period.

## FIGURE 23-1: ADC MODULE BLOCK DIAGRAM WITH CONNECTION OPTIONS FOR ANx PINS AND OP AMPS

This diagram depicts all of the available ADC connection options to the four S&H amplifiers, which are designated: CH0, CH1, CH2 and CH3.

The ANx analog pins or op amp outputs are connected to the CH0-CH3 amplifiers through the multiplexers, controlled by the SFR control bits, CH0Sx, CHONx, CH123Sx and CH123Nx.




**Note 1:** VREF+, VREF- inputs can be multiplexed with other analog inputs.
**2:** Channels 1, 2 and 3 are not applicable for the 12-bit mode of operation.
**3:** These bits can be updated with Step commands from the PTG module. See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
**4:** When ADDMAEN (AD1CON4[8]) = 1, enabling DMA, only ADC1BUF0 is used.
**5:** OA3 is not available for 28-pin devices.


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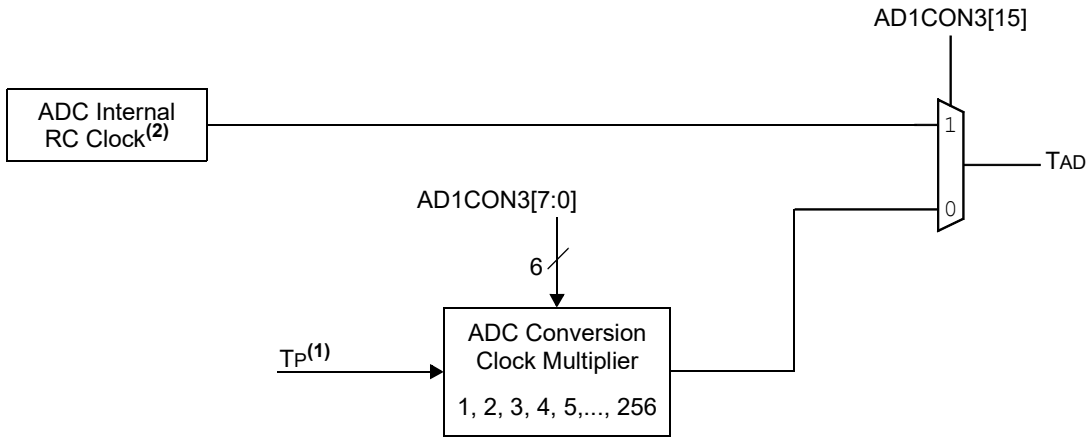
**FIGURE 23-2: ADC CONVERSION CLOCK PERIOD BLOCK DIAGRAM**




**Note 1:** TP = 1/FP.

**2:** See the ADC electrical specifications in **Section 30.0 "Electrical Characteristics"** for the exact RC clock value.

## 23.2 ADC Helpful Tips

1. The SMPIx control bits in the AD1CON2 register:
   a) Determine when the ADC interrupt flag is set and an interrupt is generated, if enabled.
   b) When the CSCNA bit in the AD1CON2 register is set to '1', this determines when the ADC analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
   c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
   d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADC buffer used in this mode. The ADC Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA.
2. When the DMA module is disabled (ADDMAEN = 0), the ADC has 16 result buffers. ADC conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMPIx bits and the condition described in 1c) above. There is no relationship between the ANx input being measured and which ADC buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
3. When the DMA module is enabled (ADDMAEN = 1), the ADC module has only one ADC result buffer (i.e., ADC1BUF0) per ADC peripheral and the ADC conversion result must be read, either by the CPU or DMA Controller, before the next ADC conversion is complete to avoid overwriting the previous value.
4. The DONE bit (AD1CON1[0]) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADC. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (AD1CON1[1]), the DONE bit should also be cleared by the user application just before setting the SAMP bit.
5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for AN0, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use AN0-AN2. Carefully study the ADC block diagram to determine the configuration that will best suit your application. Configuration examples are available in the **"Analog-to-Digital Converter (ADC)"** (www.microchip.com/DS70621) section in the *"dsPIC33/PIC24 Family Reference Manual"*.

## 23.3 ADC Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |
|---|---|

### 23.3.1 KEY RESOURCES

- **"Analog-to-Digital Converter (ADC)"** (www.microchip.com/DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools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## 23.4 ADC Control Registers

**REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADON | — | ADSIDL | ADDMABM | — | AD12B | FORM1 | FORM0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | HC/HS/R/W-0 | HC/HS/R/C-0 |
|---|---|---|---|---|---|---|---|
| SSRC2 | SSRC1 | SSRC0 | SSRCG | SIMSAM | ASAM | SAMP | DONE(3) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HC = Hardware Clearable bit | HS = Hardware Settable bit | C = Clearable bit |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ADON:** ADC1 Operating Mode bit
1 = ADC module is operating
0 = ADC is off

bit 14 **Unimplemented:** Read as '0'

bit 13 **ADSIDL:** ADC1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ADDMABM:** DMA Buffer Build Mode bit
1 = DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer
0 = DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather address to the DMA channel, based on the index of the analog input and the size of the DMA buffer.

bit 11 **Unimplemented:** Read as '0'

bit 10 **AD12B:** ADC1 10-Bit or 12-Bit Operation Mode bit
1 = 12-bit, 1-channel ADC operation
0 = 10-bit, 4-channel ADC operation

bit 9-8 **FORM[1:0]:** Data Output Format bits
For 10-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dd00 0000, where s = .NOT.d[9])
10 = Fractional (DOUT = dddd dddd dd00 0000)
01 = Signed integer (DOUT = ssss sssd dddd dddd, where s = .NOT.d[9])
00 = Integer (DOUT = 0000 00dd dddd dddd)
For 12-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dddd 0000, where s = .NOT.d[11])
10 = Fractional (DOUT = dddd dddd dddd 0000)
01 = Signed integer (DOUT = ssss sddd dddd dddd, where s = .NOT.d[11])
00 = Integer (DOUT = 0000 dddd dddd dddd)

**Note 1:** See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.
**2:** This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
**3:** Do not clear the DONE bit in software if auto-sample is enabled (ASAM = 1).

**REGISTER 23-1: AD1CON1: ADC1 CONTROL REGISTER 1 (CONTINUED)**

bit 7-5 **SSRC[2:0]:** Sample Trigger Source Select bits

If SSRCG = 1:

111 = Reserved
110 = PTGO15 primary trigger compare ends sampling and starts conversion(1)
101 = PTGO14 primary trigger compare ends sampling and starts conversion(1)
100 = PTGO13 primary trigger compare ends sampling and starts conversion(1)
011 = PTGO12 primary trigger compare ends sampling and starts conversion(1)
010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion(2)
001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion(2)
000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion(2)

If SSRCG = 0:

111 = Internal counter ends sampling and starts conversion (auto-convert)
110 = CTMU ends sampling and starts conversion
101 = Reserved
100 = Timer5 compare ends sampling and starts conversion
011 = PWM primary Special Event Trigger ends sampling and starts conversion(2)
010 = Timer3 compare ends sampling and starts conversion
001 = Active transition on the INT0 pin ends sampling and starts conversion
000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)

bit 4 **SSRCG:** Sample Trigger Source Group bit

See SSRC[2:0] for details.

bit 3 **SIMSAM:** Simultaneous Sample Select bit (only applicable when CHPS[1:0] = 01 or 1x)

In 12-bit mode (AD21B = 1), SIMSAM is Unimplemented and is Read as '0':

1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS[1:0] = 1x); or samples CH0 and CH1 simultaneously (when CHPS[1:0] = 01)
0 = Samples multiple channels individually in sequence

bit 2 **ASAM:** ADC1 Sample Auto-Start bit

1 = Sampling begins immediately after the last conversion; SAMP bit is auto-set
0 = Sampling begins when the SAMP bit is set

bit 1 **SAMP:** ADC1 Sample Enable bit

1 = ADC Sample-and-Hold amplifiers are sampling
0 = ADC Sample-and-Hold amplifiers are holding

If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1. If SSRC[2:0] = 000, software can write '0' to end sampling and start conversion. If SSRC[2:0] ≠ 000, automatically cleared by hardware to end sampling and start conversion.

bit 0 **DONE:** ADC1 Conversion Status bit(3)

1 = ADC conversion cycle has completed
0 = ADC conversion has not started or is in progress

Automatically set by hardware when the ADC conversion is complete. Software can write '0' to clear the DONE status bit (software is not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at the start of a new conversion.

**Note 1:** See **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.
**2:** This setting is available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
**3:** Do not clear the DONE bit in software if auto-sample is enabled (ASAM = 1).


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**REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| VCFG2 | VCFG1 | VCFG0 | — | — | CSCNA | CHPS1 | CHPS0 |
| bit 15 | | | | | | | bit 8 |

| R-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| BUFS | SMPI4 | SMPI3 | SMPI2 | SMPI1 | SMPI0 | BUFM | ALTS |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **VCFG[2:0]:** Converter Voltage Reference Configuration bits

| Value | VREFH | VREFL |
|---|---|---|
| 000 | AVDD | AVSS |
| 001 | External VREF+ | AVSS |
| 010 | AVDD | External VREF- |
| 011 | External VREF+ | External VREF- |
| 1xx | AVDD | AVSS |

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **CSCNA:** Input Scan Select bit

1 = Scans inputs for CH0+ during Sample MUXA
0 = Does not scan inputs

bit 9-8 **CHPS[1:0]:** Channel Select bits

In 12-bit mode (AD21B = 1), the CHPS[1:0] bits are Unimplemented and are Read as '0':
1x = Converts CH0, CH1, CH2 and CH3
01 = Converts CH0 and CH1
00 = Converts CH0

bit 7 **BUFS:** Buffer Fill Status bit (only valid when BUFM = 1)

1 = ADC is currently filling the second half of the buffer; the user application should access data in the first half of the buffer
0 = ADC is currently filling the first half of the buffer; the user application should access data in the second half of the buffer

bit 6-2 **SMPI[4:0]:** Increment Rate bits

When ADDMAEN = 0:
x1111 = Generates interrupt after completion of every 16th sample/conversion operation
x1110 = Generates interrupt after completion of every 15th sample/conversion operation
•
•
•
x0001 = Generates interrupt after completion of every 2nd sample/conversion operation
x0000 = Generates interrupt after completion of every sample/conversion operation

When ADDMAEN = 1:
11111 = Increments the DMA address after completion of every 32nd sample/conversion operation
11110 = Increments the DMA address after completion of every 31st sample/conversion operation
•
•
•
00001 = Increments the DMA address after completion of every 2nd sample/conversion operation
00000 = Increments the DMA address after completion of every sample/conversion operation

**REGISTER 23-2: AD1CON2: ADC1 CONTROL REGISTER 2 (CONTINUED)**

bit 1 **BUFM:** Buffer Fill Mode Select bit
1 = Starts the buffer filling the first half of the buffer on the first interrupt and the second half of the buffer on next interrupt
0 = Always starts filling the buffer from the start address

bit 0 **ALTS:** Alternate Input Sample Mode Select bit
1 = Uses channel input selects for Sample MUXA on first sample and Sample MUXB on next sample
0 = Always uses channel input selects for Sample MUXA


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**REGISTER 23-3: AD1CON3: ADC1 CONTROL REGISTER 3**

| R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADRC | — | — | SAMC[4:0](1) | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADCS[7:0](2) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ADRC:** ADC1 Conversion Clock Source bit
1 = ADC internal RC clock
0 = Clock derived from system clock

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **SAMC[4:0]:** Auto-Sample Time bits(1)
11111 = 31 TAD
•
•
•
00001 = 1 TAD
00000 = 0 TAD

bit 7-0 **ADCS[7:0]:** ADC1 Conversion Clock Select bits(2)
11111111 = TP • (ADCS[7:0] + 1) = TP •256 = TAD
•
•
•
00000010 = TP • (ADCS[7:0] + 1) = TP •3 = TAD
00000001 = TP • (ADCS[7:0] + 1) = TP •2 = TAD
00000000 = TP • (ADCS[7:0] + 1) = TP •1 = TAD

**Note 1:** This bit is only used if SSRC[2:0] (AD1CON1[7:5]) = 111 and SSRCG (AD1CON1[4]) = 0.
**2:** This bit is not used if ADRC (AD1CON3[15]) = 1.

**REGISTER 23-4: AD1CON4: ADC1 CONTROL REGISTER 4**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | ADDMAEN |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | DMABL[2:0] | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **ADDMAEN:** ADC1 DMA Enable bit
1 = Conversion results are stored in the ADC1BUF0 register for transfer to RAM using DMA
0 = Conversion results are stored in ADC1BUF0 through ADC1BUFF registers; DMA will not be used

bit 7-3 **Unimplemented:** Read as '0'

bit 2-0 **DMABL[2:0]:** Selects Number of DMA Buffer Locations per Analog Input bits
111 = Allocates 128 words of buffer to each analog input
110 = Allocates 64 words of buffer to each analog input
101 = Allocates 32 words of buffer to each analog input
100 = Allocates 16 words of buffer to each analog input
011 = Allocates 8 words of buffer to each analog input
010 = Allocates 4 words of buffer to each analog input
001 = Allocates 2 words of buffer to each analog input
000 = Allocates 1 word of buffer to each analog input


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**REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNELS 1, 2, 3 SELECT REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | CH123NB1 | CH123NB0 | CH123SB |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | CH123NA1 | CH123NA0 | CH123SA |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-11 **Unimplemented:** Read as '0'

bit 10-9 **CH123NB[1:0]:** Channel 1, 2, 3 Negative Input Select for Sample MUXB bits

In 12-Bit Mode (AD21B = 1), CH123NB is Unimplemented and is Read as '0':

| Value | ADC Channel | | |
|---|---|---|---|
| | CH1 | CH2 | CH3 |
| 11 | AN9 | AN10 | AN11 |
| 10(1,2) | OA3/AN6 | AN7 | AN8 |
| 0x | VREFL | VREFL | VREFL |

bit 8 **CH123SB:** Channel 1, 2, 3 Positive Input Select for Sample MUXB bit

In 12-Bit Mode (AD21B = 1), CH123SB is Unimplemented and is Read as '0':

| Value | ADC Channel | | |
|---|---|---|---|
| | CH1 | CH2 | CH3 |
| 1(2) | OA1/AN3 | OA2/AN0 | OA3/AN6 |
| 0(1,2) | OA2/AN0 | AN1 | AN2 |

bit 7-3 **Unimplemented:** Read as '0'

bit 2-1 **CH123NA[1:0]:** Channel 1, 2, 3 Negative Input Select for Sample MUXA bits

In 12-Bit Mode (AD21B = 1), CH123NA is Unimplemented and is Read as '0':

| Value | ADC Channel | | |
|---|---|---|---|
| | CH1 | CH2 | CH3 |
| 11 | AN9 | AN10 | AN11 |
| 10(1,2) | OA3/AN6 | AN7 | AN8 |
| 0x | VREFL | VREFL | VREFL |

**Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

**2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON[10]) = 1); otherwise, the ANx input is used.

**REGISTER 23-5: AD1CHS123: ADC1 INPUT CHANNELS 1, 2, 3 SELECT REGISTER (CONTINUED)**

bit 0 **CH123SA:** Channel 1, 2, 3 Positive Input Select for Sample MUXA bit

In 12-bit mode (AD21B = 1), CH123SA is Unimplemented and is Read as '0':

| Value | ADC Channel | | |
|---|---|---|---|
| | CH1 | CH2 | CH3 |
| 1(2) | OA1/AN3 | OA2/AN0 | OA3/AN6 |
| 0(1,2) | OA2/AN0 | AN1 | AN2 |

**Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

**2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON[10]) = 1); otherwise, the ANx input is used.


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**REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER**

| R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CH0NB | — | — | CH0SB[4:0](1) | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CH0NA | — | — | CH0SA[4:0](1) | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample MUXB bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 14-13 **Unimplemented:** Read as '0'

bit 12-8 **CH0SB[4:0]:** Channel 0 Positive Input Select for Sample MUXB bits(1)
11111 = Open; use this selection with CTMU capacitive and time measurement
11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
11101 = Reserved
11100 = Reserved
11011 = Reserved
11010 = Channel 0 positive input is the output of OA3/AN6(2,3)
11001 = Channel 0 positive input is the output of OA2/AN0(2)
11000 = Channel 0 positive input is the output of OA1/AN3(2)
10111 = Reserved
•
•
•
10000 = Reserved
01111 = Channel 0 positive input is AN15(3)
01110 = Channel 0 positive input is AN14(3)
01101 = Channel 0 positive input is AN13(3)
•
•
•
00010 = Channel 0 positive input is AN2(3)
00001 = Channel 0 positive input is AN1(3)
00000 = Channel 0 positive input is AN0(3)

bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample MUXA bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 6-5 **Unimplemented:** Read as '0'

**Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

**2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON[10]) = 1); otherwise, the ANx input is used.

**3:** See the **"Pin Diagrams"** section for the available analog channels for each device.

**REGISTER 23-6: AD1CHS0: ADC1 INPUT CHANNEL 0 SELECT REGISTER (CONTINUED)**

bit 4-0 **CH0SA[4:0]:** Channel 0 Positive Input Select for Sample MUXA bits(1)

11111 = Open; use this selection with CTMU capacitive and time measurement
11110 = Channel 0 positive input is connected to the CTMU temperature measurement diode (CTMU TEMP)
11101 = Reserved
11100 = Reserved
11011 = Reserved
11010 = Channel 0 positive input is the output of OA3/AN6(2,3)
11001 = Channel 0 positive input is the output of OA2/AN0(2)
11000 = Channel 0 positive input is the output of OA1/AN3(2)
10110 = Reserved
•
•
•
10000 = Reserved
01111 = Channel 0 positive input is AN15(1,3)
01110 = Channel 0 positive input is AN14(1,3)
01101 = Channel 0 positive input is AN13(1,3)
•
•
•
00010 = Channel 0 positive input is AN2(1,3)
00001 = Channel 0 positive input is AN1(1,3)
00000 = Channel 0 positive input is AN0(1,3)

**Note 1:** AN0 through AN7 are repurposed when comparator and op amp functionality is enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

**2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON[10]) = 1); otherwise, the ANx input is used.

**3:** See the **"Pin Diagrams"** section for the available analog channels for each device.


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**REGISTER 23-7: AD1CSSH: ADC1 INPUT SCAN SELECT REGISTER HIGH(1)**

| R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSS31 | CSS30 | — | — | — | CSS26(2) | CSS25(2) | CSS24(2) |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CSS31:** ADC1 Input Scan Selection bit
1 = Selects CTMU capacitive and time measurement for input scan (Open)
0 = Skips CTMU capacitive and time measurement for input scan (Open)

bit 14 **CSS30:** ADC1 Input Scan Selection bit
1 = Selects CTMU on-chip temperature measurement for input scan (CTMU TEMP)
0 = Skips CTMU on-chip temperature measurement for input scan (CTMU TEMP)

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **CSS26:** ADC1 Input Scan Selection bit(2)
1 = Selects OA3/AN6 for input scan
0 = Skips OA3/AN6 for input scan

bit 9 **CSS25:** ADC1 Input Scan Selection bit(2)
1 = Selects OA2/AN0 for input scan
0 = Skips OA2/AN0 for input scan

bit 8 **CSS24:** ADC1 Input Scan Selection bit(2)
1 = Selects OA1/AN3 for input scan
0 = Skips OA1/AN3 for input scan

bit 7-0 **Unimplemented:** Read as '0'

**Note 1:** All AD1CSSH bits can be selected by user software. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

**2:** The OAx input is used if the corresponding op amp is selected (OPMODE (CMxCON[10]) = 1); otherwise, the ANx input is used.

**REGISTER 23-8: AD1CSSL: ADC1 INPUT SCAN SELECT REGISTER LOW(1,2,3)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSS[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CSS[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **CSS[15:0]:** ADC1 Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

**Note 1:** On devices with less than 16 analog inputs, all AD1CSSL bits can be selected by the user. However, inputs selected for scan, without a corresponding input on the device, convert VREFL.

**2:** CSSx = ANx, where x = 0-15. The outputs for Op Amps 1, 2 and 3 can be scanned by selecting analog inputs, AN3, AN0 and AN6, respectively.

**3:** For analog inputs that have op amp output function (OAxOUT), op amp output can be accessed for input scan if the corresponding op amp is selected (OPMODE (CMxCON[10[) = 1); otherwise, the ANx input is used.


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# 24.0 PERIPHERAL TRIGGER GENERATOR (PTG) MODULE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Peripheral Trigger Generator (PTG)"** (www.microchip.com/DS70000669) in the *"dsPIC33/PIC24 Family Reference Manual"*.

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

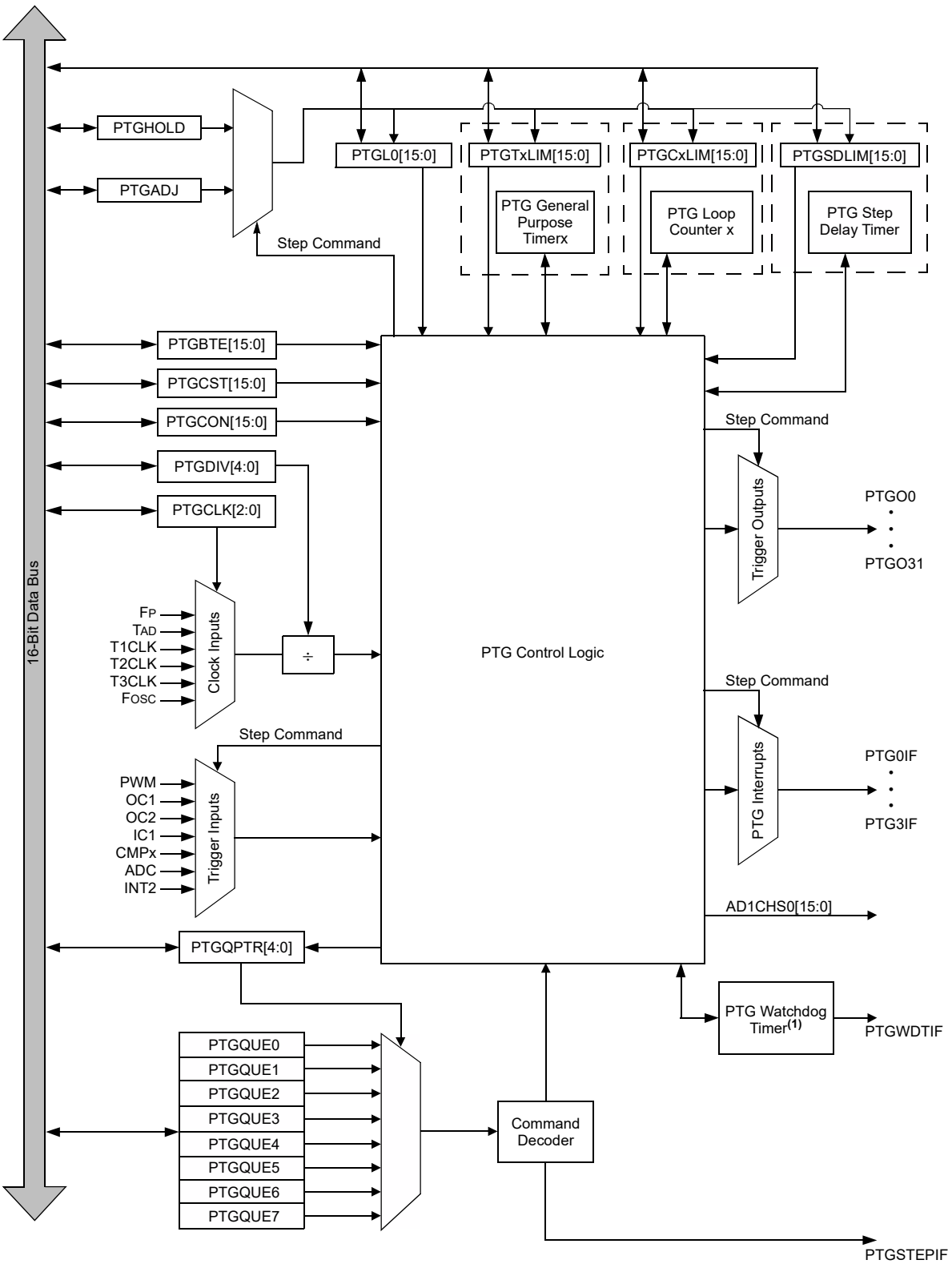
## 24.1 Module Introduction

The Peripheral Trigger Generator (PTG) provides a means to schedule complex high-speed peripheral operations that would be difficult to achieve using software. The PTG module uses 8-bit commands, called "Steps", that the user writes to the PTG Queue registers (PTGQUE0-PTGQUE7). The registers perform operations, such as wait for input signal, generate output trigger and wait for timer.

The PTG module has the following major features:

- Multiple Clock Sources
- Two 16-Bit General Purpose Timers
- Two 16-Bit General Limit Counters
- Configurable for Rising or Falling Edge Triggering
- Generates Processor Interrupts to Include:
  - Four configurable processor interrupts
  - Interrupt on a Step event in Single-Step mode
  - Interrupt on a PTG Watchdog Timer time-out
- Able to Receive Trigger Signals from these Peripherals:
  - ADC
  - PWM
  - Output Compare
  - Input Capture
  - Op Amp/Comparator
  - INT2
- Able to Trigger or Synchronize to these Peripherals:
  - Watchdog Timer
  - Output Compare
  - Input Capture
  - ADC
  - PWM
  - Op Amp/Comparator

**FIGURE 24-1: PTG BLOCK DIAGRAM**




**Note 1:** This is a dedicated Watchdog Timer for the PTG module and is independent of the device Watchdog Timer.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## 24.2 PTG Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| | |
|---|---|
| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464 |

### 24.2.1 KEY RESOURCES

- **"Peripheral Trigger Generator"** (www.microchip.com/DS70000669) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 24.3 PTG Control Registers

**REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGEN | — | PTGSIDL | PTGTOGL | — | PTGSWT(2) | PTGSSEN(3) | PTGIVIS |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | HS-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGSTRT | PTGWDTO | — | — | — | — | PTGITM1(1) | PTGITM0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PTGEN:** Module Enable bit
1 = PTG module is enabled
0 = PTG module is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **PTGSIDL:** PTG Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **PTGTOGL:** PTG TRIG Output Toggle Mode bit
1 = Toggles state of the PTGOx for each execution of the PTGTRIG command
0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits

bit 11 **Unimplemented:** Read as '0'

bit 10 **PTGSWT:** PTG Software Trigger bit(2)
1 = Triggers the PTG module
0 = No action (clearing this bit will have no effect)

bit 9 **PTGSSEN:** PTG Enable Single-Step bit(3)
1 = Enables Single-Step mode
0 = Disables Single-Step mode

bit 8 **PTGIVIS:** PTG Counter/Timer Visibility Control bit
1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding counter/timer registers (PTGSD, PTGCx, PTGTx)
0 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those limit registers

bit 7 **PTGSTRT:** PTG Start Sequencer bit
1 = Starts to sequentially execute commands (Continuous mode)
0 = Stops executing commands

bit 6 **PTGWDTO:** PTG Watchdog Timer Time-out Status bit
1 = PTG Watchdog Timer has timed out
0 = PTG Watchdog Timer has not timed out

bit 5-2 **Unimplemented:** Read as '0'

**Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.
**2:** This bit is only used with the PTGCTRL Step command software trigger option.
**3:** Use of the PTG Single-Step mode is reserved for debugging tools only.


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**REGISTER 24-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)**

bit 1-0 **PTGITM[1:0]:** PTG Input Trigger Command Operating Mode bits(1)

11 = Single level detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
10 = Single level detect with Step delay executed on exit of command
01 = Continuous edge detect with Step delay not executed on exit of command (regardless of the PTGCTRL command)
00 = Continuous edge detect with Step delay executed on exit of command

**Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.

**2:** This bit is only used with the PTGCTRL Step command software trigger option.

**3:** Use of the PTG Single-Step mode is reserved for debugging tools only.

**REGISTER 24-2: PTGCON: PTG CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGCLK2 | PTGCLK1 | PTGCLK0 | PTGDIV4 | PTGDIV3 | PTGDIV2 | PTGDIV1 | PTGDIV0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGPWD3 | PTGPWD2 | PTGPWD1 | PTGPWD0 | — | PTGWDT2 | PTGWDT1 | PTGWDT0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-13 **PTGCLK[2:0]:** Select PTG Module Clock Source bits
111 = Reserved
110 = Reserved
101 = PTG module clock source will be T3CLK
100 = PTG module clock source will be T2CLK
011 = PTG module clock source will be T1CLK
010 = PTG module clock source will be TAD
001 = PTG module clock source will be FOSC
000 = PTG module clock source will be FP

bit 12-8 **PTGDIV[4:0]:** PTG Module Clock Prescaler (divider) bits
11111 = Divide-by-32
11110 = Divide-by-31
•
•
•
00001 = Divide-by-2
00000 = Divide-by-1

bit 7-4 **PTGPWD[3:0]:** PTG Trigger Output Pulse-Width bits
1111 = All trigger outputs are 16 PTG clock cycles wide
1110 = All trigger outputs are 15 PTG clock cycles wide
•
•
•
0001 = All trigger outputs are 2 PTG clock cycles wide
0000 = All trigger outputs are 1 PTG clock cycle wide

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **PTGWDT[2:0]:** Select PTG Watchdog Timer Time-out Count Value bits
111 = Watchdog Timer will time-out after 512 PTG clocks
110 = Watchdog Timer will time-out after 256 PTG clocks
101 = Watchdog Timer will time-out after 128 PTG clocks
100 = Watchdog Timer will time-out after 64 PTG clocks
011 = Watchdog Timer will time-out after 32 PTG clocks
010 = Watchdog Timer will time-out after 16 PTG clocks
001 = Watchdog Timer will time-out after 8 PTG clocks
000 = Watchdog Timer is disabled


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**REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER(1,2)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| ADCTS4 | ADCTS3 | ADCTS2 | ADCTS1 | IC4TSS | IC3TSS | IC2TSS | IC1TSS |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| OC4CS | OC3CS | OC2CS | OC1CS | OC4TSS | OC3TSS | OC2TSS | OC1TSS |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ADCTS4:** Sample Trigger PTGO15 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed

bit 14 **ADCTS3:** Sample Trigger PTGO14 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed

bit 13 **ADCTS2:** Sample Trigger PTGO13 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed

bit 12 **ADCTS1:** Sample Trigger PTGO12 for ADC bit
1 = Generates Trigger when the broadcast command is executed
0 = Does not generate Trigger when the broadcast command is executed

bit 11 **IC4TSS:** Trigger/Synchronization Source for IC4 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 10 **IC3TSS:** Trigger/Synchronization Source for IC3 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 9 **IC2TSS:** Trigger/Synchronization Source for IC2 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 8 **IC1TSS:** Trigger/Synchronization Source for IC1 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 7 **OC4CS:** Clock Source for OC4 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 6 **OC3CS:** Clock Source for OC3 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 5 **OC2CS:** Clock Source for OC2 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**2:** This register is only used with the PTGCTRL OPTION = 1111 Step command.

**REGISTER 24-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER(1,2) (CONTINUED)**

bit 4 **OC1CS:** Clock Source for OC1 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 3 **OC4TSS:** Trigger/Synchronization Source for OC4 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 2 **OC3TSS:** Trigger/Synchronization Source for OC3 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 1 **OC2TSS:** Trigger/Synchronization Source for OC2 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

bit 0 **OC1TSS:** Trigger/Synchronization Source for OC1 bit
1 = Generates Trigger/Synchronization when the broadcast command is executed
0 = Does not generate Trigger/Synchronization when the broadcast command is executed

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**2:** This register is only used with the PTGCTRL OPTION = 1111 Step command.


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**REGISTER 24-4: PTGT0LIM: PTG TIMER0 LIMIT REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGT0LIM[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGT0LIM[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTGT0LIM[15:0]:** PTG Timer0 Limit Register bits
General Purpose Timer0 Limit register (effective only with a `PTGT0` Step command).

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = `1` and PTGSTRT = `1`).

**REGISTER 24-5: PTGT1LIM: PTG TIMER1 LIMIT REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGT1LIM[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGT1LIM[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTGT1LIM[15:0]:** PTG Timer1 Limit Register bits
General Purpose Timer1 Limit register (effective only with a `PTGT1` Step command).

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = `1` and PTGSTRT = `1`).

**REGISTER 24-6: PTGSDLIM: PTG STEP DELAY LIMIT REGISTER(1,2)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGSDLIM[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGSDLIM[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTGSDLIM[15:0]:** PTG Step Delay Limit Register bits
Holds a PTG Step delay value representing the number of additional PTG clocks between the start of a Step command and the completion of a Step command.

**Note 1:** A base Step delay of one PTG clock is added to any value written to the PTGSDLIM register (Step Delay = (PTGSDLIM) + 1).

**2:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**REGISTER 24-7: PTGC0LIM: PTG COUNTER 0 LIMIT REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGC0LIM[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGC0LIM[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTGC0LIM[15:0]:** PTG Counter 0 Limit Register bits
May be used to specify the loop count for the PTGJMPC0 Step command or as a limit register for the General Purpose Counter 0.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).


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**REGISTER 24-8: PTGC1LIM: PTG COUNTER 1 LIMIT REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGC1LIM[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGC1LIM[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTGC1LIM[15:0]:** PTG Counter 1 Limit Register bits
May be used to specify the loop count for the `PTGJMPC1` Step command or as a limit register for the General Purpose Counter 1.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = `1` and PTGSTRT = `1`).

**REGISTER 24-9: PTGHOLD: PTG HOLD REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGHOLD[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGHOLD[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTGHOLD[15:0]:** PTG General Purpose Hold Register bits
Holds user-supplied data to be copied to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the `PTGCOPY` command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = `1` and PTGSTRT = `1`).

**REGISTER 24-10: PTGADJ: PTG ADJUST REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGADJ[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGADJ[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTGADJ[15:0]:** PTG Adjust Register bits
This register holds user-supplied data to be added to the PTGTxLIM, PTGCxLIM, PTGSDLIM or PTGL0 registers with the `PTGADD` command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = `1` and PTGSTRT = `1`).

**REGISTER 24-11: PTGL0: PTG LITERAL 0 REGISTER(1)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGL0[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGL0[7:0] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **PTGL0[15:0]:** PTG Literal 0 Register bits
This register holds the 16-bit value to be written to the AD1CHS0 register with the `PTGCTRL` Step command.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = `1` and PTGSTRT = `1`).


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**REGISTER 24-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER(1)**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | PTGQPTR[4:0] | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **PTGQPTR[4:0]:** PTG Step Queue Pointer Register bits
This register points to the currently active Step command in the Step queue.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**REGISTER 24-13: PTGQUEx: PTG STEP QUEUE REGISTER x (x = 0-7)(1,3)**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STEP(2x + 1)[7:0](2) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| STEP(2x)[7:0](2) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **STEP(2x + 1)[7:0]:** PTG Step Queue Pointer Register bits(2)
A queue location for storage of the STEP(2x + 1) command byte.

bit 7-0 **STEP(2x)[7:0]:** PTG Step Queue Pointer Register bits(2)
A queue location for storage of the STEP(2x) command byte.

**Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

**2:** Refer to Table 24-1 for the Step command encoding.

**3:** The Step registers maintain their values on any type of Reset.

## 24.4 Step Commands and Format

**TABLE 24-1: PTG STEP COMMAND FORMAT**

| Step Command Byte: | | | |
|---|---|---|---|
| STEPx[7:0] | | | |
| CMD[3:0] | | OPTION[3:0] | |
| bit 7 | bit 4 | bit 3 | bit 0 |

| bit 7-4 | CMD[3:0] | Step Command | Command Description |
|---|---|---|---|
| | 0000 | PTGCTRL | Execute control command as described by OPTION[3:0]. |
| | 0001 | PTGADD | Add contents of PTGADJ register to target register as described by OPTION[3:0]. |
| | | PTGCOPY | Copy contents of PTGHOLD register to target register as described by OPTION[3:0]. |
| | 001x | PTGSTRB | Copy the value contained in CMD[0]:OPTION[3:0] to the CH0SA[4:0] bits (AD1CHS0[4:0]). |
| | 0100 | PTGWHI | Wait for a low-to-high edge input from the selected PTG trigger input as described by OPTION[3:0]. |
| | 0101 | PTGWLO | Wait for a high-to-low edge input from the selected PTG trigger input as described by OPTION[3:0]. |
| | 0110 | Reserved | Reserved. |
| | 0111 | PTGIRQ | Generate individual interrupt request as described by OPTION3[:0]. |
| | 100x | PTGTRIG | Generate individual trigger output as described by <<CMD[0]:OPTION[3:0]>. |
| | 101x | PTGJMP | Copy the value indicated in <<CMD[0]:OPTION[3:0]> to the Queue Pointer (PTGQPTR) and jump to that Step queue. |
| | 110x | PTGJMPC0 | PTGC0 = PTGC0LIM: Increment the Queue Pointer (PTGQPTR). |
| | | | PTGC0 ≠ PTGC0LIM: Increment Counter 0 (PTGC0) and copy the value indicated in <<CMD[0]:OPTION[3:0]> to the Queue Pointer (PTGQPTR), and jump to that Step queue |
| | 111x | PTGJMPC1 | PTGC1 = PTGC1LIM: Increment the Queue Pointer (PTGQPTR). |
| | | | PTGC1 ≠ PTGC1LIM: Increment Counter 1 (PTGC1) and copy the value indicated in <<CMD[0]:OPTION[3:0]> to the Queue Pointer (PTGQPTR), and jump to that Step queue. |

**Note 1:** All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

**2:** Refer to Table 24-2 for the trigger output descriptions.

**3:** This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.


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**TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)**

| bit 3-0 | Step Command | OPTION[3:0] | Option Description |
|---|---|---|---|
| | PTGCTRL(1) | 0000 | Reserved. |
| | | 0001 | Reserved. |
| | | 0010 | Disable Step Delay Timer (PTGSD). |
| | | 0011 | Reserved. |
| | | 0100 | Reserved. |
| | | 0101 | Reserved. |
| | | 0110 | Enable Step Delay Timer (PTGSD). |
| | | 0111 | Reserved. |
| | | 1000 | Start and wait for the PTG Timer0 to match the Timer0 Limit Register. |
| | | 1001 | Start and wait for the PTG Timer1 to match the Timer1 Limit Register. |
| | | 1010 | Reserved. |
| | | 1011 | Wait for the software trigger bit transition from low-to-high before continuing (PTGSWT = 0 to 1). |
| | | 1100 | Copy contents of the Counter 0 register to the AD1CHS0 register. |
| | | 1101 | Copy contents of the Counter 1 register to the AD1CHS0 register. |
| | | 1110 | Copy contents of the Literal 0 register to the AD1CHS0 register. |
| | | 1111 | Generate triggers indicated in the Broadcast Trigger Enable register (PTGBTE). |
| | PTGADD(1) | 0000 | Add contents of the PTGADJ register to the Counter 0 Limit register (PTGC0LIM). |
| | | 0001 | Add contents of the PTGADJ register to the Counter 1 Limit register (PTGC1LIM). |
| | | 0010 | Add contents of the PTGADJ register to the Timer0 Limit register (PTGT0LIM). |
| | | 0011 | Add contents of the PTGADJ register to the Timer1 Limit register (PTGT1LIM). |
| | | 0100 | Add contents of the PTGADJ register to the Step Delay Limit register (PTGSDLIM). |
| | | 0101 | Add contents of the PTGADJ register to the Literal 0 register (PTGL0). |
| | | 0110 | Reserved. |
| | | 0111 | Reserved. |
| | PTGCOPY(1) | 1000 | Copy contents of the PTGHOLD register to the Counter 0 Limit register (PTGC0LIM). |
| | | 1001 | Copy contents of the PTGHOLD register to the Counter 1 Limit register (PTGC1LIM). |
| | | 1010 | Copy contents of the PTGHOLD register to the Timer0 Limit register (PTGT0LIM). |
| | | 1011 | Copy contents of the PTGHOLD register to the Timer1 Limit register (PTGT1LIM). |
| | | 1100 | Copy contents of the PTGHOLD register to the Step Delay Limit register (PTGSDLIM). |
| | | 1101 | Copy contents of the PTGHOLD register to the Literal 0 register (PTGL0). |
| | | 1110 | Reserved. |
| | | 1111 | Reserved. |

**Note 1:** All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

**2:** Refer to Table 24-2 for the trigger output descriptions.

**3:** This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**TABLE 24-1: PTG STEP COMMAND FORMAT (CONTINUED)**

| bit 3-0 | Step Command | OPTION[3:0] | Option Description |
|---|---|---|---|
| | PTGWHI[1] or PTGWLO[1] | 0000 | PWM Special Event Trigger.[3] |
| | | 0001 | PWM master time base synchronization output.[3] |
| | | 0010 | PWM1 interrupt.[3] |
| | | 0011 | PWM2 interrupt.[3] |
| | | 0100 | PWM3 interrupt.[3] |
| | | 0101 | Reserved. |
| | | 0110 | Reserved. |
| | | 0111 | OC1 Trigger event. |
| | | 1000 | OC2 Trigger event. |
| | | 1001 | IC1 Trigger event. |
| | | 1010 | CMP1 Trigger event. |
| | | 1011 | CMP2 Trigger event. |
| | | 1100 | CMP3 Trigger event. |
| | | 1101 | CMP4 Trigger event. |
| | | 1110 | ADC conversion done interrupt. |
| | | 1111 | INT2 external interrupt. |
| | PTGIRQ[1] | 0000 | Generate PTG Interrupt 0. |
| | | 0001 | Generate PTG Interrupt 1. |
| | | 0010 | Generate PTG Interrupt 2. |
| | | 0011 | Generate PTG Interrupt 3. |
| | | 0100 | Reserved. |
| | | • • • | • • • |
| | | 1111 | Reserved. |
| | PTGTRIG[2] | 00000 | PTGO0. |
| | | 00001 | PTGO1. |
| | | • • • | • • • |
| | | 11110 | PTGO30. |
| | | 11111 | PTGO31. |

**Note 1:** All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

**2:** Refer to Table 24-2 for the trigger output descriptions.

**3:** This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.


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**TABLE 24-2: PTG OUTPUT DESCRIPTIONS**

| PTG Output Number | PTG Output Description |
|---|---|
| PTGO0 | Trigger/Synchronization Source for OC1 |
| PTGO1 | Trigger/Synchronization Source for OC2 |
| PTGO2 | Trigger/Synchronization Source for OC3 |
| PTGO3 | Trigger/Synchronization Source for OC4 |
| PTGO4 | Clock Source for OC1 |
| PTGO5 | Clock Source for OC2 |
| PTGO6 | Clock Source for OC3 |
| PTGO7 | Clock Source for OC4 |
| PTGO8 | Trigger/Synchronization Source for IC1 |
| PTGO9 | Trigger/Synchronization Source for IC2 |
| PTGO10 | Trigger/Synchronization Source for IC3 |
| PTGO11 | Trigger/Synchronization Source for IC4 |
| PTGO12 | Sample Trigger for ADC |
| PTGO13 | Sample Trigger for ADC |
| PTGO14 | Sample Trigger for ADC |
| PTGO15 | Sample Trigger for ADC |
| PTGO16 | PWM Time Base Synchronous Source for PWM(1) |
| PTGO17 | PWM Time Base Synchronous Source for PWM(1) |
| PTGO18 | Mask Input Select for Op Amp/Comparator |
| PTGO19 | Mask Input Select for Op Amp/Comparator |
| PTGO20 | Reserved |
| PTGO21 | Reserved |
| PTGO22 | Reserved |
| PTGO23 | Reserved |
| PTGO24 | Reserved |
| PTGO25 | Reserved |
| PTGO26 | Reserved |
| PTGO27 | Reserved |
| PTGO28 | Reserved |
| PTGO29 | Reserved |
| PTGO30 | PTG Output to PPS Input Selection |
| PTGO31 | PTG Output to PPS Input Selection |

**Note 1:** This feature is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**NOTES:**


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## 25.0 OP AMP/COMPARATOR MODULE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Op Amp/Comparator"** (www.microchip.com/DS70000357) in the *"dsPIC33/PIC24 Family Reference Manual"*.

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain up to four comparators, which can be configured in various ways. Comparators, CMP1, CMP2 and CMP3, also have the option to be configured as op amps, with the output being brought to an external pin for gain/filtering connections. As shown in Figure 25-1, individual comparator options are specified by the comparator module's Special Function Register (SFR) control bits.

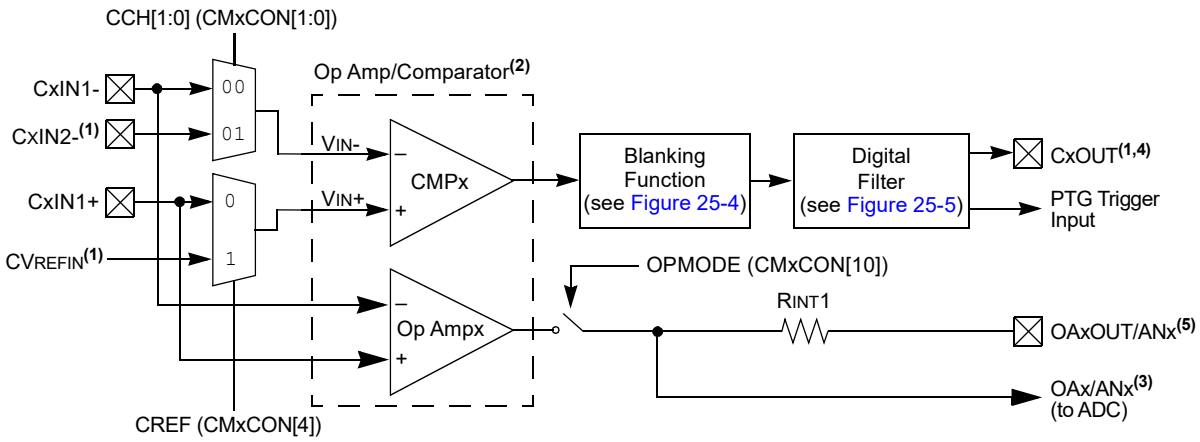
**Note:** Op Amp/Comparator 3 is not available on the dsPIC33EPXXXGP502/MC502/MC202 and PIC24EP256GP/MC202 (28-pin) devices.

These options allow users to:

- Select the edge for trigger and interrupt generation
- Configure the comparator voltage reference
- Configure output blanking and masking
- Configure as a comparator or op amp (CMP1, CMP2 and CMP3 only)

**Note:** Not all op amp/comparator input/output connections are available on all devices. See the **"Pin Diagrams"** section for available connections.

**FIGURE 25-1: OP AMP/COMPARATOR x MODULE BLOCK DIAGRAM (MODULES 1, 2 AND 3)**




**Note 1:** This input/output is not available as a selection when configured as an op amp (OPMODE (CMxCON[10]) = 1).

**2:** This module can be configured either as an op amp or a comparator using the OPMODE bit.

**3:** When configured as an op amp (OPMODE = 1), the ADC samples the op amp output; otherwise, the ADC samples the ANx pin.

**4:** CxOUT is not a predefined pin; instead, it must be mapped to a physical pin using Peripheral Pin Select.

**5:** In order to use the op amp function, OAxOUT/ANx, on the relevant pin, set the corresponding TRISx bit to '1' and the ANSELx bit to '1'.

**FIGURE 25-2: COMPARATOR MODULE BLOCK DIAGRAM (MODULE 4)**

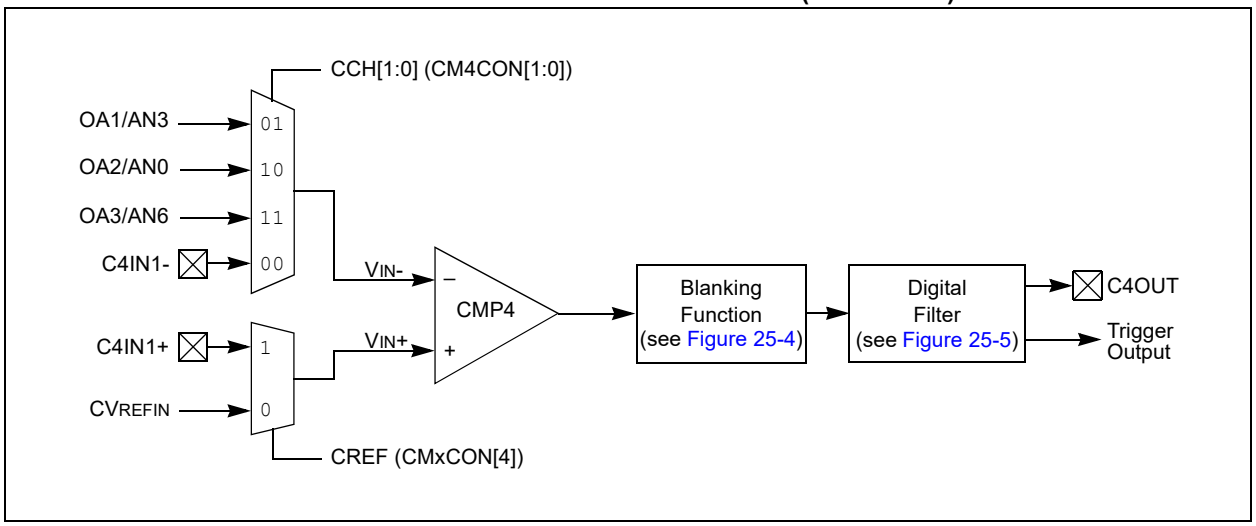
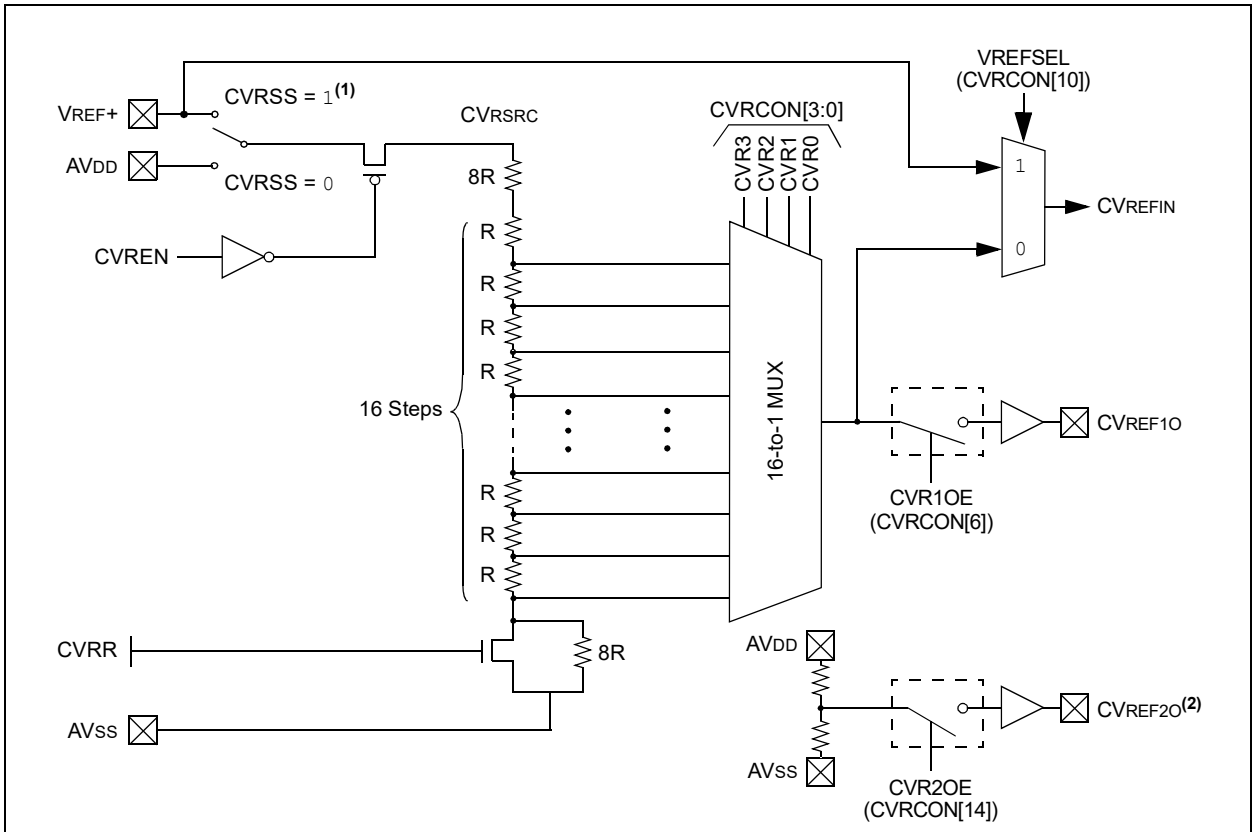



**FIGURE 25-3: OP AMP/COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM**




**Note 1:** In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.

**2:** This reference is (AVDD + AVSS)/2.


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**FIGURE 25-4: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM**

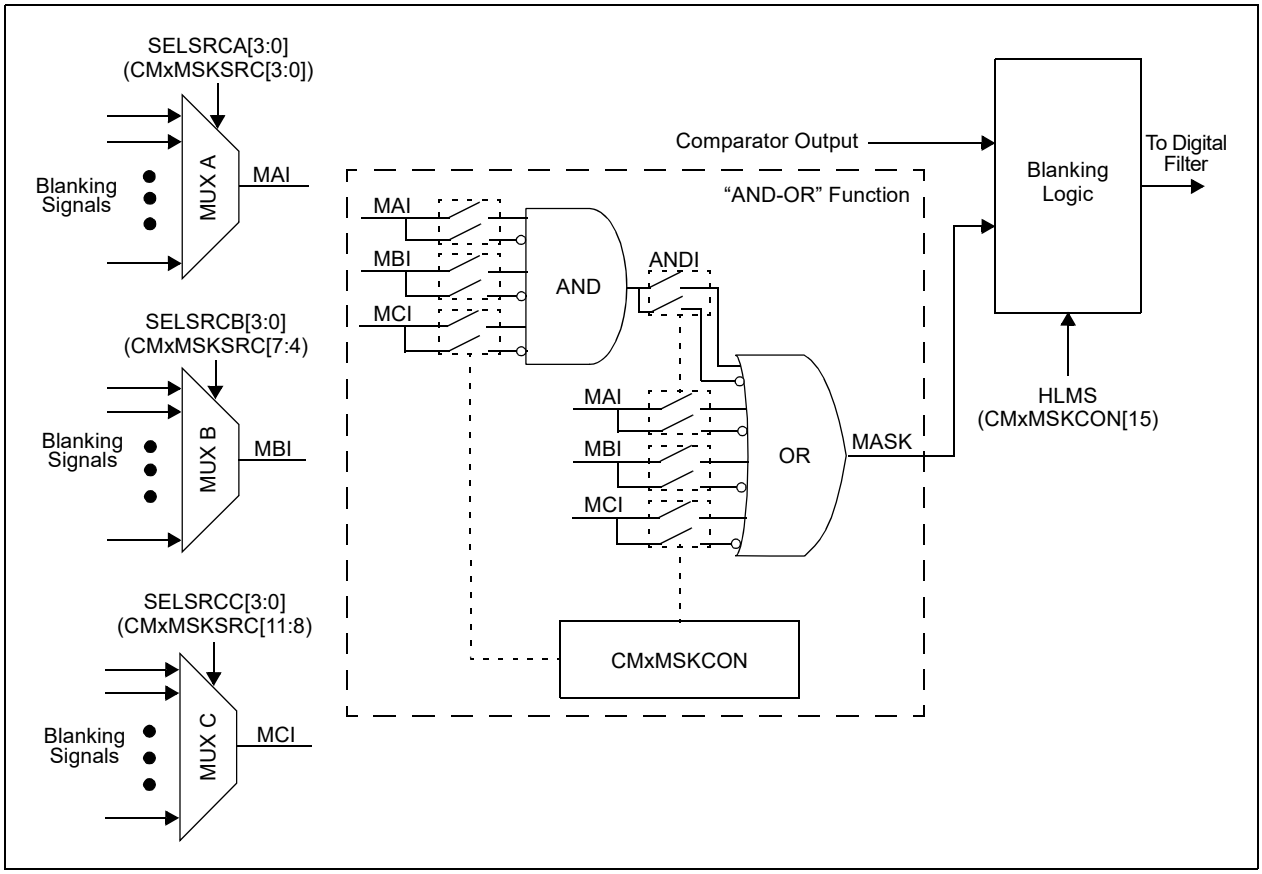
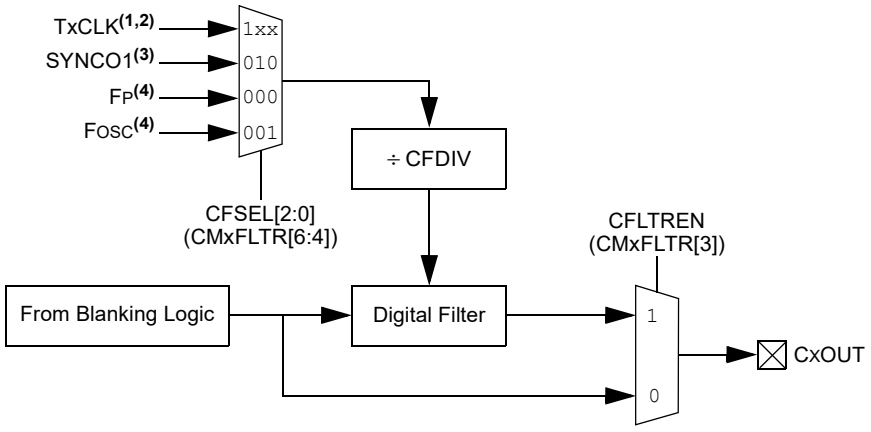



**FIGURE 25-5: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM**




**Note 1:** See the Type C Timer Block Diagram (Figure 13-2).
**2:** See the Type B Timer Block Diagram (Figure 13-1).
**3:** See the High-Speed PWMx Module Register Interconnection Diagram (Figure 16-2).
**4:** See the Oscillator System Diagram (Figure 9-1).

## 25.1 Op Amp Application Considerations

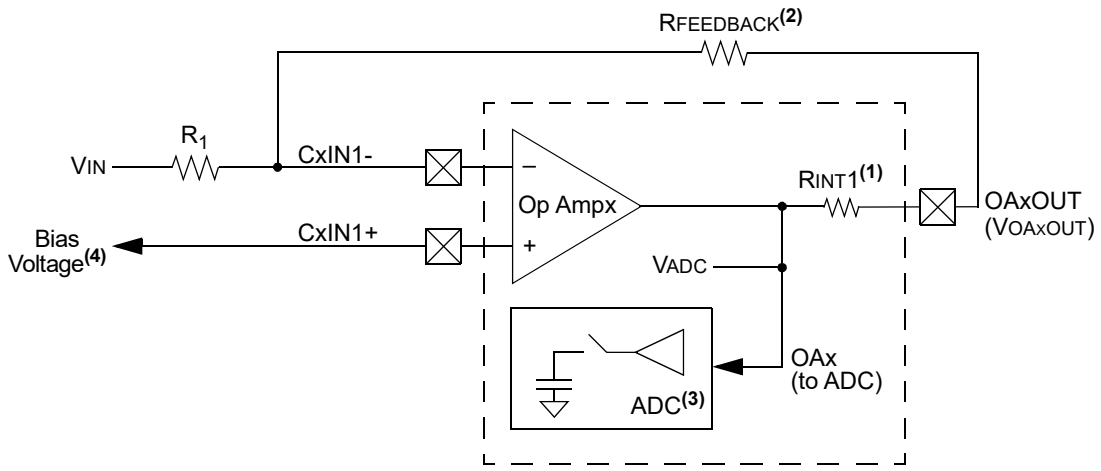
There are two configurations to take into consideration when designing with the op amp modules that are available in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices. Configuration A (see Figure 25-6) takes advantage of the internal connection to the ADC module to route the output of the op amp directly to the ADC for measurement. Configuration B (see Figure 25-7) requires that the designer externally route the output of the op amp (OAxOUT) to a separate analog input pin (ANy) on the device. Table 30-55 in **Section 30.0 "Electrical Characteristics"** describes the performance characteristics for the op amps, distinguishing between the two configuration types where applicable.

When the op amp output is made available on the corresponding OAxOUT pin, set both the pin's TRISx bit and the corresponding ANSELx bit to '1'.

### 25.1.1 OP AMP CONFIGURATION A

Figure 25-6 shows a typical inverting amplifier circuit taking advantage of the internal connections from the op amp output to the input of the ADC. The advantage of this configuration is that the user does not need to consume another analog input (ANy) on the device, and allows the user to simultaneously sample all three op amps with the ADC module, if needed. However, the presence of the internal resistance, RINT1, adds an error in the feedback path. Since RINT1 is an internal resistance, in relation to the op amp output (VOAXOUT) and ADC internal connection (VADC), RINT1 must be included in the numerator term of the transfer function. See Table 30-53 in **Section 30.0 "Electrical Characteristics"** for the typical value of RINT1. Table 30-60 and Table 30-61 in **Section 30.0 "Electrical Characteristics"** describe the minimum Sample Time (TSAMP) requirements for the ADC module in this configuration. Figure 25-6 also defines the equations that should be used when calculating the expected voltages at points, VADC and VOAXOUT.

**FIGURE 25-6: OP AMP CONFIGURATION A**




$$V_{ADC} = \left(\frac{R_{FEEDBACK} + R_{INT1}}{R_1}\right)( \ Bias\ Voltage - V_{IN} \ )$$

$$V_{OAxOUT} = \left(\frac{R_{FEEDBACK}}{R_1}\right)( \ Bias\ Voltage - V_{IN} \ )$$

**Note 1:** See Table 30-53 for the Typical value.
**2:** See Table 30-53 for the Minimum value for the feedback resistor.
**3:** See Table 30-60 and Table 30-61 for the minimum Sample Time (TSAMP).
**4:** CVREF1O or CVREF2O are two options that are available for supplying bias voltage to the op amps.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### 25.1.2 OP AMP CONFIGURATION B

Figure 25-7 shows a typical inverting amplifier circuit with the output of the op amp (OAxOUT) externally routed to a separate analog input pin (ANy) on the device. This op amp configuration is slightly different in terms of the op amp output and the ADC input connection, therefore, RINT1 is not included in the transfer function. However, this configuration requires the designer to externally route the op amp output (OAxOUT) to another analog input pin (ANy). See Table 30-53 in **Section 30.0 "Electrical Characteristics"** for the typical value of RINT1.

Table 30-60 and Table 30-61 in **Section 30.0 "Electrical Characteristics"** describe the minimum Sample Time (TSAMP) requirements for the ADC module in this configuration.

Figure 25-7 also defines the equation to be used to calculate the expected voltage at point VOAxOUT. This is the typical inverting amplifier equation.

Table 25-1 is a summary of the availability of the comparators (1 to 4) and the op amp (1 to 3) for the different packages.

**TABLE 25-1: OP AMP/COMPARATOR ANALYSIS**

| Comparators/ Op Amps | Reference | 28-Pin (SOIC/SPDIP) | | | | 28-Pin (QFN) | | | | 36-Pin | | | | 44/48-Pin | | | | 64-Pin | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Comparator | | Op Amp | | Comparator | | Op Amp | | Comparator | | Op Amp | | Comparator | | Op Amp | | Comparator | | Op Amp | |
| | | Neg | Pos | Neg | Pos | Neg | Pos | Neg | Pos | Neg | Pos | Neg | Pos | Neg | Pos | Neg | Pos | Neg | Pos | Neg | Pos |
| Comparator/Op Amp 1 | OA1INM1 | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | |
| | OA1INM2 | N/A | | | | N/A | | | | N/A | | | | N/A | | | | ✓ | | | |
| | OA1INP | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ |
| | VREF | | ✓ | | | | ✓ | | | | ✓ | | | | ✓ | | | | ✓ | | |
| Comparator/Op Amp 2 | OA2INM1 | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | |
| | OA2INM2 | N/A | | | | N/A | | | | N/A | | | | N/A | | | | ✓ | | | |
| | OA2INP | | | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ |
| | VREF | | | | | | ✓ | | | | ✓ | | | | ✓ | | | | ✓ | | |
| Comparator/Op Amp 3 | OA3INM1 | N/A | | N/A | | N/A | | N/A | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | | ✓ | |
| | OA3INM2 | N/A | | | | N/A | | | | N/A | | | | N/A | | | | ✓ | | | |
| | OA3INP | | N/A | | N/A | | N/A | | N/A | | N/A | | N/A | | ✓ | | ✓ | | ✓ | | ✓ |
| | VREF | | ✓ | | | | ✓ | | | | ✓ | | | | ✓ | | | | ✓ | | |
| Comparator 4 | C4INB | N/A | | | | N/A | | | | ✓ | | | | ✓ | | | | ✓ | | | |
| | OA1OUT | ✓ | | | | ✓ | | | | ✓ | | | | ✓ | | | | ✓ | | | |
| | OA2OUT | ✓ | | | | ✓ | | | | ✓ | | | | ✓ | | | | ✓ | | | |
| | OA3OUT/ C4INA | N/A | | | | N/A | | | | ✓ | | | | ✓ | | | | ✓ | | | |
| | C4INA/ OA3OUT | | N/A | | | | N/A | | | | ✓ | | | | ✓ | | | | ✓ | | |
| | VREF | | ✓ | | | | ✓ | | | | ✓ | | | | ✓ | | | | ✓ | | |

**Legend:** X = Available connection;
N/A = Unavailable connection (nominal module input not connected to any device pin);
Grayed out cells = Op amp functionality not available for Comparator 4

## 25.2 Op Amp/Comparator Resources

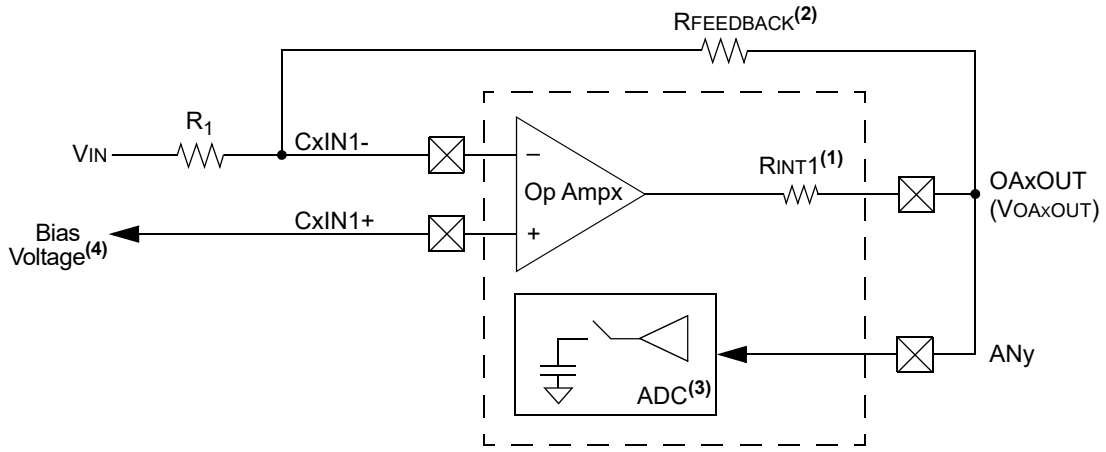
Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

### 25.2.1 KEY RESOURCES

- **"Op Amp/Comparator"** (www.microchip.com/DS70000357) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

**FIGURE 25-7: OP AMP CONFIGURATION B**




$$V_{OAxOUT} = \left(\frac{R_{FEEDBACK}}{R_1}\right)( \ Bias\ Voltage - V_{IN} \ )$$

**Note 1:** See Table 30-53 for the Typical value.
**2:** See Table 30-53 for the Minimum value for the feedback resistor.
**3:** See Table 30-60 and Table 30-61 for the minimum Sample Time (TSAMP).
**4:** CVREF1O or CVREF2O are two options that are available for supplying bias voltage to the op amps.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## 25.3 Op Amp/Comparator Registers

**REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER**

| R/W-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PSIDL | — | — | — | C4EVT(1) | C3EVT(1) | C2EVT(1) | C1EVT(1) |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | C4OUT(2) | C3OUT(2) | C2OUT(2) | C1OUT(2) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **PSIDL:** Comparator Stop in Idle Mode bit
1 = Discontinues operation of all comparators when device enters Idle mode
0 = Continues operation of all comparators in Idle mode

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **C4EVT:** Op Amp/Comparator 4 Event Status bit(1)
1 = Op amp/comparator event occurred
0 = Op amp/comparator event did not occur

bit 10 **C3EVT:** Comparator 3 Event Status bit(1)
1 = Comparator event occurred
0 = Comparator event did not occur

bit 9 **C2EVT:** Comparator 2 Event Status bit(1)
1 = Comparator event occurred
0 = Comparator event did not occur

bit 8 **C1EVT:** Comparator 1 Event Status bit(1)
1 = Comparator event occurred
0 = Comparator event did not occur

bit 7-4 **Unimplemented:** Read as '0'

bit 3 **C4OUT:** Comparator 4 Output Status bit(2)
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 2 **C3OUT:** Comparator 3 Output Status bit(2)
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

**Note 1:** Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON[9].

**2:** Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON[8].

**REGISTER 25-1: CMSTAT: OP AMP/COMPARATOR STATUS REGISTER (CONTINUED)**

bit 1 **C2OUT:** Comparator 2 Output Status bit(2)
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

bit 0 **C1OUT:** Comparator 1 Output Status bit(2)
When CPOL = 0:
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1:
1 = VIN+ < VIN-
0 = VIN+ > VIN-

**Note 1:** Reflects the value of the of the CEVT bit in the respective Op Amp/Comparator Control register, CMxCON[9].

**2:** Reflects the value of the COUT bit in the respective Op Amp/Comparator Control register, CMxCON[8].


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**REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3)(3)**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CON | COE(2) | CPOL | — | — | OPMODE | CEVT | COUT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| EVPOL1 | EVPOL0 | — | CREF(1) | — | — | CCH1(1) | CCH0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CON:** Op Amp/Comparator Enable bit
1 = Op amp/comparator is enabled
0 = Op amp/comparator is disabled

bit 14 **COE:** Comparator Output Enable bit(2)
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **OPMODE:** Op Amp/Comparator Operation Mode Select bit
1 = Circuit operates as an op amp
0 = Circuit operates as a comparator

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to the EVPOL[1:0] settings occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (noninverted polarity):
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1 (inverted polarity):
1 = VIN+ < VIN-
0 = VIN+ > VIN-

**Note 1:** Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.
**2:** This output is not available when OPMODE (CMxCON[10]) = 1.
**3:** CM3CON is not available on 28-pin devices.

**REGISTER 25-2: CMxCON: COMPARATOR x CONTROL REGISTER (x = 1, 2 OR 3)(3) (CONTINUED)**

bit 7-6 **EVPOL[1:0]:** Trigger/Event/Interrupt Polarity Select bits
- 11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)
- 10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)
  - If CPOL = 1 (inverted polarity):
    Low-to-high transition of the comparator output.
  - If CPOL = 0 (noninverted polarity):
    High-to-low transition of the comparator output.
- 01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity-selected comparator output (while CEVT = 0)
  - If CPOL = 1 (inverted polarity):
    High-to-low transition of the comparator output.
  - If CPOL = 0 (noninverted polarity):
    Low-to-high transition of the comparator output
- 00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit (VIN+ input)(1)
- 1 = VIN+ input connects to internal CVREFIN voltage(2)
- 0 = VIN+ input connects to CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH[1:0]:** Op Amp/Comparator Channel Select bits(1)
- 11 = Unimplemented
- 10 = Unimplemented
- 01 = Inverting input of the comparator connects to the CxIN2- pin(2)
- 00 = Inverting input of the op amp/comparator connects to the CxIN1- pin

**Note 1:** Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.

**2:** This output is not available when OPMODE (CMxCON[10]) = 1.

**3:** CM3CON is not available on 28-pin devices.


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**REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CON | COE | CPOL | — | — | — | CEVT | COUT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| EVPOL1 | EVPOL0 | — | CREF(1) | — | — | CCH1(1) | CCH0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-10 **Unimplemented:** Read as '0'

bit 9 **CEVT:** Comparator Event bit
1 = Comparator event according to EVPOL[1:0] settings occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (noninverted polarity):
1 = VIN+ > VIN-
0 = VIN+ < VIN-
When CPOL = 1 (inverted polarity):
1 = VIN+ < VIN-
0 = VIN+ > VIN-

**Note 1:** Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.

**2:** This input pin is not available in 28-pin devices. Refer to Table 25-1.

**REGISTER 25-3: CM4CON: COMPARATOR 4 CONTROL REGISTER (CONTINUED)**

bit 7-6 **EVPOL[1:0]:** Trigger/Event/Interrupt Polarity Select bits

11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)

10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.

If CPOL = 0 (noninverted polarity):
High-to-low transition of the comparator output.

01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.

If CPOL = 0 (noninverted polarity):
Low-to-high transition of the comparator output.

00 = Trigger/event/interrupt generation is disabled

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit (VIN+ input)(1)

1 = VIN+ input connects to internal CVREFIN voltage

0 = VIN+ input connects to C4IN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH[1:0]:** Comparator Channel Select bits(1)

11 = VIN- input of comparator connects to OA3/AN6(2)

10 = VIN- input of comparator connects to OA2/AN0

01 = VIN- input of comparator connects to OA1/AN3

00 = VIN- input of comparator connects to C4IN1-(2)

**Note 1:** Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.

**2:** This input pin is not available in 28-pin devices. Refer to Table 25-1.


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**REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | RW-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | SELSRCC3 | SELSRCC2 | SELSRCC1 | SELSRCC0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **SELSRCC[3:0]:** Mask C Input Select bits
1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 7-4 **SELSRCB[3:0]:** Mask B Input Select bits
1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

**REGISTER 25-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER (CONTINUED)**

bit 3-0 **SELSRCA[3:0]:** Mask A Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = Reserved
1010 = Reserved
1001 = Reserved
1000 = Reserved
0111 = Reserved
0110 = Reserved
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L


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**REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| HLMS | — | OCEN | OCNEN | OBEN | OBNEN | OAEN | OANEN |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| NAGS | PAGS | ACEN | ACNEN | ABEN | ABNEN | AAEN | AANEN |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **HLMS:** High or Low-Level Masking Select bits
1 = The masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
0 = The masking (blanking) function will prevent any asserted ('1') comparator signal from propagating

bit 14 **Unimplemented:** Read as '0'

bit 13 **OCEN:** OR Gate C Input Enable bit
1 = MCI is connected to OR gate
0 = MCI is not connected to OR gate

bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to OR gate
0 = Inverted MCI is not connected to OR gate

bit 11 **OBEN:** OR Gate B Input Enable bit
1 = MBI is connected to OR gate
0 = MBI is not connected to OR gate

bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to OR gate
0 = Inverted MBI is not connected to OR gate

bit 9 **OAEN:** OR Gate A Input Enable bit
1 = MAI is connected to OR gate
0 = MAI is not connected to OR gate

bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to OR gate
0 = Inverted MAI is not connected to OR gate

bit 7 **NAGS:** AND Gate Output Inverted Enable bit
1 = Inverted ANDI is connected to OR gate
0 = Inverted ANDI is not connected to OR gate

bit 6 **PAGS:** AND Gate Output Enable bit
1 = ANDI is connected to OR gate
0 = ANDI is not connected to OR gate

bit 5 **ACEN:** AND Gate C Input Enable bit
1 = MCI is connected to AND gate
0 = MCI is not connected to AND gate

bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to AND gate
0 = Inverted MCI is not connected to AND gate

**REGISTER 25-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER (CONTINUED)**

bit 3 **ABEN:** AND Gate B Input Enable bit
1 = MBI is connected to AND gate
0 = MBI is not connected to AND gate

bit 2 **ABNEN:** AND Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to AND gate
0 = Inverted MBI is not connected to AND gate

bit 1 **AAEN:** AND Gate A Input Enable bit
1 = MAI is connected to AND gate
0 = MAI is not connected to AND gate

bit 0 **AANEN:** AND Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to AND gate
0 = Inverted MAI is not connected to AND gate


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**REGISTER 25-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | CFSEL2 | CFSEL1 | CFSEL0 | CFLTREN | CFDIV2 | CFDIV1 | CFDIV0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-4 **CFSEL[2:0]:** Comparator Filter Input Clock Select bits
111 = T5CLK(1)
110 = T4CLK(2)
101 = T3CLK(1)
100 = T2CLK(2)
011 = Reserved
010 = SYNCO1(3)
001 = FOSC(4)
000 = FP(4)

bit 3 **CFLTREN:** Comparator Filter Enable bit
1 = Digital filter is enabled
0 = Digital filter is disabled

bit 2-0 **CFDIV[2:0]:** Comparator Filter Clock Divide Select bits
111 = Clock Divide 1:128
110 = Clock Divide 1:64
101 = Clock Divide 1:32
100 = Clock Divide 1:16
011 = Clock Divide 1:8
010 = Clock Divide 1:4
001 = Clock Divide 1:2
000 = Clock Divide 1:1

**Note 1:** See the Type C Timer Block Diagram (Figure 13-2).
**2:** See the Type B Timer Block Diagram (Figure 13-1).
**3:** See the High-Speed PWMx Module Register Interconnection Diagram (Figure 16-2).
**4:** See the Oscillator System Diagram (Figure 9-1).

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**REGISTER 25-7: CVRCON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER**

| U-0 | R/W-0 | U-0 | U-0 | U-0 | R/W-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | CVR2OE(1) | — | — | — | VREFSEL | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CVREN | CVR1OE(1) | CVRR | CVRSS(2) | CVR3 | CVR2 | CVR1 | CVR0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14 **CVR2OE:** Comparator Voltage Reference 2 Output Enable bit(1)
1 = (AVDD – AVSS)/2 is connected to the CVREF2O pin
0 = (AVDD – AVSS)/2 is disconnected from the CVREF2O pin

bit 13-11 **Unimplemented:** Read as '0'

bit 10 **VREFSEL:** Comparator Voltage Reference Select bit
1 = CVREFIN = VREF+
0 = CVREFIN is generated by the resistor network

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 6 **CVR1OE:** Comparator Voltage Reference 1 Output Enable bit(1)
1 = Voltage level is output on the CVREF1O pin
0 = Voltage level is disconnected from then CVREF1O pin

bit 5 **CVRR:** Comparator Voltage Reference Range Selection bit
1 = CVRSRC/24 step-size
0 = CVRSRC/32 step-size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit(2)
1 = Comparator voltage reference source, CVRSRC = (VREF+) – (AVSS)
0 = Comparator voltage reference source, CVRSRC = AVDD – AVSS

bit 3-0 **CVR[3:0]** Comparator Voltage Reference Value Selection 0 ≤ CVR[3:0] ≤ 15 bits
When CVRR = 1:
CVREFIN = (CVR[3:0]/24) • (CVRSRC)
When CVRR = 0:
CVREFIN = (CVRSRC/4) + (CVR[3:0]/32) • (CVRSRC)

**Note 1:** The ANSELx register controls the operation of the analog port pins. The port pins that are to function as analog inputs or outputs must have their corresponding ANSELx and TRISx bits set.

**2:** In order to operate with CVRSS = 1, at least one of the comparator modules must be enabled.


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## 26.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Programmable Cyclic Redundancy Check (CRC)"** (www.microchip.com/DS70346) of the *"dsPIC33/PIC24 Family Reference Manual"*.

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

- User-Programmable (up to 32nd order) Polynomial CRC Equation
- Interrupt Output
- Data FIFO

The programmable CRC generator provides a hardware implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-Programmable CRC Polynomial Equation, Up to 32 Bits
- Programmable Shift Direction (little or big-endian)
- Independent Data and Polynomial Lengths
- Configurable Interrupt Output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 26-1. A simple version of the CRC shift engine is shown in Figure 26-2.

**FIGURE 26-1: CRC BLOCK DIAGRAM**

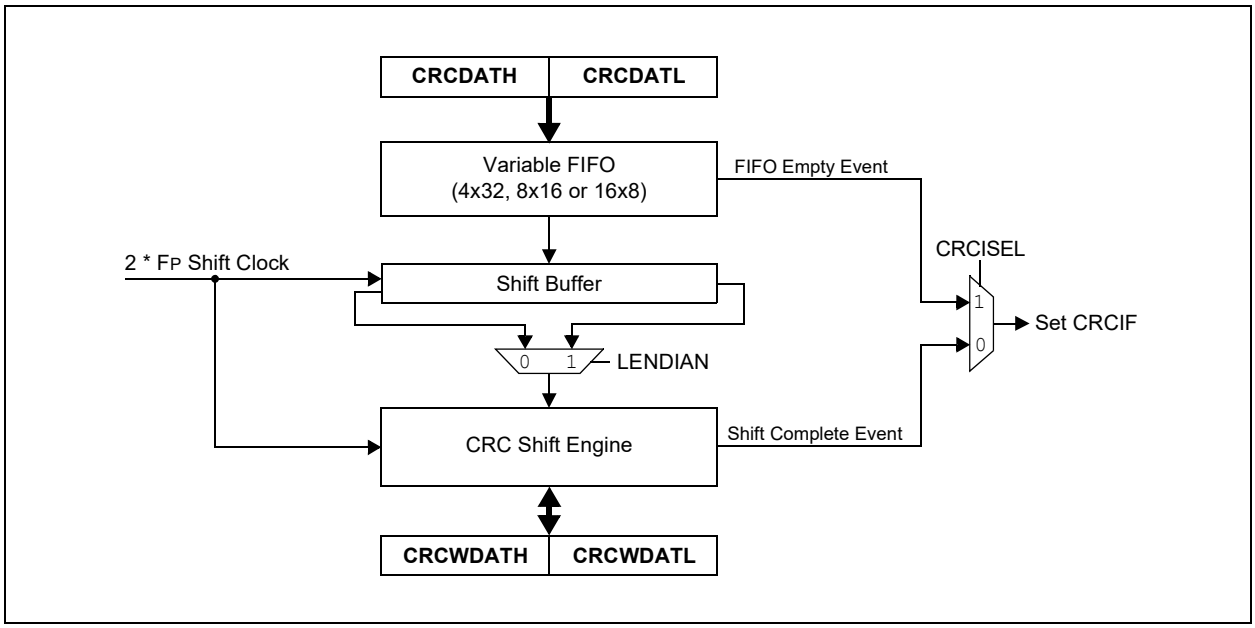
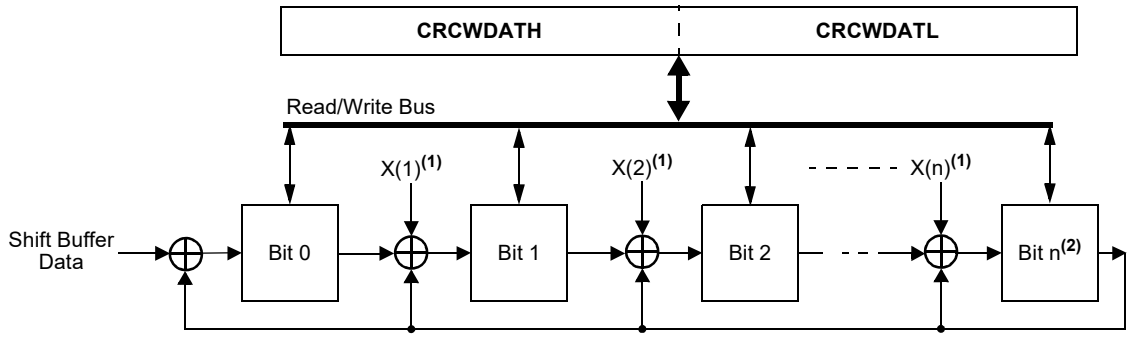


**FIGURE 26-2: CRC SHIFT ENGINE DETAIL**




**Note 1:** Each XOR stage of the shift engine is programmable. See text for details.
**2:** Polynomial length n is determined by ([PLEN[4:0]] + 1).

## 26.1 Overview

The CRC module can be programmed for CRC polynomials of up to the 32nd order, using up to 32 bits. Polynomial length, which reflects the highest exponent in the equation, is selected by the PLEN[4:0] bits (CRCCON2[4:0]).

The CRCXORL and CRCXORH registers control which exponent terms are included in the equation. Setting a particular bit includes that exponent term in the equation; functionally, this includes an XOR operation on the corresponding bit in the CRC engine. Clearing the bit disables the XOR.

For example, consider two CRC polynomials, one a 16-bit equation and the other a 32-bit equation:

$$x16 + x12 + x5 + 1$$

and

$$x32 + x26 + x23 + x22 + x16 + x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x + 1$$

To program these polynomials into the CRC generator, set the register bits as shown in Table 26-1.

Note that the appropriate positions are set to '1' to indicate that they are used in the equation (for example, X26 and X23). The 0 bit required by the equation is always XORed; thus, X0 is a don't care. For a polynomial of length N, it is assumed that the *N*th bit will always be used, regardless of the bit setting. Therefore, for a polynomial length of 32, there is no 32nd bit in the CRCxOR register.

**TABLE 26-1: CRC SETUP EXAMPLES FOR 16 AND 32-BIT POLYNOMIAL**

| CRC Control Bits | Bit Values | |
|---|---|---|
| | 16-Bit Polynomial | 32-Bit Polynomial |
| PLEN[4:0] | 01111 | 11111 |
| X[31:16] | 0000 0000<br>0000 000x | 0000 0100<br>1100 0001 |
| X[15:0] | 0001 0000<br>0010 000x | 0001 1101<br>1011 011x |

## 26.2 Programmable CRC Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

**Note:** In the event you are not able to access the product page using the link above, enter this URL in your browser:
http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464

### 26.2.1 KEY RESOURCES

- **"Programmable Cyclic Redundancy Check (CRC)"** (www.microchip.com/DS70346) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools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## 26.3 Programmable CRC Registers

**REGISTER 26-1: CRCCON1: CRC CONTROL REGISTER 1**

| R/W-0 | U-0 | R/W-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| CRCEN | — | CSIDL | VWORD4 | VWORD3 | VWORD2 | VWORD1 | VWORD0 |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-1 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| CRCFUL | CRCMPT | CRCISEL | CRCGO | LENDIAN | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CRCEN:** CRC Enable bit
1 = CRC module is enabled
0 = CRC module is disabled; all state machines, pointers and CRCWDAT/CRCDAT are reset, other SFRs are not reset

bit 14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CRC Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **VWORD[4:0]:** Pointer Value bits
Indicates the number of valid words in the FIFO. Has a maximum value of 8 when PLEN[4:0] > 7 or 16 when PLEN[4:0] ≤ 7.

bit 7 **CRCFUL**: CRC FIFO Full bit
1 = FIFO is full
0 = FIFO is not full

bit 6 **CRCMPT:** CRC FIFO Empty Bit
1 = FIFO is empty
0 = FIFO is not empty

bit 5 **CRCISEL:** CRC Interrupt Selection bit
1 = Interrupt on FIFO is empty; final word of data is still shifting through CRC
0 = Interrupt on shift is complete and CRCWDAT results are ready

bit 4 **CRCGO:** Start CRC bit
1 = Starts CRC serial shifter
0 = CRC serial shifter is turned off

bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit
1 = Data word is shifted into the CRC starting with the LSb (little-endian)
0 = Data word is shifted into the CRC starting with the MSb (big-endian)

bit 2-0 **Unimplemented:** Read as '0'

**REGISTER 26-2: CRCCON2: CRC CONTROL REGISTER 2**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | DWIDTH[4:0] | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | PLEN[4:0] | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **DWIDTH[4:0]:** Data Width Select bits
These bits set the width of the data word (DWIDTH[4:0] + 1).

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **PLEN[4:0]:** Polynomial Length Select bits
These bits set the length of the polynomial (Polynomial Length = PLEN[4:0] + 1).


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**REGISTER 26-3: CRCXORH: CRC XOR POLYNOMIAL HIGH REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| X[31:24] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| X[23:16] | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **X[31:16]:** XOR of Polynomial Term $X^n$ Enable bits

**REGISTER 26-4: CRCXORL: CRC XOR POLYNOMIAL LOW REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| X[15:8] | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| X[7:1] | | | | | | | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-1 **X[15:1]:** XOR of Polynomial Term $X^n$ Enable bits

bit 0 **Unimplemented:** Read as '0'

**NOTES:**


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# 27.0 SPECIAL FEATURES

**Note:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip website (www.microchip.com).

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

## 27.1 Configuration Bits

In dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data are stored at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 27-1. The configuration data are automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

**Note:** Configuration data are reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be '1111 1111 1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

**Note:** Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 27-1.

**TABLE 27-1: CONFIGURATION BYTE REGISTER MAP**

| File Name | Address | Device Memory Size (Kbytes) | Bits 23-8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Reserved | 0057EC | 32 | — | — | — | — | — | — | — | — | — |
| | 00AFEC | 64 | | | | | | | | | |
| | 0157EC | 128 | | | | | | | | | |
| | 02AFEC | 256 | | | | | | | | | |
| | 0557EC | 512 | | | | | | | | | |
| Reserved | 0057EE | 32 | — | — | — | — | — | — | — | — | — |
| | 00AFEE | 64 | | | | | | | | | |
| | 0157EE | 128 | | | | | | | | | |
| | 02AFEE | 256 | | | | | | | | | |
| | 0557EE | 512 | | | | | | | | | |
| FICD | 0057F0 | 32 | — | Reserved(3) | — | JTAGEN | Reserved(2) | Reserved(3) | — | ICS[1:0] | |
| | 00AFF0 | 64 | | | | | | | | | |
| | 0157F0 | 128 | | | | | | | | | |
| | 02AFF0 | 256 | | | | | | | | | |
| | 0557F0 | 512 | | | | | | | | | |
| FPOR | 0057F2 | 32 | — | WDTWIN[1:0] | | ALTI2C2 | ALTI2C1 | Reserved(3) | — | — | — |
| | 00AFF2 | 64 | | | | | | | | | |
| | 0157F2 | 128 | | | | | | | | | |
| | 02AFF2 | 256 | | | | | | | | | |
| | 0557F2 | 512 | | | | | | | | | |
| FWDT | 0057F4 | 32 | — | FWDTEN | WINDIS | PLLKEN | WDTPRE | WDTPOST[3:0] | | | |
| | 00AFF4 | 64 | | | | | | | | | |
| | 0157F4 | 128 | | | | | | | | | |
| | 02AFF4 | 256 | | | | | | | | | |
| | 0557F4 | 512 | | | | | | | | | |
| FOSC | 0057F6 | 32 | — | FCKSM[1:0] | | IOL1WAY | — | — | OSCIOFNC | POSCMD[1:0] | |
| | 00AFF6 | 64 | | | | | | | | | |
| | 0157F6 | 128 | | | | | | | | | |
| | 02AFF6 | 256 | | | | | | | | | |
| | 0557F6 | 512 | | | | | | | | | |
| FOSCSEL | 0057F8 | 32 | — | IESO | PWMLOCK(1) | — | — | — | FNOSC[2:0] | | |
| | 00AFF8 | 64 | | | | | | | | | |
| | 0157F8 | 128 | | | | | | | | | |
| | 02AFF8 | 256 | | | | | | | | | |
| | 0557F8 | 512 | | | | | | | | | |
| FGS | 0057FA | 32 | — | — | — | — | — | — | — | GCP | GWRP |
| | 00AFFA | 64 | | | | | | | | | |
| | 0157FA | 128 | | | | | | | | | |
| | 02AFFA | 256 | | | | | | | | | |
| | 0557FA | 512 | | | | | | | | | |
| Reserved | 0057FC | 32 | — | — | — | — | — | — | — | — | — |
| | 00AFFC | 64 | | | | | | | | | |
| | 0157FC | 128 | | | | | | | | | |
| | 02AFFC | 256 | | | | | | | | | |
| | 0557FC | 512 | | | | | | | | | |
| Reserved | 057FFE | 32 | — | — | — | — | — | — | — | — | — |
| | 00AFFE | 64 | | | | | | | | | |
| | 0157FE | 128 | | | | | | | | | |
| | 02AFFE | 256 | | | | | | | | | |
| | 0557FE | 512 | | | | | | | | | |

**Legend:** — = unimplemented, read as '1'.

**Note 1:** This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**2:** This bit is reserved and must be programmed as '0'.

**3:** These bits are reserved and must be programmed as '1'.


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**TABLE 27-2: CONFIGURATION BITS DESCRIPTION**

| Bit Field | Description |
|---|---|
| GCP | General Segment Code-Protect bit<br>1 = User program memory is not code-protected<br>0 = Code protection is enabled for the entire program memory space |
| GWRP | General Segment Write-Protect bit<br>1 = User program memory is not write-protected<br>0 = User program memory is write-protected |
| IESO | Two-Speed Oscillator Start-up Enable bit<br>1 = Start up device with FRC, then automatically switch to the user-selected oscillator source when ready<br>0 = Start up device with user-selected oscillator source |
| PWMLOCK(1) | PWM Lock Enable bit<br>1 = Certain PWM registers may only be written after a key sequence<br>0 = PWM registers may be written without a key sequence |
| FNOSC[2:0] | Oscillator Selection bits<br>111 = Fast RC Oscillator with Divide-by-N (FRCDIVN)<br>110 = Reserved; do not use<br>101 = Low-Power RC Oscillator (LPRC)<br>100 = Reserved; do not use<br>011 = Primary Oscillator with PLL module (XT + PLL, HS + PLL, EC + PLL)<br>010 = Primary Oscillator (XT, HS, EC)<br>001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL)<br>000 = Fast RC Oscillator (FRC) |
| FCKSM[1:0] | Clock Switching Mode bits<br>1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled<br>01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled<br>00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled |
| IOL1WAY | Peripheral Pin Select Configuration bit<br>1 = Allow only one reconfiguration<br>0 = Allow multiple reconfigurations |
| OSCIOFNC | OSC2 Pin Function bit (except in XT and HS modes)<br>1 = OSC2 is the clock output<br>0 = OSC2 is a general purpose digital I/O pin |
| POSCMD[1:0] | Primary Oscillator Mode Select bits<br>11 = Primary Oscillator is disabled<br>10 = HS Crystal Oscillator mode<br>01 = XT Crystal Oscillator mode<br>00 = EC (External Clock) mode |
| FWDTEN | Watchdog Timer Enable bit<br>1 = Watchdog Timer is always enabled (LPRC Oscillator cannot be disabled. Clearing the SWDTEN bit in the RCON register will have no effect.)<br>0 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register) |
| WINDIS | Watchdog Timer Window Enable bit<br>1 = Watchdog Timer in Non-Window mode<br>0 = Watchdog Timer in Window mode |
| PLLKEN | PLL Lock Enable bit<br>1 = PLL lock is enabled<br>0 = PLL lock is disabled |

**Note 1:** This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**2:** When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.

**TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)**

| Bit Field | Description |
|---|---|
| WDTPRE | Watchdog Timer Prescaler bit<br>1 = 1:128<br>0 = 1:32 |
| WDTPOST[3:0] | Watchdog Timer Postscaler bits<br>1111 = 1:32,768<br>1110 = 1:16,384<br>•<br>•<br>•<br>0001 = 1:2<br>0000 = 1:1 |
| WDTWIN[1:0] | Watchdog Window Select bits<br>11 = WDT window is 25% of WDT period<br>10 = WDT window is 37.5% of WDT period<br>01 = WDT window is 50% of WDT period<br>00 = WDT window is 75% of WDT period |
| ALTI2C1 | Alternate I2C1 pin<br>1 = I2C1 is mapped to the SDA1/SCL1 pins<br>0 = I2C1 is mapped to the ASDA1/ASCL1 pins |
| ALTI2C2 | Alternate I2C2 pin<br>1 = I2C2 is mapped to the SDA2/SCL2 pins<br>0 = I2C2 is mapped to the ASDA2/ASCL2 pins |
| JTAGEN(2) | JTAG Enable bit<br>1 = JTAG is enabled<br>0 = JTAG is disabled |
| ICS[1:0] | ICD Communication Channel Select bits<br>11 = Communicate on PGEC1 and PGED1<br>10 = Communicate on PGEC2 and PGED2<br>01 = Communicate on PGEC3 and PGED3<br>00 = Reserved, do not use |

**Note 1:** This bit is only available on dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices.

**2:** When JTAGEN = 1, an internal pull-up resistor is enabled on the TMS pin. Erased devices default to JTAGEN = 1. Applications requiring I/O pins in a high-impedance state (tri-state) in Reset should use pins other than TMS for this purpose.


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**REGISTER 27-1: FGS CONFIGURATION REGISTER**

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | GCP | GWRP |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | PO = Program Once bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7-2 **Unused:** Reads contents of Flash Configuration Words

bit 1 **GCP:** General Segment Code Flash Protection Level bit
1 = General Segment has no security
0 = General Segment has high security

bit 0 **GWRP:** General Segment Program Flash Write Protection bit
1 = General Segment is not write-protected
0 = General Segment is write-protected

**REGISTER 27-2: FICD CONFIGURATION REGISTER**

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| r-1 | U-1 | R/PO-1 | U-1 | U-1 | U-1 | R/PO-1 | R/PO-1 |
|---|---|---|---|---|---|---|---|
| — | — | JTAGEN | — | — | — | ICS[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | PO = Program Once bit | r = Reserved bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7 **Reserved:** Maintain as ‘1’

bit 6 **Unimplemented:** Read as ‘1’

bit 5 **JTAGEN:** JTAG Enable bit
1 = JTAG port is enabled
0 = JTAG port is disabled

bit 4-2 **Unimplemented:** Read as ‘1’

bit 1-0 **ICS[1:0]:** ICD Communication Channel Select bits
11 = Communicates on PGEC1 and PGED1
10 = Communicates on PGEC2 and PGED2
01 = Communicates on PGEC3 and PGED3
00 = Reserved, do not use


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**REGISTER 27-3: FOSC CONFIGURATION REGISTER**

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| RW-1 | R/W-1 | R/W-0 | U-1 | U-1 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FCKSM[1:0] | | IOL1WAY | — | — | OSCIOFNC | POSCMD[1:0] | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | PO = Program Once bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7-6 **FCKSM[1:0]:** Clock Switching and Monitor Selection bits
1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled
01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled
00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled

bit 5 **IOL1WAY:** IOLOCK Bit One-Way Set Enable bit
1 = The IOLOCK bit (OSCCON[6]) can be set and cleared as needed (provided an unlocking sequence is executed)
0 = The IOLOCK bit (OSCCON[6]) can only be set once (provided an unlocking sequence is executed); once IOLOCK is set, this prevents any possible RP register changes

bit 4-3 **Unused:** Reads contents of Flash Configuration Words

bit 2 **OSCIOFNC:** CLKO Enable Configuration bit
1 = CLKO output signal is active on the OSC2 pin; Primary Oscillator must be disabled or configured for the External Clock (EC) mode for the CLKO to be active (POSCMD[1:0] = 11 or 00)
0 = CLKO output is disabled

bit 1-0 **POSCMD[1:0]:** Primary Oscillator Configuration bits
11 = Primary Oscillator is disabled
10 = HS Oscillator mode selected (10 MHz-40 MHz)
01 = MS Oscillator mode selected (3.5 MHz-10 MHz)
00 = External Clock mode selected

**REGISTER 27-4: FOSCSEL CONFIGURATION REGISTER**

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| RW-0 | R/W-0 | U-1 | U-1 | U-1 | R/W-0 | R/W-1 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IESO | PWMLOCK | — | — | — | FNOSC[2:0] | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | PO = Program Once bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7 **IESO:** Internal External Switchover bit
1 = Internal External Switchover mode enabled (Two-Speed Start-up enabled)
0 = Internal External Switchover mode disabled (Two-Speed Start-up disabled)

bit 6 **PWMLOCK:** PWM Lock Enable bit
1 = Certain PWM registers may only be written after key sequence
0 = PWM registers may be written without key

bit 5-3 **Unused:** Reads contents of Flash Configuration Words

bit 2-0 **FNOSC[2:0]:** Oscillator Selection bits
111 = Fast RC Oscillator with Divide-by-N (FRCDIV)
110 = Reserved; do not use
101 = Low-Power RC (LPRC) Oscillator
100 = Secondary Oscillator (SOSC)
011 = Primary Oscillator with PLL module (MS+PLL, HS+PLL, EC+PLL)
010 = Primary Oscillator (MS, HS, EC)
001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCDIV+PLL)
000 = Fast RC (FRC) Oscillator


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**REGISTER 27-5: FPOR CONFIGURATION REGISTER**

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| RW-1 | R/W-1 | R/W-1 | R/W-1 | r-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| WDTWIN[1:0] | | ALTI2C2 | ALTI2C1 | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | PO = Program Once bit | r = Reserved bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7-6 **WDTWIN[1:0]:** Watchdog Timer Window Select bits
11 = WDT window is 25% of WDT period
10 = WDT window is 37.5% of WDT period
01 = WDT window is 50% of WDT period
00 = WDT window is 75% of WDT period

bit 5 **ALTI2C2:** Alternate I2C2 Pin Mapping bit
1 = Default location for SCL2/SDA2 pins
0 = Alternate location for SCL2/SDA2 pins (ASCL2/ASDA2)

bit 4 **ALTI2C1:** Alternate I2C1 Pin Mapping bit
1 = Default location for SCL1/SDA1 pins
0 = Alternate location for SCL1/SDA1 pins (ASCL1/ASDA1)

bit 3 **Reserved:** Read as ‘1’

bit 2-0 **Unused:** Reads contents of Flash Configuration Words

**REGISTER 27-6: FWDT CONFIGURATION REGISTER**

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 23 | | | | | | | bit 16 |

| U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 | U-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| RW-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| FWDTEN | WINDIS | PLLKEN | WDTPRE | WDTPOST[3:0] | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | PO = Program Once bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 23-8 **Unimplemented:** Read as ‘1’

bit 7 **FWDTEN:** Watchdog Timer Enable bit
1 = WDT is enabled
0 = WDT is disabled (control is placed on the SWDTEN bit)

bit 6 **WINDIS:** Windowed Watchdog Timer Disable bit
1 = Standard WDT selected; windowed WDT is disabled
0 = Windowed WDT is enabled; note that executing a CLRWDT instruction while the WDT is disabled in hardware and software (FWDTEN = 0; SWDTEN = 0) will not cause a device Reset

bit 5 **PLLKEN:** PLL Lock Enable bit
1 = PLL lock is enabled
0 = PLL lock is disabled

bit 4 **WDTPRE:** WDT Prescaler bit
1 = WDT prescaler ratio of 1:128
0 = WDT prescaler ratio of 1:32

bit 3-0 **WDTPOST[3:0]:** Watchdog Timer Postscale Select bits
1111 = 1:32,768
1110 = 1:16,384
1101 = 1:8,192
1100 = 1:4,096
1011 = 1:2,048
1010 = 1:1,024
1001 = 1:512
1000 = 1:256
0111 = 1:128
0110 = 1:64
0101 = 1:32
0100 = 1:16
0011 = 1:8
0010 = 1:4
0001 = 1:2
0000 = 1:1


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**REGISTER 27-7: DEVID: DEVICE ID REGISTER**

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVID[23:16](1) | | | | | | | |
| bit 23 | | | | | | | bit 16 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVID[15:8](1) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVID[7:0](1) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | R = Read-Only bit | U = Unimplemented bit |
|---|---|---|

bit 23-0 **DEVID[23:0]:** Device Identifier bits(1)

**Note 1:** Refer to the *"dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70663) for the list of device ID values.

**REGISTER 27-8: DEVREV: DEVICE REVISION REGISTER**

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVREV[23:16](1) | | | | | | | |
| bit 23 | | | | | | | bit 16 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVREV[15:8](1) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R | R | R | R | R | R | R | R |
|---|---|---|---|---|---|---|---|
| DEVREV[7:0](1) | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | R = Read-only bit | U = Unimplemented bit |
|---|---|---|

bit 23-0 **DEVREV[23:0]:** Device Revision bits(1)

**Note 1:** Refer to the *"dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70663) for the list of device revision values.

## 27.2 User ID Words

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 27-3.

**TABLE 27-3: USER ID WORDS REGISTER MAP**

| File Name | Address | Bits 23-16 | Bits 15-0 |
|---|---|---|---|
| FUID0 | 0x800FF8 | — | UID0 |
| FUID1 | 0x800FFA | — | UID1 |
| FUID2 | 0x800FFC | — | UID2 |
| FUID3 | 0x800FFE | — | UID3 |

**Legend:** — = unimplemented, read as '1'.

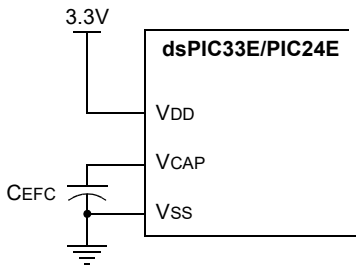
## 27.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 27-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 30-5 located in **Section 30.0 "Electrical Characteristics"**.

| **Note:** | It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin. |
|---|---|

**FIGURE 27-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR(1,2,3)**




**Note 1:** These are typical operating voltages. Refer to Table 30-5 located in **Section 30.1 "DC Characteristics"** for the full operating ranges of VDD and VCAP.

**2:** It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

**3:** Typical VCAP pin voltage = 1.8V when VDD ≥ VDDMIN.

## 27.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC[2:0] and POSCMD[1:0]).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON[5]) is '1'.

Concurrently, the PWRT Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 30-22 of **Section 30.0 "Electrical Characteristics"** for specific TFSCM values.

The BOR status bit (RCON[1]) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle modes and resets the device should VDD fall below the BOR threshold voltage.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## 27.5 Watchdog Timer (WDT)

For dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices, the WDT is driven by the LPRC Oscillator. When the WDT is enabled, the clock source is also enabled.

### 27.5.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT Time-out period (TWDT), as shown in Parameter SY12 in Table 30-22.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST[3:0] Configuration bits (FWDT[3:0]), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

**Note:** The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

### 27.5.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON[3,2]) needs to be cleared in software after the device wakes up.

### 27.5.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

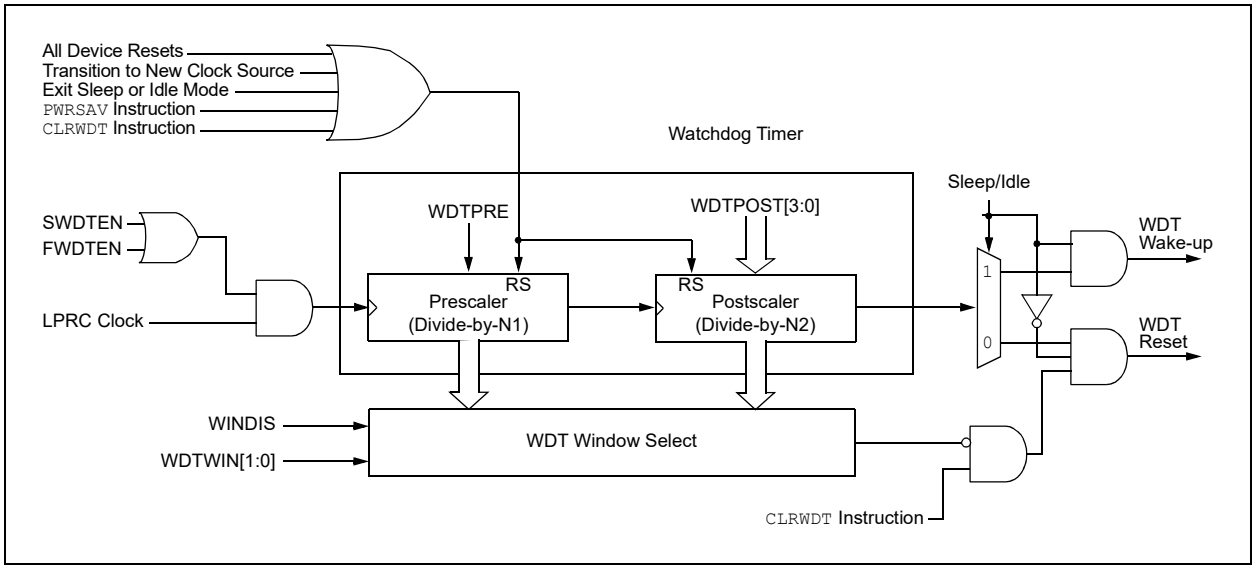
The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON[5]). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON[4]), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

### 27.5.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode, enabled by programming the WINDIS bit in the WDT Configuration register (FWDT[6]). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window select bits (WDTWIN[1:0]).

**FIGURE 27-2: WDT BLOCK DIAGRAM**



## 27.6 JTAG Interface

dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface is provided in future revisions of the document.

**Note:** Refer to **"Programming and Diagnostics"** (www.microchip.com/DS70608) in the *"dsPIC33/PIC24 Family Reference Manual"* for further information on usage, configuration and operation of the JTAG interface.

## 27.7 In-Circuit Serial Programming

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the *"dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70663) for details about In-Circuit Serial Programming (ICSP).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

## 27.8 In-Circuit Debugger

When MPLAB® ICD 3 or REAL ICE™ is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, VDD, VSS and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins (PGECx and PGEDx).

## 27.9 Code Protection and CodeGuard™ Security

The dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X devices offer basic implementation of CodeGuard Security that supports only General Segment (GS) security. This feature helps protect individual Intellectual Property.

**Note:** Refer to **"CodeGuard™ Security"** (www.microchip.com/DS70634) in the *"dsPIC33/PIC24 Family Reference Manual"* for further information on usage, configuration and operation of CodeGuard Security.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## 28.0 INSTRUCTION SET SUMMARY

**Note:** This data sheet summarizes the features of the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X families of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip website (www.microchip.com).

The dsPIC33EP instruction set is almost identical to that of the dsPIC30F and dsPIC33F. The PIC24EP instruction set is almost identical to that of the PIC24F and PIC24H.

Most instructions are a single program memory word (24 bits). Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word, divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into five basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- DSP operations
- Control operations

Table 28-1 lists the general symbols used in describing the instructions.

The dsPIC33E instruction set summary in Table 28-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register 'Wb' without any address modifier
- The second source operand, which is typically a register 'Ws' with or without an address modifier
- The destination of the result, which is typically a register 'Wd' with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value 'f'
- The destination, which could be either the file register 'f' or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register 'Wb')

The literal instructions that involve data movement can use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register 'Wb' without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register 'Wd' with or without an address modifier

The MAC class of DSP instructions can use some of the following operands:

- The accumulator (A or B) to be used (required operand)
- The W registers to be used as the two operands
- The X and Y address space prefetch operations
- The X and Y address space prefetch destinations
- The accumulator write back destination

The other DSP instructions do not involve any multiplication and can include:

- The accumulator to be used (required)
- The source or destination operand (designated as Wso or Wdo, respectively) with or without an address modifier
- The amount of shift specified by a W register 'Wn' or a literal value

The control instructions can use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed, or an SFR register is read. In these cases, the execution takes multiple instruction cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

**Note:** For more details on the instruction set, refer to the *"16-Bit MCU and DSC Programmer's Reference Manual"* (www.microchip.com/DS70000157).

For more information on instructions that take more than one instruction cycle to execute, refer to **"CPU"** (www.microchip.com/DS70359) in the *"dsPIC33/PIC24 Family Reference Manual"*, particularly the **"Instruction Flow Types"** section.

**TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS**

| Field | Description |
|---|---|
| #text | Means literal defined by "text" |
| (text) | Means "content of text" |
| [text] | Means "the location addressed by text" |
| { } | Optional field or operation |
| a ∈ {b, c, d} | a is selected from the set of values b, c, d |
| [n:m] | Register bit field |
| .b | Byte mode selection |
| .d | Double-Word mode selection |
| .S | Shadow register select |
| .w | Word mode selection (default) |
| Acc | One of two accumulators {A, B} |
| AWB | Accumulator write back destination address register ∈ {W13, [W13]+ = 2} |
| bit4 | 4-bit bit selection field (used in word addressed instructions) ∈ {0...15} |
| C, DC, N, OV, Z | MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero |
| Expr | Absolute address, label or expression (resolved by the linker) |
| f | File register address ∈ {0x0000...0x1FFF} |
| lit1 | 1-bit unsigned literal ∈ {0,1} |
| lit4 | 4-bit unsigned literal ∈ {0...15} |
| lit5 | 5-bit unsigned literal ∈ {0...31} |
| lit8 | 8-bit unsigned literal ∈ {0...255} |
| lit10 | 10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode |
| lit14 | 14-bit unsigned literal ∈ {0...16384} |
| lit16 | 16-bit unsigned literal ∈ {0...65535} |
| lit23 | 23-bit unsigned literal ∈ {0...8388608}; LSb must be '0' |
| None | Field does not require an entry, can be blank |
| OA, OB, SA, SB | DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate |
| PC | Program Counter |
| Slit10 | 10-bit signed literal ∈ {-512...511} |
| Slit16 | 16-bit signed literal ∈ {-32768...32767} |
| Slit6 | 6-bit signed literal ∈ {-16...16} |
| Wb | Base W register ∈ {W0...W15} |
| Wd | Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] } |
| Wdo | Destination W register ∈<br>{ Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] } |


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**TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS (CONTINUED)**

| Field | Description |
|---|---|
| Wm,Wn | Dividend, Divisor Working register pair (direct addressing) |
| Wm*Wm | Multiplicand and Multiplier Working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7} |
| Wm*Wn | Multiplicand and Multiplier Working register pair for DSP instructions ∈ {W4 * W5,W4 * W6,W4 * W7,W5 * W6,W5 * W7,W6 * W7} |
| Wn | One of 16 Working registers ∈ {W0...W15} |
| Wnd | One of 16 destination Working registers ∈ {W0...W15} |
| Wns | One of 16 source Working registers ∈ {W0...W15} |
| WREG | W0 (Working register used in file register instructions) |
| Ws | Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] } |
| Wso | Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] } |
| Wx | X Data Space Prefetch Address register for DSP instructions ∈ {[W8] + = 6, [W8] + = 4, [W8] + = 2, [W8], [W8] - = 6, [W8] - = 4, [W8] - = 2, [W9] + = 6, [W9] + = 4, [W9] + = 2, [W9], [W9] - = 6, [W9] - = 4, [W9] - = 2, [W9 + W12], none} |
| Wxd | X Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7} |
| Wy | Y Data Space Prefetch Address register for DSP instructions ∈ {[W10] + = 6, [W10] + = 4, [W10] + = 2, [W10], [W10] - = 6, [W10] - = 4, [W10] - = 2, [W11] + = 6, [W11] + = 4, [W11] + = 2, [W11], [W11] - = 6, [W11] - = 4, [W11] - = 2, [W11 + W12], none} |
| Wyd | Y Data Space Prefetch Destination register for DSP instructions ∈ {W4...W7} |

**TABLE 28-2: INSTRUCTION SET OVERVIEW**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | | Description | # of Words | # of Cycles[2] | Status Flags Affected |
|---|---|---|---|---|---|---|---|
| 1 | ADD | ADD | Acc[1] | Add Accumulators | 1 | 1 | OA,OB,SA,SB |
| | | ADD | f | f = f + WREG | 1 | 1 | C,DC,N,OV,Z |
| | | ADD | f,WREG | WREG = f + WREG | 1 | 1 | C,DC,N,OV,Z |
| | | ADD | #lit10,Wn | Wd = lit10 + Wd | 1 | 1 | C,DC,N,OV,Z |
| | | ADD | Wb,Ws,Wd | Wd = Wb + Ws | 1 | 1 | C,DC,N,OV,Z |
| | | ADD | Wb,#lit5,Wd | Wd = Wb + lit5 | 1 | 1 | C,DC,N,OV,Z |
| | | ADD | Wso,#Slit4,Acc | 16-bit Signed Add to Accumulator | 1 | 1 | OA,OB,SA,SB |
| 2 | ADDC | ADDC | f | f = f + WREG + (C) | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC | f,WREG | WREG = f + WREG + (C) | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC | #lit10,Wn | Wd = lit10 + Wd + (C) | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC | Wb,Ws,Wd | Wd = Wb + Ws + (C) | 1 | 1 | C,DC,N,OV,Z |
| | | ADDC | Wb,#lit5,Wd | Wd = Wb + lit5 + (C) | 1 | 1 | C,DC,N,OV,Z |
| 3 | AND | AND | f | f = f .AND. WREG | 1 | 1 | N,Z |
| | | AND | f,WREG | WREG = f .AND. WREG | 1 | 1 | N,Z |
| | | AND | #lit10,Wn | Wd = lit10 .AND. Wd | 1 | 1 | N,Z |
| | | AND | Wb,Ws,Wd | Wd = Wb .AND. Ws | 1 | 1 | N,Z |
| | | AND | Wb,#lit5,Wd | Wd = Wb .AND. lit5 | 1 | 1 | N,Z |
| 4 | ASR | ASR | f | f = Arithmetic Right Shift f | 1 | 1 | C,N,OV,Z |
| | | ASR | f,WREG | WREG = Arithmetic Right Shift f | 1 | 1 | C,N,OV,Z |
| | | ASR | Ws,Wd | Wd = Arithmetic Right Shift Ws | 1 | 1 | C,N,OV,Z |
| | | ASR | Wb,Wns,Wnd | Wnd = Arithmetic Right Shift Wb by Wns | 1 | 1 | N,Z |
| | | ASR | Wb,#lit5,Wnd | Wnd = Arithmetic Right Shift Wb by lit5 | 1 | 1 | N,Z |
| 5 | BCLR | BCLR | f,#bit4 | Bit Clear f | 1 | 1 | None |
| | | BCLR | Ws,#bit4 | Bit Clear Ws | 1 | 1 | None |
| 6 | BRA | BRA | C,Expr | Branch if Carry | 1 | 1 (4) | None |
| | | BRA | GE,Expr | Branch if Greater Than or Equal | 1 | 1 (4) | None |
| | | BRA | GEU,Expr | Branch if Unsigned Greater Than or Equal | 1 | 1 (4) | None |
| | | BRA | GT,Expr | Branch if Greater Than | 1 | 1 (4) | None |
| | | BRA | GTU,Expr | Branch if Unsigned Greater Than | 1 | 1 (4) | None |
| | | BRA | LE,Expr | Branch if Less Than or Equal | 1 | 1 (4) | None |
| | | BRA | LEU,Expr | Branch if Unsigned Less Than or Equal | 1 | 1 (4) | None |
| | | BRA | LT,Expr | Branch if Less Than | 1 | 1 (4) | None |
| | | BRA | LTU,Expr | Branch if Unsigned Less Than | 1 | 1 (4) | None |
| | | BRA | N,Expr | Branch if Negative | 1 | 1 (4) | None |
| | | BRA | NC,Expr | Branch if Not Carry | 1 | 1 (4) | None |
| | | BRA | NN,Expr | Branch if Not Negative | 1 | 1 (4) | None |
| | | BRA | NOV,Expr | Branch if Not Overflow | 1 | 1 (4) | None |
| | | BRA | NZ,Expr | Branch if Not Zero | 1 | 1 (4) | None |
| | | BRA | OA,Expr[1] | Branch if Accumulator A overflow | 1 | 1 (4) | None |
| | | BRA | OB,Expr[1] | Branch if Accumulator B overflow | 1 | 1 (4) | None |
| | | BRA | OV,Expr[1] | Branch if Overflow | 1 | 1 (4) | None |
| | | BRA | SA,Expr[1] | Branch if Accumulator A saturated | 1 | 1 (4) | None |
| | | BRA | SB,Expr[1] | Branch if Accumulator B saturated | 1 | 1 (4) | None |
| | | BRA | Expr | Branch Unconditionally | 1 | 4 | None |
| | | BRA | Z,Expr | Branch if Zero | 1 | 1 (4) | None |
| | | BRA | Wn | Computed Branch | 1 | 4 | None |
| 7 | BSET | BSET | f,#bit4 | Bit Set f | 1 | 1 | None |
| | | BSET | Ws,#bit4 | Bit Set Ws | 1 | 1 | None |
| 8 | BSW | BSW.C | Ws,Wb | Write C bit to Ws[Wb] | 1 | 1 | None |
| | | BSW.Z | Ws,Wb | Write Z bit to Ws[Wb] | 1 | 1 | None |

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.


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**TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|---|
| 9 | BTG | BTG | f,#bit4 | Bit Toggle f | 1 | 1 | None |
| | | BTG | Ws,#bit4 | Bit Toggle Ws | 1 | 1 | None |
| 10 | BTSC | BTSC | f,#bit4 | Bit Test f, Skip if Clear | 1 | 1 (2 or 3) | None |
| | | BTSC | Ws,#bit4 | Bit Test Ws, Skip if Clear | 1 | 1 (2 or 3) | None |
| 11 | BTSS | BTSS | f,#bit4 | Bit Test f, Skip if Set | 1 | 1 (2 or 3) | None |
| | | BTSS | Ws,#bit4 | Bit Test Ws, Skip if Set | 1 | 1 (2 or 3) | None |
| 12 | BTST | BTST | f,#bit4 | Bit Test f | 1 | 1 | Z |
| | | BTST.C | Ws,#bit4 | Bit Test Ws to C | 1 | 1 | C |
| | | BTST.Z | Ws,#bit4 | Bit Test Ws to Z | 1 | 1 | Z |
| | | BTST.C | Ws,Wb | Bit Test Ws[Wb] to C | 1 | 1 | C |
| | | BTST.Z | Ws,Wb | Bit Test Ws[Wb] to Z | 1 | 1 | Z |
| 13 | BTSTS | BTSTS | f,#bit4 | Bit Test then Set f | 1 | 1 | Z |
| | | BTSTS.C | Ws,#bit4 | Bit Test Ws to C, then Set | 1 | 1 | C |
| | | BTSTS.Z | Ws,#bit4 | Bit Test Ws to Z, then Set | 1 | 1 | Z |
| 14 | CALL | CALL | lit23 | Call Subroutine | 2 | 4 | SFA |
| | | CALL | Wn | Call Indirect Subroutine | 1 | 4 | SFA |
| | | CALL.L | Wn | Call Indirect Subroutine (long address) | 1 | 4 | SFA |
| 15 | CLR | CLR | f | f = 0x0000 | 1 | 1 | None |
| | | CLR | WREG | WREG = 0x0000 | 1 | 1 | None |
| | | CLR | Ws | Ws = 0x0000 | 1 | 1 | None |
| | | CLR | Acc,Wx,Wxd,Wy,Wyd,AWB(1) | Clear Accumulator | 1 | 1 | OA,OB,SA,SB |
| 16 | CLRWDT | CLRWDT | | Clear Watchdog Timer | 1 | 1 | WDTO,Sleep |
| 17 | COM | COM | f | $f = \overline{f}$ | 1 | 1 | N,Z |
| | | COM | f,WREG | $WREG = \overline{f}$ | 1 | 1 | N,Z |
| | | COM | Ws,Wd | $Wd = \overline{Ws}$ | 1 | 1 | N,Z |
| 18 | CP | CP | f | Compare f with WREG | 1 | 1 | C,DC,N,OV,Z |
| | | CP | Wb,#lit8 | Compare Wb with lit8 | 1 | 1 | C,DC,N,OV,Z |
| | | CP | Wb,Ws | Compare Wb with Ws (Wb – Ws) | 1 | 1 | C,DC,N,OV,Z |
| 19 | CP0 | CP0 | f | Compare f with 0x0000 | 1 | 1 | C,DC,N,OV,Z |
| | | CP0 | Ws | Compare Ws with 0x0000 | 1 | 1 | C,DC,N,OV,Z |
| 20 | CPB | CPB | f | Compare f with WREG, with Borrow | 1 | 1 | C,DC,N,OV,Z |
| | | CPB | Wb,#lit8 | Compare Wb with lit8, with Borrow | 1 | 1 | C,DC,N,OV,Z |
| | | CPB | Wb,Ws | Compare Wb with Ws, with Borrow ($Wb – Ws – \overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 21 | CPSEQ | CPSEQ | Wb,Wn | Compare Wb with Wn, Skip if = | 1 | 1 (2 or 3) | None |
| | CPBEQ | CPBEQ | Wb,Wn,Expr | Compare Wb with Wn, Branch if = | 1 | 1 (5) | None |
| 22 | CPSGT | CPSGT | Wb,Wn | Compare Wb with Wn, Skip if > | 1 | 1 (2 or 3) | None |
| | CPBGT | CPBGT | Wb,Wn,Expr | Compare Wb with Wn, Branch if > | 1 | 1 (5) | None |
| 23 | CPSLT | CPSLT | Wb,Wn | Compare Wb with Wn, Skip if < | 1 | 1 (2 or 3) | None |
| | CPBLT | CPBLT | Wb,Wn,Expr | Compare Wb with Wn, Branch if < | 1 | 1 (5) | None |
| 24 | CPSNE | CPSNE | Wb,Wn | Compare Wb with Wn, Skip if ≠ | 1 | 1 (2 or 3) | None |
| | CPBNE | CPBNE | Wb,Wn,Expr | Compare Wb with Wn, Branch if ≠ | 1 | 1 (5) | None |

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

**TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|---|
| 25 | DAW | DAW | Wn | Wn = Decimal Adjust Wn | 1 | 1 | C |
| 26 | DEC | DEC | f | f = f – 1 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC | f,WREG | WREG = f – 1 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC | Ws,Wd | Wd = Ws – 1 | 1 | 1 | C,DC,N,OV,Z |
| 27 | DEC2 | DEC2 | f | f = f – 2 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC2 | f,WREG | WREG = f – 2 | 1 | 1 | C,DC,N,OV,Z |
| | | DEC2 | Ws,Wd | Wd = Ws – 2 | 1 | 1 | C,DC,N,OV,Z |
| 28 | DISI | DISI | #lit14 | Disable Interrupts for k Instruction Cycles | 1 | 1 | None |
| 29 | DIV | DIV.S | Wm,Wn | Signed 16/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | DIV.SD | Wm,Wn | Signed 32/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | DIV.U | Wm,Wn | Unsigned 16/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | DIV.UD | Wm,Wn | Unsigned 32/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| 30 | DIVF | DIVF | Wm,Wn(1) | Signed 16/16-bit Fractional Divide | 1 | 18 | N,Z,C,OV |
| 31 | DO | DO | #lit15,Expr(1) | Do code to PC + Expr, lit15 + 1 Times | 2 | 2 | None |
| | | DO | Wn,Expr(1) | Do code to PC + Expr, (Wn) + 1 Times | 2 | 2 | None |
| 32 | ED | ED | Wm*Wm,Acc,Wx,Wy,Wxd(1) | Euclidean Distance (no accumulate) | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 33 | EDAC | EDAC | Wm*Wm,Acc,Wx,Wy,Wxd(1) | Euclidean Distance | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 34 | EXCH | EXCH | Wns,Wnd | Swap Wns with Wnd | 1 | 1 | None |
| 35 | FBCL | FBCL | Ws,Wnd | Find Bit Change from Left (MSb) Side | 1 | 1 | C |
| 36 | FF1L | FF1L | Ws,Wnd | Find First One from Left (MSb) Side | 1 | 1 | C |
| 37 | FF1R | FF1R | Ws,Wnd | Find First One from Right (LSb) Side | 1 | 1 | C |
| 38 | GOTO | GOTO | Expr | Go to Address | 2 | 4 | None |
| | | GOTO | Wn | Go to Indirect | 1 | 4 | None |
| | | GOTO.L | Wn | Go to Indirect (long address) | 1 | 4 | None |
| 39 | INC | INC | f | f = f + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | INC | f,WREG | WREG = f + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | INC | Ws,Wd | Wd = Ws + 1 | 1 | 1 | C,DC,N,OV,Z |
| 40 | INC2 | INC2 | f | f = f + 2 | 1 | 1 | C,DC,N,OV,Z |
| | | INC2 | f,WREG | WREG = f + 2 | 1 | 1 | C,DC,N,OV,Z |
| | | INC2 | Ws,Wd | Wd = Ws + 2 | 1 | 1 | C,DC,N,OV,Z |
| 41 | IOR | IOR | f | f = f .IOR. WREG | 1 | 1 | N,Z |
| | | IOR | f,WREG | WREG = f .IOR. WREG | 1 | 1 | N,Z |
| | | IOR | #lit10,Wn | Wd = lit10 .IOR. Wd | 1 | 1 | N,Z |
| | | IOR | Wb,Ws,Wd | Wd = Wb .IOR. Ws | 1 | 1 | N,Z |
| | | IOR | Wb,#lit5,Wd | Wd = Wb .IOR. lit5 | 1 | 1 | N,Z |
| 42 | LAC | LAC | Wso,#Slit4,Acc | Load Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 43 | LNK | LNK | #lit14 | Link Frame Pointer | 1 | 1 | SFA |
| 44 | LSR | LSR | f | f = Logical Right Shift f | 1 | 1 | C,N,OV,Z |
| | | LSR | f,WREG | WREG = Logical Right Shift f | 1 | 1 | C,N,OV,Z |
| | | LSR | Ws,Wd | Wd = Logical Right Shift Ws | 1 | 1 | C,N,OV,Z |
| | | LSR | Wb,Wns,Wnd | Wnd = Logical Right Shift Wb by Wns | 1 | 1 | N,Z |
| | | LSR | Wb,#lit5,Wnd | Wnd = Logical Right Shift Wb by lit5 | 1 | 1 | N,Z |
| 45 | MAC | MAC | Wm*Wn,Acc,Wx,Wxd,Wy,Wyd,AWB(1) | Multiply and Accumulate | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | MAC | Wm*Wm,Acc,Wx,Wxd,Wy,Wyd(1) | Square and Accumulate | 1 | 1 | OA,OB,OAB, SA,SB,SAB |

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.


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**TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|
| 46 | MOV | MOV f,Wn | Move f to Wn | 1 | 1 | None |
| | | MOV f | Move f to f | 1 | 1 | None |
| | | MOV f,WREG | Move f to WREG | 1 | 1 | None |
| | | MOV #lit16,Wn | Move 16-bit Literal to Wn | 1 | 1 | None |
| | | MOV.b #lit8,Wn | Move 8-bit Literal to Wn | 1 | 1 | None |
| | | MOV Wn,f | Move Wn to f | 1 | 1 | None |
| | | MOV Wso,Wdo | Move Ws to Wd | 1 | 1 | None |
| | | MOV WREG,f | Move WREG to f | 1 | 1 | None |
| | | MOV.D Wns,Wd | Move Double from W(ns):W(ns + 1) to Wd | 1 | 2 | None |
| | | MOV.D Ws,Wnd | Move Double from Ws to W(nd + 1):W(nd) | 1 | 2 | None |
| 47 | MOVPAG | MOVPAG #lit10,DSRPAG | Move 10-bit Literal to DSRPAG | 1 | 1 | None |
| | | MOVPAG #lit9,DSWPAG | Move 9-bit Literal to DSWPAG | 1 | 1 | None |
| | | MOVPAG #lit8,TBLPAG | Move 8-bit Literal to TBLPAG | 1 | 1 | None |
| | | MOVPAG Ws, DSRPAG | Move Ws[9:0] to DSRPAG | 1 | 1 | None |
| | | MOVPAG Ws, DSWPAG | Move Ws[8:0] to DSWPAG | 1 | 1 | None |
| | | MOVPAG Ws, TBLPAG | Move Ws[7:0] to TBLPAG | 1 | 1 | None |
| 48 | MOVSAC | MOVSAC Acc,Wx,Wxd,Wy,Wyd,AWB(1) | Prefetch and Store Accumulator | 1 | 1 | None |
| 49 | MPY | MPY Wm*Wn,Acc,Wx,Wxd,Wy,Wyd(1) | Multiply Wm by Wn to Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | MPY Wm*Wm,Acc,Wx,Wxd,Wy,Wyd(1) | Square Wm to Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 50 | MPY.N | MPY.N Wm*Wn,Acc,Wx,Wxd,Wy,Wyd(1) | -(Multiply Wm by Wn) to Accumulator | 1 | 1 | None |
| 51 | MSC | MSC Wm*Wm,Acc,Wx,Wxd,Wy,Wyd,AWB(1) | Multiply and Subtract from Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| 52 | MUL | MUL.SS Wb,Ws,Wnd | {Wnd + 1, Wnd} = signed(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.SS Wb,Ws,Acc(1) | Accumulator = signed(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.SU Wb,Ws,Wnd | {Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.SU Wb,Ws,Acc(1) | Accumulator = signed(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.SU Wb,#lit5,Acc(1) | Accumulator = signed(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.US Wb,Ws,Wnd | {Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.US Wb,Ws,Acc(1) | Accumulator = unsigned(Wb) * signed(Ws) | 1 | 1 | None |
| | | MUL.UU Wb,Ws,Wnd | {Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.UU Wb,#lit5,Acc(1) | Accumulator = unsigned(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.UU Wb,Ws,Acc(1) | Accumulator = unsigned(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MULW.SS Wb,Ws,Wnd | Wnd = signed(Wb) * signed(Ws) | 1 | 1 | None |
| | | MULW.SU Wb,Ws,Wnd | Wnd = signed(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MULW.US Wb,Ws,Wnd | Wnd = unsigned(Wb) * signed(Ws) | 1 | 1 | None |
| | | MULW.UU Wb,Ws,Wnd | Wnd = unsigned(Wb) * unsigned(Ws) | 1 | 1 | None |
| | | MUL.SU Wb,#lit5,Wnd | {Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.SU Wb,#lit5,Wnd | Wnd = signed(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.UU Wb,#lit5,Wnd | {Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL.UU Wb,#lit5,Wnd | Wnd = unsigned(Wb) * unsigned(lit5) | 1 | 1 | None |
| | | MUL f | W3:W2 = f * WREG | 1 | 1 | None |

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

**TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|
| 53 | NEG | NEG Acc(1) | Negate Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | NEG f | f = $\bar{f}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | NEG f,WREG | WREG = $\bar{f}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | NEG Ws,Wd | Wd = $\overline{Ws}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| 54 | NOP | NOP | No Operation | 1 | 1 | None |
| | | NOPR | No Operation | 1 | 1 | None |
| 55 | POP | POP f | Pop f from Top-of-Stack (TOS) | 1 | 1 | None |
| | | POP Wdo | Pop from Top-of-Stack (TOS) to Wdo | 1 | 1 | None |
| | | POP.D Wnd | Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1) | 1 | 2 | None |
| | | POP.S | Pop Shadow Registers | 1 | 1 | All |
| 56 | PUSH | PUSH f | Push f to Top-of-Stack (TOS) | 1 | 1 | None |
| | | PUSH Wso | Push Wso to Top-of-Stack (TOS) | 1 | 1 | None |
| | | PUSH.D Wns | Push W(ns):W(ns + 1) to Top-of-Stack (TOS) | 1 | 2 | None |
| | | PUSH.S | Push Shadow Registers | 1 | 1 | None |
| 57 | PWRSAV | PWRSAV #lit1 | Go into Sleep or Idle mode | 1 | 1 | WDTO,Sleep |
| 58 | RCALL | RCALL Expr | Relative Call | 1 | 4 | SFA |
| | | RCALL Wn | Computed Call | 1 | 4 | SFA |
| 59 | REPEAT | REPEAT #lit15 | Repeat Next Instruction lit15 + 1 Times | 1 | 1 | None |
| | | REPEAT Wn | Repeat Next Instruction (Wn) + 1 Times | 1 | 1 | None |
| 60 | RESET | RESET | Software Device Reset | 1 | 1 | None |
| 61 | RETFIE | RETFIE | Return from Interrupt | 1 | 6 (5) | SFA |
| 62 | RETLW | RETLW #lit10,Wn | Return with Literal in Wn | 1 | 6 (5) | SFA |
| 63 | RETURN | RETURN | Return from Subroutine | 1 | 6 (5) | SFA |
| 64 | RLC | RLC f | f = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC f,WREG | WREG = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC Ws,Wd | Wd = Rotate Left through Carry Ws | 1 | 1 | C,N,Z |
| 65 | RLNC | RLNC f | f = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC f,WREG | WREG = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC Ws,Wd | Wd = Rotate Left (No Carry) Ws | 1 | 1 | N,Z |
| 66 | RRC | RRC f | f = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC f,WREG | WREG = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC Ws,Wd | Wd = Rotate Right through Carry Ws | 1 | 1 | C,N,Z |
| 67 | RRNC | RRNC f | f = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC f,WREG | WREG = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC Ws,Wd | Wd = Rotate Right (No Carry) Ws | 1 | 1 | N,Z |
| 68 | SAC | SAC Acc,#Slit4,Wdo(1) | Store Accumulator | 1 | 1 | None |
| | | SAC.R Acc,#Slit4,Wdo(1) | Store Rounded Accumulator | 1 | 1 | None |
| 69 | SE | SE Ws,Wnd | Wnd = Sign-Extended Ws | 1 | 1 | C,N,Z |
| 70 | SETM | SETM f | f = 0xFFFF | 1 | 1 | None |
| | | SETM WREG | WREG = 0xFFFF | 1 | 1 | None |
| | | SETM Ws | Ws = 0xFFFF | 1 | 1 | None |
| 71 | SFTAC | SFTAC Acc,Wn(1) | Arithmetic Shift Accumulator by (Wn) | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SFTAC Acc,#Slit6(1) | Arithmetic Shift Accumulator by Slit6 | 1 | 1 | OA,OB,OAB, SA,SB,SAB |

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.

**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.


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**TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | | Description | # of Words | # of Cycles(2) | Status Flags Affected |
|---|---|---|---|---|---|---|---|
| 72 | SL | SL | f | f = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL | f,WREG | WREG = Left Shift f | 1 | 1 | C,N,OV,Z |
| | | SL | Ws,Wd | Wd = Left Shift Ws | 1 | 1 | C,N,OV,Z |
| | | SL | Wb,Wns,Wnd | Wnd = Left Shift Wb by Wns | 1 | 1 | N,Z |
| | | SL | Wb,#lit5,Wnd | Wnd = Left Shift Wb by lit5 | 1 | 1 | N,Z |
| 73 | SUB | SUB | Acc(1) | Subtract Accumulators | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SUB | f | f = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | f,WREG | WREG = f – WREG | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | #lit10,Wn | Wn = Wn – lit10 | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | Wb,Ws,Wd | Wd = Wb – Ws | 1 | 1 | C,DC,N,OV,Z |
| | | SUB | Wb,#lit5,Wd | Wd = Wb – lit5 | 1 | 1 | C,DC,N,OV,Z |
| 74 | SUBB | SUBB | f | f = f – WREG – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | f,WREG | WREG = f – WREG – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | #lit10,Wn | Wn = Wn – lit10 – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | Wb,Ws,Wd | Wd = Wb – Ws – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBB | Wb,#lit5,Wd | Wd = Wb – lit5 – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 75 | SUBR | SUBR | f | f = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | f,WREG | WREG = WREG – f | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | Wb,Ws,Wd | Wd = Ws – Wb | 1 | 1 | C,DC,N,OV,Z |
| | | SUBR | Wb,#lit5,Wd | Wd = lit5 – Wb | 1 | 1 | C,DC,N,OV,Z |
| 76 | SUBBR | SUBBR | f | f = WREG – f – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | f,WREG | WREG = WREG – f – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | Wb,Ws,Wd | Wd = Ws – Wb – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| | | SUBBR | Wb,#lit5,Wd | Wd = lit5 – Wb – ($\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 77 | SWAP | SWAP.b | Wn | Wn = Nibble Swap Wn | 1 | 1 | None |
| | | SWAP | Wn | Wn = Byte Swap Wn | 1 | 1 | None |
| 78 | TBLRDH | TBLRDH | Ws,Wd | Read Prog[23:16] to Wd[7:0] | 1 | 5 | None |
| 79 | TBLRDL | TBLRDL | Ws,Wd | Read Prog[15:0] to Wd | 1 | 5 | None |
| 80 | TBLWTH | TBLWTH | Ws,Wd | Write Ws[7:0] to Prog[23:16] | 1 | 2 | None |
| 81 | TBLWTL | TBLWTL | Ws,Wd | Write Ws to Prog[15:0] | 1 | 2 | None |
| 82 | ULNK | ULNK | | Unlink Frame Pointer | 1 | 1 | SFA |
| 83 | XOR | XOR | f | f = f .XOR. WREG | 1 | 1 | N,Z |
| | | XOR | f,WREG | WREG = f .XOR. WREG | 1 | 1 | N,Z |
| | | XOR | #lit10,Wn | Wd = lit10 .XOR. Wd | 1 | 1 | N,Z |
| | | XOR | Wb,Ws,Wd | Wd = Wb .XOR. Ws | 1 | 1 | N,Z |
| | | XOR | Wb,#lit5,Wd | Wd = Wb .XOR. lit5 | 1 | 1 | N,Z |
| 84 | ZE | ZE | Ws,Wnd | Wnd = Zero-Extend Ws | 1 | 1 | C,Z,N |

**Note 1:** These instructions are available in dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X devices only.
**2:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

**NOTES:**


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## 29.0 DEVELOPMENT SUPPORT

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Go to the following website for more information and details:

https://www.microchip.com/development-tools/

**NOTES:**


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# 30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

## Absolute Maximum Ratings(1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant, with respect to $V_{SS}$(3) ..... -0.3V to ($V_{DD}$ + 0.3V)
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} \geq 3.0V$(3) ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $V_{DD} < 3.0V$(3) ..... -0.3V to +3.6V
Maximum current out of $V_{SS}$ pin ..... 300 mA
Maximum current into $V_{DD}$ pin(2) ..... 300 mA
Maximum current sunk/sourced by any 4x I/O pin ..... 15 mA
Maximum current sunk/sourced by any 8x I/O pin ..... 25 mA
Maximum current sunk by all ports(2,4) ..... 200 mA

**Note 1:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**2:** Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

**3:** See the **“Pin Diagrams”** section for the 5V tolerant pins.

**4:** Exceptions are: dsPIC33EPXXXGP502, dsPIC33EPXXXMC202/502 and PIC24EPXXXGP/MC202 devices, which have a maximum sink/source capability of 130 mA.

## 30.1 DC Characteristics

**TABLE 30-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts) | Temp Range (in °C) | Maximum MIPS |
|---|---|---|---|
| | | | dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X |
| — | 3.0V to 3.6V(1) | -40°C to +85°C | 70 |
| — | 3.0V to 3.6V(1) | -40°C to +125°C | 60 |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**TABLE 30-2: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Industrial Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +85 | °C |
| Extended Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +140 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +125 | °C |
| Power Dissipation:<br>Internal chip power dissipation:<br>PINT = VDD x (IDD – Σ IOH)<br>I/O Pin Power Dissipation:<br>I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL) | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJ – TA)/θJA | | | W |

**TABLE 30-3: THERMAL PACKAGING CHARACTERISTICS**

| Characteristic | Symbol | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|
| Package Thermal Resistance, 64-Pin QFN | θJA | 28.0 | — | °C/W | 1 |
| Package Thermal Resistance, 64-Pin TQFP 10x10 mm | θJA | 48.3 | — | °C/W | 1 |
| Package Thermal Resistance, 48-Pin UQFN 6x6 mm | θJA | 41 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin QFN | θJA | 29.0 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin TQFP 10x10 mm | θJA | 49.8 | — | °C/W | 1 |
| Package Thermal Resistance, 44-Pin VTLA 6x6 mm | θJA | 25.2 | — | °C/W | 1 |
| Package Thermal Resistance, 36-Pin VTLA 5x5 mm | θJA | 28.5 | — | °C/W | 1 |
| Package Thermal Resistance, 36-Pin UQFN 5x5 mm | θJA | 29.2 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin QFN-S | θJA | 30.0 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SSOP | θJA | 71.0 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SOIC | θJA | 69.7 | — | °C/W | 1 |
| Package Thermal Resistance, 28-Pin SPDIP | θJA | 60.0 | — | °C/W | 1 |

**Note 1:** Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.


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**TABLE 30-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Operating Voltage** | | | | | | | |
| DC10 | VDD | **Supply Voltage** | 3.0 | — | 3.6 | V | |
| DC16 | VPOR | **VDD Start Voltage** to Ensure Internal Power-on Reset Signal | — | — | VSS | V | |
| DC17 | SVDD | **VDD Rise Rate** to Ensure Internal Power-on Reset Signal | 0.03 | — | — | V/ms | 0V-1V in 100 ms |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**TABLE 30-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS**

| **Standard Operating Conditions (unless otherwise stated):**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Comments** |
| | CEFC | External Filter Capacitor Value(1) | 4.7 | 10 | — | µF | Capacitor must have a low series resistance (< 1 Ohm) |

**Note 1:** Typical VCAP voltage = 1.8 volts when VDD ≥ VDDMIN.

**TABLE 30-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typ.** | **Max.** | **Units** | **Conditions** | | |
| **Operating Current (IDD)(1)** | | | | | | |
| DC20d | 9 | 15 | mA | -40°C | 3.3V | 10 MIPS |
| DC20a | 9 | 15 | mA | +25°C | | |
| DC20b | 9 | 15 | mA | +85°C | | |
| DC20c | 9 | 15 | mA | +125°C | | |
| DC22d | 16 | 25 | mA | -40°C | 3.3V | 20 MIPS |
| DC22a | 16 | 25 | mA | +25°C | | |
| DC22b | 16 | 25 | mA | +85°C | | |
| DC22c | 16 | 25 | mA | +125°C | | |
| DC24d | 27 | 40 | mA | -40°C | 3.3V | 40 MIPS |
| DC24a | 27 | 40 | mA | +25°C | | |
| DC24b | 27 | 40 | mA | +85°C | | |
| DC24c | 27 | 40 | mA | +125°C | | |
| DC25d | 36 | 55 | mA | -40°C | 3.3V | 60 MIPS |
| DC25a | 36 | 55 | mA | +25°C | | |
| DC25b | 36 | 55 | mA | +85°C | | |
| DC25c | 36 | 55 | mA | +125°C | | |
| DC26d | 41 | 60 | mA | -40°C | 3.3V | 70 MIPS |
| DC26a | 41 | 60 | mA | +25°C | | |
| DC26b | 41 | 60 | mA | +85°C | | |

**Note 1:** IDD is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDD measurements are as follows:

- Oscillator is configured in EC mode with PLL, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins (except OSC1) are configured as outputs and driven low
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all '1's)
- `NOP` instructions are executed in `while(1)` loop
- JTAG is disabled


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**TABLE 30-7: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Parameter No.** | **Typ.** | **Max.** | **Units** | **Conditions** | | |
| **Idle Current (IIDLE)(1)** | | | | | | |
| DC40d | 3 | 8 | mA | -40°C | 3.3V | 10 MIPS |
| DC40a | 3 | 8 | mA | +25°C | | |
| DC40b | 3 | 8 | mA | +85°C | | |
| DC40c | 3 | 8 | mA | +125°C | | |
| DC42d | 6 | 12 | mA | -40°C | 3.3V | 20 MIPS |
| DC42a | 6 | 12 | mA | +25°C | | |
| DC42b | 6 | 12 | mA | +85°C | | |
| DC42c | 6 | 12 | mA | +125°C | | |
| DC44d | 11 | 18 | mA | -40°C | 3.3V | 40 MIPS |
| DC44a | 11 | 18 | mA | +25°C | | |
| DC44b | 11 | 18 | mA | +85°C | | |
| DC44c | 11 | 18 | mA | +125°C | | |
| DC45d | 17 | 27 | mA | -40°C | 3.3V | 60 MIPS |
| DC45a | 17 | 27 | mA | +25°C | | |
| DC45b | 17 | 27 | mA | +85°C | | |
| DC45c | 17 | 27 | mA | +125°C | | |
| DC46d | 20 | 35 | mA | -40°C | 3.3V | 70 MIPS |
| DC46a | 20 | 35 | mA | +25°C | | |
| DC46b | 20 | 35 | mA | +85°C | | |

**Note 1:** Base Idle current (IIDLE) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- The NVMSIDL bit (NVMCON[12]) = 1 (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON[11]) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

**TABLE 30-8: DC CHARACTERISTICS: POWER-DOWN CURRENT ($I_{PD}$)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | |
|---|---|---|---|---|---|
| **Parameter No.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| **Power-Down Current ($I_{PD}$)(1) – dsPIC33EP32GP50X, dsPIC33EP32MC20X/50X and PIC24EP32GP/MC20X** | | | | | |
| DC60d | 30 | 100 | µA | -40°C | 3.3V |
| DC60a | 35 | 100 | µA | +25°C | |
| DC60b | 150 | 200 | µA | +85°C | |
| DC60c | 250 | 500 | µA | +125°C | |
| **Power-Down Current ($I_{PD}$)(1) – dsPIC33EP64GP50X, dsPIC33EP64MC20X/50X and PIC24EP64GP/MC20X** | | | | | |
| DC60d | 25 | 100 | µA | -40°C | 3.3V |
| DC60a | 30 | 100 | µA | +25°C | |
| DC60b | 150 | 350 | µA | +85°C | |
| DC60c | 350 | 800 | µA | +125°C | |
| **Power-Down Current ($I_{PD}$)(1) – dsPIC33EP128GP50X, dsPIC33EP128MC20X/50X and PIC24EP128GP/MC20X** | | | | | |
| DC60d | 30 | 100 | µA | -40°C | 3.3V |
| DC60a | 35 | 100 | µA | +25°C | |
| DC60b | 150 | 350 | µA | +85°C | |
| DC60c | 550 | 1000 | µA | +125°C | |
| **Power-Down Current ($I_{PD}$)(1) – dsPIC33EP256GP50X, dsPIC33EP256MC20X/50X and PIC24EP256GP/MC20X** | | | | | |
| DC60d | 35 | 100 | µA | -40°C | 3.3V |
| DC60a | 40 | 100 | µA | +25°C | |
| DC60b | 250 | 450 | µA | +85°C | |
| DC60c | 1000 | 1200 | µA | +125°C | |
| **Power-Down Current ($I_{PD}$)(1) – dsPIC33EP512GP50X, dsPIC33EP512MC20X/50X and PIC24EP512GP/MC20X** | | | | | |
| DC60d | 40 | 100 | µA | -40°C | 3.3V |
| DC60a | 45 | 100 | µA | +25°C | |
| DC60b | 350 | 800 | µA | +85°C | |
| DC60c | 1100 | 1500 | µA | +125°C | |

**Note 1:** $I_{PD}$ (Sleep) current is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active; OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- All peripheral modules are disabled (PMDx bits are all set)
- The VREGS bit (RCON[8]) = 0 (i.e., core regulator is set to standby while the device is in Sleep mode)
- The VREGSF bit (RCON[11]) = 0 (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled


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**TABLE 30-9: DC CHARACTERISTICS: WATCHDOG TIMER DELTA CURRENT (ΔIWDT)(1)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | |
|---|---|---|---|---|---|
| **Parameter No.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| DC61d | 8 | — | µA | -40°C | 3.3V |
| DC61a | 10 | — | µA | +25°C | |
| DC61b | 12 | — | µA | +85°C | |
| DC61c | 13 | — | µA | +125°C | |

**Note 1:** The ΔIWDT current is the additional current consumed when the module is enabled. This current should be added to the base IPD current. All parameters are characterized but not tested during manufacturing.

**TABLE 30-10: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Parameter No.** | **Typ.** | **Max.** | **Doze Ratio** | **Units** | **Conditions** | | |
| **Doze Current (IDOZE)(1)** | | | | | | | |
| DC73a(2) | 35 | — | 1:2 | mA | -40°C | 3.3V | FOSC = 140 MHz |
| DC73g | 20 | 30 | 1:128 | mA | | | |
| DC70a(2) | 35 | — | 1:2 | mA | +25°C | 3.3V | FOSC = 140 MHz |
| DC70g | 20 | 30 | 1:128 | mA | | | |
| DC71a(2) | 35 | — | 1:2 | mA | +85°C | 3.3V | FOSC = 140 MHz |
| DC71g | 20 | 30 | 1:128 | mA | | | |
| DC72a(2) | 28 | — | 1:2 | mA | +125°C | 3.3V | FOSC = 120 MHz |
| DC72g | 15 | 30 | 1:128 | mA | | | |

**Note 1:** IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{\text{MCLR}}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating; however, every peripheral is being clocked (all PMDx bits are zeroed)
- CPU is executing `while(1)` statement
- JTAG is disabled

**2:** Parameter is characterized but not tested in manufacturing.

**TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| | VIL | **Input Low Voltage** | | | | | |
| DI10 | | Any I/O Pin and $\overline{MCLR}$ | VSS | — | 0.2 VDD | V | |
| DI18 | | I/O Pins with SDAx, SCLx | VSS | — | 0.3 VDD | V | SMBus disabled |
| DI19 | | I/O Pins with SDAx, SCLx | VSS | — | 0.8 | V | SMBus enabled |
| | VIH | **Input High Voltage** | | | | | |
| DI20 | | I/O Pins Not 5V Tolerant | 0.8 VDD | — | VDD | V | **Note 3** |
| | | I/O Pins 5V Tolerant and $\overline{MCLR}$ | 0.8 VDD | — | 5.5 | V | **Note 3** |
| | | I/O Pins with SDAx, SCLx | 0.8 VDD | — | 5.5 | V | SMBus disabled |
| | | I/O Pins with SDAx, SCLx | 2.1 | — | 5.5 | V | SMBus enabled |
| | ICNPU | **Change Notification Pull-up Current** | | | | | |
| DI30 | | | 150 | 250 | 550 | µA | VDD = 3.3V, VPIN = VSS |
| | ICNPD | **Change Notification Pull-Down Current(4)** | | | | | |
| DI31 | | | 20 | 50 | 100 | µA | VDD = 3.3V, VPIN = VDD |

**Note 1:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

**2:** Negative current is defined as current sourced by the pin.

**3:** See the **"Pin Diagrams"** section for the 5V tolerant pins.

**4:** VIL source < (VSS – 0.3). Characterized but not tested.

**5:** VIH source > (VDD + 0.3) for non-5V tolerant pins only.

**6:** Digital 5V tolerant pins do not have an internal high-side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

**7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

**8:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.


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**TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| | IIL | **Input Leakage Current(1,2)** | | | | | |
| DI50 | | I/O Pins 5V Tolerant(3) | -1 | — | +1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance |
| DI51 | | I/O Pins Not 5V Tolerant(3) | -1 | — | +1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance, -40°C ≤ TA ≤ +85°C |
| DI51a | | I/O Pins Not 5V Tolerant(3) | -1 | — | +1 | µA | Analog pins shared with external reference pins, -40°C ≤ TA ≤ +85°C |
| DI51b | | I/O Pins Not 5V Tolerant(3) | -1 | — | +1 | µA | VSS ≤ VPIN ≤ VDD, Pin at high-impedance, -40°C ≤ TA ≤ +125°C |
| DI51c | | I/O Pins Not 5V Tolerant(3) | -1 | — | +1 | µA | Analog pins shared with external reference pins, -40°C ≤ TA ≤ +125°C |
| DI55 | | $\overline{\text{MCLR}}$ | -5 | — | +5 | µA | VSS ≤ VPIN ≤ VDD |
| DI56 | | OSC1 | -5 | — | +5 | µA | VSS ≤ VPIN ≤ VDD, XT and HS modes |

**Note 1:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

**2:** Negative current is defined as current sourced by the pin.

**3:** See the **"Pin Diagrams"** section for the 5V tolerant pins.

**4:** VIL source < (VSS – 0.3). Characterized but not tested.

**5:** VIH source > (VDD + 0.3) for non-5V tolerant pins only.

**6:** Digital 5V tolerant pins do not have an internal high-side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

**7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

**8:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

**TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| DI60a | IICL | **Input Low Injection Current** | 0 | — | -5(4,7) | mA | All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP and RB7 |
| DI60b | IICH | **Input High Injection Current** | 0 | — | +5(5,6,7) | mA | All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB7 and all 5V tolerant pins(6) |
| DI60c | ∑IICT | **Total Input Injection Current (sum of all I/O and control pins)** | -20(8) | — | +20(8) | mA | Absolute instantaneous sum of all ± input injection currents from all I/O pins ( \| IICL + \| IICH \| ) ≤ ∑IICT |

**Note 1:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

**2:** Negative current is defined as current sourced by the pin.

**3:** See the **"Pin Diagrams"** section for the 5V tolerant pins.

**4:** VIL source < (VSS – 0.3). Characterized but not tested.

**5:** VIH source > (VDD + 0.3) for non-5V tolerant pins only.

**6:** Digital 5V tolerant pins do not have an internal high-side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

**7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.

**8:** Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.


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**TABLE 30-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| DO10 | VOL | **Output Low Voltage**<br>4x Sink Driver Pins(2) | — | — | 0.4 | V | VDD = 3.3V,<br>IOL ≤ 6 mA, -40°C ≤ TA ≤ +85°C,<br>IOL ≤ 5 mA, +85°C < TA ≤ +125°C |
| | | **Output Low Voltage**<br>8x Sink Driver Pins(3) | — | — | 0.4 | V | VDD = 3.3V,<br>IOL ≤ 12 mA, -40°C ≤ TA ≤ +85°C,<br>IOL ≤ 8 mA, +85°C < TA ≤ +125°C |
| DO20 | VOH | **Output High Voltage**<br>4x Source Driver Pins(2) | 2.4 | — | — | V | IOH ≥ -10 mA, VDD = 3.3V |
| | | **Output High Voltage**<br>8x Source Driver Pins(3) | 2.4 | — | — | V | IOH ≥ -15 mA, VDD = 3.3V |
| DO20A | VOH1 | **Output High Voltage**<br>4x Source Driver Pins(2) | 1.5(1) | — | — | V | IOH ≥ -14 mA, VDD = 3.3V |
| | | | 2.0(1) | — | — | | IOH ≥ -12 mA, VDD = 3.3V |
| | | | 3.0(1) | — | — | | IOH ≥ -7 mA, VDD = 3.3V |
| | | **Output High Voltage**<br>8x Source Driver Pins(3) | 1.5(1) | — | — | V | IOH ≥ -22 mA, VDD = 3.3V |
| | | | 2.0(1) | — | — | | IOH ≥ -18 mA, VDD = 3.3V |
| | | | 3.0(1) | — | — | | IOH ≥ -10 mA, VDD = 3.3V |

**Note 1:** Parameters are characterized but not tested.

**2:** Includes all I/O pins that are not 8x Sink Driver pins (see below).

**3:** Includes the following pins:
**For devices with less than 64 pins:** RA3, RA4, RA9, RB[7:15] and RC3
**For 64-pin devices:** RA4, RA9, RB[7:15], RC3 and RC15

**TABLE 30-13: ELECTRICAL CHARACTERISTICS: BOR**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)(1)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.(2)** | **Typ.** | **Max.** | **Units** | **Conditions** |
| BO10 | VBOR | BOR Event on VDD Transition High-to-Low | 2.65 | — | 2.95 | V | VDD (**Notes 2** and **3**) |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance.

**2:** Parameters are for design guidance only and are not tested in manufacturing.

**3:** The VBOR specification is relative to VDD.

**TABLE 30-14: DC CHARACTERISTICS: PROGRAM MEMORY**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| | | **Program Flash Memory** | | | | | |
| D130 | EP | Cell Endurance | 10,000 | — | — | E/W | -40°C to +125°C |
| D131 | VPR | VDD for Read | 3.0 | — | 3.6 | V | |
| D132b | VPEW | VDD for Self-Timed Write | 3.0 | — | 3.6 | V | |
| D134 | TRETD | Characteristic Retention | 20 | — | — | Year | Provided no other specifications are violated, -40°C to +125°C |
| D135 | IDDP | Supply Current during Programming(2) | — | 10 | — | mA | |
| D136 | IPEAK | Instantaneous Peak Current During Start-up | — | — | 150 | mA | |
| D137a | TPE | Page Erase Time | — | 146,893 | — | FRC cycles | TA = +85°C |
| D137b | TPE | Page Erase Time | — | 146,893 | — | FRC cycles | TA = +125°C |
| D138a | TWW | Word Write Cycle Time | — | 346 | — | FRC cycles | TA = +85°C |
| D138b | TWW | Word Write Cycle Time | — | 346 | — | FRC cycles | TA = +125°C |

**Note 1:** Data in “Typical” column are at 3.3V, +25°C unless otherwise stated.

**2:** Parameter characterized but not tested in manufacturing.


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## 30.2 AC Characteristics and Timing Parameters

This section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters.

**TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC**

| | |
|---|---|
| **AC CHARACTERISTICS** | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended<br>Operating voltage VDD range as described in **Section 30.1 "DC Characteristics"**. |

**FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

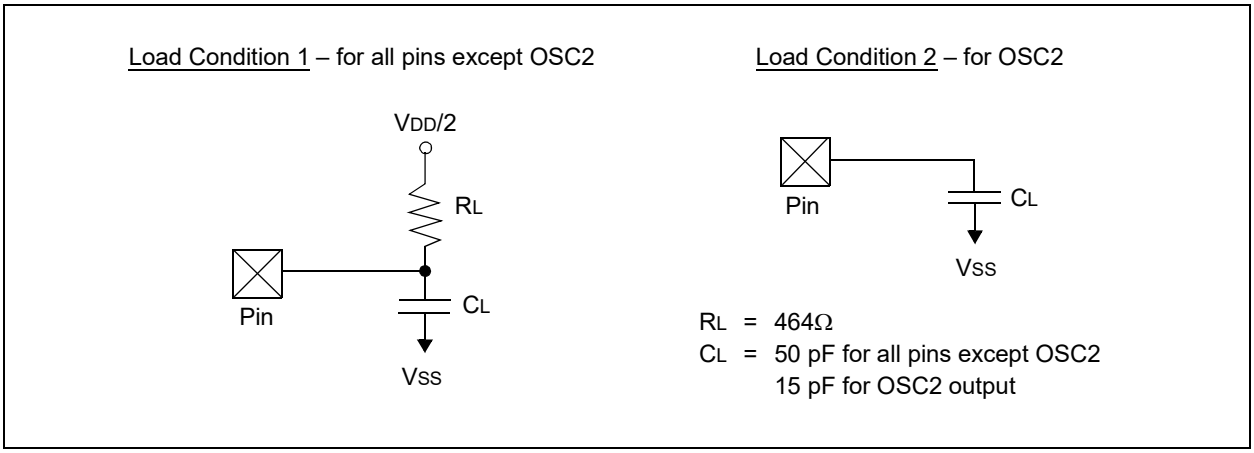


**TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS**

| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| DO50 | COSCO | OSC2 Pin | — | — | 15 | pF | In XT and HS modes, when external clock is used to drive OSC1 |
| DO56 | CIO | All I/O Pins and OSC2 | — | — | 50 | pF | EC mode |
| DO58 | CB | SCLx, SDAx | — | — | 400 | pF | In $I^2C$ mode |

**FIGURE 30-2: EXTERNAL CLOCK TIMING**

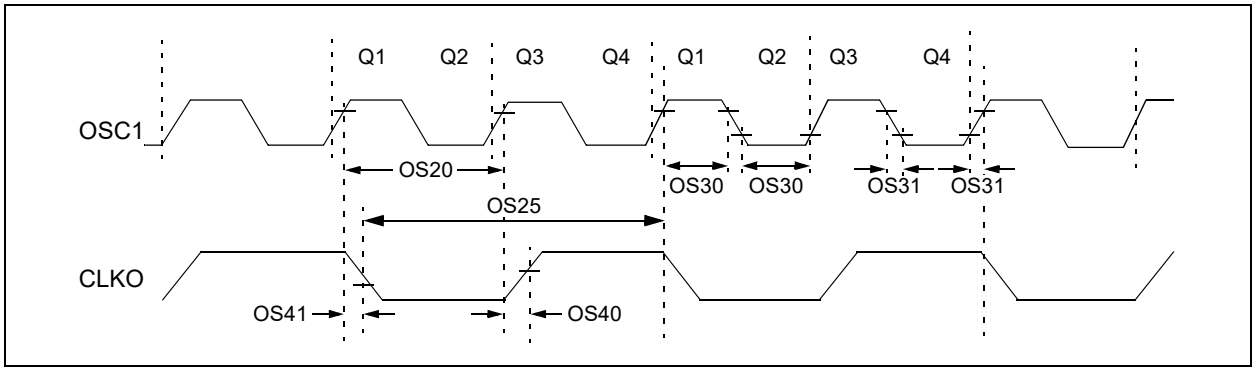


**TABLE 30-17: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symb** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| OS10 | FIN | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes) | DC | — | 60 | MHz | EC |
| | | Oscillator Crystal Frequency | 3.5<br>10 | —<br>— | 10<br>25 | MHz<br>MHz | XT<br>HS |
| OS20 | TOSC | TOSC = 1/FOSC | 8.33 | — | DC | ns | +125°C |
| | | TOSC = 1/FOSC | 7.14 | — | DC | ns | +85°C |
| OS25 | TCY | Instruction Cycle Time(2) | 16.67 | — | DC | ns | +125°C |
| | | Instruction Cycle Time(2) | 14.28 | — | DC | ns | +85°C |
| OS30 | TosL, TosH | External Clock in (OSC1) High or Low Time | 0.45 x TOSC | — | 0.55 x TOSC | ns | EC |
| OS31 | TosR, TosF | External Clock in (OSC1) Rise or Fall Time | — | — | 20 | ns | EC |
| OS40 | TckR | CLKO Rise Time(3,4) | — | 5.2 | — | ns | |
| OS41 | TckF | CLKO Fall Time(3,4) | — | 5.2 | — | ns | |
| OS42 | GM | External Oscillator Transconductance(4) | — | 12 | — | mA/V | HS, VDD = 3.3V, TA = +25°C |
| | | | — | 6 | — | mA/V | XT, VDD = 3.3V, TA = +25°C |

**Note 1:** Data in “Typical” column are at 3.3V, +25°C unless otherwise stated.

**2:** Instruction cycle period (TCY) equals two times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “Minimum” values with an external clock applied to the OSC1 pin. When an external clock input is used, the “Maximum” cycle time limit is “DC” (no clock) for all devices.

**3:** Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

**4:** This parameter is characterized, but not tested in manufacturing.


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**TABLE 30-18: PLL CLOCK TIMING SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range | 0.8 | — | 8.0 | MHz | ECPLL, XTPLL modes |
| OS51 | FVCO | On-Chip VCO System Frequency | 120 | — | 340 | MHz | |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | 0.9 | 1.5 | 3.1 | ms | |
| OS53 | DCLK | CLKO Stability (Jitter)(2) | -3 | 0.5 | 3 | % | |

**Note 1:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases, or communication clocks used by the application, use the following formula:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{FOSC}{Time\ Base\ or\ Communication\ Clock}}}$$

For example, if FOSC = 120 MHz and the SPIx bit rate = 10 MHz, the effective jitter is as follows:

$$Effective\ Jitter = \frac{DCLK}{\sqrt{\frac{120}{10}}} = \frac{DCLK}{\sqrt{12}} = \frac{DCLK}{3.464}$$

**TABLE 30-19: INTERNAL FRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| **Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1)** | | | | | | | |
| F20a | FRC | -1.5 | 0.5 | +1.5 | % | -40°C ≤ TA ≤ -10°C | VDD = 3.0-3.6V |
| | | -1 | 0.5 | +1 | % | -10°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F20b | FRC | -2 | 1 | +2 | % | +85°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

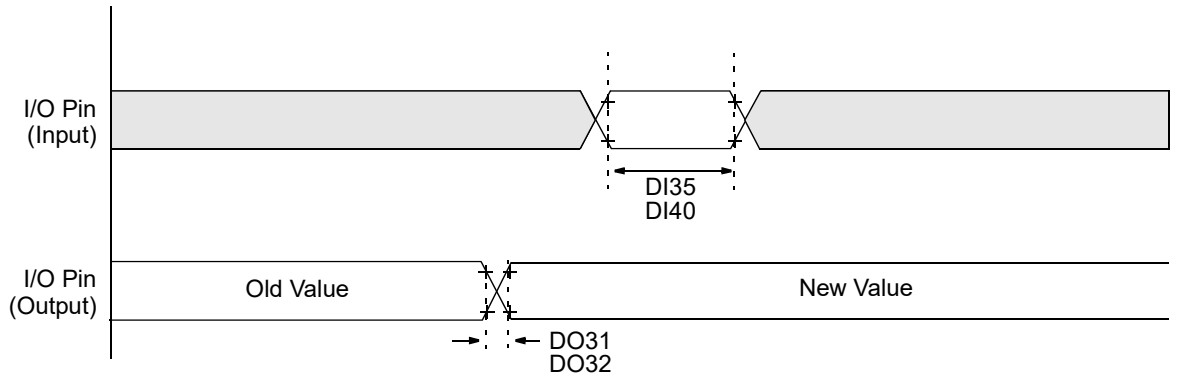
**Note 1:** Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

**TABLE 30-20: INTERNAL LPRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| **LPRC @ 32.768 kHz(1)** | | | | | | | |
| F21a | LPRC | -30 | — | +30 | % | -40°C ≤ TA ≤ -10°C | VDD = 3.0-3.6V |
| | | -20 | — | +20 | % | -10°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F21b | LPRC | -30 | — | +30 | % | +85°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

**Note 1:** The change of LPRC frequency as VDD changes.

**FIGURE 30-3: I/O TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-21: I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| DO31 | TIOR | Port Output Rise Time | — | 5 | 10 | ns | |
| DO32 | TIOF | Port Output Fall Time | — | 5 | 10 | ns | |
| DI35 | TINP | INTx Pin High or Low Time (input) | 20 | — | — | ns | |
| DI40 | TRBP | CNx High or Low Time (input) | 2 | — | — | TCY | |

**Note 1:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated.

**FIGURE 30-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS**

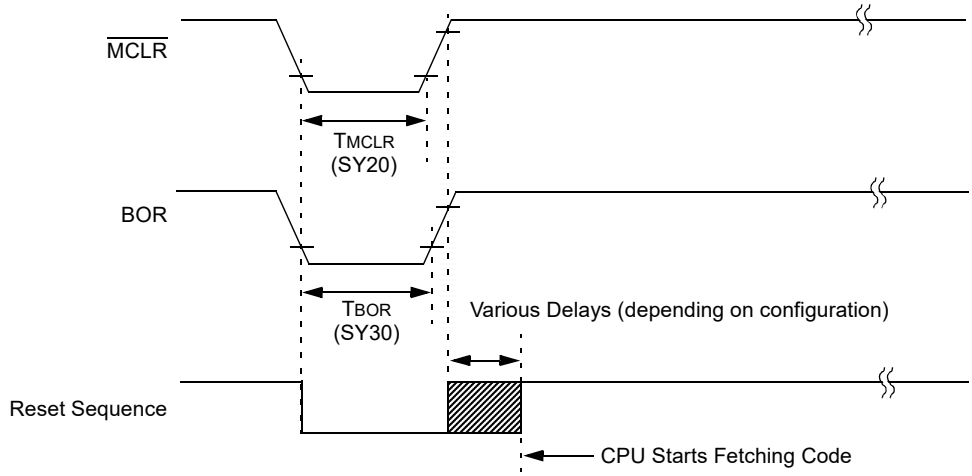




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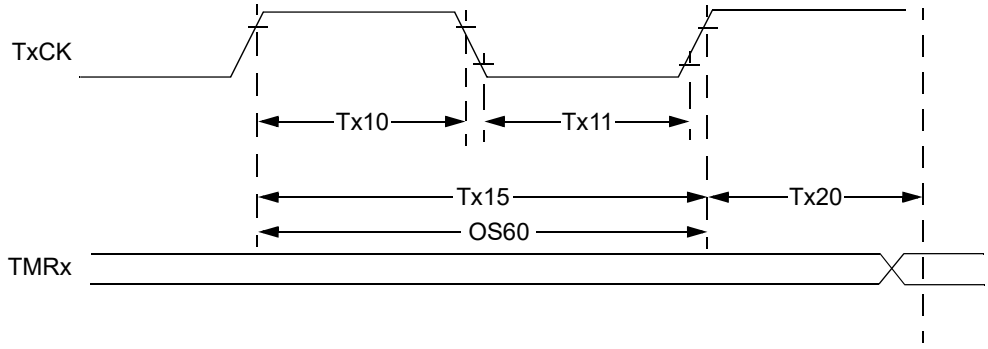
**TABLE 30-22: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SY00 | TPU | Power-up Period | — | 400 | 600 | µs | |
| SY10 | TOST | Oscillator Start-up Time | — | 1024 TOSC | — | — | TOSC = OSC1 period |
| SY12 | TWDT | Watchdog Timer Time-out Period | 0.81 | 0.98 | 1.22 | ms | WDTPRE = 0, WDTPOST[3:0] = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85ºC |
| | | | 3.26 | 3.91 | 4.88 | ms | WDTPRE = 1, WDTPOST[3:0] = 0000, using LPRC tolerances indicated in F21 (see Table 30-20) at +85ºC |
| SY13 | TIOZ | I/O High-Impedance from MCLR Low or Watchdog Timer Reset | 0.68 | 0.72 | 1.2 | µs | |
| SY20 | TMCLR | MCLR Pulse Width (low) | 2 | — | — | µs | |
| SY30 | TBOR | BOR Pulse Width (low) | 1 | — | — | µs | |
| SY35 | TFSCM | Fail-Safe Clock Monitor Delay | — | 500 | 900 | µs | -40°C to +85°C |
| SY36 | TVREG | Voltage Regulator Standby-to-Active mode Transition Time | — | — | 30 | µs | |
| SY37 | TOSCDFRC | FRC Oscillator Start-up Delay | 46 | 48 | 54 | µs | |
| SY38 | TOSCDLPRC | LPRC Oscillator Start-up Delay | — | — | 70 | µs | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in “Typical” column are at 3.3V, +25°C unless otherwise stated.

**FIGURE 30-5: TIMER1-TIMER5 EXTERNAL CLOCK TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-23: TIMER1 EXTERNAL CLOCK TIMING REQUIREMENTS(1)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(2)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TA10 | TTXH | T1CK High Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256) |
| | | | Asynchronous | 35 | — | — | ns | |
| TA11 | TTXL | T1CK Low Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TA15, N = prescaler value (1, 8, 64, 256) |
| | | | Asynchronous | 10 | — | — | ns | |
| TA15 | TTXP | T1CK Input Period | Synchronous mode | Greater of: 40 or (2 TCY + 40)/N | — | — | ns | N = prescale value (1, 8, 64, 256) |
| OS60 | Ft1 | T1CK Oscillator Input Frequency Range (oscillator enabled by setting bit, TCS (T1CON[1])) | | DC | — | 50 | kHz | |
| TA20 | TCKEXTMRL | Delay from External T1CK Clock Edge to Timer Increment | | 0.75 TCY + 40 | — | 1.75 TCY + 40 | ns | |

**Note 1:** Timer1 is a Type A.

**2:** These parameters are characterized, but are not tested in manufacturing.


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**TABLE 30-24: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TB10 | TtxH | TxCK High Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256) |
| TB11 | TtxL | TxCK Low Time | Synchronous mode | Greater of: 20 or (TCY + 20)/N | — | — | ns | Must also meet Parameter TB15, N = prescale value (1, 8, 64, 256) |
| TB15 | TtxP | TxCK Input Period | Synchronous mode | Greater of: 40 or (2 TCY + 40)/N | — | — | ns | N = prescale value (1, 8, 64, 256) |
| TB20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | 0.75 TCY + 40 | — | 1.75 TCY + 40 | ns | |

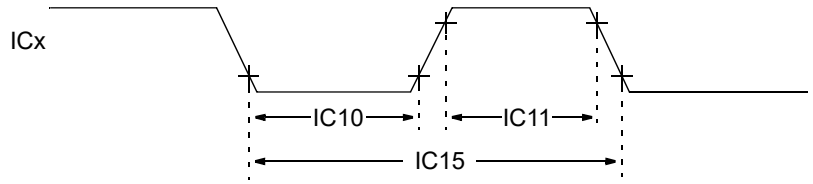
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**TABLE 30-25: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TC10 | TtxH | TxCK High Time | Synchronous | TCY + 20 | — | — | ns | Must also meet Parameter TC15 |
| TC11 | TtxL | TxCK Low Time | Synchronous | TCY + 20 | — | — | ns | Must also meet Parameter TC15 |
| TC15 | TtxP | TxCK Input Period | Synchronous, with prescaler | 2 TCY + 40 | — | — | ns | N = prescale value (1, 8, 64, 256) |
| TC20 | TCKEXTMRL | Delay from External TxCK Clock Edge to Timer Increment | | 0.75 TCY + 40 | — | 1.75 TCY + 40 | ns | |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**FIGURE 30-6: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-26: INPUT CAPTURE x MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristics(1)** | **Min.** | **Max.** | **Units** | **Conditions** | |
| IC10 | TccL | ICx Input Low Time | Greater of 12.5 + 25 or (0.5 TCY/N) + 25 | — | ns | Must also meet Parameter IC15 | N = prescale value (1, 4, 16) |
| IC11 | TccH | ICx Input High Time | Greater of 12.5 + 25 or (0.5 TCY/N) + 25 | — | ns | Must also meet Parameter IC15 | |
| IC15 | TccP | ICx Input Period | Greater of 25 + 50 or (1 TCY/N) + 50 | — | ns | | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.


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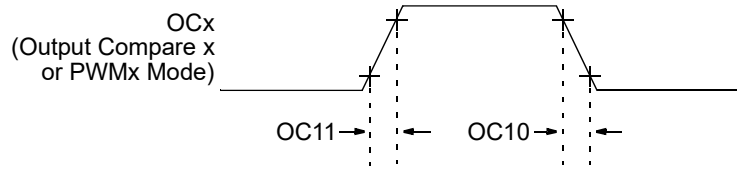
**FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-27: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| OC10 | TccF | OCx Output Fall Time | — | — | — | ns | See Parameter DO32 |
| OC11 | TccR | OCx Output Rise Time | — | — | — | ns | See Parameter DO31 |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS**

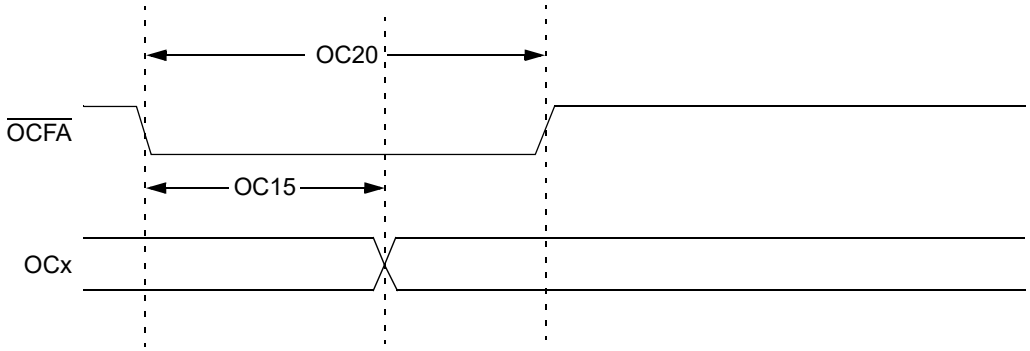



**TABLE 30-28: OCx/PWMx MODE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| OC15 | TFD | Fault Input to PWMx I/O Change | — | — | TCY + 20 | ns | |
| OC20 | TFLT | Fault Input Pulse Width | TCY + 20 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**FIGURE 30-9: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

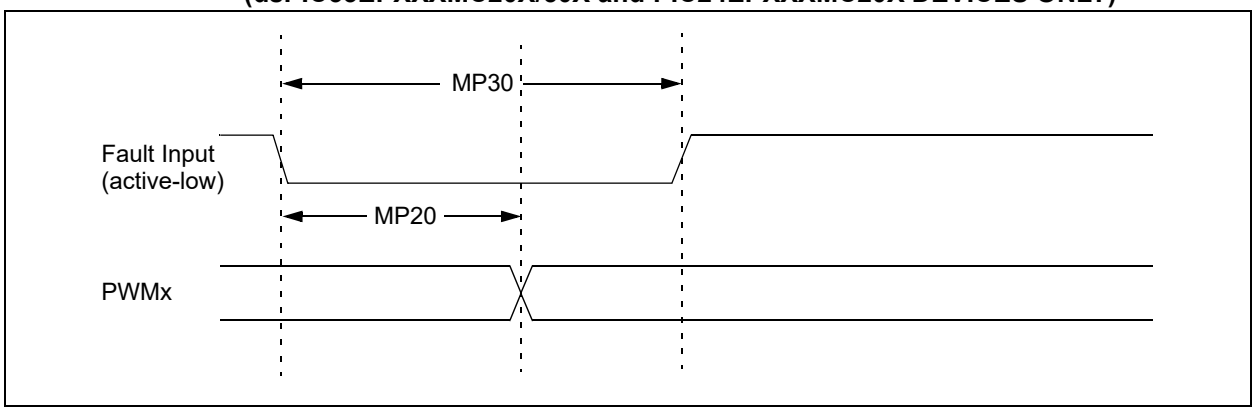
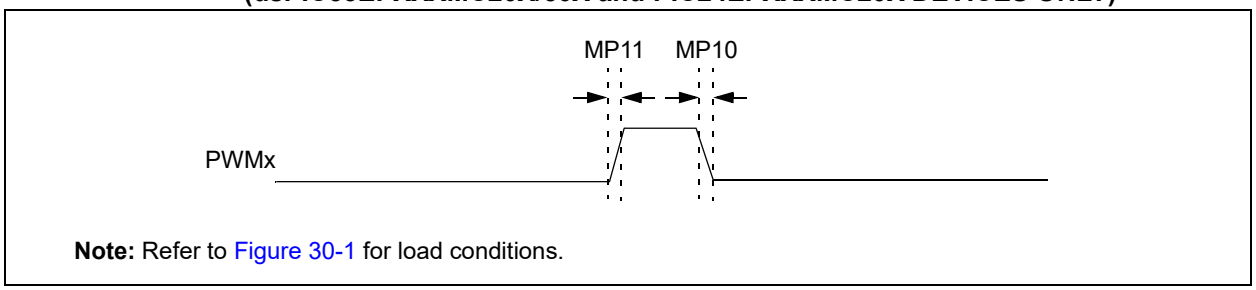



**FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-29: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| MP10 | TFPWM | PWMx Output Fall Time | — | — | — | ns | See Parameter DO32 |
| MP11 | TRPWM | PWMx Output Rise Time | — | — | — | ns | See Parameter DO31 |
| MP20 | TFD | Fault Input ↓ to PWMx I/O Change | — | — | 15 | ns | |
| MP30 | TFH | Fault Input Pulse Width | 15 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.


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**FIGURE 30-11: TIMERQ (QEI MODULE) EXTERNAL CLOCK TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)**

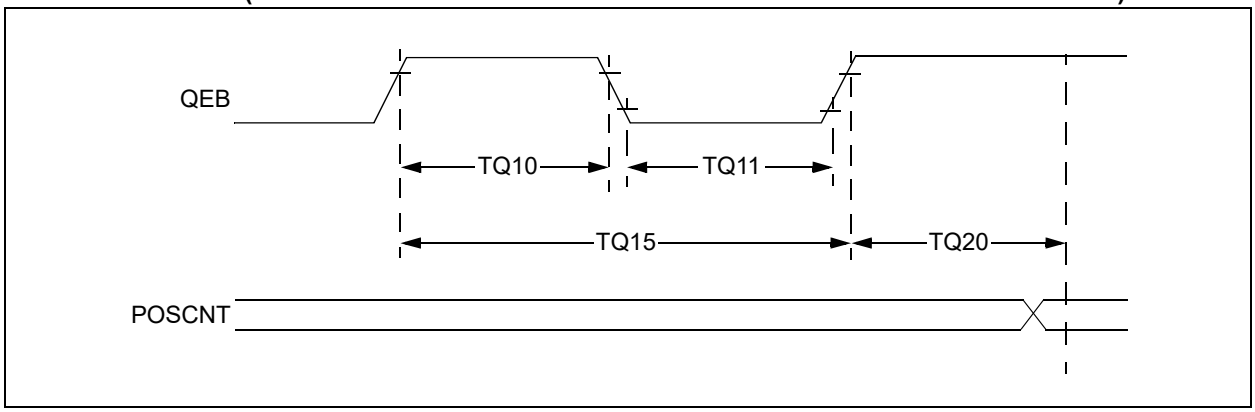


**TABLE 30-30: QEI MODULE EXTERNAL CLOCK TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X AND PIC24EPXXXMC20X DEVICES ONLY)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| TQ10 | TtQH | TQCK High Time | Synchronous, with prescaler | Greater of 12.5 + 25 or (0.5 TCY/N) + 25 | — | — | ns | Must also meet Parameter TQ15 |
| TQ11 | TtQL | TQCK Low Time | Synchronous, with prescaler | Greater of 12.5 + 25 or (0.5 TCY/N) + 25 | — | — | ns | Must also meet Parameter TQ15 |
| TQ15 | TtQP | TQCP Input Period | Synchronous, with prescaler | Greater of 25 + 50 or (1 TCY/N) + 50 | — | — | ns | |
| TQ20 | TCKEXTMRL | Delay from External TQCK Clock Edge to Timer Increment | | — | 1 | TCY | — | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**FIGURE 30-12: QEA/QEB INPUT CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

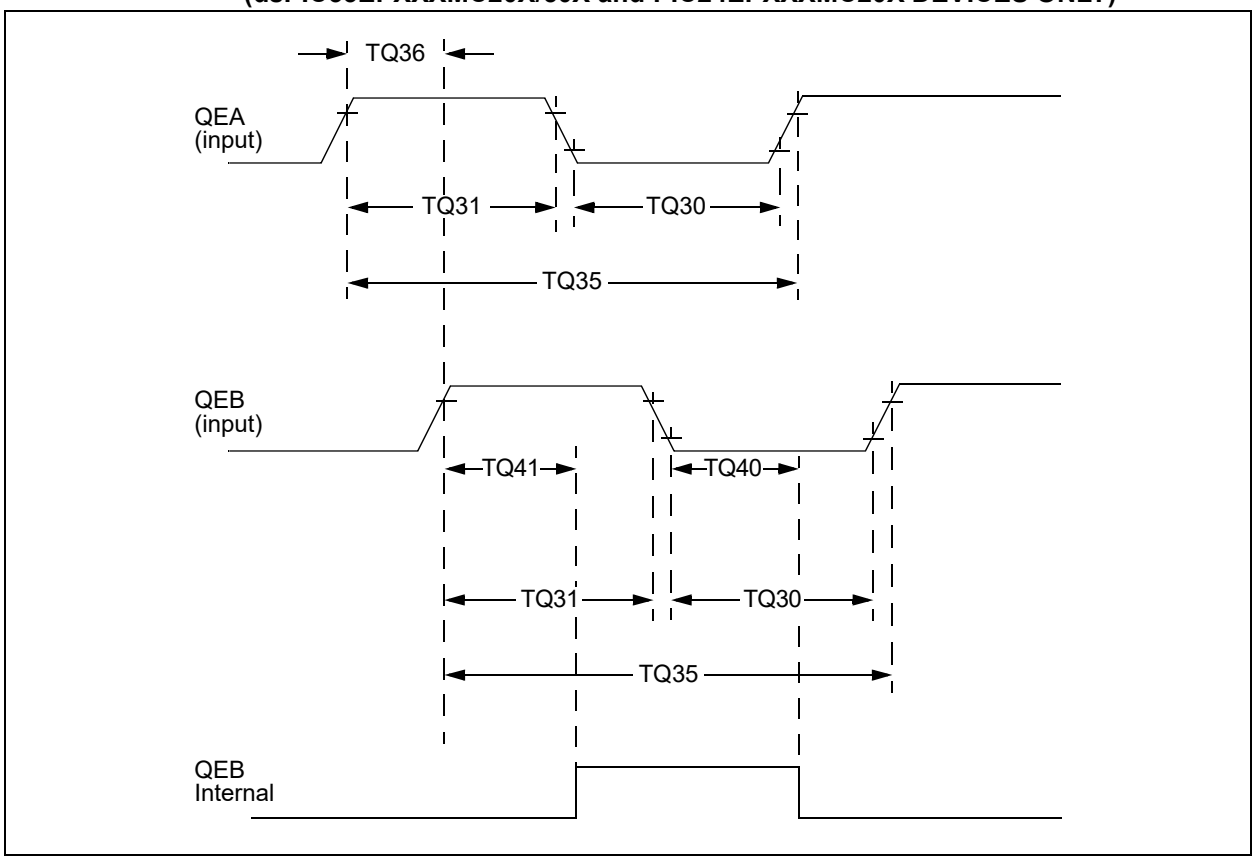


**TABLE 30-31: QUADRATURE DECODER TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| TQ30 | TQUL | Quadrature Input Low Time | 6 TCY | — | ns | |
| TQ31 | TQUH | Quadrature Input High Time | 6 TCY | — | ns | |
| TQ35 | TQUIN | Quadrature Input Period | 12 TCY | — | ns | |
| TQ36 | TQUP | Quadrature Phase Period | 3 TCY | — | ns | |
| TQ40 | TQUFL | Filter Time to Recognize Low, with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)** |
| TQ41 | TQUFH | Filter Time to Recognize High, with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 3)** |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**3:** N = Index Channel Digital Filter Clock Divide Select bits. Refer to **"Quadrature Encoder Interface (QEI)"** (www.microchip.com/DS70000601) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip website for the latest family reference manual sections.


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**FIGURE 30-13: QEI MODULE INDEX PULSE TIMING CHARACTERISTICS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

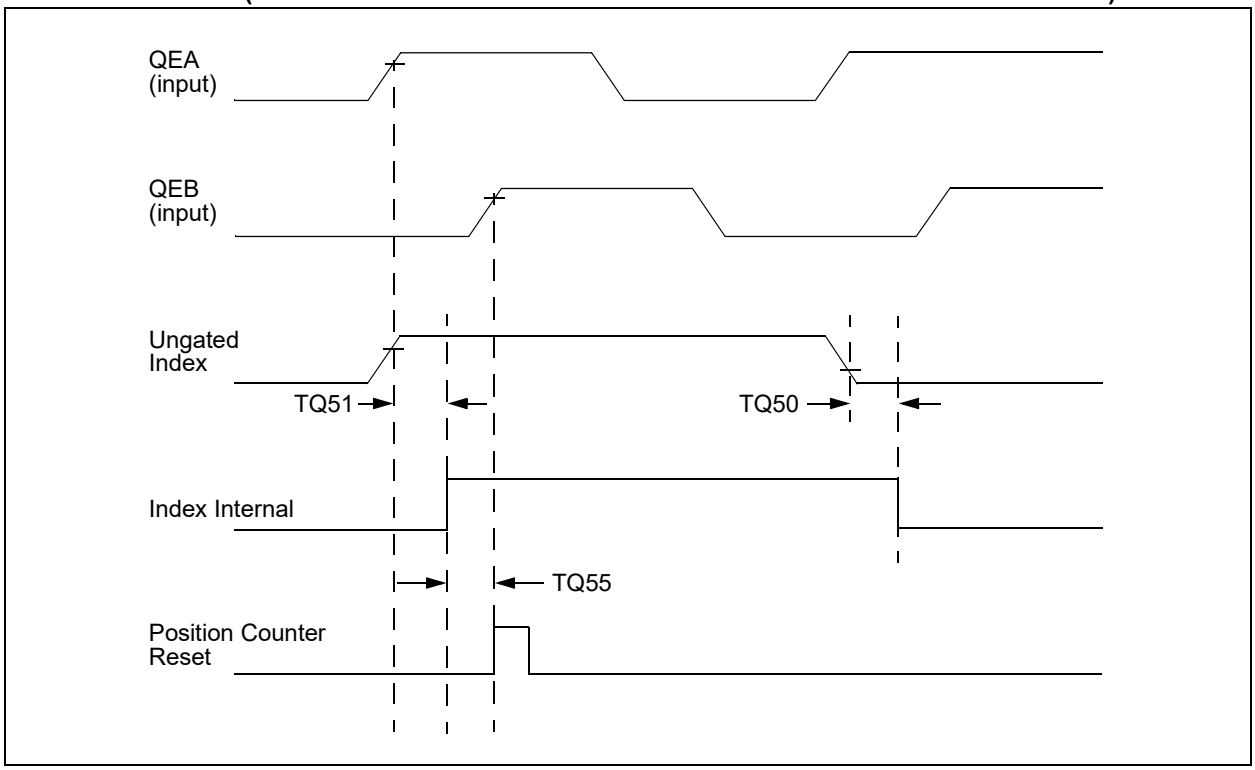



**TABLE 30-32: QEI INDEX PULSE TIMING REQUIREMENTS (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X DEVICES ONLY)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min.** | **Max.** | **Units** | **Conditions** |
| TQ50 | TqiL | Filter Time to Recognize Low, with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)** |
| TQ51 | TqiH | Filter Time to Recognize High, with Digital Filter | 3 * N * TCY | — | ns | N = 1, 2, 4, 16, 32, 64, 128 and 256 **(Note 2)** |
| TQ55 | Tqidxr | Index Pulse Recognized to Position Counter Reset (ungated index) | 3 TCY | — | ns | |

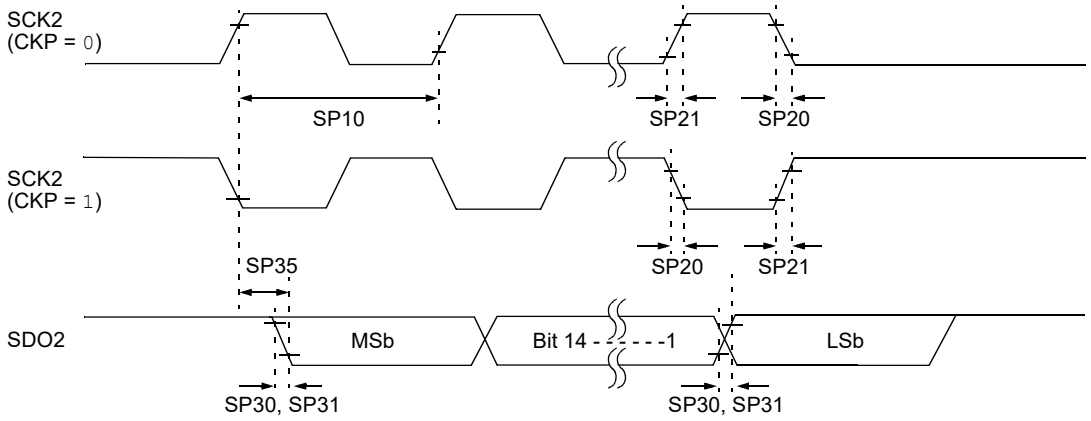
**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Alignment of index pulses to QEA and QEB is shown for position counter Reset timing only. Shown for forward direction only (QEA leads QEB). Same timing applies for reverse direction (QEA lags QEB) but index pulse recognition occurs on the falling edge.

**TABLE 30-33: SPI2 MAXIMUM DATA/CLOCK RATE SUMMARY**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Maximum Data Rate** | **Master Transmit Only (Half-Duplex)** | **Master Transmit/Receive (Full-Duplex)** | **Slave Transmit/Receive (Full-Duplex)** | **CKE** | **CKP** | **SMP** |
| 15 MHz | Table 30-33 | — | — | 0,1 | 0,1 | 0,1 |
| 9 MHz | — | Table 30-34 | — | 1 | 0,1 | 1 |
| 9 MHz | — | Table 30-35 | — | 0 | 0,1 | 1 |
| 15 MHz | — | — | Table 30-36 | 1 | 0 | 0 |
| 11 MHz | — | — | Table 30-37 | 1 | 1 | 0 |
| 15 MHz | — | — | Table 30-38 | 0 | 1 | 0 |
| 11 MHz | — | — | Table 30-39 | 0 | 0 | 0 |

**FIGURE 30-14: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.


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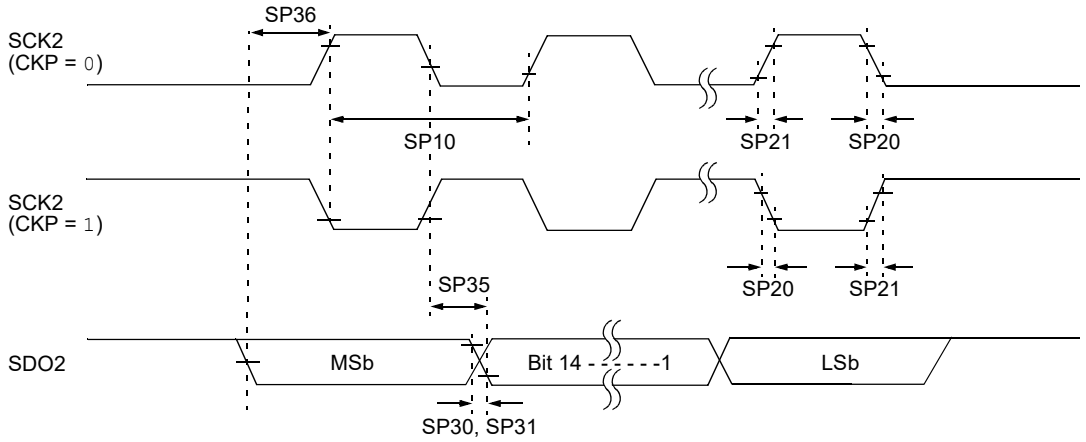
**FIGURE 30-15: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-34: SPI2 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | FscP | Maximum SCK2 Frequency | — | — | 15 | MHz | **Note 3** |
| SP20 | TscF | SCK2 Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP21 | TscR | SCK2 Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdiV2scH, TdiV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |

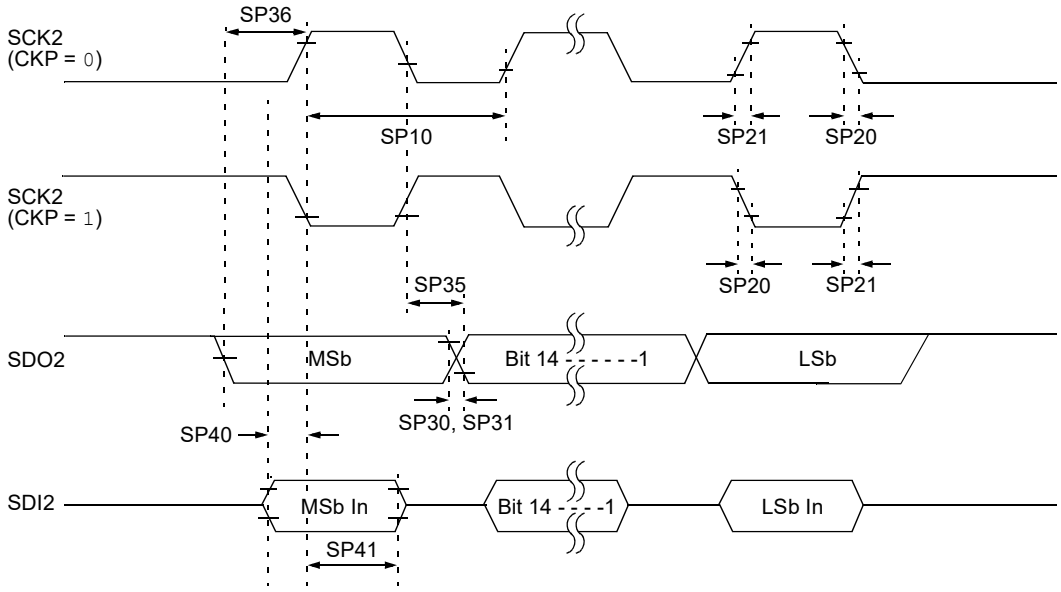
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**FIGURE 30-16: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-35: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | FscP | Maximum SCK2 Frequency | — | — | 9 | MHz | **Note 3** |
| SP20 | TscF | SCK2 Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP21 | TscR | SCK2 Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2sc, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typical” column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.


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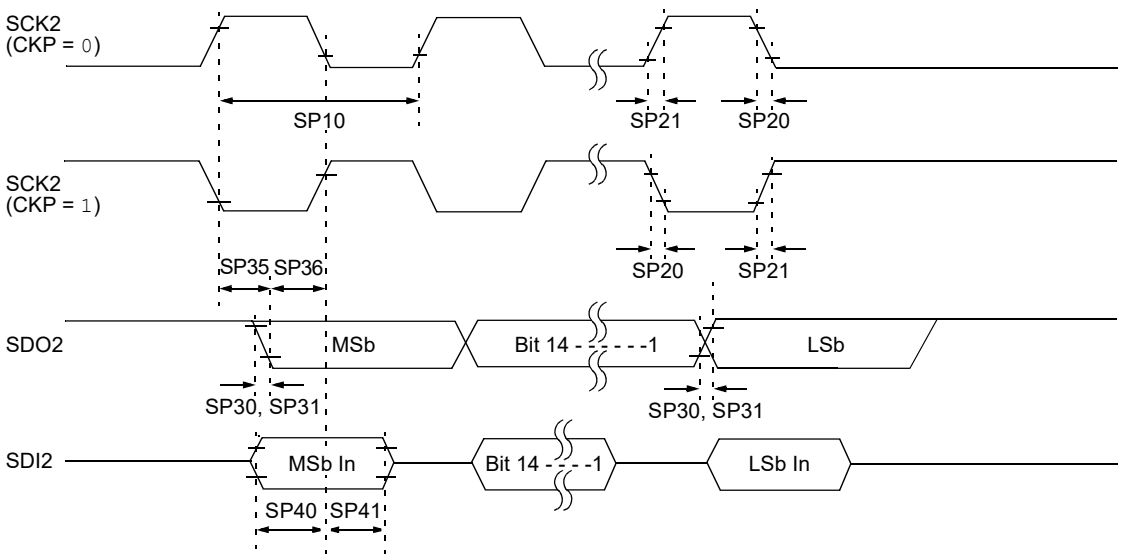
**FIGURE 30-17: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-36: SPI2 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | FscP | Maximum SCK2 Frequency | — | — | 9 | MHz | -40ºC to +125ºC **(Note 3)** |
| SP20 | TscF | SCK2 Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP21 | TscR | SCK2 Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |

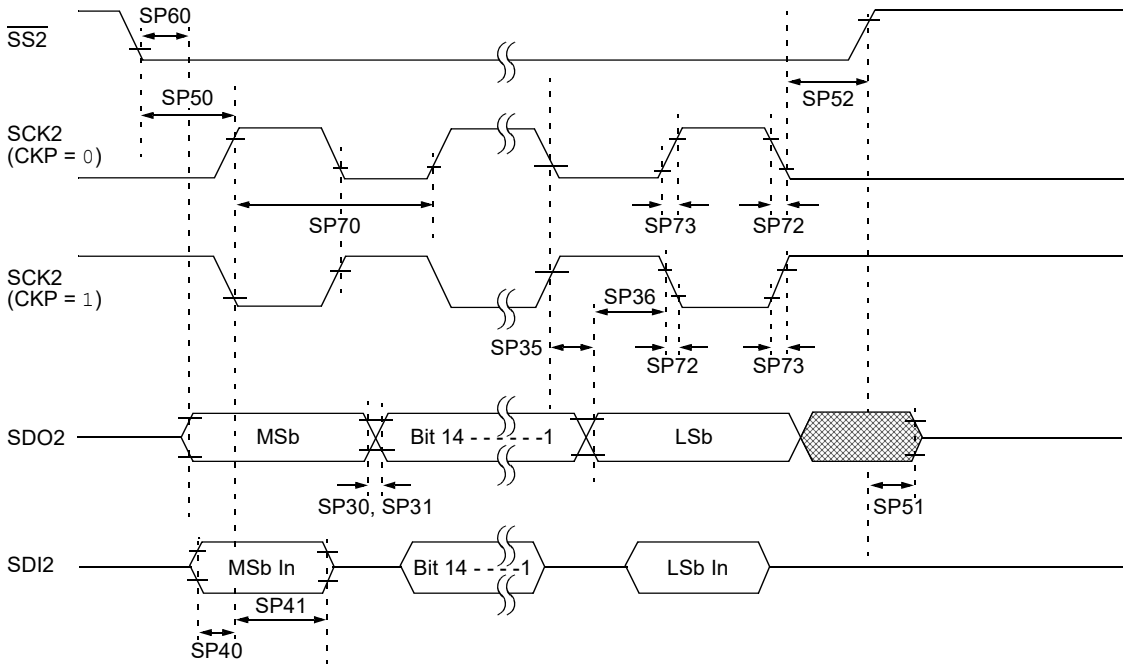
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 111 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**FIGURE 30-18: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.


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**TABLE 30-37: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK2 Input Frequency | — | — | Lesser of FP or 15 | MHz | **Note 3** |
| SP72 | TscF | SCK2 Input Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP73 | TscR | SCK2 Input Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS2}$ ↑ to SDO2 Output High-Impedance | 10 | — | 50 | ns | **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SS2}$ ↑ after SCK2 Edge | 1.5 TCY + 40 | — | — | ns | **Note 4** |
| SP60 | TssL2doV | SDO2 Data Output Valid after $\overline{SS2}$ Edge | — | — | 50 | ns | |

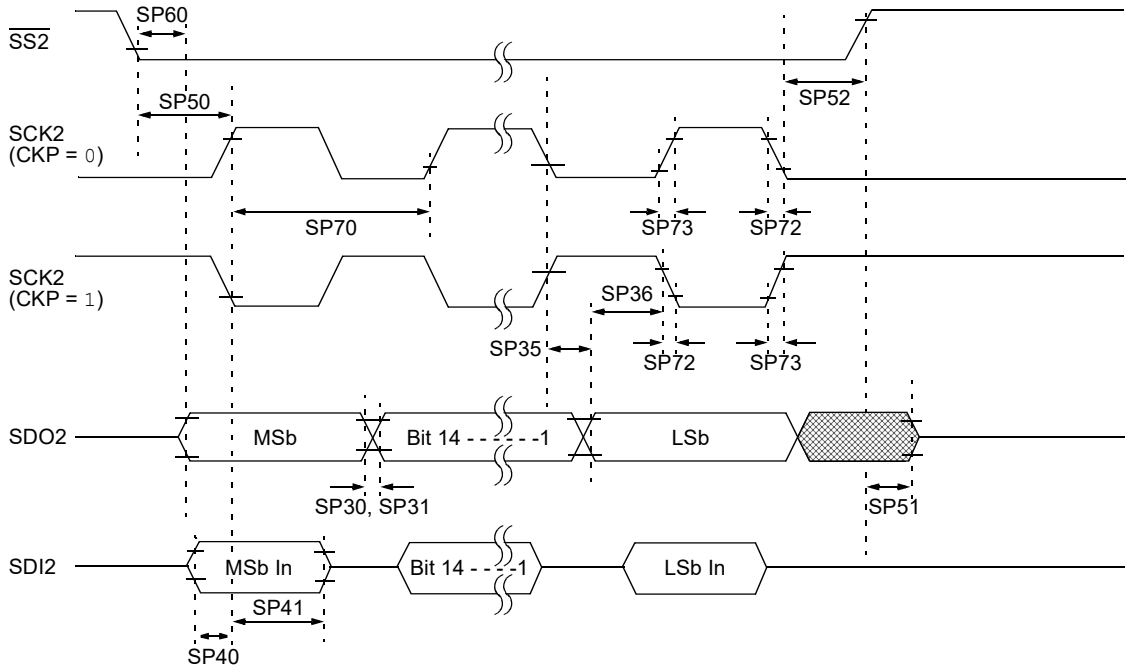
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**FIGURE 30-19: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.


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**TABLE 30-38: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK2 Input Frequency | — | — | Lesser of FP or 11 | MHz | **Note 3** |
| SP72 | TscF | SCK2 Input Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP73 | TscR | SCK2 Input Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS2}$ ↑ to SDO2 Output High-Impedance | 10 | — | 50 | ns | **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SS2}$ ↑ after SCK2 Edge | 1.5 TCY + 40 | — | — | ns | **Note 4** |
| SP60 | TssL2doV | $\overline{SDO2}$ Data Output Valid after $\overline{SS2}$ Edge | — | — | 50 | ns | |

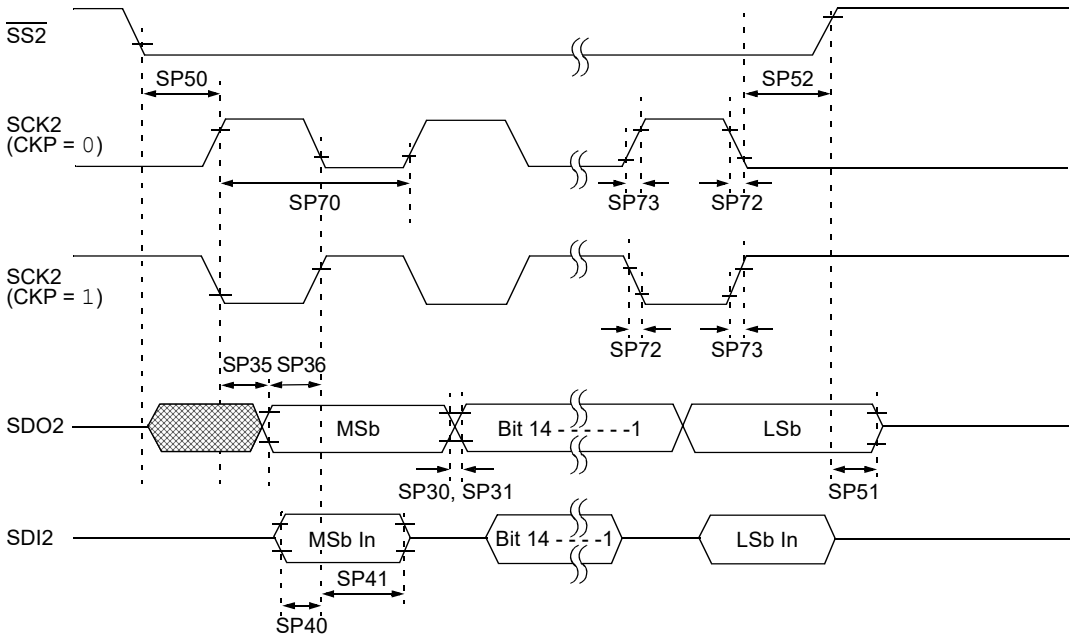
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**FIGURE 30-20: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.


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**TABLE 30-39: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK2 Input Frequency | — | — | 15 | MHz | **Note 3** |
| SP72 | TscF | SCK2 Input Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP73 | TscR | SCK2 Input Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS2}$ ↑ to SDO2 Output High-Impedance | 10 | — | 50 | ns | **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SS2}$ ↑ after SCK2 Edge | 1.5 TCY + 40 | — | — | ns | **Note 4** |

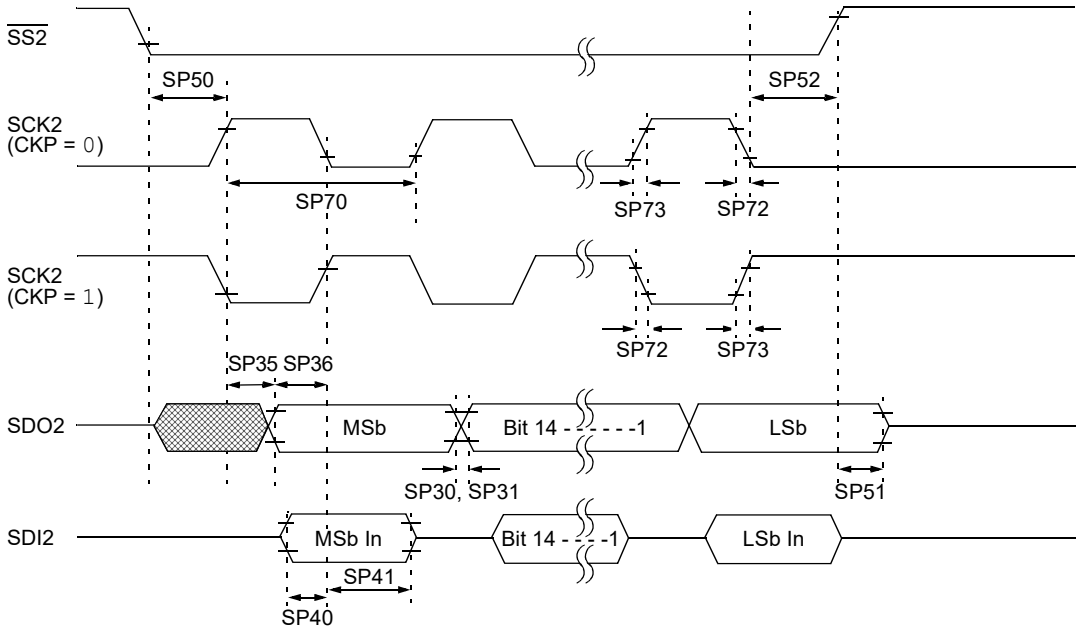
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typical” column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK2 is 66.7 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**FIGURE 30-21: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.


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**TABLE 30-40: SPI2 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK2 Input Frequency | — | — | 11 | MHz | **Note 3** |
| SP72 | TscF | SCK2 Input Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP73 | TscR | SCK2 Input Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP30 | TdoF | SDO2 Data Output Fall Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP31 | TdoR | SDO2 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP35 | TscH2doV, TscL2doV | SDO2 Data Output Valid after SCK2 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO2 Data Output Setup to First SCK2 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI2 Data Input to SCK2 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS2}$ ↓ to SCK2 ↑ or SCK2 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS2}$ ↑ to SDO2 Output High-Impedance | 10 | — | 50 | ns | **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SS2}$ ↑ after SCK2 Edge | 1.5 TCY + 40 | — | — | ns | **Note 4** |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typical” column are at 3.3V, +25°C unless otherwise stated.

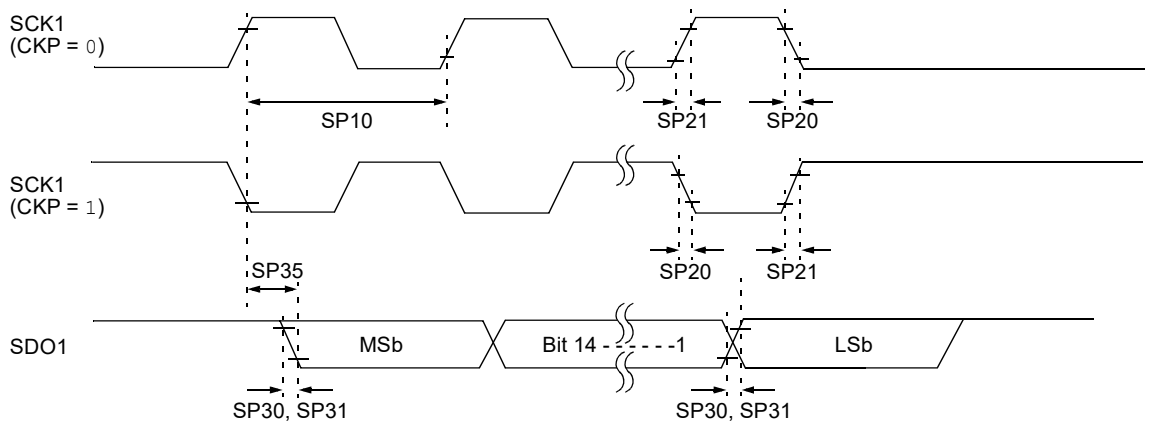
**3:** The minimum clock period for SCK2 is 91 ns. Therefore, the SCK2 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI2 pins.

**TABLE 30-41: SPI1 MAXIMUM DATA/CLOCK RATE SUMMARY**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Maximum Data Rate** | **Master Transmit Only (Half-Duplex)** | **Master Transmit/Receive (Full-Duplex)** | **Slave Transmit/Receive (Full-Duplex)** | **CKE** | **CKP** | **SMP** |
| 15 MHz | Table 30-42 | — | — | 0,1 | 0,1 | 0,1 |
| 10 MHz | — | Table 30-43 | — | 1 | 0,1 | 1 |
| 10 MHz | — | Table 30-44 | — | 0 | 0,1 | 1 |
| 15 MHz | — | — | Table 30-45 | 1 | 0 | 0 |
| 11 MHz | — | — | Table 30-46 | 1 | 1 | 0 |
| 15 MHz | — | — | Table 30-47 | 0 | 1 | 0 |
| 11 MHz | — | — | Table 30-48 | 0 | 0 | 0 |

**FIGURE 30-22: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.


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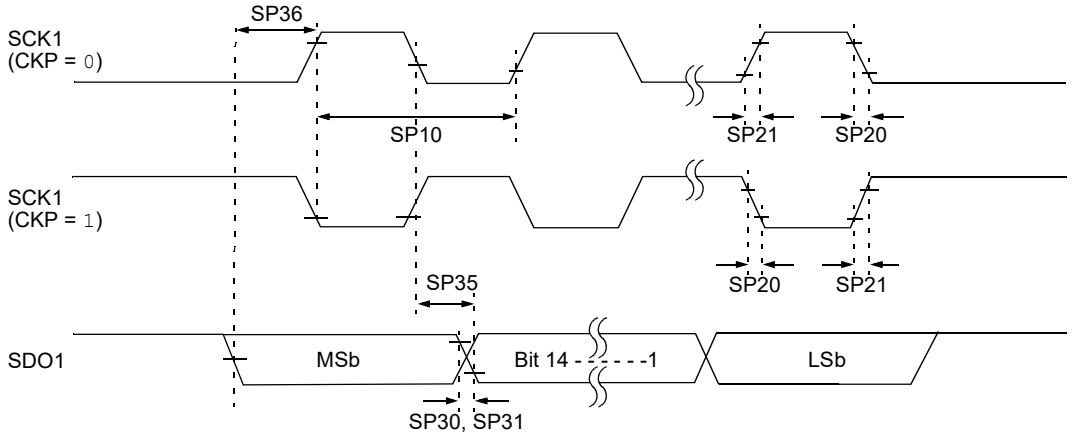
**FIGURE 30-23: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-42: SPI1 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | FscP | Maximum SCK1 Frequency | — | — | 15 | MHz | **Note 3** |
| SP20 | TscF | SCK1 Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP21 | TscR | SCK1 Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP35 | TscH2doV, TscL2doV | SDO1 Data Output Valid after SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdiV2scH, TdiV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |

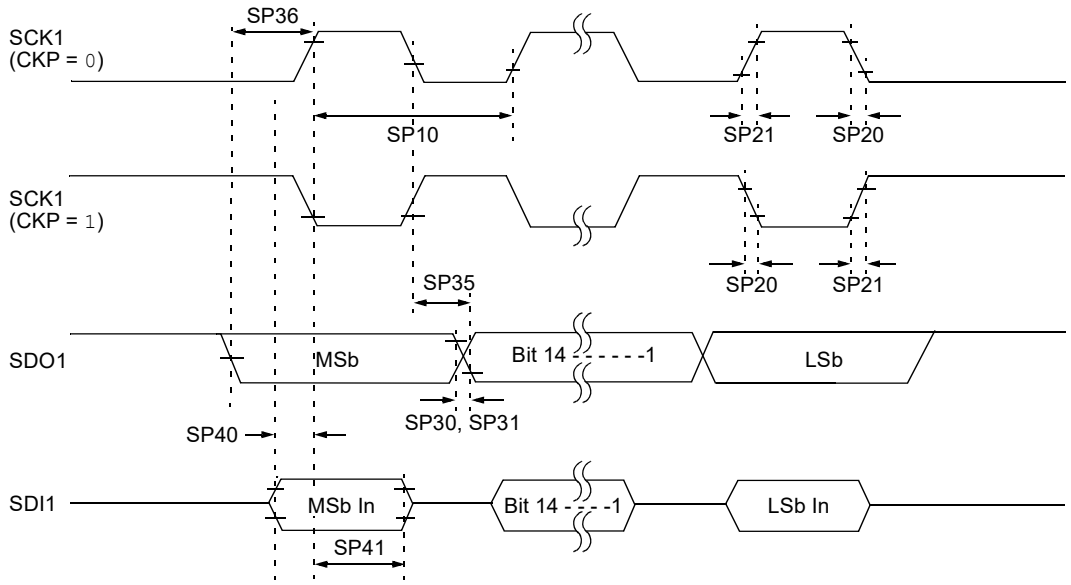
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typical” column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

**FIGURE 30-24: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-43: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 1, CKP = x, SMP = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | FscP | Maximum SCK1 Frequency | — | — | 10 | MHz | **Note 3** |
| SP20 | TscF | SCK1 Output Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP21 | TscR | SCK1 Output Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP35 | TscH2doV, TscL2doV | SDO1 Data Output Valid after SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2sc, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |

**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typical” column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.


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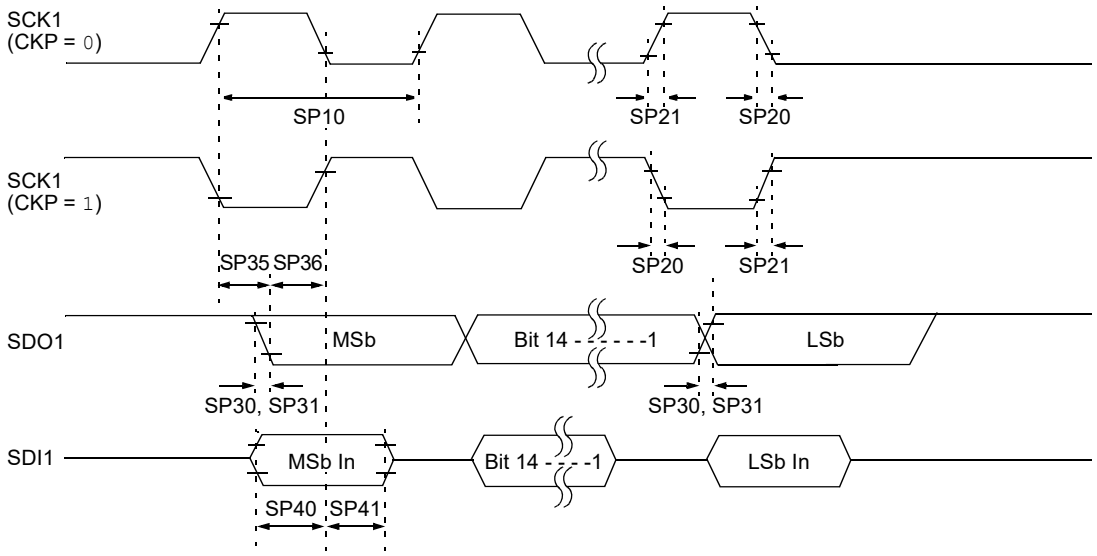
**FIGURE 30-25: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.

**TABLE 30-44: SPI1 MASTER MODE (FULL-DUPLEX, CKE = 0, CKP = x, SMP = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP10 | FscP | Maximum SCK1 Frequency | — | — | 10 | MHz | -40ºC to +125ºC **(Note 3)** |
| SP20 | TscF | SCK1 Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP21 | TscR | SCK1 Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP35 | TscH2doV, TscL2doV | SDO1 Data Output Valid after SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |

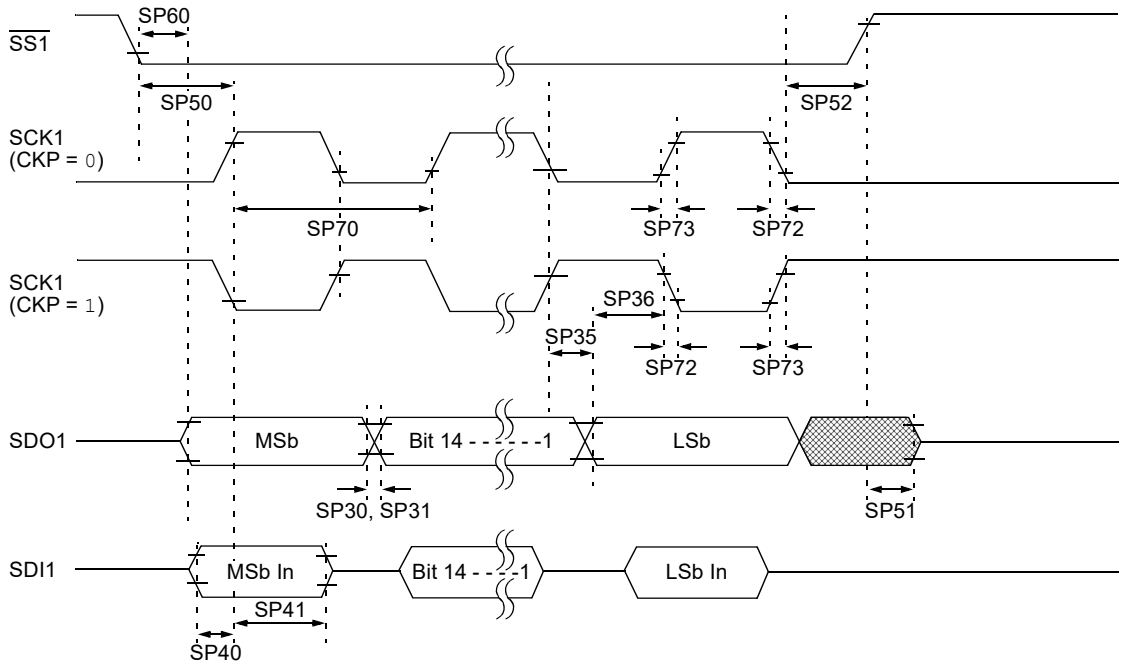
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 100 ns. The clock generated in Master mode must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

**FIGURE 30-26: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.


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**TABLE 30-45: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | — | Lesser of FP or 15 | MHz | **Note 3** |
| SP72 | TscF | SCK1 Input Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP73 | TscR | SCK1 Input Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP35 | TscH2doV, TscL2doV | SDO1 Data Output Valid after SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS1}$ ↑ to SDO1 Output High-Impedance | 10 | — | 50 | ns | **Note 4** |
| SP52 | TscH2ssH TscL2ssH | $\overline{SS1}$ ↑ after SCK1 Edge | 1.5 TCY + 40 | — | — | ns | **Note 4** |
| SP60 | TssL2doV | SDO1 Data Output Valid after $\overline{SS1}$ Edge | — | — | 50 | ns | |

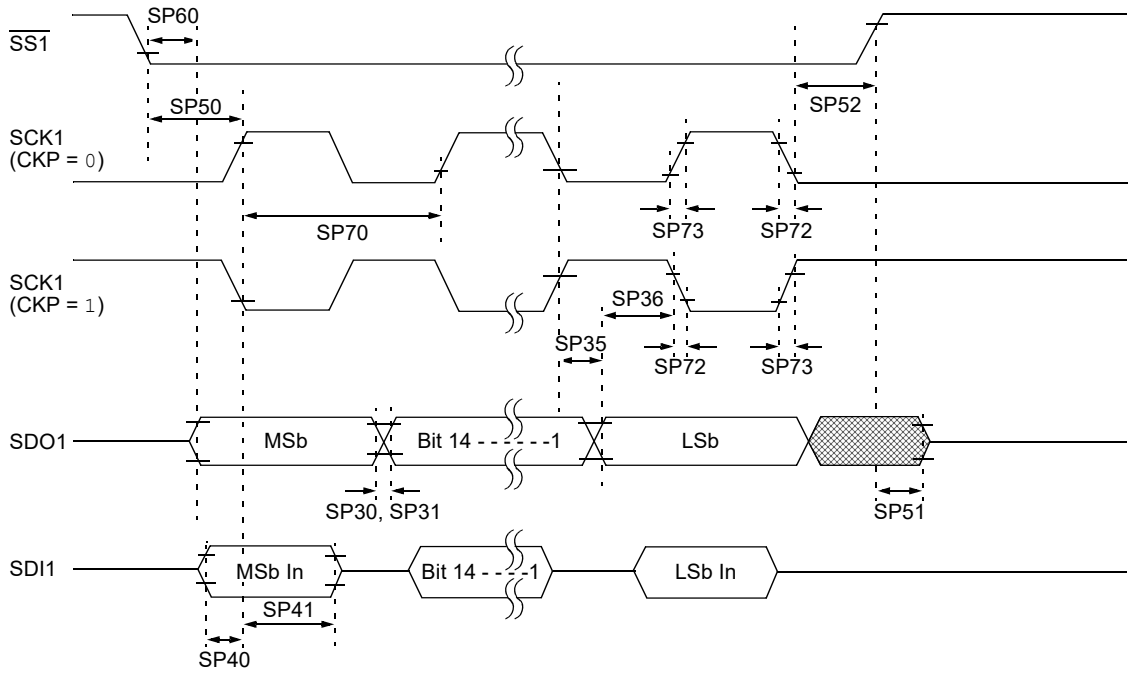
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

**FIGURE 30-27: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.


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**TABLE 30-46: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | — | Lesser of FP or 11 | MHz | **Note 3** |
| SP72 | TscF | SCK1 Input Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP73 | TscR | SCK1 Input Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 **(Note 4)** |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 **(Note 4)** |
| SP35 | TscH2doV, TscL2doV | SDO1 Data Output Valid after SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS1}$ ↑ to SDO1 Output High-Impedance | 10 | — | 50 | ns | **Note 4** |
| SP52 | TscH2ssH, TscL2ssH | $\overline{SS1}$ ↑ after SCK1 Edge | 1.5 TCY + 40 | — | — | ns | **Note 4** |
| SP60 | TssL2doV | $\overline{SDO1}$ Data Output Valid after $\overline{SS1}$ Edge | — | — | 50 | ns | |

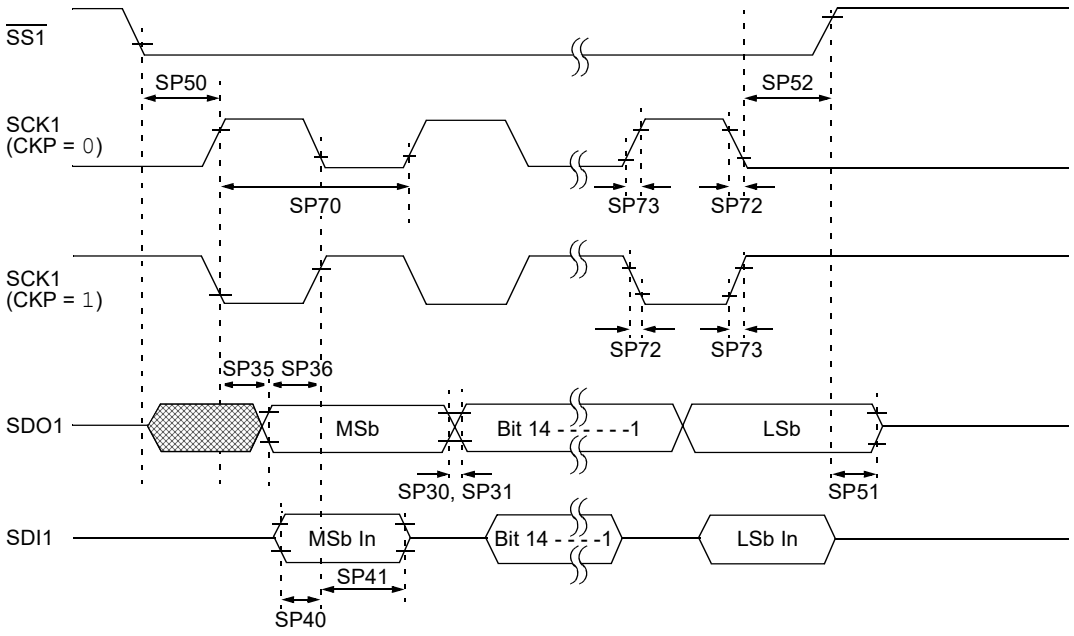
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

**FIGURE 30-28: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.


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**TABLE 30-47: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | — | 15 | MHz | **Note 3** |
| SP72 | TscF | SCK1 Input Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP73 | TscR | SCK1 Input Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP35 | TscH2doV, TscL2doV | SDO1 Data Output Valid after SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS1}$ ↑ to SDO1 Output High-Impedance | 10 | — | 50 | ns | **Note 4** |
| SP52 | TscH2ssH, TscL2ssH | $\overline{SS1}$ ↑ after SCK1 Edge | 1.5 TCY + 40 | — | — | ns | **Note 4** |

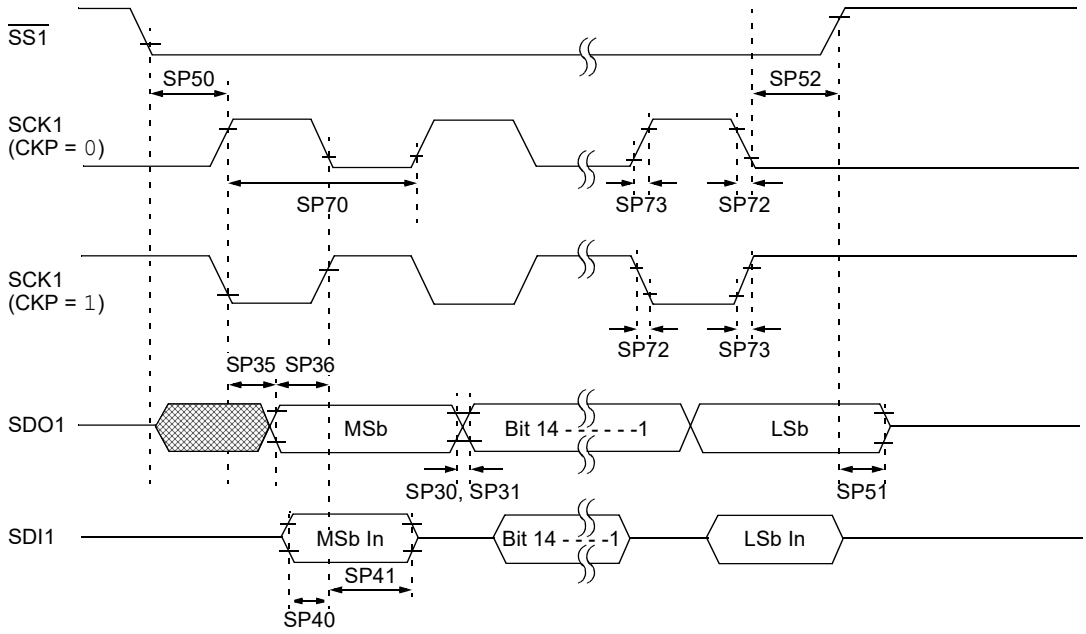
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typical” column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 66.7 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

**4:** Assumes 50 pF load on all SPI1 pins.

**FIGURE 30-29: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 30-1 for load conditions.


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**TABLE 30-48: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| SP70 | FscP | Maximum SCK1 Input Frequency | — | — | 11 | MHz | **Note 3** |
| SP72 | TscF | SCK1 Input Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP73 | TscR | SCK1 Input Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP30 | TdoF | SDO1 Data Output Fall Time | — | — | — | ns | See Parameter DO32 (**Note 4**) |
| SP31 | TdoR | SDO1 Data Output Rise Time | — | — | — | ns | See Parameter DO31 (**Note 4**) |
| SP35 | TscH2doV, TscL2doV | SDO1 Data Output Valid after SCK1 Edge | — | 6 | 20 | ns | |
| SP36 | TdoV2scH, TdoV2scL | SDO1 Data Output Setup to First SCK1 Edge | 30 | — | — | ns | |
| SP40 | TdiV2scH, TdiV2scL | Setup Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP41 | TscH2diL, TscL2diL | Hold Time of SDI1 Data Input to SCK1 Edge | 30 | — | — | ns | |
| SP50 | TssL2scH, TssL2scL | $\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input | 120 | — | — | ns | |
| SP51 | TssH2doZ | $\overline{SS1}$ ↑ to SDO1 Output High-Impedance | 10 | — | 50 | ns | **Note 4** |
| SP52 | TscH2ssH, TscL2ssH | $\overline{SS1}$ ↑ after SCK1 Edge | 1.5 TCY + 40 | — | — | ns | **Note 4** |

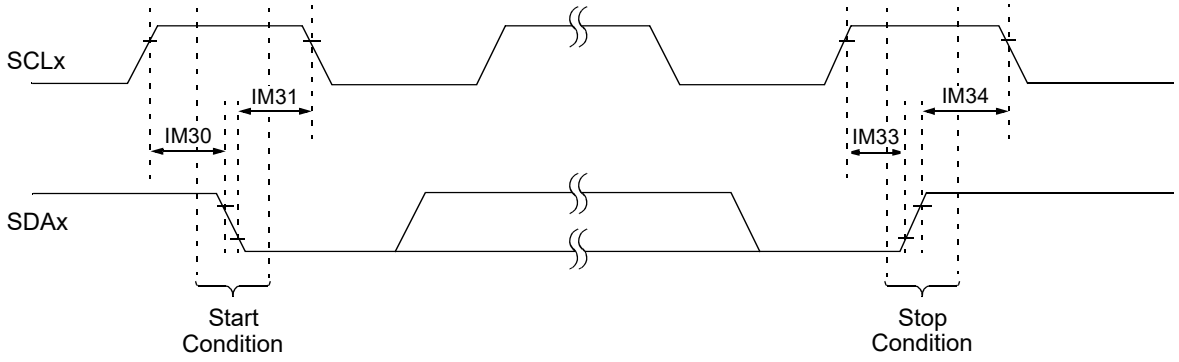
**Note 1:** These parameters are characterized, but are not tested in manufacturing.

**2:** Data in “Typical” column are at 3.3V, +25°C unless otherwise stated.

**3:** The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

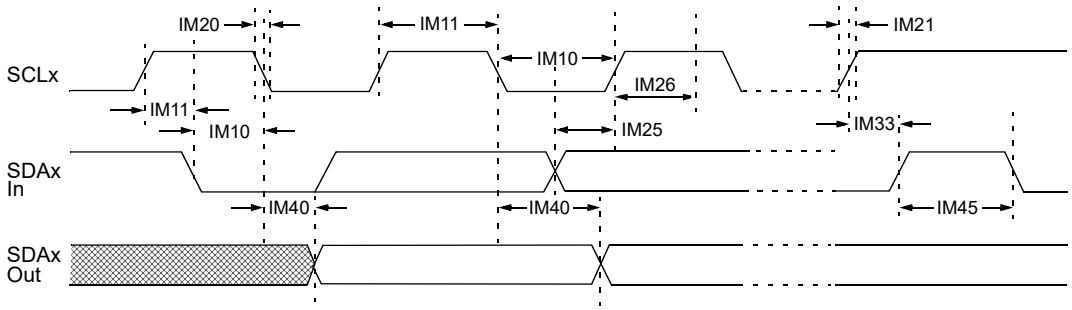
**4:** Assumes 50 pF load on all SPI1 pins.

**FIGURE 30-30: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 30-1 for load conditions.

**FIGURE 30-31: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)**




**Note:** Refer to Figure 30-1 for load conditions.


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**TABLE 30-49: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(4)** | | **Min.(1)** | **Max.** | **Units** | **Conditions** |
| IM10 | TLO:SCL | Clock Low Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM11 | THI:SCL | Clock High Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(2) | — | 100 | ns | |
| IM21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(2) | — | 300 | ns | |
| IM25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode(2) | 40 | — | ns | |
| IM26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | µs | |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| | | | 1 MHz mode(2) | 0.2 | — | µs | |
| IM30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM31 | THD:STA | Start Condition Hold Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | TCY/2 (BRG +2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 400 kHz mode | TCY/2 (BRG + 2) | — | µs | |
| | | | 1 MHz mode(2) | TCY/2 (BRG + 2) | — | µs | |
| IM40 | TAA:SCL | Output Valid From Clock | 100 kHz mode | — | 3500 | ns | |
| | | | 400 kHz mode | — | 1000 | ns | |
| | | | 1 MHz mode(2) | — | 400 | ns | |
| IM45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode(2) | 0.5 | — | µs | |
| IM50 | CB | Bus Capacitive Loading | | — | 400 | pF | |
| IM51 | TPGD | Pulse Gobbler Delay | | 65 | 390 | ns | **Note 3** |

**Note 1:** BRG is the value of the $I^2C$ Baud Rate Generator. Refer to **"Inter-Integrated Circuit ($I^2C$)"** (www.microchip.com/DS70000195) in the "*dsPIC33/PIC24 Family Reference Manual*". Please see the Microchip website for the latest family reference manual sections.

**2:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**3:** Typical value for this parameter is 130 ns.

**4:** These parameters are characterized, but not tested in manufacturing.

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**FIGURE 30-32: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**

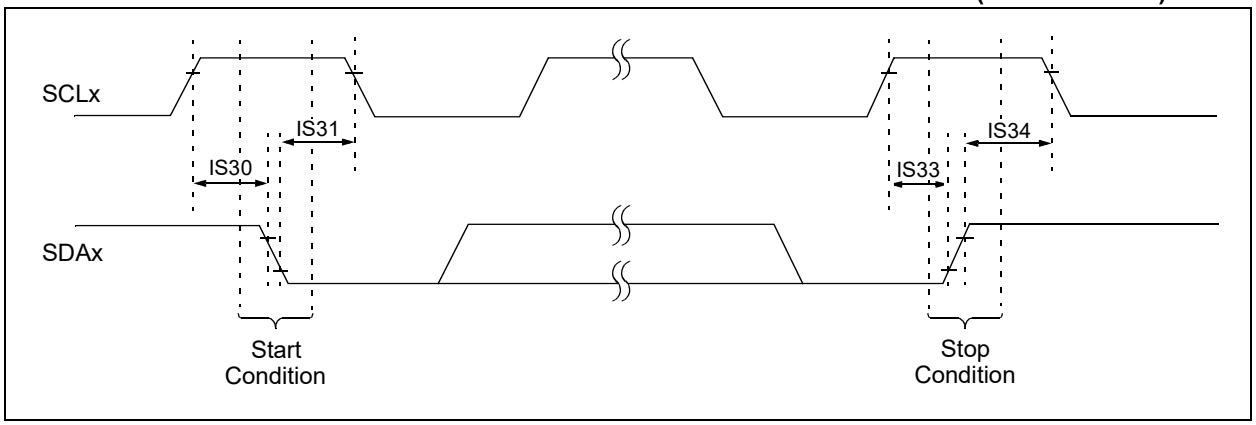


**FIGURE 30-33: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**

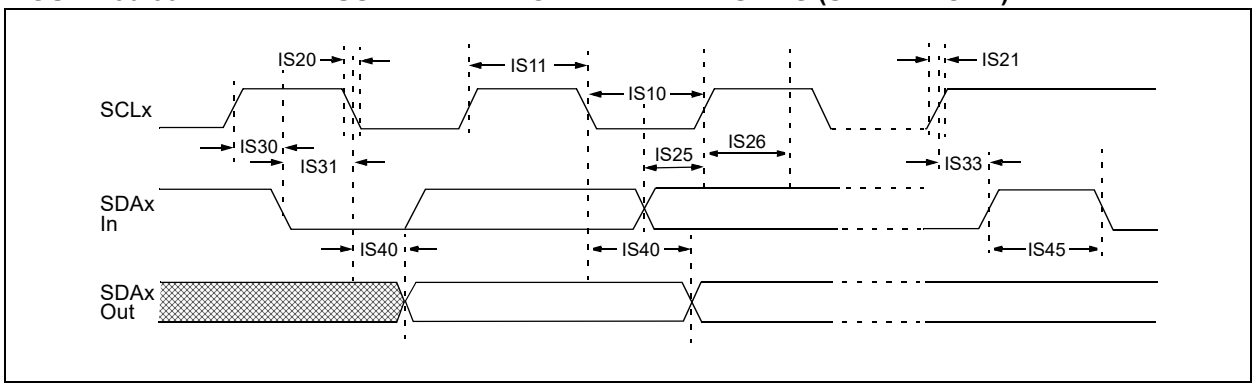



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**TABLE 30-50: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Symbol** | **Characteristic(3)** | | **Min.** | **Max.** | **Units** | **Conditions** |
| IS10 | TLO:SCL | Clock Low Time | 100 kHz mode | 4.7 | — | µs | |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode(1) | 0.5 | — | µs | |
| IS11 | THI:SCL | Clock High Time | 100 kHz mode | 4.0 | — | µs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 0.6 | — | µs | Device must operate at a minimum of 10 MHz |
| | | | 1 MHz mode(1) | 0.5 | — | µs | |
| IS20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 100 | ns | |
| IS21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 300 | ns | |
| IS25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode(1) | 100 | — | ns | |
| IS26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | µs | |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| | | | 1 MHz mode(1) | 0 | 0.3 | µs | |
| IS30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 4.7 | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode(1) | 0.25 | — | µs | |
| IS31 | THD:STA | Start Condition Hold Time | 100 kHz mode | 4.0 | — | µs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode(1) | 0.25 | — | µs | |
| IS33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 4.7 | — | µs | |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode(1) | 0.6 | — | µs | |
| IS34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | 4 | — | µs | |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode(1) | 0.25 | | µs | |
| IS40 | TAA:SCL | Output Valid From Clock | 100 kHz mode | 0 | 3500 | ns | |
| | | | 400 kHz mode | 0 | 1000 | ns | |
| | | | 1 MHz mode(1) | 0 | 350 | ns | |
| IS45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode(1) | 0.5 | — | µs | |
| IS50 | CB | Bus Capacitive Loading | | — | 400 | pF | |
| IS51 | TPGD | Pulse Gobbler Delay | | 65 | 390 | ns | Note 2 |

**Note 1:** Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**2:** Typical value for this parameter is 130 ns.

**3:** These parameters are characterized, but not tested in manufacturing.

**FIGURE 30-34: ECANx MODULE I/O TIMING CHARACTERISTICS**

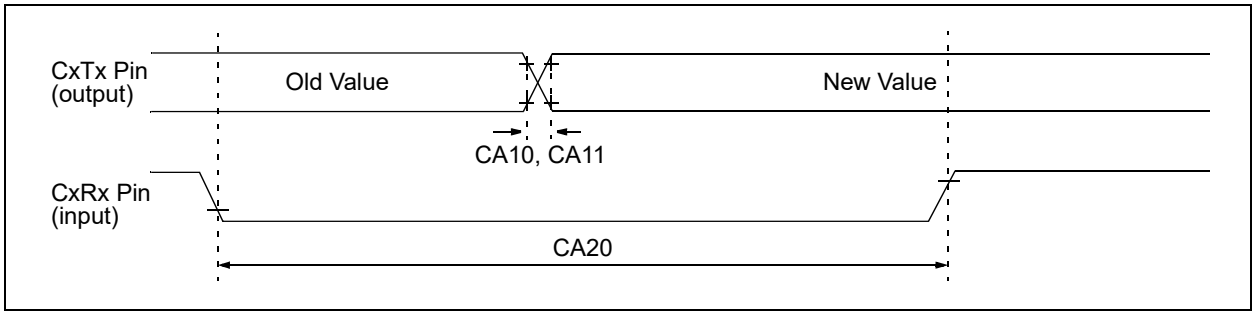


**TABLE 30-51: ECANx MODULE I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| CA10 | TIOF | Port Output Fall Time | — | — | — | ns | See Parameter DO32 |
| CA11 | TIOR | Port Output Rise Time | — | — | — | ns | See Parameter DO31 |
| CA20 | TCWF | Pulse Width to Trigger CAN Wake-up Filter | 120 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**FIGURE 30-35: UARTx MODULE I/O TIMING CHARACTERISTICS**

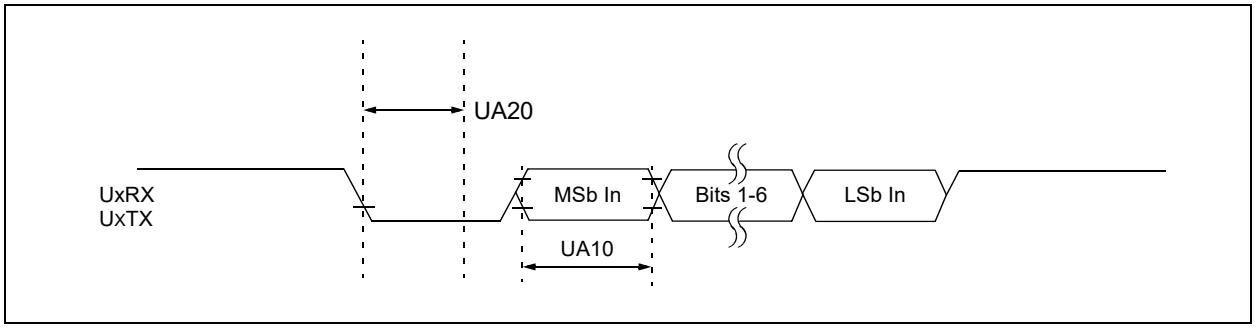


**TABLE 30-52: UARTx MODULE I/O TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +125°C | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.(2)** | **Max.** | **Units** | **Conditions** |
| UA10 | TUABAUD | UARTx Baud Time | 66.67 | — | — | ns | |
| UA11 | FBAUD | UARTx Baud Frequency | — | — | 15 | Mbps | |
| UA20 | TCWF | Start Bit Pulse Width to Trigger UARTx Wake-up | 500 | — | — | ns | |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Data in "Typical" column are at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.


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**TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1]<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.[2]** | **Max.** | **Units** | **Conditions** |
| **Comparator AC Characteristics** | | | | | | | |
| CM10 | TRESP | Response Time[3] | — | 19 | — | ns | V+ input step of 100 mV, V- input held at VDD/2 |
| CM11 | TMC2OV | Comparator Mode Change to Output Valid | — | — | 10 | µs | |
| **Comparator DC Characteristics** | | | | | | | |
| CM30 | VOFFSET | Comparator Offset Voltage | — | ±10 | ±15[7] | mV | |
| CM31 | VHYST | Input Hysteresis Voltage[3] | — | 30 | 65[7] | mV | |
| CM32 | TRISE/TFALL | Comparator Output Rise/ Fall Time[3] | — | 20 | — | ns | 1 pF load capacitance on input |
| CM33 | VGAIN | Open-Loop Voltage Gain[3] | — | 90 | — | db | |
| CM34 | VICM | Input Voltage Range | AVSS | — | AVDD | V | |
| **Op Amp AC Characteristics** | | | | | | | |
| CM20 | SR | Slew Rate[3] | 3.7 | 7.5 | 16 | V/µs | 10 pF load |
| CM21a | PM | Phase Margin (Configuration A)[3,4] | — | 55 | — | Degree | G = 4V/V; 10 pF load |
| CM21b | PM | Phase Margin (Configuration B)[3,5] | — | 40 | — | Degree | G = 4V/V; 10 pF load |
| CM22 | GM | Gain Margin[3] | — | 20 | — | db | G = 100V/V; 10 pF load |
| CM23a | GBW | Gain Bandwidth (Configuration A)[3,4] | — | 10 | — | MHz | 10 pF load |
| CM23b | GBW | Gain Bandwidth (Configuration B)[3,5] | — | 6 | — | MHz | 10 pF load |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** Data in "Typ" column are at 3.3V, +25°C unless otherwise stated.

**3:** Parameter is characterized but not tested in manufacturing.

**4:** See Figure 25-6 for configuration information.

**5:** See Figure 25-7 for configuration information.

**6:** Resistances can vary by ±10% between op amps.

**7:** These parameters have a combined effect on the actual performance of the comparator.

**8:** Input resistance (R1) must be less than or equal to 2 kOhm. The resulting minimum gain of the op amp circuit is equal to four.

**TABLE 30-53: OP AMP/COMPARATOR SPECIFICATIONS (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1]<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.[2]** | **Max.** | **Units** | **Conditions** |
| **Op Amp DC Characteristics** | | | | | | | |
| CM40 | VCMR | Common-Mode Input Voltage Range | AVSS | — | AVDD | V | |
| CM41 | CMRR | Common-Mode Rejection Ratio[3] | — | 40 | — | db | VCM = AVDD/2 |
| CM42 | VOFFSET | Op Amp Offset Voltage[3] | -30 | ±5 | +30 | mV | |
| CM43 | VGAIN | Open-Loop Voltage Gain[3] | — | 90 | — | db | |
| CM44 | IOS | Input Offset Current | — | — | — | — | See pad leakage currents in Table 30-11 |
| CM45 | IB | Input Bias Current | — | — | — | — | See pad leakage currents in Table 30-11 |
| CM46 | IOUT | Output Current | — | — | 420 | µA | With minimum value of RFEEDBACK (CM48) |
| CM48 | RFEEDBACK[8] | Feedback Resistance Value | 8 | — | — | kΩ | |
| CM49a | VOADC | Output Voltage Measured at OAx Using ADC[3,4] | AVSS + 0.077<br>AVSS + 0.037<br>AVSS + 0.018 | —<br>—<br>— | AVDD – 0.077<br>AVDD – 0.037<br>AVDD – 0.018 | V<br>V<br>V | IOUT = 420 µA<br>IOUT = 200 µA<br>IOUT = 100 µA |
| CM49b | VOUT | Output Voltage Measured at OAxOUT Pin[3,4,5] | AVSS + 0.210<br>AVSS + 0.100<br>AVSS + 0.050 | —<br>—<br>— | AVDD – 0.210<br>AVDD – 0.100<br>AVDD – 0.050 | V<br>V<br>V | IOUT = 420 µA<br>IOUT = 200 µA<br>IOUT = 100 µA |
| CM51 | RINT1[6] | Internal Resistance 1 (Configuration A and B)[3,4,5] | 198 | 264 | 317 | Ω | Min = -40ºC<br>Typ = +25ºC<br>Max = +125ºC |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** Data in "Typ" column are at 3.3V, +25°C unless otherwise stated.

**3:** Parameter is characterized but not tested in manufacturing.

**4:** See Figure 25-6 for configuration information.

**5:** See Figure 25-7 for configuration information.

**6:** Resistances can vary by ±10% between op amps.

**7:** These parameters have a combined effect on the actual performance of the comparator.

**8:** Input resistance (R1) must be less than or equal to 2 kOhm. The resulting minimum gain of the op amp circuit is equal to four.


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**TABLE 30-54: OP AMP/COMPARATOR VOLTAGE REFERENCE SETTLING TIME SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 2): 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| VR310 | TSET | Settling Time | — | 1 | 10 | µs | Note 1 |

**Note 1:** Settling time is measured while CVRR = 1 and CVR[3:0] bits transition from '0000' to '1111'.

**2:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**TABLE 30-55: OP AMP/COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| VRD310 | CVRES | Resolution | CVRSRC/24 | — | CVRSRC/32 | LSb | |
| VRD311 | CVRAA | Absolute Accuracy(2) | — | ±25 | — | mV | CVRSRC = 3.3V |
| VRD313 | CVRSRC | Input Reference Voltage | 0 | — | AVDD + 0.3 | V | |
| VRD314 | CVROUT | Buffer Output Resistance(2) | — | 1.5k | — | Ω | |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** Parameter is characterized but not tested in manufacturing.

**TABLE 30-56: CTMU CURRENT SOURCE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions:3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **CTMU Current Source** | | | | | | | |
| CTMUI1 | IOUT1 | Base Range(1) | 0.29 | — | 0.77 | µA | CTMUICON[9:8] = 01 |
| CTMUI2 | IOUT2 | 10x Range(1) | 3.85 | — | 7.7 | µA | CTMUICON[9:8] = 10 |
| CTMUI3 | IOUT3 | 100x Range(1) | 38.5 | — | 77 | µA | CTMUICON[9:8] = 11 |
| CTMUI4 | IOUT4 | 1000x Range(1) | 385 | — | 770 | µA | CTMUICON[9:8] = 00 |
| CTMUFV1 | VF | Temperature Diode Forward Voltage(1,2) | — | 0.598 | — | V | TA = +25°C, CTMUICON[9:8] = 01 |
| | | | — | 0.658 | — | V | TA = +25°C, CTMUICON[9:8] = 10 |
| | | | — | 0.721 | — | V | TA = +25°C, CTMUICON[9:8] = 11 |
| CTMUFV2 | VFVR | Temperature Diode Rate of Change(1,2,3) | — | -1.92 | — | mV/ºC | CTMUICON[9:8] = 01 |
| | | | — | -1.74 | — | mV/ºC | CTMUICON[9:8] = 10 |
| | | | — | -1.56 | — | mV/ºC | CTMUICON[9:8] = 11 |

**Note 1:** Nominal value at center point of current trim range (CTMUICON[15:10] = 000000).

**2:** Parameters are characterized but not tested in manufacturing.

**3:** Measurements taken with the following conditions:

- VREF+ = AVDD = 3.3V
- ADC configured for 10-bit mode
- ADC module configured for conversion speed of 500 ksps
- All PMDx bits are cleared (PMDx = 0)
- Executing a `while(1)` statement
- Device operating from the FRC with no PLL


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**TABLE 30-57: ADC MODULE SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1]<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Device Supply** | | | | | | | |
| AD01 | AVDD | Module VDD Supply | Greater of: VDD – 0.3 or 3.0 | — | Lesser of: VDD + 0.3 or 3.6 | V | |
| AD02 | AVSS | Module VSS Supply | VSS – 0.3 | — | VSS + 0.3 | V | |
| **Reference Inputs** | | | | | | | |
| AD05 | VREFH | Reference Voltage High | AVSS + 2.5 | — | AVDD | V | VREFH = VREF+<br>VREFL = VREF- **(Note 1)** |
| AD05a | | | 3.0 | — | 3.6 | V | VREFH = AVDD<br>VREFL = AVSS = 0 |
| AD06 | VREFL | Reference Voltage Low | AVSS | — | AVDD – 2.5 | V | **Note 1** |
| AD06a | | | 0 | — | 0 | V | VREFH = AVDD<br>VREFL = AVSS = 0 |
| AD07 | VREF | Absolute Reference Voltage | 2.5 | — | 3.6 | V | VREF = VREFH - VREFL |
| AD08 | IREF | Current Drain | —<br>— | —<br>— | 10<br>600 | µA<br>µA | ADC off<br>ADC on |
| AD09 | IAD | Operating Current[2] | — | 5 | — | mA | ADC operating in 10-bit mode **(Note 1)** |
| | | | — | 2 | — | mA | ADC operating in 12-bit mode **(Note 1)** |
| **Analog Input** | | | | | | | |
| AD12 | VINH | Input Voltage Range VINH | VINL | — | VREFH | V | This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input |
| AD13 | VINL | Input Voltage Range VINL | VREFL | — | AVSS + 1V | V | This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input |
| AD17 | RIN | Recommended Impedance of Analog Voltage Source | — | — | 200 | Ω | Impedance to achieve maximum performance of ADC |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** Parameter is characterized but not tested in manufacturing.

**TABLE 30-58: ADC MODULE SPECIFICATIONS (12-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1]<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **ADC Accuracy (12-Bit Mode)** | | | | | | | |
| AD20a | Nr | Resolution | 12 Data Bits | | | bits | |
| AD21a | INL | Integral Nonlinearity | -2.5 | — | 2.5 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -5.5 | — | 5.5 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD22a | DNL | Differential Nonlinearity | -1 | — | 1 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -1 | — | 1 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD23a | GERR | Gain Error[3] | -10 | — | 10 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -10 | — | 10 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD24a | EOFF | Offset Error | -5 | — | 5 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -5 | — | 5 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD25a | — | Monotonicity | — | — | — | — | Guaranteed |
| **Dynamic Performance (12-Bit Mode)** | | | | | | | |
| AD30a | THD | Total Harmonic Distortion[3] | — | 75 | — | dB | |
| AD31a | SINAD | Signal to Noise and Distortion[3] | — | 68 | — | dB | |
| AD32a | SFDR | Spurious Free Dynamic Range[3] | — | 80 | — | dB | |
| AD33a | FNYQ | Input Signal Bandwidth[3] | — | 250 | — | kHz | |
| AD34a | ENOB | Effective Number of Bits[3] | 11.09 | 11.3 | — | bits | |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

**3:** Parameters are characterized but not tested in manufacturing.


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**TABLE 30-59: ADC MODULE SPECIFICATIONS (10-BIT MODE)**

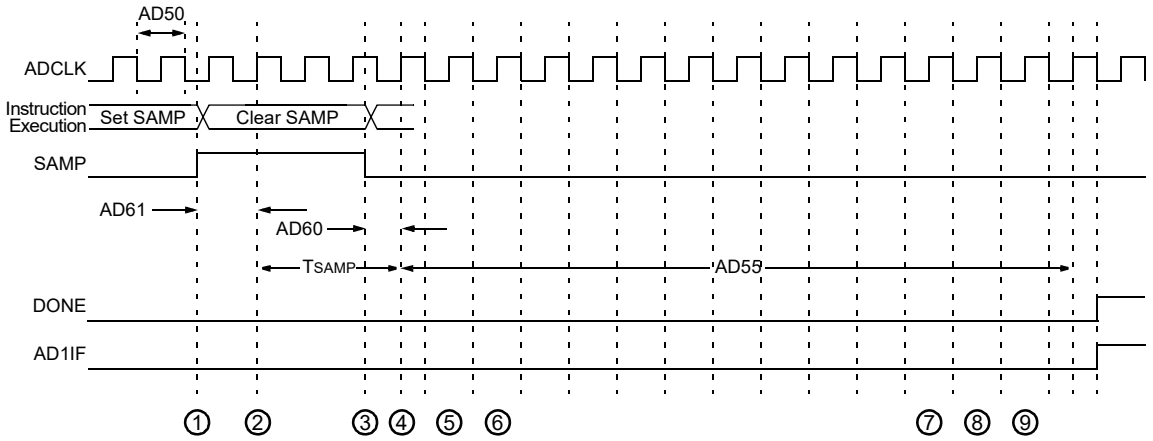
| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1]<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **ADC Accuracy (10-Bit Mode)** | | | | | | | |
| AD20b | Nr | Resolution | 10 Data Bits | | | bits | |
| AD21b | INL | Integral Nonlinearity | -0.625 | — | 0.625 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -1.5 | — | 1.5 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD22b | DNL | Differential Nonlinearity | -0.25 | — | 0.25 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -0.25 | — | 0.25 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD23b | GERR | Gain Error | -2.5 | — | 2.5 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -2.5 | — | 2.5 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD24b | EOFF | Offset Error | -1.25 | — | 1.25 | LSb | -40°C ≤ TA ≤ +85°C **(Note 2)** |
| | | | -1.25 | — | 1.25 | LSb | +85°C < TA ≤ +125°C **(Note 2)** |
| AD25b | — | Monotonicity | — | — | — | — | Guaranteed |
| **Dynamic Performance (10-Bit Mode)** | | | | | | | |
| AD30b | THD | Total Harmonic Distortion[3] | — | 64 | — | dB | |
| AD31b | SINAD | Signal to Noise and Distortion[3] | — | 57 | — | dB | |
| AD32b | SFDR | Spurious Free Dynamic Range[3] | — | 72 | — | dB | |
| AD33b | FNYQ | Input Signal Bandwidth[3] | — | 550 | — | kHz | |
| AD34b | ENOB | Effective Number of Bits[3] | — | 9.4 | — | bits | |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

**3:** Parameters are characterized but not tested in manufacturing.

**FIGURE 30-36: ADC CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC[2:0] = 000, SSRCG = 0)**




1 – Software sets AD1CON1. SAMP to start sampling.

2 – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*.

3 – Software clears AD1CON1. SAMP to start conversion.

4 – Sampling ends, conversion sequence starts.

5 – Convert bit 11.

6 – Convert bit 10.

7 – Convert bit 1.

8 – Convert bit 0.

9 – One TAD for end of conversion.


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**TABLE 30-60: ADC CONVERSION (12-BIT MODE) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1]<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| AD50 | TAD | ADC Clock Period | 117.6 | — | — | ns | |
| AD51 | tRC | ADC Internal RC Oscillator Period[2] | — | 250 | — | ns | |
| **Conversion Rate** | | | | | | | |
| AD55 | tCONV | Conversion Time | — | 14 TAD | | ns | |
| AD56 | FCNV | Throughput Rate | — | — | 500 | ksps | |
| AD57a | TSAMP | Sample Time when Sampling any ANx Input | 3 TAD | — | — | — | |
| AD57b | TSAMP | Sample Time when Sampling the Op Amp Outputs (Configuration A and Configuration B)[4,5] | 3 TAD | — | — | — | |
| **Timing Parameters** | | | | | | | |
| AD60 | tPCS | Conversion Start from Sample Trigger[2,3] | 2 TAD | — | 3 TAD | — | Auto-convert trigger is not selected |
| AD61 | tPSS | Sample Start from Setting Sample (SAMP) bit[2,3] | 2 TAD | — | 3 TAD | — | |
| AD62 | tCSS | Conversion Completion to Sample Start (ASAM = 1)[2,3] | — | 0.5 TAD | — | — | |
| AD63 | tDPU | Time to Stabilize Analog Stage from ADC Off to ADC On[2,3] | — | — | 20 | μs | **Note 6** |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** Parameters are characterized but not tested in manufacturing.

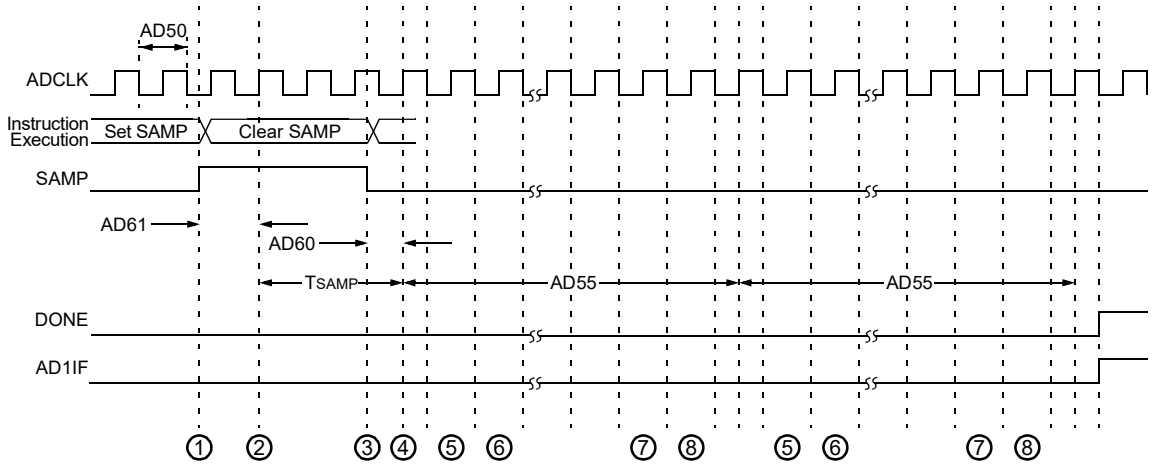
**3:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

**4:** See Figure 25-6 for configuration information.

**5:** See Figure 25-7 for configuration information.

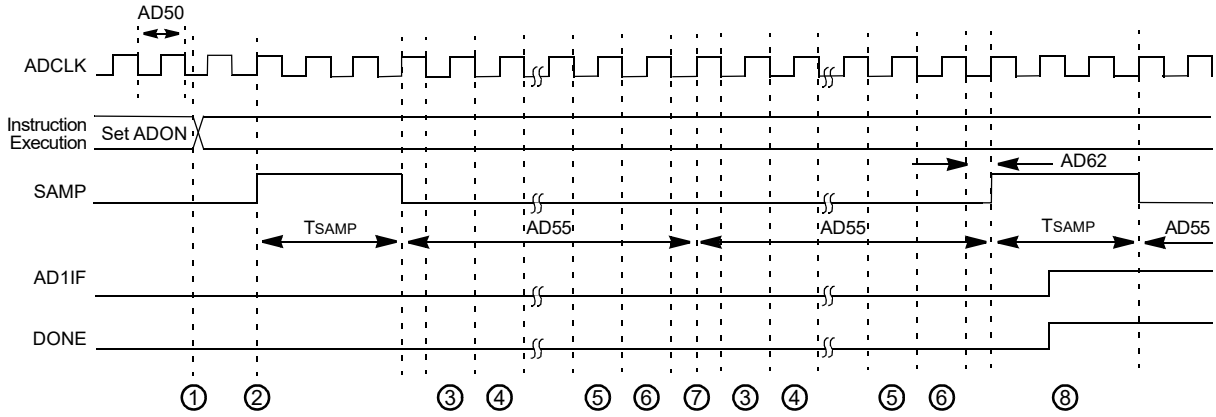
**6:** The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1[15]) = 1). During this time, the ADC result is indeterminate.

**FIGURE 30-37: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS[1:0] = 01, SIMSAM = 0, ASAM = 0, SSRC[2:0] = 000, SSRCG = 0)**




1. – Software sets AD1CON1. SAMP to start sampling.
2. – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*.
3. – Software clears AD1CON1. SAMP to start conversion.
4. – Sampling ends, conversion sequence starts.
5. – Convert bit 9.
6. – Convert bit 8.
7. – Convert bit 0.
8. – One TAD for end of conversion.

**FIGURE 30-38: ADC CONVERSION (10-BIT MODE) TIMING CHARACTERISTICS (CHPS[1:0] = 01, SIMSAM = 0, ASAM = 1, SSRC[2:0] = 111, SSRCG = 0, SAMC[4:0] = 00010)**




1. – Software sets AD1CON1. ADON to start AD operation.
2. – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) in the *"dsPIC33/PIC24 Family Reference Manual"*.
3. – Convert bit 9.
4. – Convert bit 8.
5. – Convert bit 0.
6. – One TAD for end of conversion.
7. – Begin conversion of next channel.
8. – Sample for time specified by SAMC[4:0].


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**TABLE 30-61: ADC CONVERSION (10-BIT MODE) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1]<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **Clock Parameters** | | | | | | | |
| AD50 | TAD | ADC Clock Period | 76 | — | — | ns | |
| AD51 | tRC | ADC Internal RC Oscillator Period[2] | — | 250 | — | ns | |
| **Conversion Rate** | | | | | | | |
| AD55 | tCONV | Conversion Time | — | 12 TAD | — | — | |
| AD56 | FCNV | Throughput Rate | — | — | 1.1 | Msps | Using simultaneous sampling |
| AD57a | TSAMP | Sample Time when Sampling any ANx Input | 2 TAD | — | — | — | |
| AD57b | TSAMP | Sample Time when Sampling the Op Amp Outputs (Configuration A and Configuration B)[4,5] | 4 TAD | — | — | — | |
| **Timing Parameters** | | | | | | | |
| AD60 | tPCS | Conversion Start from Sample Trigger[2,3] | 2 TAD | — | 3 TAD | — | Auto-convert trigger is not selected |
| AD61 | tPSS | Sample Start from Setting Sample (SAMP) bit[2,3]) | 2 TAD | — | 3 TAD | — | |
| AD62 | tCSS | Conversion Completion to Sample Start (ASAM = 1)[2,3] | — | 0.5 TAD | — | — | |
| AD63 | tDPU | Time to Stabilize Analog Stage from ADC Off to ADC On[2,3] | — | — | 20 | μs | **Note 6** |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, op amp/comparator and comparator voltage reference) may have degraded performance. Refer to Parameter BO10 in Table 30-13 for the minimum and maximum BOR values.

**2:** Parameters are characterized but not tested in manufacturing.

**3:** Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

**4:** See Figure 25-6 for configuration information.

**5:** See Figure 25-7 for configuration information.

**6:** The parameter, tDPU, is the time required for the ADC module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1[15]) = 1). During this time, the ADC result is indeterminate.

**TABLE 30-62: DMA MODULE TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.[1]** | **Max.** | **Units** | **Conditions** |
| DM1 | DMA Byte/Word Transfer Latency | 1 TCY[2] | — | — | ns | |

**Note 1:** These parameters are characterized, but not tested in manufacturing.

**2:** Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.

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**NOTES:**


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# 31.0 HIGH-TEMPERATURE ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X electrical characteristics for devices operating in an ambient temperature range of -40°C to +150°C.

The specifications between -40°C to +150°C are identical to those shown in **Section 30.0 "Electrical Characteristics"** for operation between -40°C to +125°C, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter DC10 in **Section 30.0 "Electrical Characteristics"** is the Industrial and Extended temperature equivalent of HDC10.

Absolute maximum ratings for the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X high-temperature devices are listed below. Exposure to these maximum rating conditions for extended periods can affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

## Absolute Maximum Ratings(1)

Ambient temperature under bias(2) ..... -40°C to +150°C
Storage temperature ..... -65°C to +160°C
Voltage on $V_{DD}$ with respect to $V_{SS}$ ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to $V_{SS}$(3) ..... -0.3V to ($V_{DD}$ + 0.3V)
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD}$ < 3.0V(3) ..... -0.3V to 3.6V
Voltage on any 5V tolerant pin with respect to $V_{SS}$ when $V_{DD} \geq 3.0V$(3) ..... -0.3V to 5.5V
Maximum current out of $V_{SS}$ pin ..... 60 mA
Maximum current into $V_{DD}$ pin(4) ..... 60 mA
Maximum junction temperature ..... +155°C
Maximum current sourced/sunk by any 4x I/O pin ..... 10 mA
Maximum current sourced/sunk by any 8x I/O pin ..... 15 mA
Maximum current sunk by all ports combined ..... 70 mA
Maximum current sourced by all ports combined(4) ..... 70 mA

**Note 1:** Stresses above those listed under "Absolute Maximum Ratings" can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods can affect device reliability.

**2:** AEC-Q100 reliability testing for devices intended to operate at +150°C is 1,000 hours. Any design in which the total operating time from +125°C to +150°C will be greater than 1,000 hours is not warranted without prior written approval from Microchip Technology Inc.

**3:** Refer to the **"Pin Diagrams"** section for 5V tolerant pins.

**4:** Maximum allowable current is a function of device maximum power dissipation (see Table 31-2).

## 31.1 High-Temperature DC Characteristics

**TABLE 31-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts) | Temperature Range (in °C) | Max MIPS |
|---|---|---|---|
| | | | dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X |
| HDC5 | 3.0 to 3.6V(1) | -40°C to +150°C | 40 |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules, such as the ADC, may have degraded performance. Device functionality is tested but not characterized.

**TABLE 31-2: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| High-Temperature Devices | | | | | |
| Operating Junction Temperature Range | TJ | -40 | — | +165 | °C |
| Operating Ambient Temperature Range | TA | -40 | — | +150 | °C |
| Power Dissipation:<br>Internal Chip Power Dissipation:<br>PINT = VDD x (IDD – Σ IOH)<br>I/O Pin Power Dissipation:<br>I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL) | PD | PINT + PI/O | | | W |
| Maximum Allowed Power Dissipation | PDMAX | (TJ – TA)/θJA | | | W |

**TABLE 31-3: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| Parameter No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions |
| **Operating Voltage** | | | | | | | |
| HDC10 | **Supply Voltage** | | | | | | |
| | VDD | — | 3.0 | 3.3 | 3.6 | V | -40°C to +150°C |


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**TABLE 31-4: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | |
|---|---|---|---|---|---|---|
| Parameter No. | Typical | Max | Units | Conditions | | |
| **Power-Down Current (IPD)** | | | | | | |
| HDC60e | 1400 | 2500 | µA | +150°C | 3.3V | Base Power-Down Current (Notes 1 and 3) |
| HDC61c | 15 | — | µA | +150°C | 3.3V | Watchdog Timer Current: ΔIWDT (Notes 2 and 4) |

**Note 1:** Base IPD is measured with all peripherals and clocks shut down. All I/Os are configured as inputs and pulled to VSS. WDT, etc., are all switched off and VREGS (RCON[8]) = 1.

**2:** The Δ current is the additional current consumed when the module is enabled. This current should be added to the base IPD current.

**3:** These currents are measured on the device containing the most memory in this family.

**4:** These parameters are characterized, but are not tested in manufacturing.

**TABLE 31-5: DC CHARACTERISTICS: IDLE CURRENT (IIDLE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | |
|---|---|---|---|---|---|---|
| Parameter No. | Typical | Max | Units | Conditions | | |
| HDC44e | 12 | 30 | mA | +150°C | 3.3V | 40 MIPS |

**TABLE 31-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | |
|---|---|---|---|---|---|---|
| Parameter No. | Typical | Max | Units | Conditions | | |
| HDC20 | 9 | 15 | mA | +150°C | 3.3V | 10 MIPS |
| HDC22 | 16 | 25 | mA | +150°C | 3.3V | 20 MIPS |
| HDC23 | 30 | 50 | mA | +150°C | 3.3V | 40 MIPS |

**TABLE 31-7: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| Parameter No. | Typical | Max | Doze Ratio | Units | Conditions | | |
| HDC72a | 24 | 35 | 1:2 | mA | +150°C | 3.3V | 40 MIPS |
| HDC72f(1) | 14 | — | 1:64 | mA | | | |
| HDC72g(1) | 12 | — | 1:128 | mA | | | |

**Note 1:** Parameters with Doze ratios of 1:64 and 1:128 are characterized, but are not tested in manufacturing.

**TABLE 31-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| HDO10 | VOL | **Output Low Voltage**<br>4x Sink Driver Pins(2) | — | — | 0.4 | V | IOL ≤ 5 mA, VDD = 3.3V<br>**(Note 1)** |
| | | **Output Low Voltage**<br>8x Sink Driver Pins(3) | — | — | 0.4 | V | IOL ≤ 8 mA, VDD = 3.3V<br>**(Note 1)** |
| HDO20 | VOH | **Output High Voltage**<br>4x Source Driver Pins(2) | 2.4 | — | — | V | IOH ≥ -10 mA, VDD = 3.3V<br>**(Note 1)** |
| | | **Output High Voltage**<br>8x Source Driver Pins(3) | 2.4 | — | — | V | IOH ≥ 15 mA, VDD = 3.3V<br>**(Note 1)** |
| HDO20A | VOH1 | **Output High Voltage**<br>4x Source Driver Pins(2) | 1.5 | — | — | V | IOH ≥ -3.9 mA, VDD = 3.3V<br>**(Note 1)** |
| | | | 2.0 | — | — | | IOH ≥ -3.7 mA, VDD = 3.3V<br>**(Note 1)** |
| | | | 3.0 | — | — | | IOH ≥ -2 mA, VDD = 3.3V<br>**(Note 1)** |
| | | **Output High Voltage**<br>8x Source Driver Pins(3) | 1.5 | — | — | V | IOH ≥ -7.5 mA, VDD = 3.3V<br>**(Note 1)** |
| | | | 2.0 | — | — | | IOH ≥ -6.8 mA, VDD = 3.3V<br>**(Note 1)** |
| | | | 3.0 | — | — | | IOH ≥ -3 mA, VDD = 3.3V<br>**(Note 1)** |

**Note 1:** Parameters are characterized, but not tested.

**2:** Includes all I/O pins that are not 8x Sink Driver pins (see below).

**3:** Includes the following pins:
**For devices with less than 64 pins:** RA3, RA4, RA9, RB[15:7] and RC3
**For 64-pin devices:** RA4, RA9, RB[15:7], RC3 and RC15

**TABLE 31-9: DC CHARACTERISTICS: PROGRAM MEMORY**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | |
|---|---|---|---|---|---|---|---|
| **Param.** | **Symbol** | **Characteristic(1)** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| | | **Program Flash Memory** | | | | | |
| HD130 | EP | Cell Endurance | 10,000 | — | — | E/W | -40°C to +150°C(2) |
| HD134 | TRETD | Characteristic Retention | 20 | — | — | Year | 1000 E/W cycles or less and no other specifications are violated |

**Note 1:** These parameters are assured by design, but are not characterized or tested in manufacturing.

**2:** Programming of the Flash memory is allowed up to +150°C.


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## 31.2 AC Characteristics and Timing Parameters

The information contained in this section defines dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X and PIC24EPXXXGP/MC20X AC characteristics and timing parameters for high-temperature devices. However, all AC timing specifications in this section are the same as those in **Section 30.2 "AC Characteristics and Timing Parameters"**, with the exception of the parameters listed in this section.

Parameters in this section begin with an H, which denotes High temperature. For example, Parameter OS53 in **Section 30.2 "AC Characteristics and Timing Parameters"** is the Industrial and Extended temperature equivalent of HOS53.

**TABLE 31-10: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC**

| AC CHARACTERISTICS | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +150°C<br>Operating voltage VDD range as described in Table 31-1. |
|---|---|

**FIGURE 31-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS**

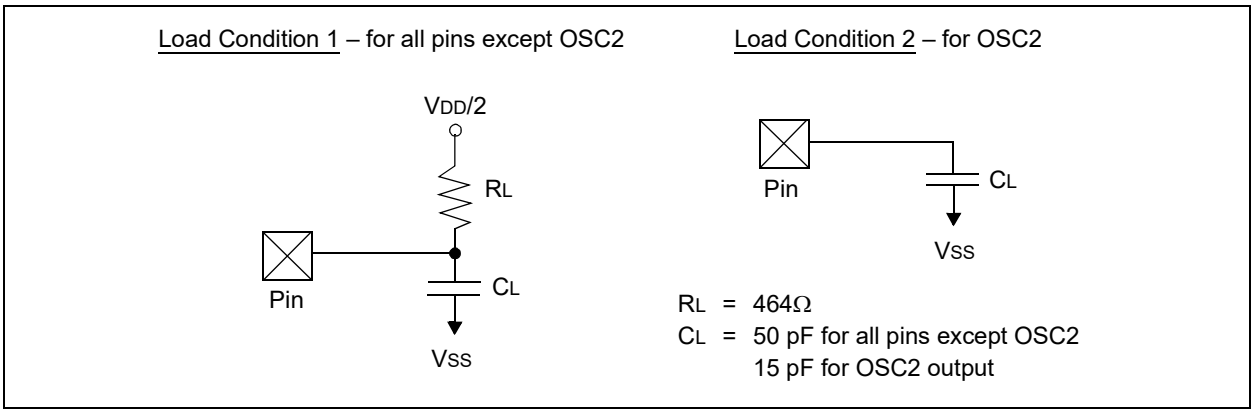


**TABLE 31-11: PLL CLOCK TIMING SPECIFICATIONS**

| AC CHARACTERISTICS | | | **Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| HOS53 | DCLK | CLKO Stability (Jitter)(1) | -5 | 0.5 | 5 | % | Measured over 100 ms period |

**Note 1:** These parameters are characterized by similarity, but are not tested in manufacturing. This specification is based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks use this formula:

$$Peripheral\ Clock\ Jitter = \frac{DCLK}{\sqrt{\left(\frac{FOSC}{Peripheral\ Bit\ Rate\ Clock}\right)}}$$

For example: FOSC = 32 MHz, DCLK = 5%, SPIx bit rate clock (i.e., SCKx) is 2 MHz.

$$SPI\ SCK\ Jitter = \left[\frac{DCLK}{\sqrt{\left(\frac{32\ MHz}{2\ MHz}\right)}}\right] = \left[\frac{5\%}{\sqrt{16}}\right] = \left[\frac{5\%}{4}\right] = 1.25\%$$

**TABLE 31-12: INTERNAL FRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature +125°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Characteristic | Min | Typ | Max | Units | Conditions | |
| | **Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1)** | | | | | | |
| H20 | FRC | -3 | -2 | +3 | % | +125°C ≤ TA ≤ +150°C | VDD = 3.0-3.6V |

**Note 1:** Frequency is calibrated at +25°C and 3.3V.

**TABLE 31-13: INTERNAL RC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Characteristic | Min | Typ | Max | Units | Conditions | |
| | **LPRC @ 32.768 kHz(1,2)** | | | | | | |
| HF21 | LPRC | -30 | — | +30 | % | -40°C ≤ TA ≤ +150°C | VDD = 3.0-3.6V |

**Note 1:** Change of LPRC frequency as VDD changes.

**2:** LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT). See **Section 27.5 "Watchdog Timer (WDT)"** for more information.

**TABLE 31-14: OP AMP/COMPARATOR SPECIFICATIONS**

| DC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min. | Typ. | Max. | Units | Conditions |
| **Op Amp DC Characteristics** | | | | | | | |
| HCM42 | VOFFSET | Op Amp Offset Voltage | -40 | ±5 | +40 | mV | |


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**TABLE 31-15: ADC MODULE SPECIFICATIONS (12-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions |
| **ADC Accuracy (12-Bit Mode)(1)** | | | | | | | |
| HAD20a | Nr | Resolution(3) | 12 Data Bits | | | bits | |
| HAD21a | INL | Integral Nonlinearity | -5.5 | — | 5.5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD22a | DNL | Differential Nonlinearity | -1 | — | 1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD23a | GERR | Gain Error | -10 | — | 10 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD24a | EOFF | Offset Error | -5 | — | 5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| **Dynamic Performance (12-Bit Mode)(2)** | | | | | | | |
| HAD33a | FNYQ | Input Signal Bandwidth | — | — | 200 | kHz | |

**Note 1:** These parameters are characterized, but are tested at 20 ksps only.

**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

**3:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**TABLE 31-16: ADC MODULE SPECIFICATIONS (10-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C | | | | |
|---|---|---|---|---|---|---|---|
| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions |
| **ADC Accuracy (10-Bit Mode)(1)** | | | | | | | |
| HAD20b | Nr | Resolution(3) | 10 Data Bits | | | bits | |
| HAD21b | INL | Integral Nonlinearity | -1.5 | — | 1.5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD22b | DNL | Differential Nonlinearity | -0.25 | — | 0.25 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD23b | GERR | Gain Error | -2.5 | — | 2.5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| HAD24b | EOFF | Offset Error | -1.25 | — | 1.25 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V |
| **Dynamic Performance (10-Bit Mode)(2)** | | | | | | | |
| HAD33b | FNYQ | Input Signal Bandwidth | — | — | 400 | kHz | |

**Note 1:** These parameters are characterized, but are tested at 20 ksps only.

**2:** These parameters are characterized by similarity, but are not tested in manufacturing.

**3:** Injection currents > | 0 | can affect the ADC results by approximately 4-6 counts.

**NOTES:**


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## 32.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

**Note:** The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

**FIGURE 32-1: VOH – 4x DRIVER PINS**

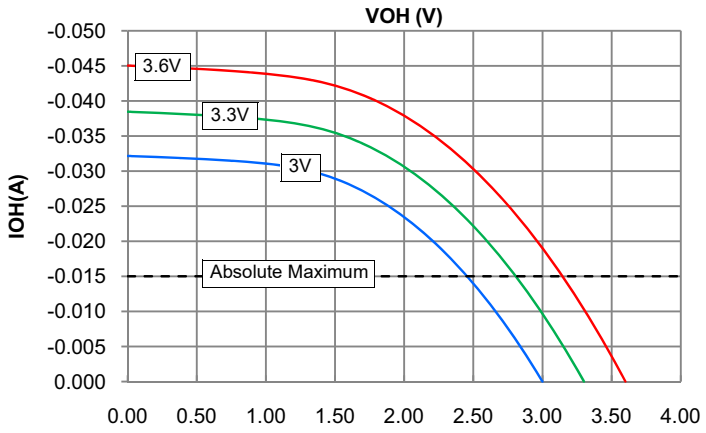


**FIGURE 32-2: VOH – 8x DRIVER PINS**

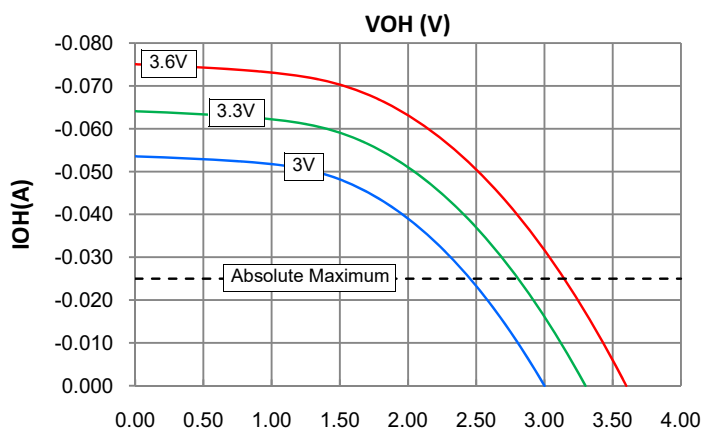


**FIGURE 32-3: VOL – 4x DRIVER PINS**

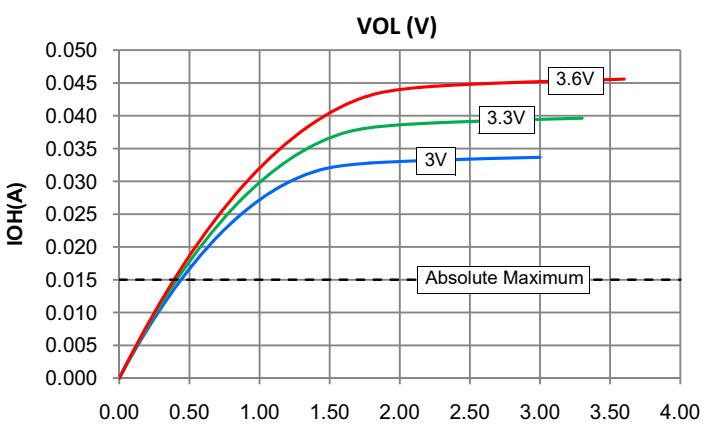


**FIGURE 32-4: VOL – 8x DRIVER PINS**

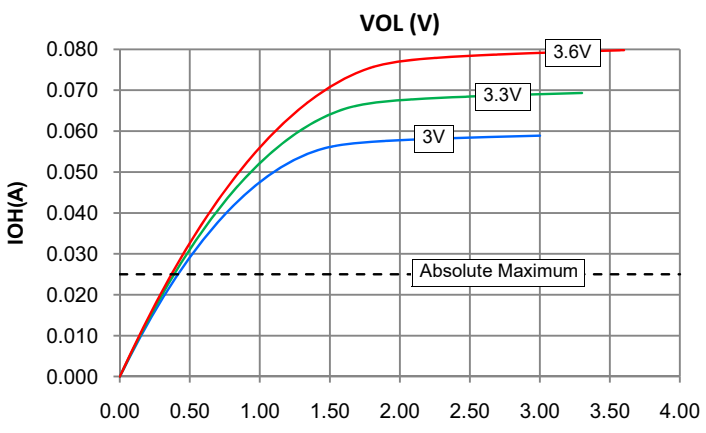


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**FIGURE 32-5: TYPICAL IPD CURRENT @ VDD = 3.3V**

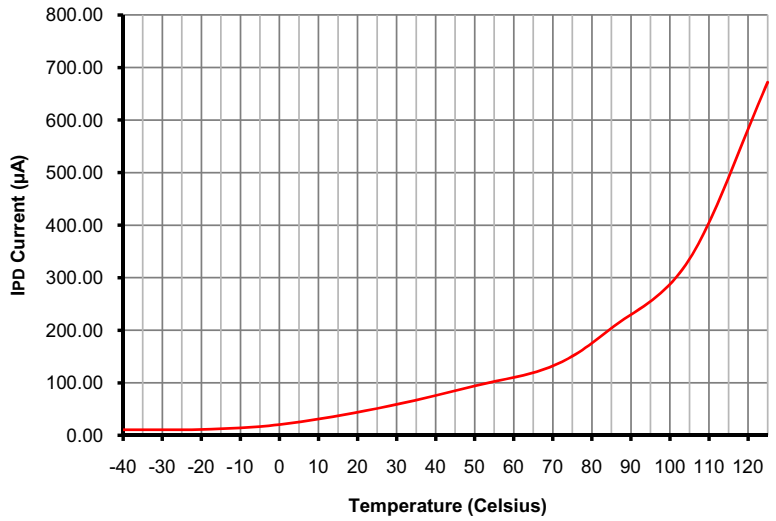


**FIGURE 32-6: TYPICAL/MAXIMUM IDD CURRENT @ VDD = 3.3V**

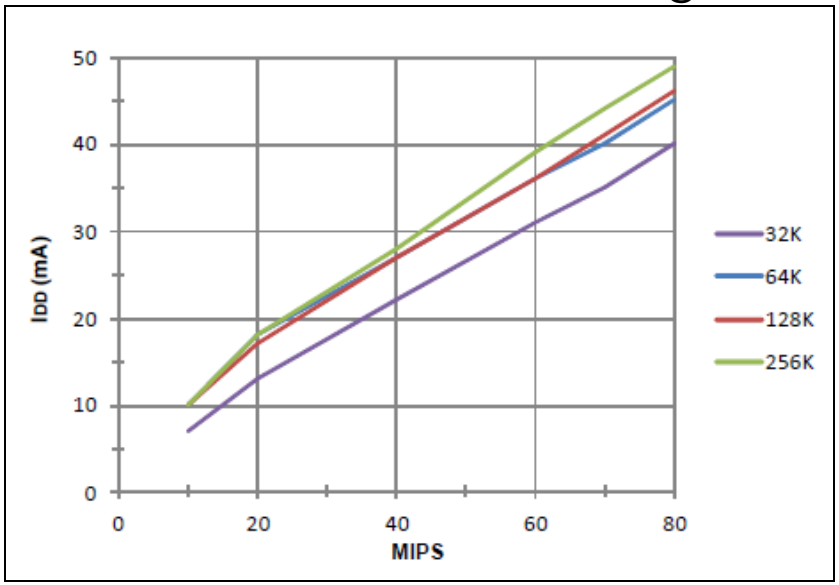


**FIGURE 32-7: TYPICAL IDOZE CURRENT @ VDD = 3.3V**

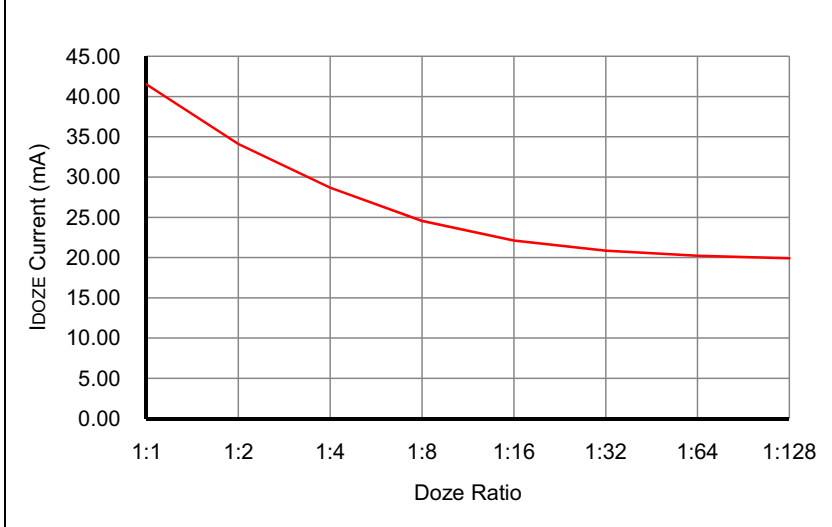


**FIGURE 32-8: TYPICAL IIDLE CURRENT @ VDD = 3.3V**

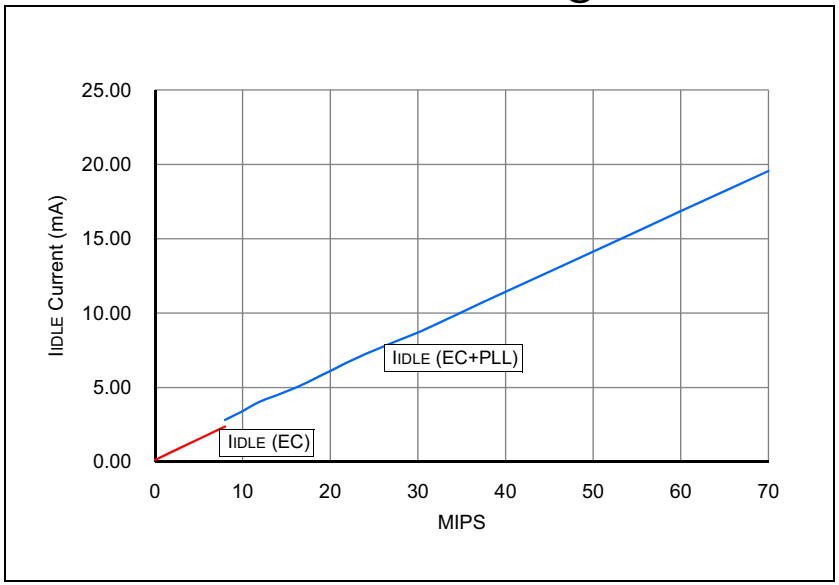




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**FIGURE 32-9: TYPICAL FRC FREQUENCY @ VDD = 3.3V**

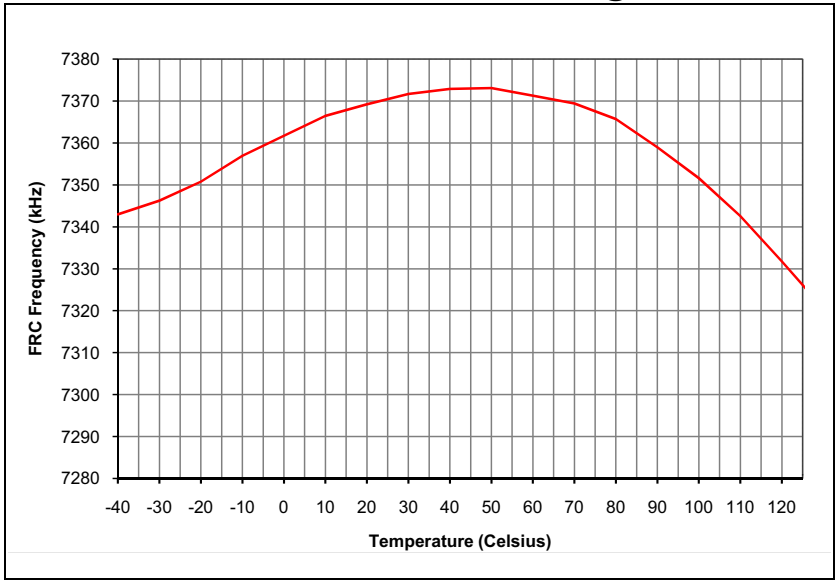
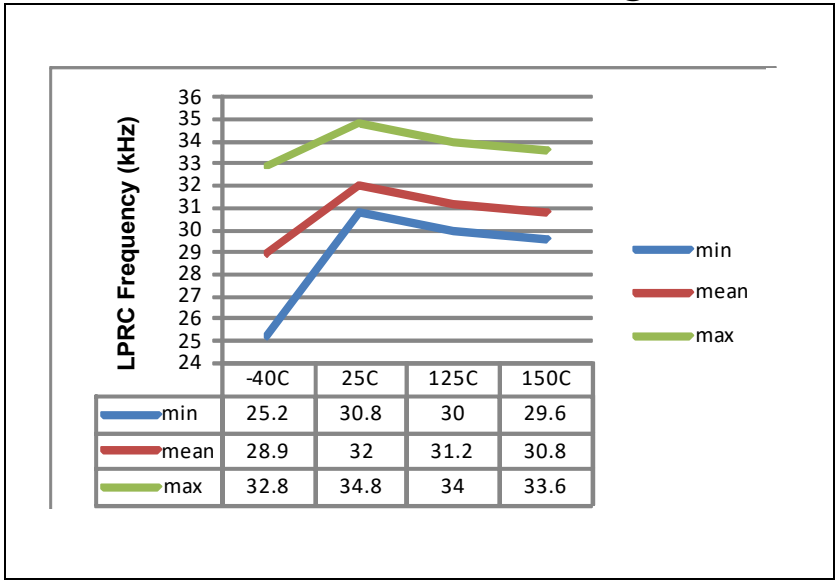
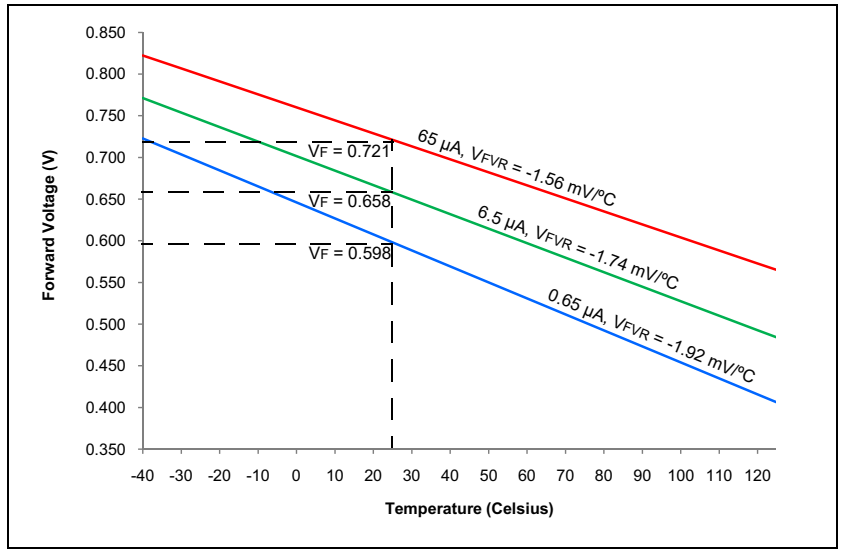



**FIGURE 32-10: TYPICAL LPRC FREQUENCY @ VDD = 3.3V**




| | -40C | 25C | 125C | 150C |
|---|---|---|---|---|
| min | 25.2 | 30.8 | 30 | 29.6 |
| mean | 28.9 | 32 | 31.2 | 30.8 |
| max | 32.8 | 34.8 | 34 | 33.6 |

**FIGURE 32-11: TYPICAL CTMU TEMPERATURE DIODE FORWARD VOLTAGE**

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**NOTES:**


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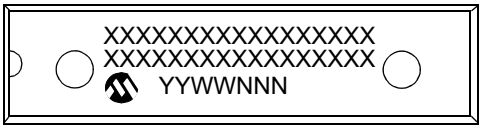
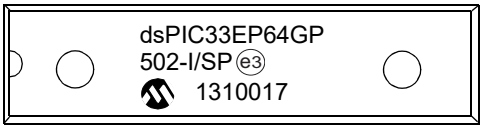
# 33.0 PACKAGING INFORMATION

## 33.1 Package Marking Information

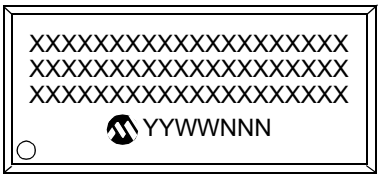
28-Lead SPDIP



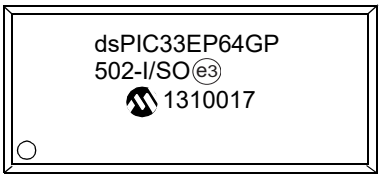

Example




28-Lead SOIC (.300”)



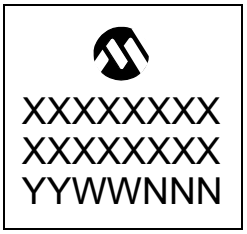

Example




28-Lead SSOP

Example

28-Lead QFN-S (6x6x0.9 mm)



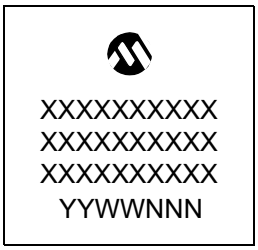

Example

| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | e3 | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

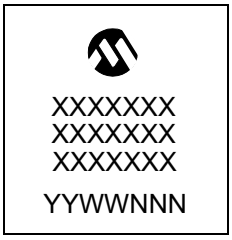
## 33.1 Package Marking Information (Continued)

36-Lead VTLA (TLA)



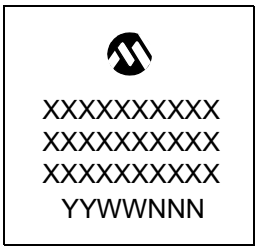

Example

36-Lead UQFN (5x5 mm)



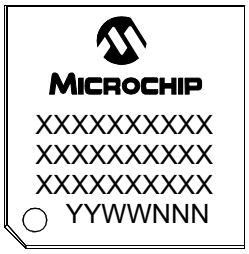

Example

44-Lead VTLA (TLA)



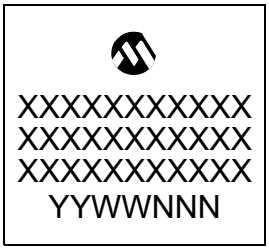

Example

44-Lead TQFP




Example

44-Lead QFN (8x8x0.9 mm)




Example

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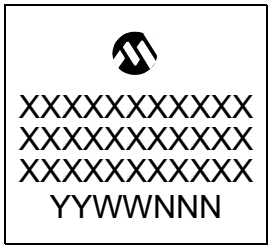
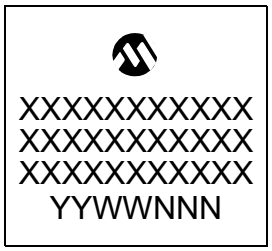
## 33.1 Package Marking Information (Continued)

48-Lead UQFN (6x6x0.5 mm)



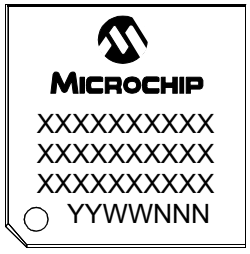

Example

64-Lead QFN (9x9x0.9 mm)

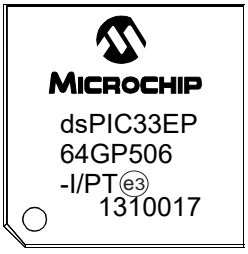



Example

64-Lead TQFP (10x10x1 mm)



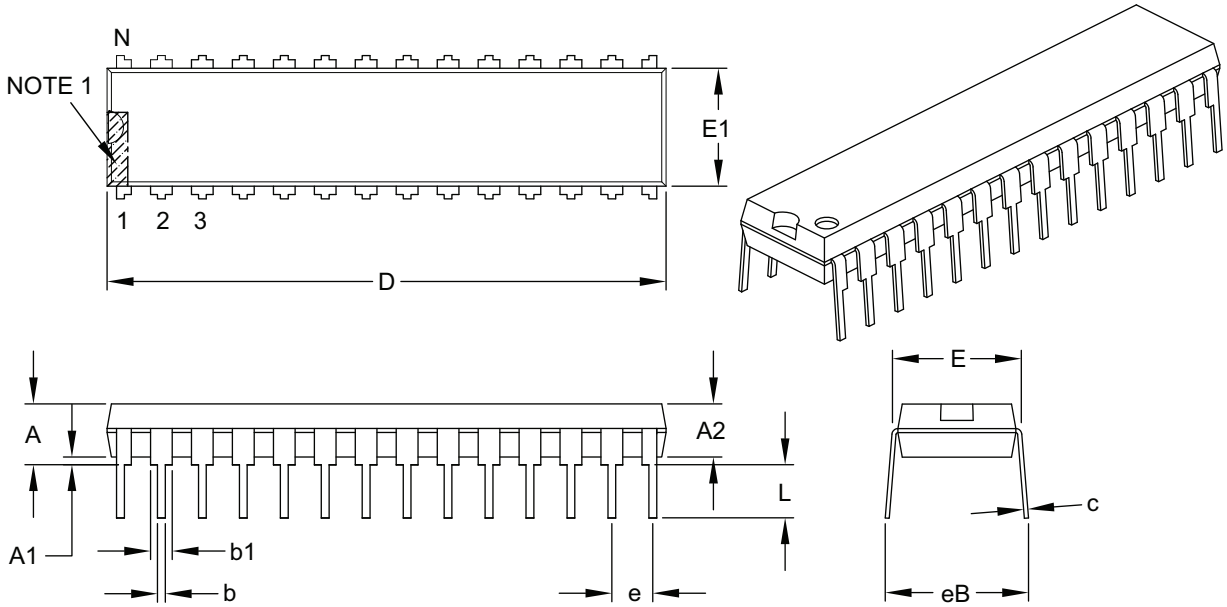

Example



## 33.2 Package Details

### 28-Lead Skinny Plastic Dual In-Line (SP) – 300 mil Body [SPDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | INCHES | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | .100 BSC | |
| Top to Seating Plane | A | – | – | .200 |
| Molded Package Thickness | A2 | .120 | .135 | .150 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .290 | .310 | .335 |
| Molded Package Width | E1 | .240 | .285 | .295 |
| Overall Length | D | 1.345 | 1.365 | 1.400 |
| Tip to Seating Plane | L | .110 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .015 |
| Upper Lead Width | b1 | .040 | .050 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-070B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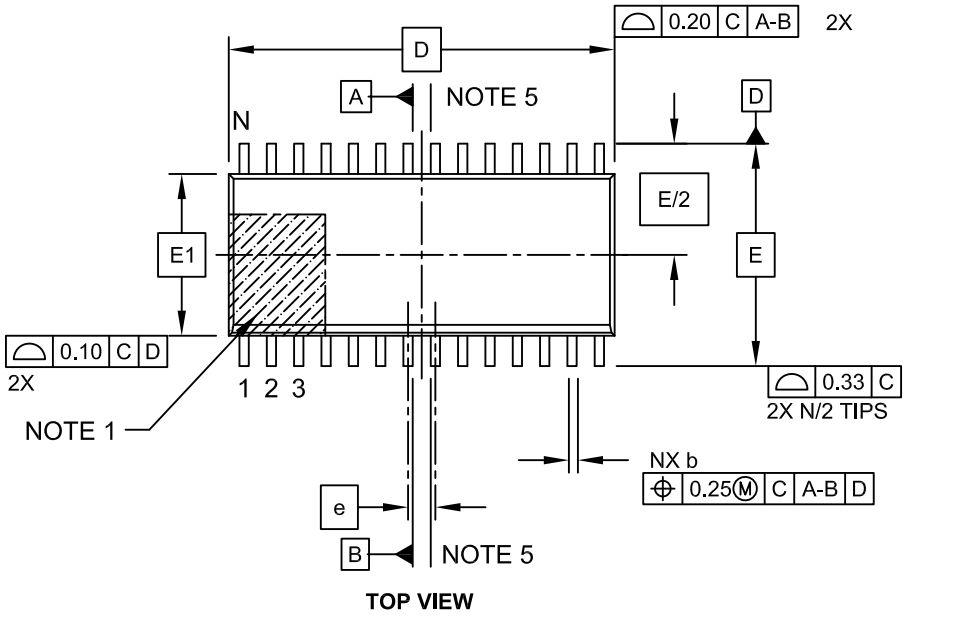
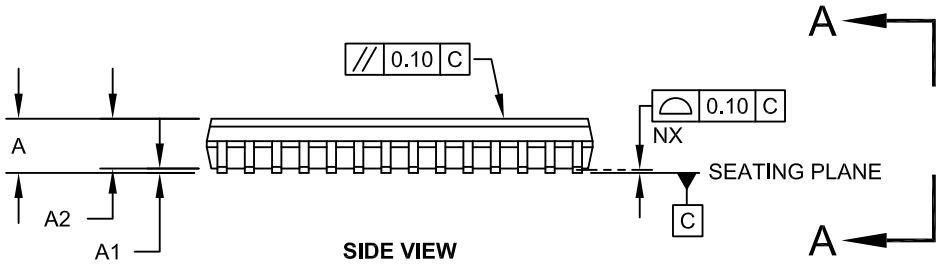
## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

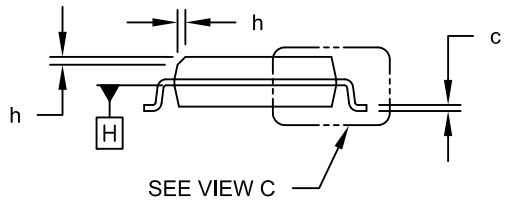
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**TOP VIEW**




**SIDE VIEW**

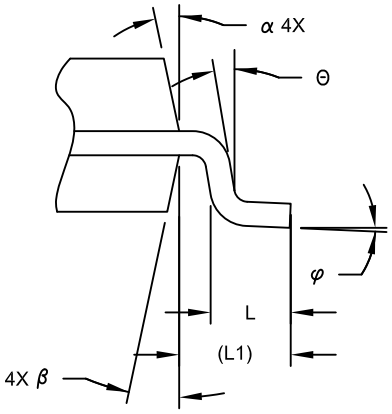



**VIEW A-A**

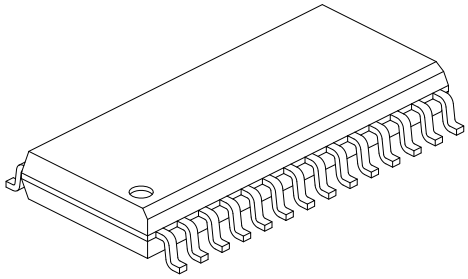
Microchip Technology Drawing C04-052C Sheet 1 of 2

## 28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




VIEW C



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 1.27 BSC | |
| Overall Height | A | - | - | 2.65 |
| Molded Package Thickness | A2 | 2.05 | - | - |
| Standoff § | A1 | 0.10 | - | 0.30 |
| Overall Width | E | | 10.30 BSC | |
| Molded Package Width | E1 | | 7.50 BSC | |
| Overall Length | D | | 17.90 BSC | |
| Chamfer (Optional) | h | 0.25 | - | 0.75 |
| Foot Length | L | 0.40 | - | 1.27 |
| Footprint | L1 | | 1.40 REF | |
| Lead Angle | Θ | 0° | - | - |
| Foot Angle | φ | 0° | - | 8° |
| Lead Thickness | c | 0.18 | - | 0.33 |
| Lead Width | b | 0.31 | - | 0.51 |
| Mold Draft Angle Top | α | 5° | - | 15° |
| Mold Draft Angle Bottom | β | 5° | - | 15° |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing C04-052C Sheet 2 of 2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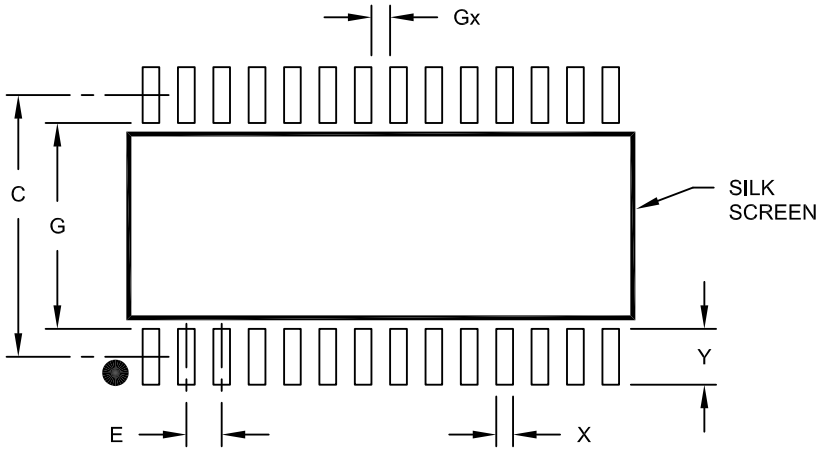
28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 1.27 BSC | | |
| Contact Pad Spacing | C | | 9.40 | |
| Contact Pad Width (X28) | X | | | 0.60 |
| Contact Pad Length (X28) | Y | | | 2.00 |
| Distance Between Pads | Gx | 0.67 | | |
| Distance Between Pads | G | 7.40 | | |

Notes:

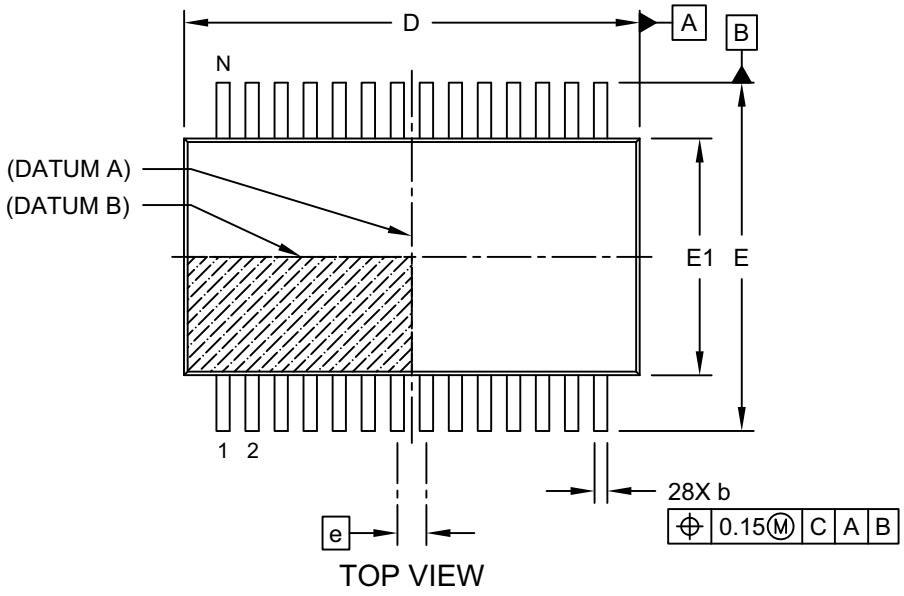
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

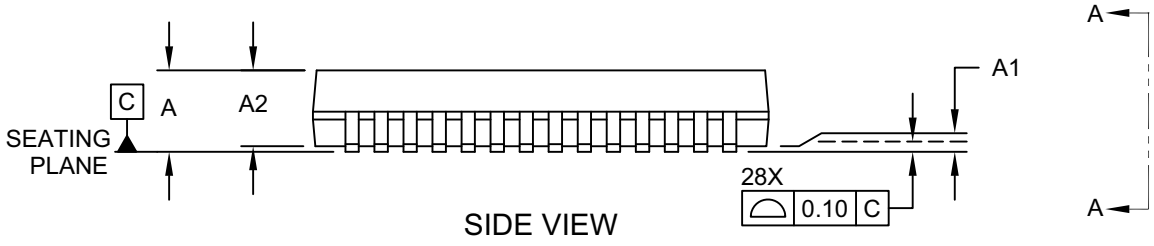
Microchip Technology Drawing No. C04-2052A

## 28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

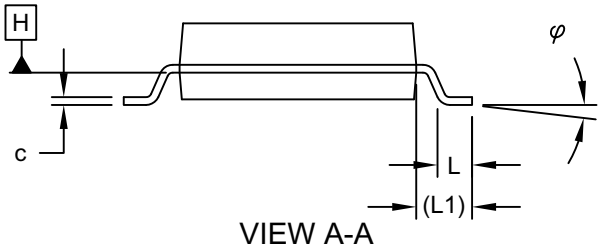
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW




VIEW A-A

Microchip Technology Drawing C04-073 Rev C Sheet 1 of 2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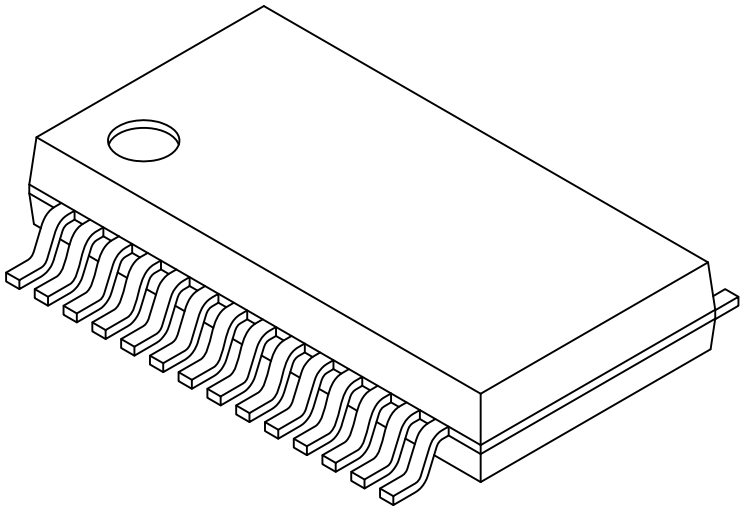
## 28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | - | - | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | - | - |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 9.90 | 10.20 | 10.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | | 1.25 REF | |
| Lead Thickness | c | 0.09 | - | 0.25 |
| Foot Angle | φ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | - | 0.38 |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

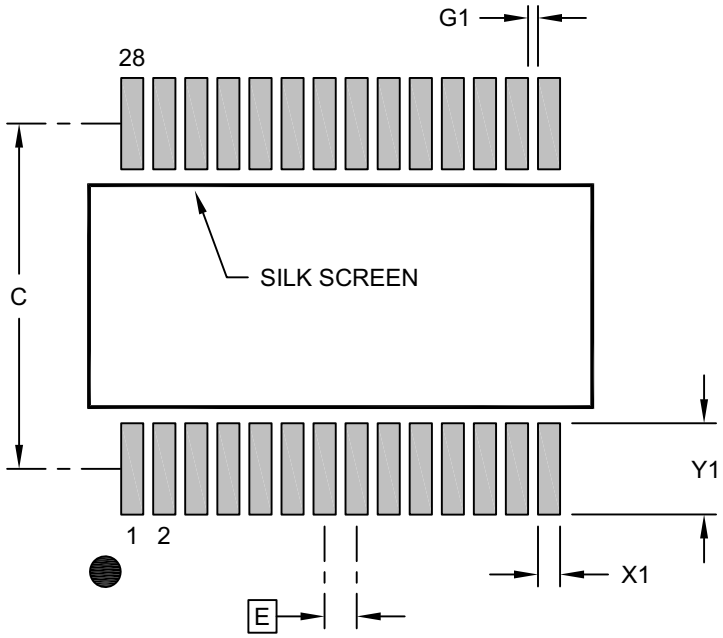
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073 Rev C Sheet 2 of 2

## 28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.65 BSC | | |
| Contact Pad Spacing | C | | 7.00 | |
| Contact Pad Width (X28) | X1 | | | 0.45 |
| Contact Pad Length (X28) | Y1 | | | 1.85 |
| Contact Pad to Center Pad (X26) | G1 | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2073 Rev B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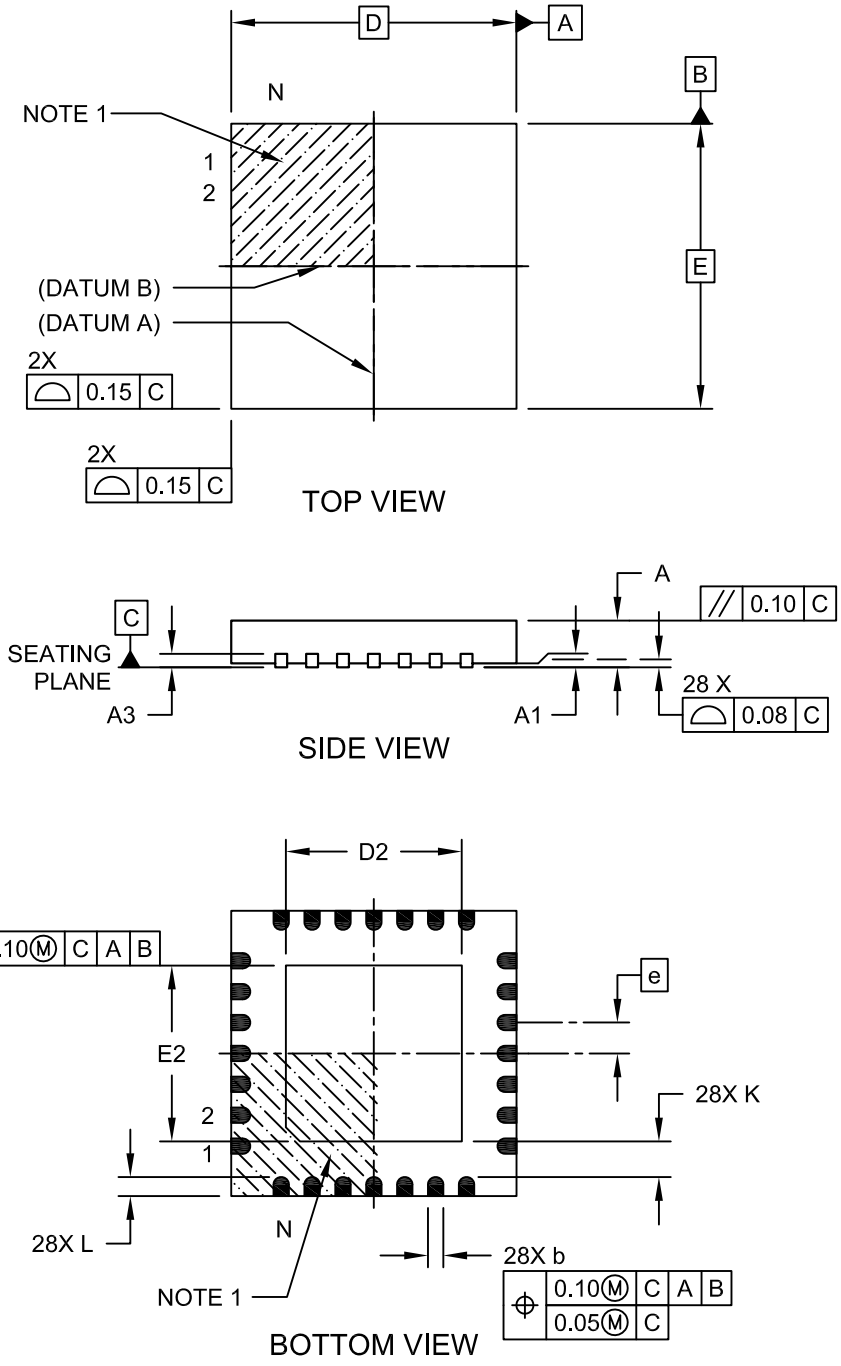
**28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S]**
**With 0.40 mm Terminal Length**

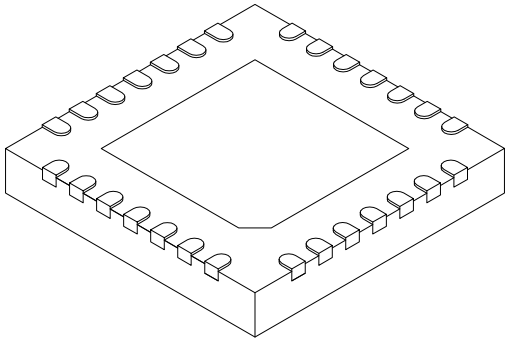
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-124C Sheet 1 of 2

## 28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 28 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 3.65 | 3.70 | 4.70 |
| Overall Length | D | | 6.00 BSC | |
| Exposed Pad Length | D2 | 3.65 | 3.70 | 4.70 |
| Terminal Width | b | 0.23 | 0.30 | 0.35 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-124C Sheet 2 of 2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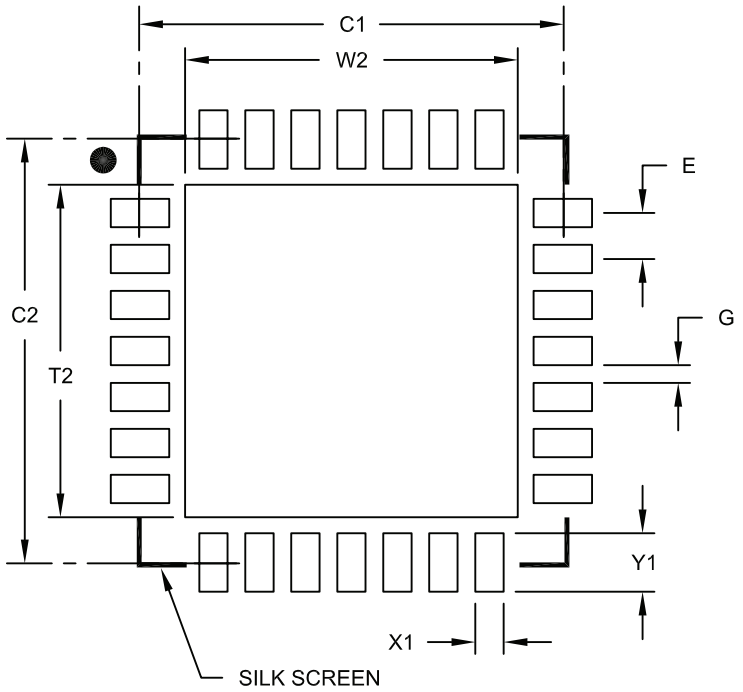
**28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Optional Center Pad Width | W2 | | | 4.70 |
| Optional Center Pad Length | T2 | | | 4.70 |
| Contact Pad Spacing | C1 | | 6.00 | |
| Contact Pad Spacing | C2 | | 6.00 | |
| Contact Pad Width (X28) | X1 | | | 0.40 |
| Contact Pad Length (X28) | Y1 | | | 0.85 |
| Distance Between Pads | G | 0.25 | | |

Notes:

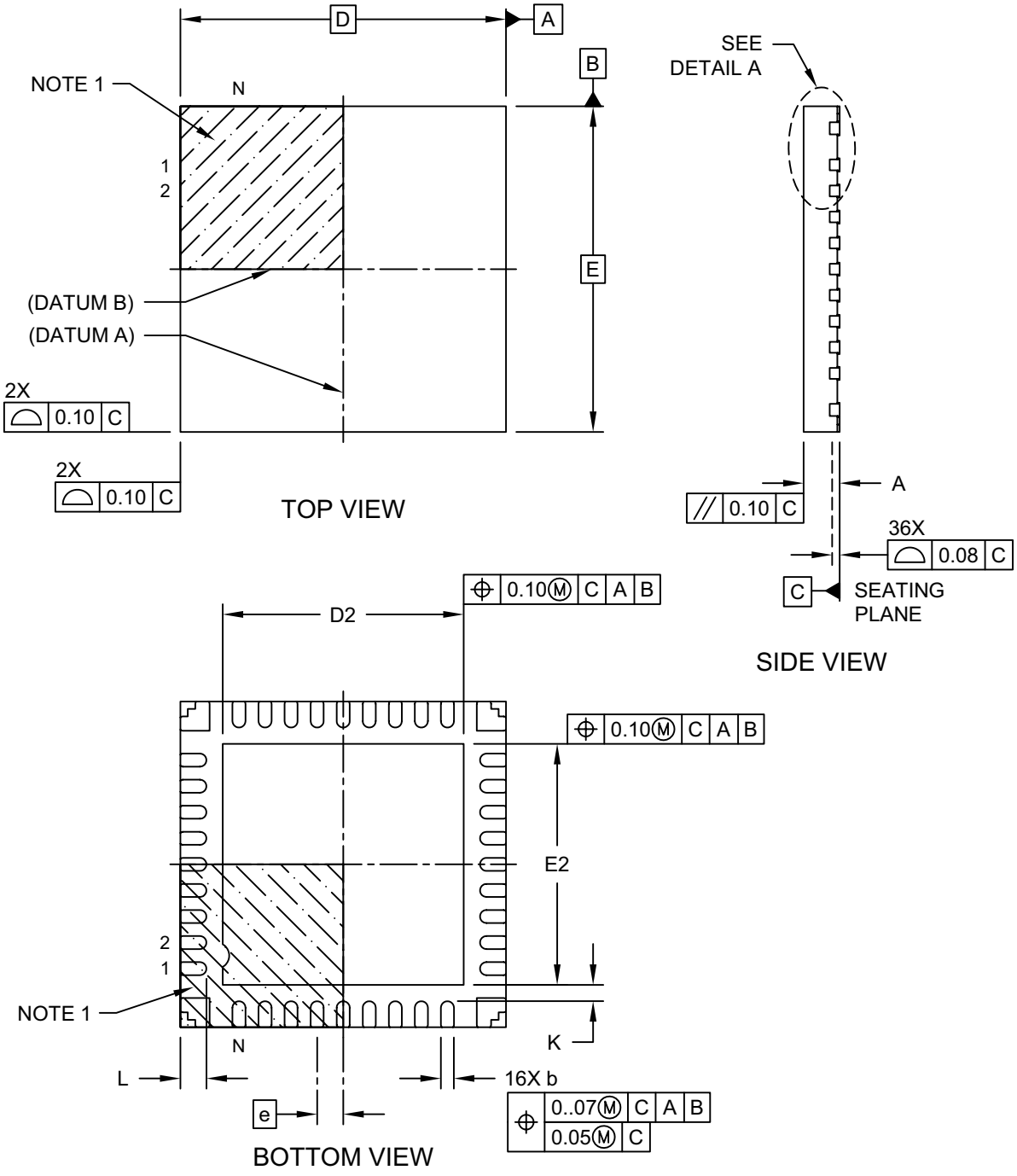
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

## 36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-436–M5 Rev B Sheet 1 of 2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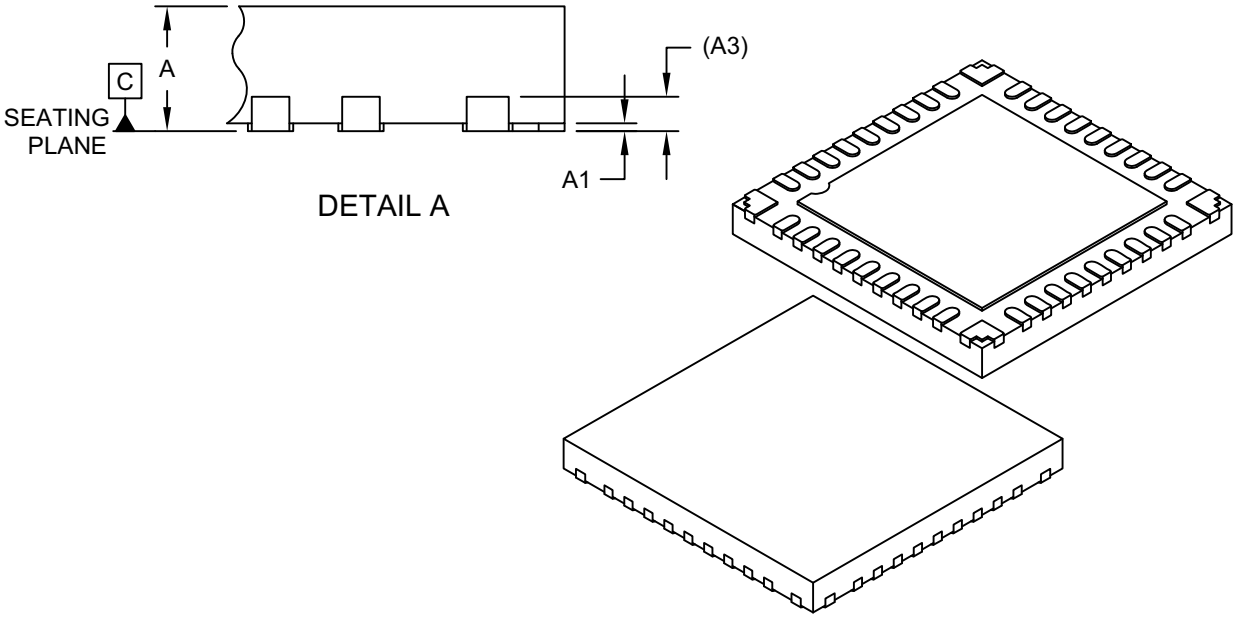
## 36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | N | | 36 | |
| Pitch | e | | 0.40 BSC | |
| Overall Height | A | 0.50 | 0.55 | 0.60 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.152 REF | |
| Overall Length | D | | 5.00 BSC | |
| Exposed Pad Length | D2 | 3.60 | 3.70 | 3.80 |
| Overall Width | E | | 5.00 BSC | |
| Exposed Pad Width | E2 | 3.60 | 3.70 | 3.80 |
| Terminal Width | b | 0.15 | 0.20 | 0.25 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed-Pad | K | | 0.25 REF | |

Notes:

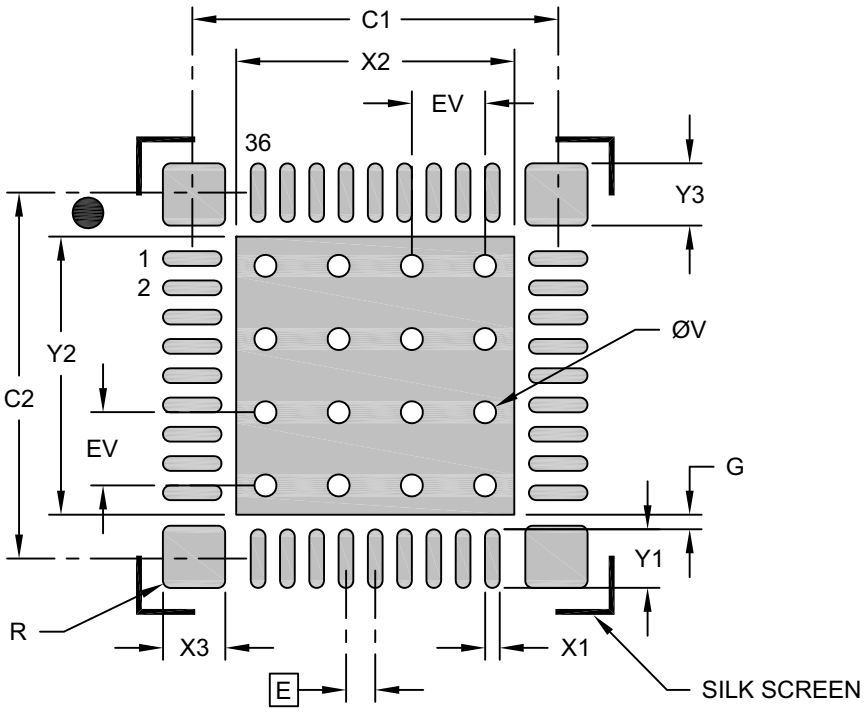
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-436–M5 Rev B Sheet 2 of 2

## 36-Lead Ultra Thin Plastic Quad Flat, No Lead Package (M5) - 5x5 mm Body [UQFN] With Corner Anchors

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.40 BSC | |
| Center Pad Width | X2 | | | 3.80 |
| Center Pad Length | Y2 | | | 3.80 |
| Contact Pad Spacing | C1 | | 5.00 | |
| Contact Pad Spacing | C2 | | 5.00 | |
| Contact Pad Width (X36) | X1 | | | 0.20 |
| Contact Pad Length (X36 | Y1 | | | 0.80 |
| Corner Pad Width (X4) | X3 | | | 0.85 |
| Corner Pad Length (X4) | Y3 | | | 0.85 |
| Corner Pad Radius | R | | 0.10 | |
| Contact Pad to Center Pad (X36) | G | 0.20 | | |
| Thermal Via Diameter | V | | 0.30 | |
| Thermal Via Pitch | EV | | 1.00 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2436–M5 Rev B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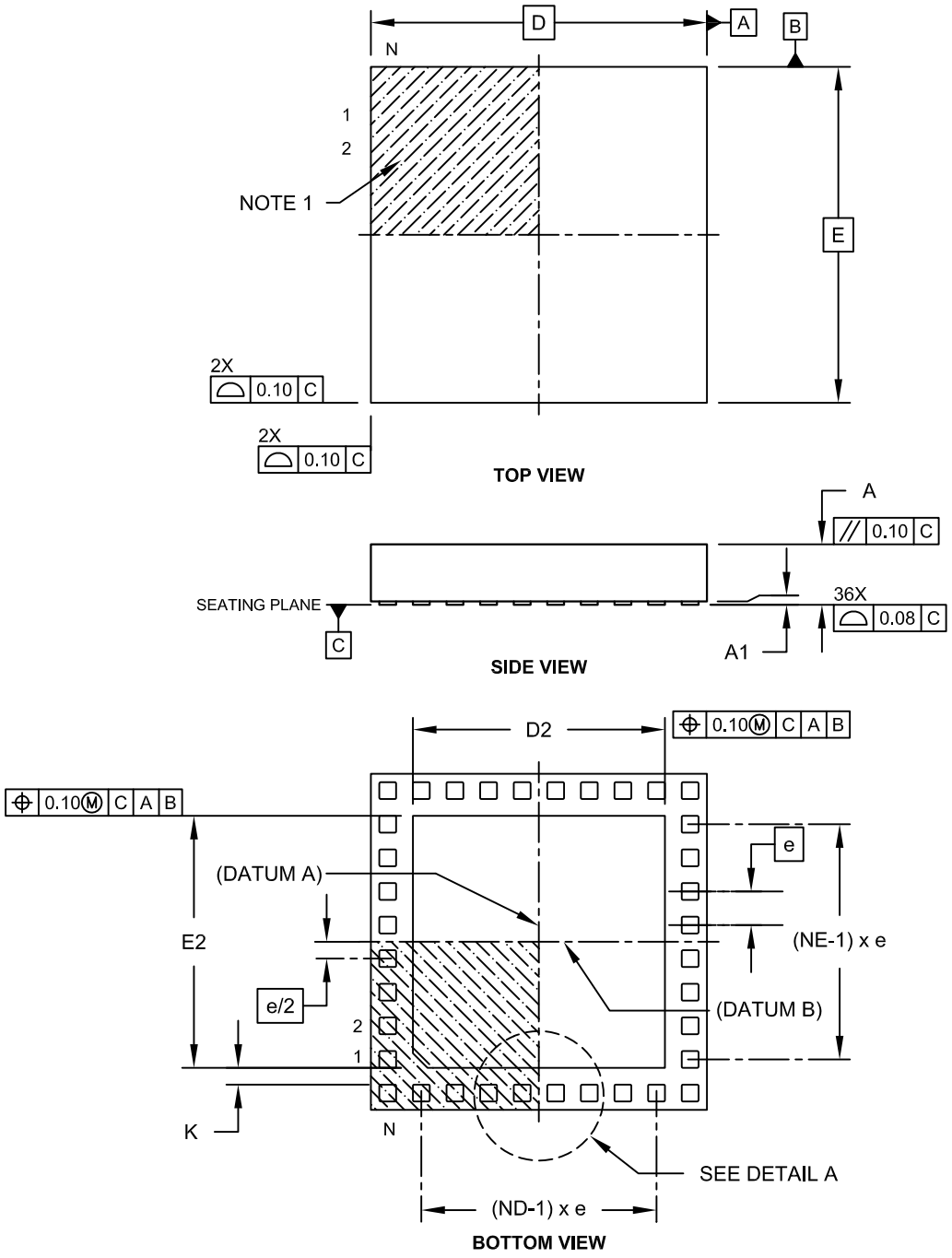
## 36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

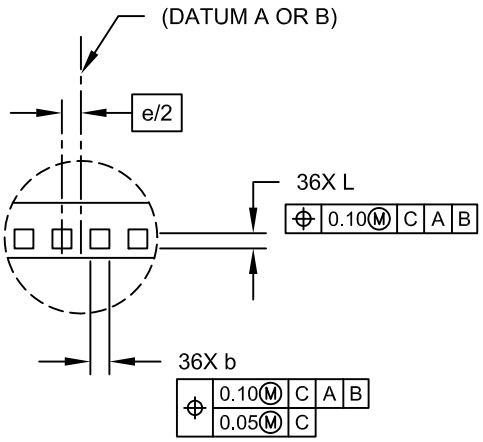
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



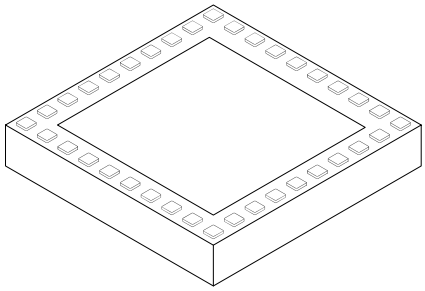

Microchip Technology Drawing C04-187C Sheet 1 of 2

## 36-Terminal Very Thin Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




**DETAIL A**



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension | Limits | MIN | NOM | MAX |
| Number of Pins | N | | 36 | |
| Number of Pins per Side | ND | | 10 | |
| Number of Pins per Side | NE | | 8 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.025 | - | 0.075 |
| Overall Width | E | | 5.00 BSC | |
| Exposed Pad Width | E2 | 3.60 | 3.75 | 3.90 |
| Overall Length | D | | 5.00 BSC | |
| Exposed Pad Length | D2 | 3.60 | 3.75 | 3.90 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.20 | 0.25 | 0.30 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-187C Sheet 2 of 2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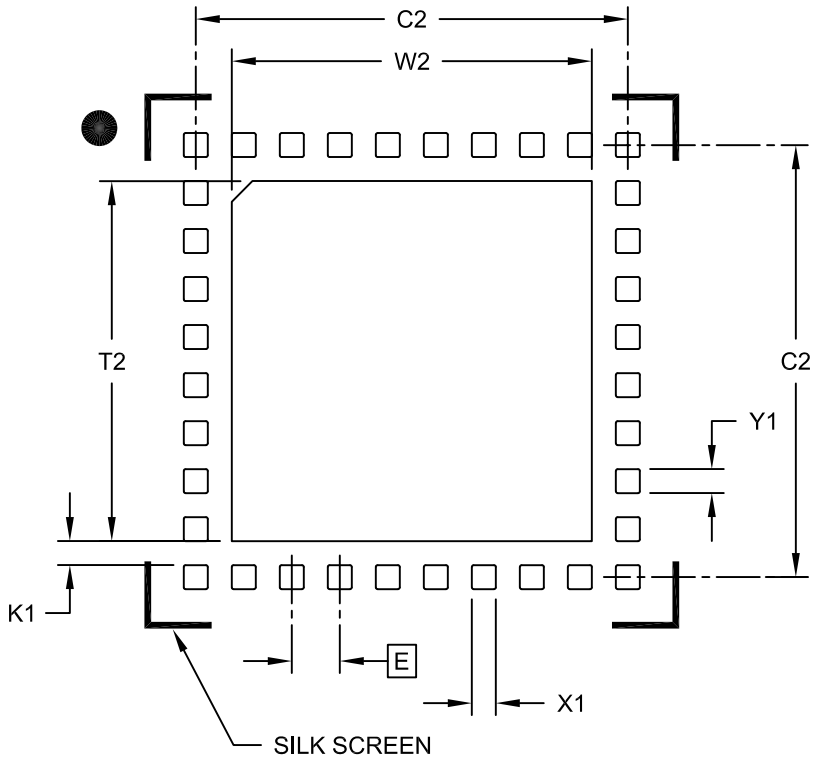
## 36-Lead Thermal Leadless Array Package (TL) – 5x5x0.9 mm Body with Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 3.75 |
| Optional Center Pad Length | T2 | | | 3.75 |
| Contact Pad Spacing | C1 | | 4.50 | |
| Contact Pad Spacing | C2 | | 4.50 | |
| Contact Pad Width (X36) | X1 | | | 0.25 |
| Contact Pad Length (X36) | Y1 | | | 0.25 |
| Distance Between Pads | K1 | 0.15 | 0.25 | |

Notes:

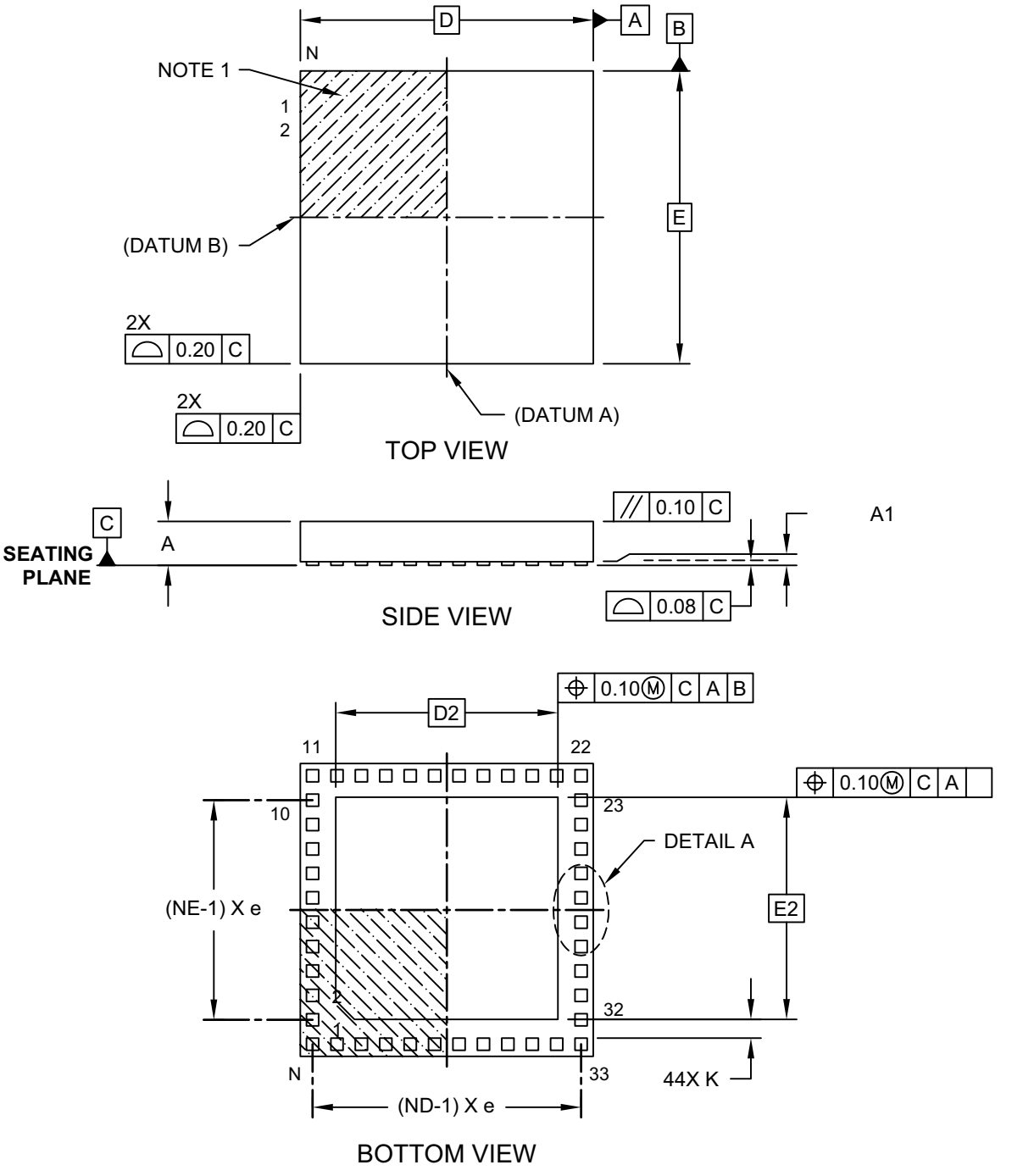
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2187B

## 44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-157D Sheet 1 of 2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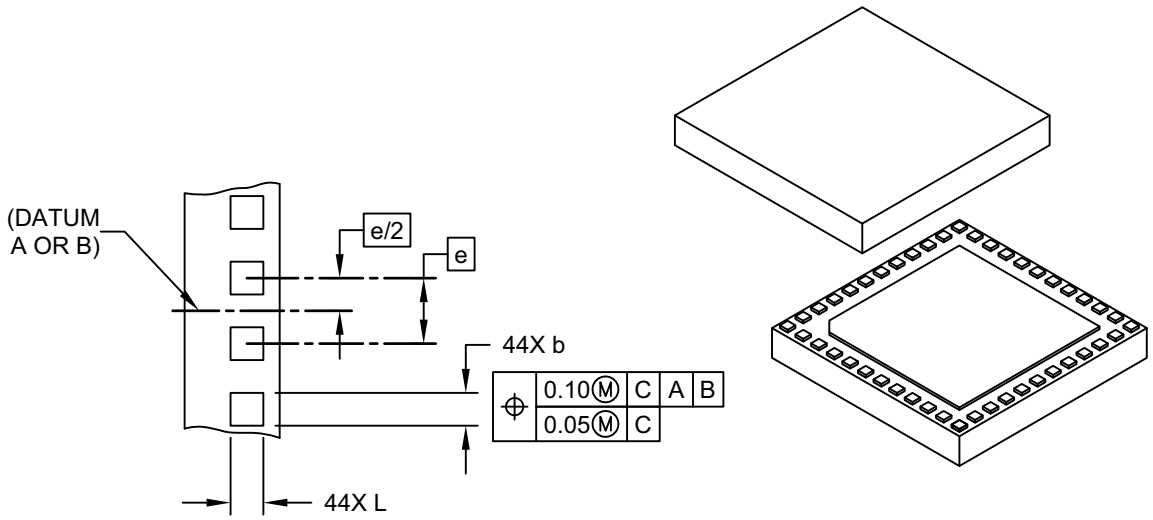
## 44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




DETAIL A

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension | Limits | MIN | NOM | MAX |
| Number of Terminals | N | | 44 | |
| Number of Terminals per Side | ND | | 12 | |
| Number of Terminals per Side | NE | | 10 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.025 | - | 0.075 |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 4.40 | 4.55 | 4.70 |
| Overall Length | D | | 6.00 BSC | |
| Exposed Pad Length | D2 | 4.40 | 4.55 | 4.70 |
| Terminal Width | b | 0.20 | 0.25 | 0.30 |
| Terminal Length | L | 0.20 | 0.25 | 0.30 |
| Terminal-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

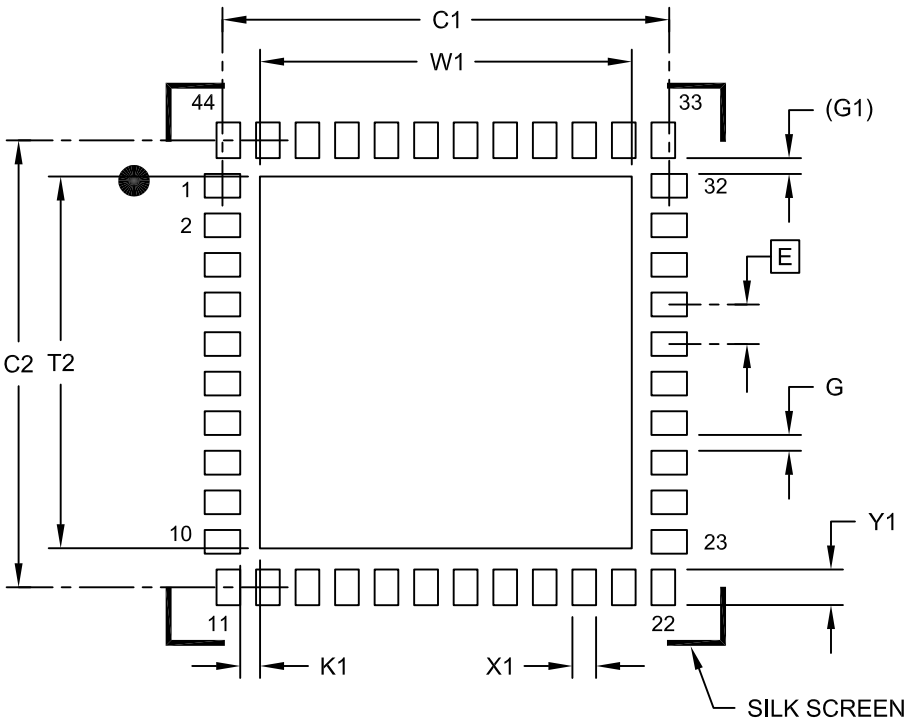
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-157D Sheet 2 of 2

## 44-Terminal Very Thin Leadless Array Package (TL) – 6x6x0.9 mm Body With Exposed Pad [VTLA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Terminal Pitch | E | | 0.50 BSC | |
| Optional Center Pad Width | W2 | | | 4.70 |
| Optional Center Pad Length | T2 | | | 4.70 |
| Terminal Pad Spacing | C1 | | 5.65 | |
| Terminal Pad Spacing | C2 | | 5.65 | |
| Terminal Pad Width (X44) | X1 | | | 0.30 |
| Terminal Pad Length (X44) | Y1 | | | 0.45 |
| Distance Between Pads | (G1) | | 0.20 REF. | |
| Distance Between Pads | G | 0.20 | | |
| Distance Between Pads | K1 | 0.267 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2157A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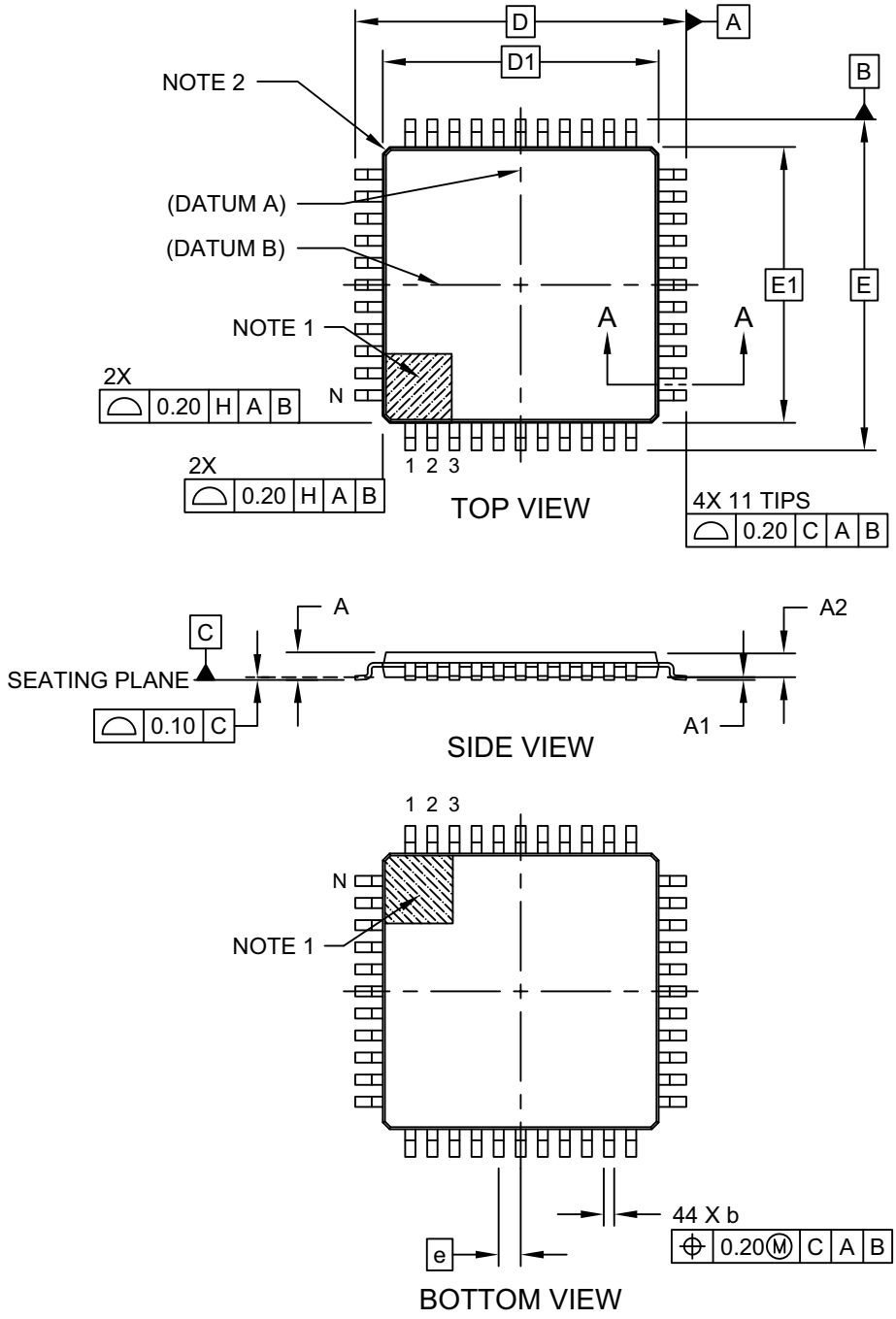
### 44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

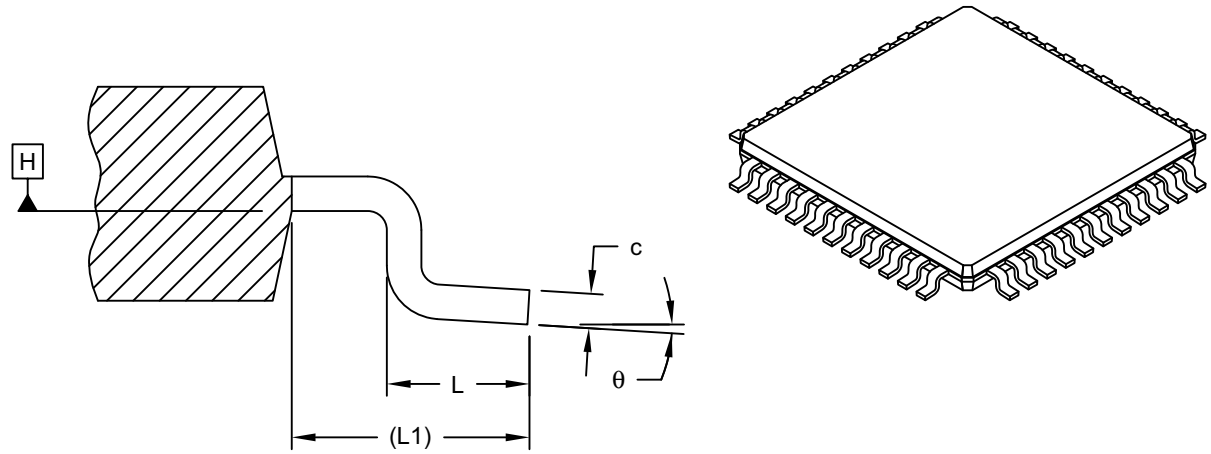
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-076C Sheet 1 of 2

## 44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




SECTION A-A

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 44 | |
| Lead Pitch | e | | 0.80 BSC | |
| Overall Height | A | - | - | 1.20 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Overall Width | E | | 12.00 BSC | |
| Molded Package Width | E1 | | 10.00 BSC | |
| Overall Length | D | | 12.00 BSC | |
| Molded Package Length | D1 | | 10.00 BSC | |
| Lead Width | b | 0.30 | 0.37 | 0.45 |
| Lead Thickness | c | 0.09 | - | 0.20 |
| Lead Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | θ | 0° | 3.5° | 7° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Exact shape of each corner is optional.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076C Sheet 2 of 2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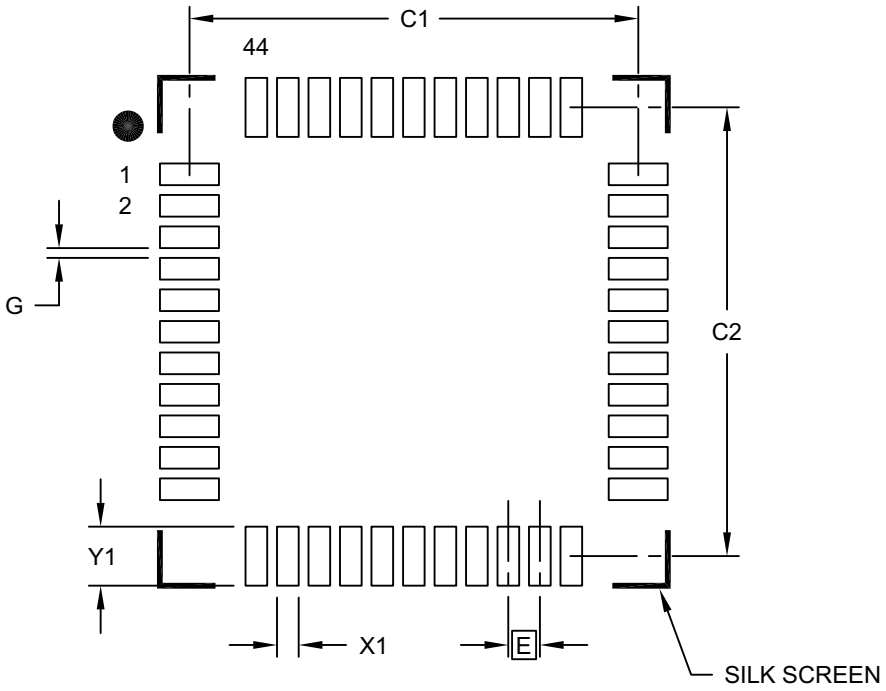
## 44-Lead Plastic Thin Quad Flatpack (PT) - 10X10X1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.80 BSC | |
| Contact Pad Spacing | C1 | | 11.40 | |
| Contact Pad Spacing | C2 | | 11.40 | |
| Contact Pad Width (X44) | X1 | | | 0.55 |
| Contact Pad Length (X44) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.25 | | |

Notes:

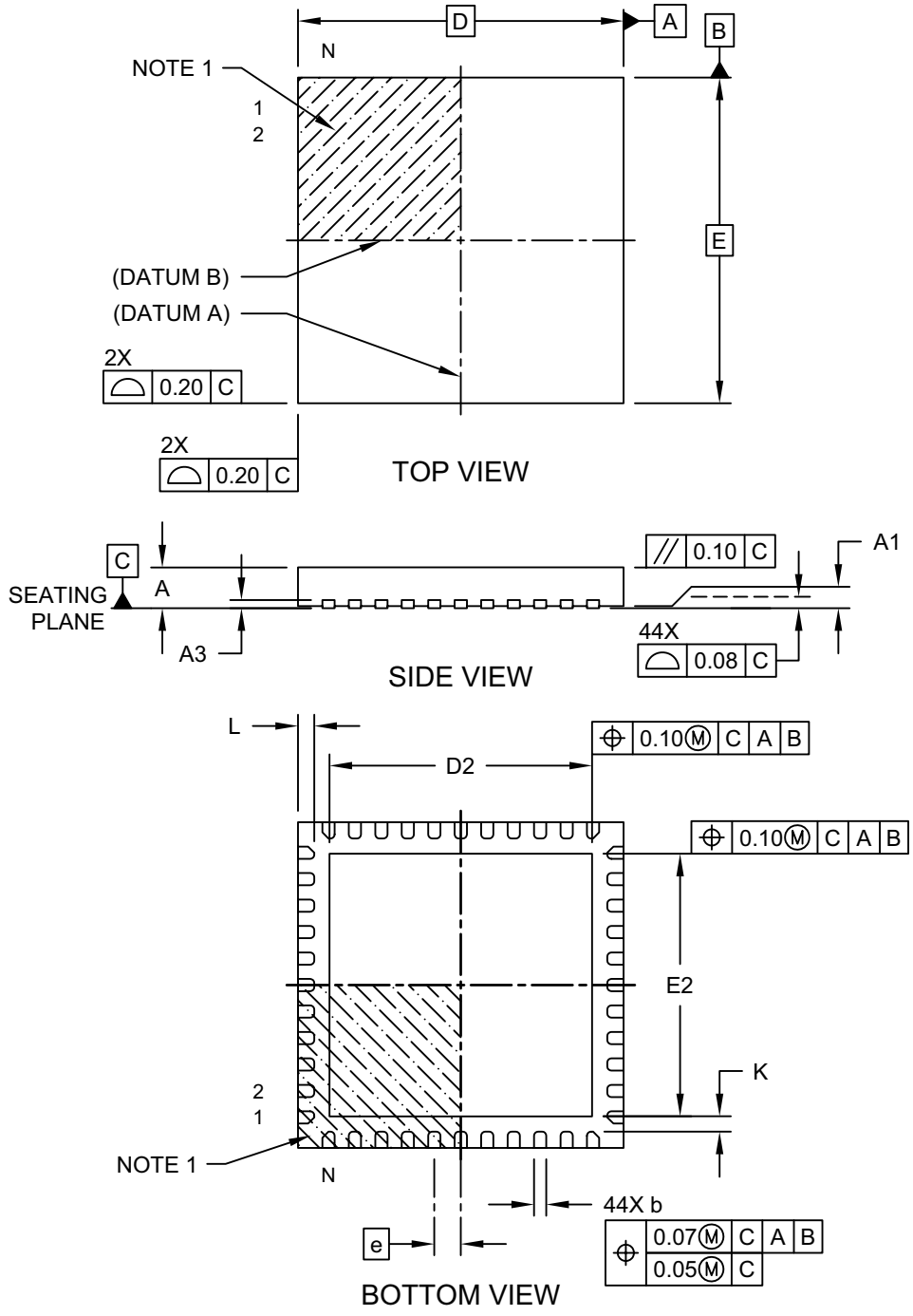
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076B

### 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-103D Sheet 1 of 2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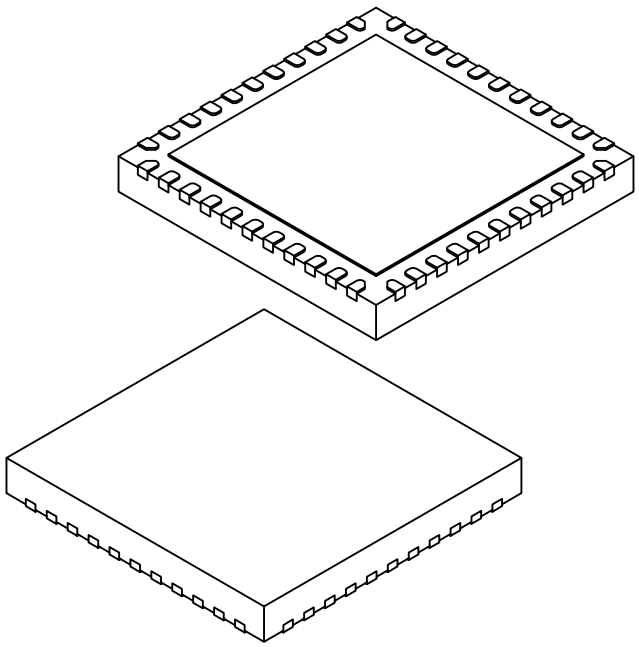
## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 44 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Terminal Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 8.00 BSC | |
| Exposed Pad Width | E2 | 6.25 | 6.45 | 6.60 |
| Overall Length | D | | 8.00 BSC | |
| Exposed Pad Length | D2 | 6.25 | 6.45 | 6.60 |
| Terminal Width | b | 0.20 | 0.30 | 0.35 |
| Terminal Length | L | 0.30 | 0.40 | 0.50 |
| Terminal-to-Exposed-Pad | K | 0.20 | - | - |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

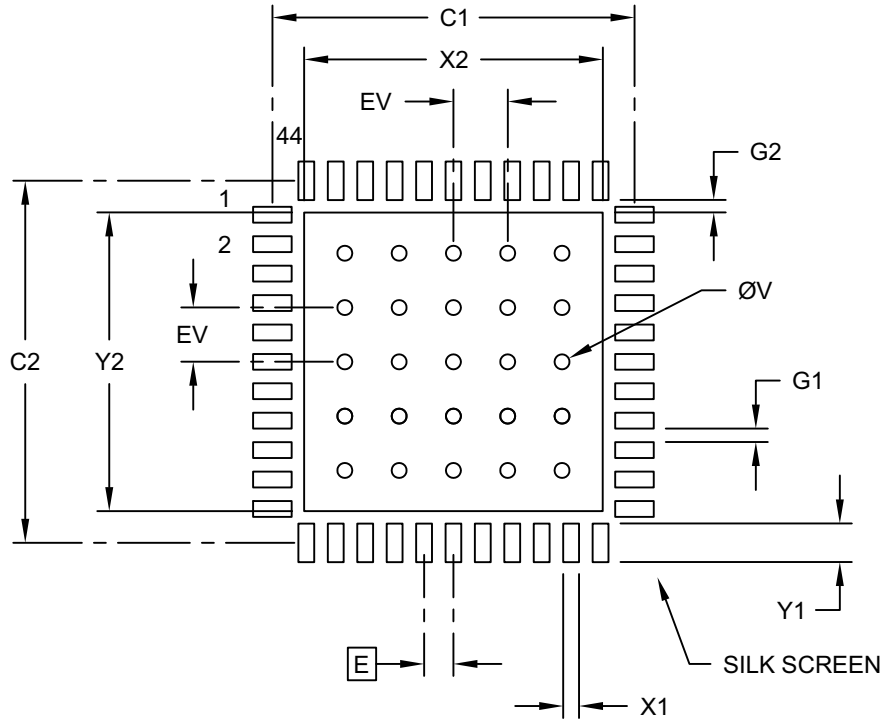
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103D Sheet 2 of 2

## 44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.65 BSC | |
| Optional Center Pad Width | X2 | | | 6.60 |
| Optional Center Pad Length | Y2 | | | 6.60 |
| Contact Pad Spacing | C1 | | 8.00 | |
| Contact Pad Spacing | C2 | | 8.00 | |
| Contact Pad Width (X44) | X1 | | | 0.35 |
| Contact Pad Length (X44) | Y1 | | | 0.85 |
| Contact Pad to Contact Pad (X40) | G1 | 0.30 | | |
| Contact Pad to Center Pad (X44) | G2 | 0.28 | | |
| Thermal Via Diameter | V | | 0.33 | |
| Thermal Via Pitch | EV | | 1.20 | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-2103C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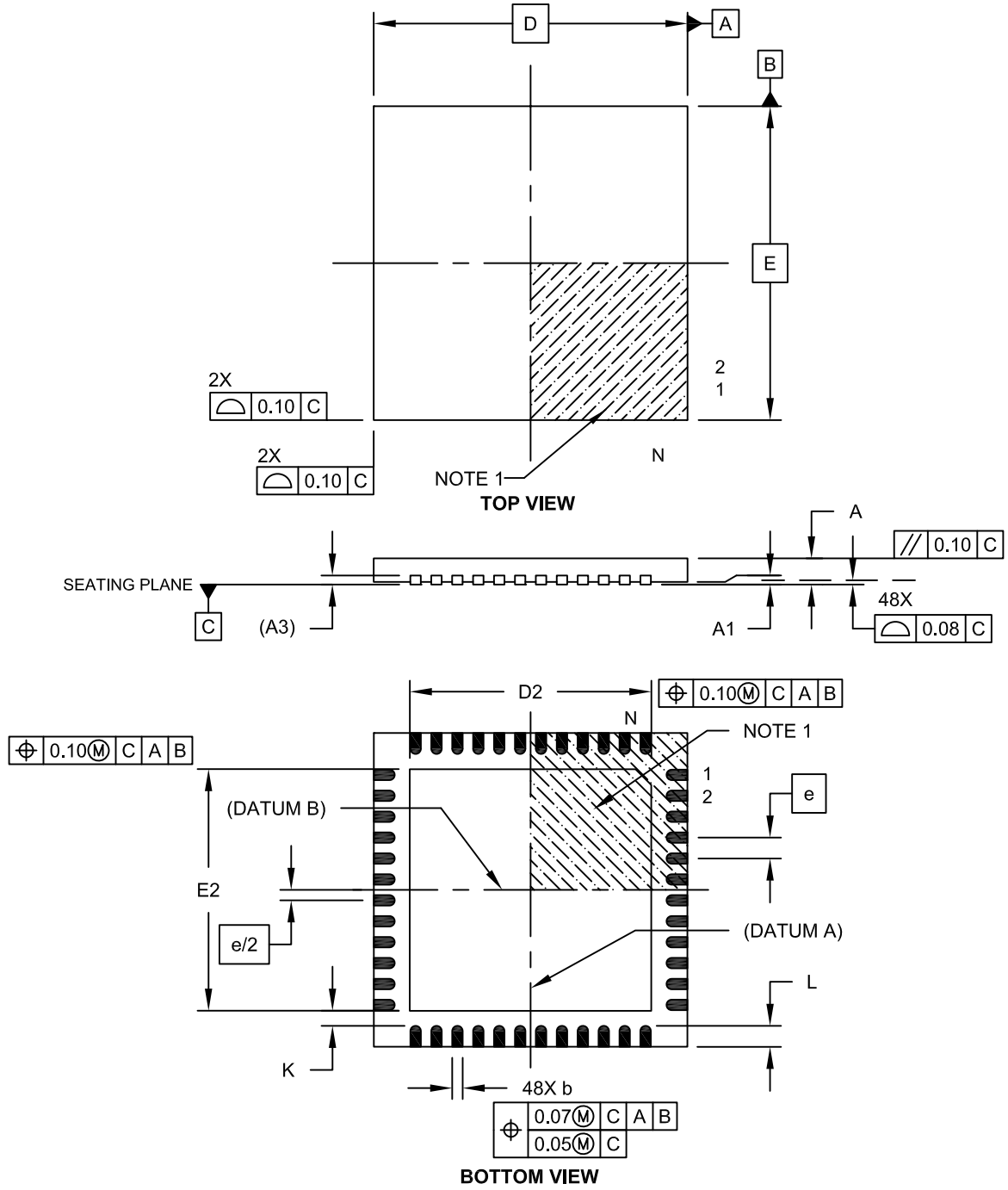
**48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]**

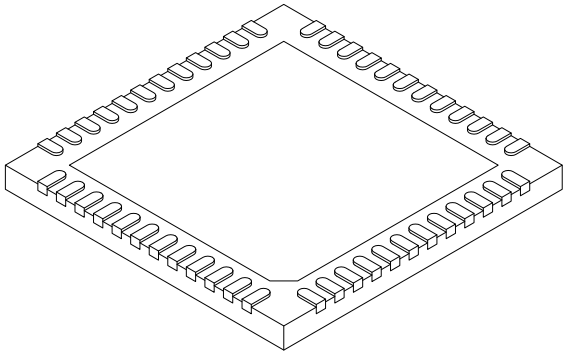
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-153A Sheet 1 of 2

## 48-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 6x6x0.5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 48 | |
| Pitch | e | | 0.40 BSC | |
| Overall Height | A | 0.45 | 0.50 | 0.55 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.127 REF | |
| Overall Width | E | | 6.00 BSC | |
| Exposed Pad Width | E2 | 4.45 | 4.60 | 4.75 |
| Overall Length | D | | 6.00 BSC | |
| Exposed Pad Length | D2 | 4.45 | 4.60 | 4.75 |
| Contact Width | b | 0.15 | 0.20 | 0.25 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-153A Sheet 2 of 2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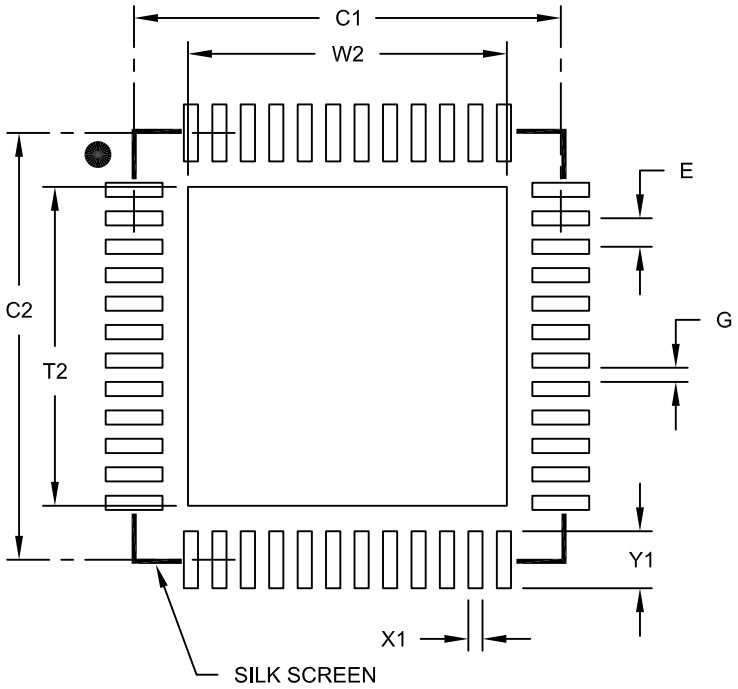
48-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 6x6 mm Body [UQFN]
With 0.40 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | | 0.40 BSC | |
| Optional Center Pad Width | W2 | | | 4.45 |
| Optional Center Pad Length | T2 | | | 4.45 |
| Contact Pad Spacing | C1 | | 6.00 | |
| Contact Pad Spacing | C2 | | 6.00 | |
| Contact Pad Width (X28) | X1 | | | 0.20 |
| Contact Pad Length (X28) | Y1 | | | 0.80 |
| Distance Between Pads | G | 0.20 | | |

Notes:

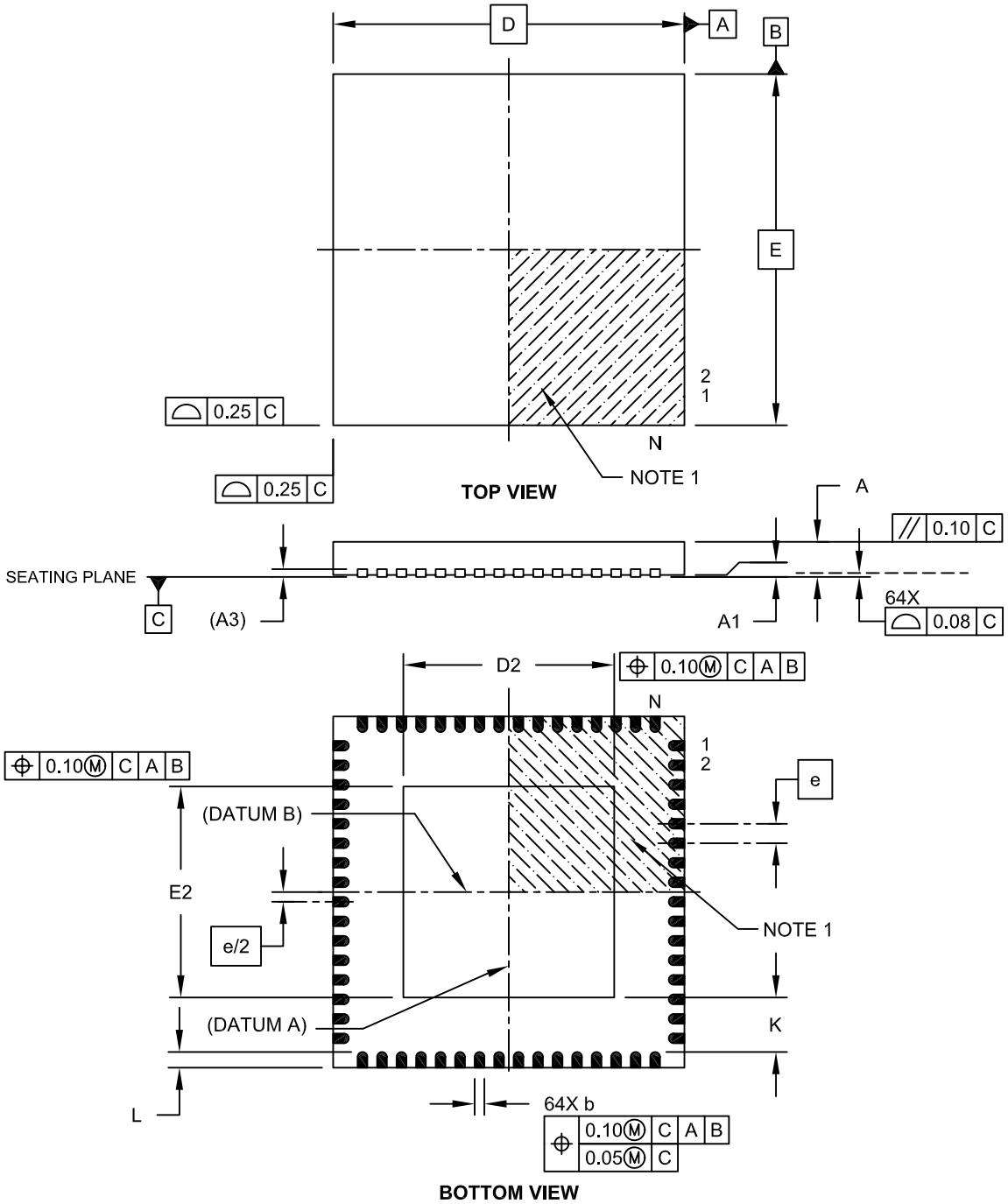
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2153A

## 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




Microchip Technology Drawing C04-154A Sheet 1 of 2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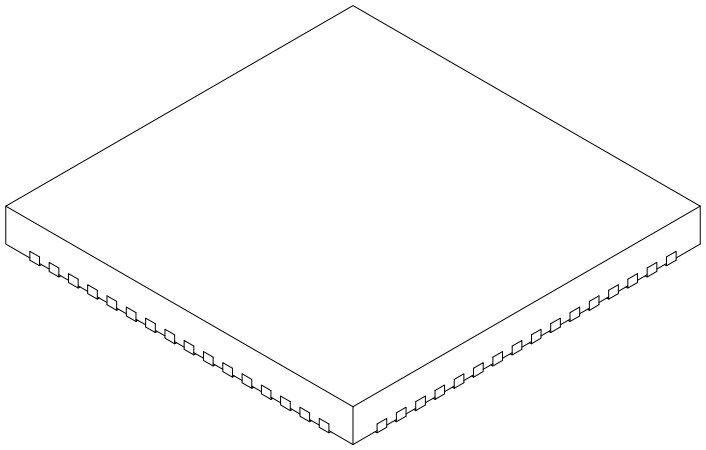
## 64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body with 5.40 x 5.40 Exposed Pad [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 64 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.80 | 0.90 | 1.00 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | | 0.20 REF | |
| Overall Width | E | | 9.00 BSC | |
| Exposed Pad Width | E2 | 5.30 | 5.40 | 5.50 |
| Overall Length | D | | 9.00 BSC | |
| Exposed Pad Length | D2 | 5.30 | 5.40 | 5.50 |
| Contact Width | b | 0.20 | 0.25 | 0.30 |
| Contact Length | L | 0.30 | 0.40 | 0.50 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

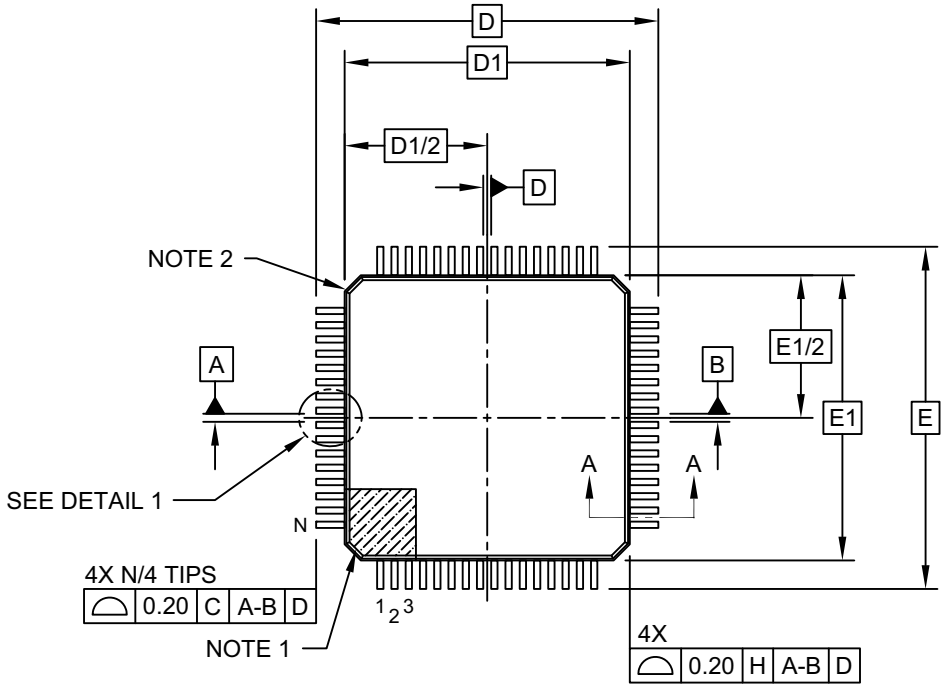
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

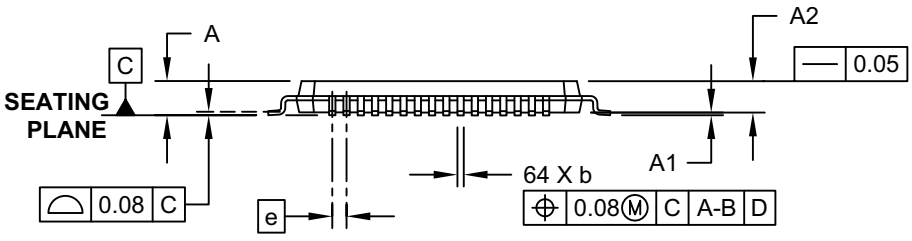
Microchip Technology Drawing C04-154A Sheet 2 of 2

## 64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




TOP VIEW




SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2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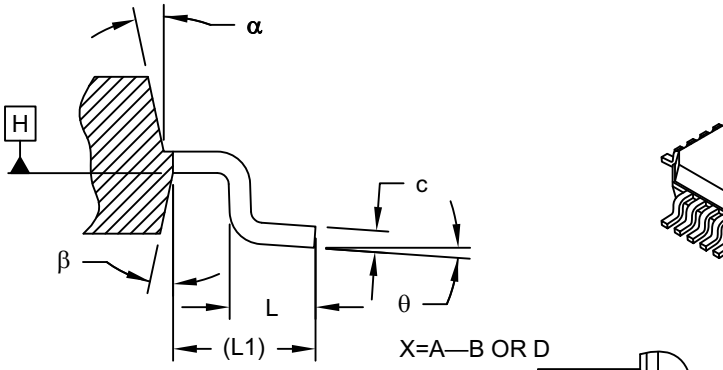
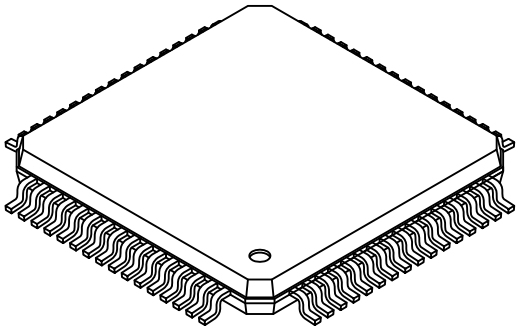
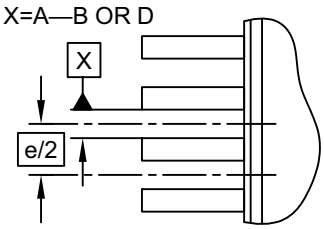
## 64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




SECTION A-A






DETAIL 1

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 64 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | - | - | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | ϕ | 0° | 3.5° | 7° |
| Overall Width | E | | 12.00 BSC | |
| Overall Length | D | | 12.00 BSC | |
| Molded Package Width | E1 | | 10.00 BSC | |
| Molded Package Length | D1 | | 10.00 BSC | |
| Lead Thickness | c | 0.09 | - | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

Notes:

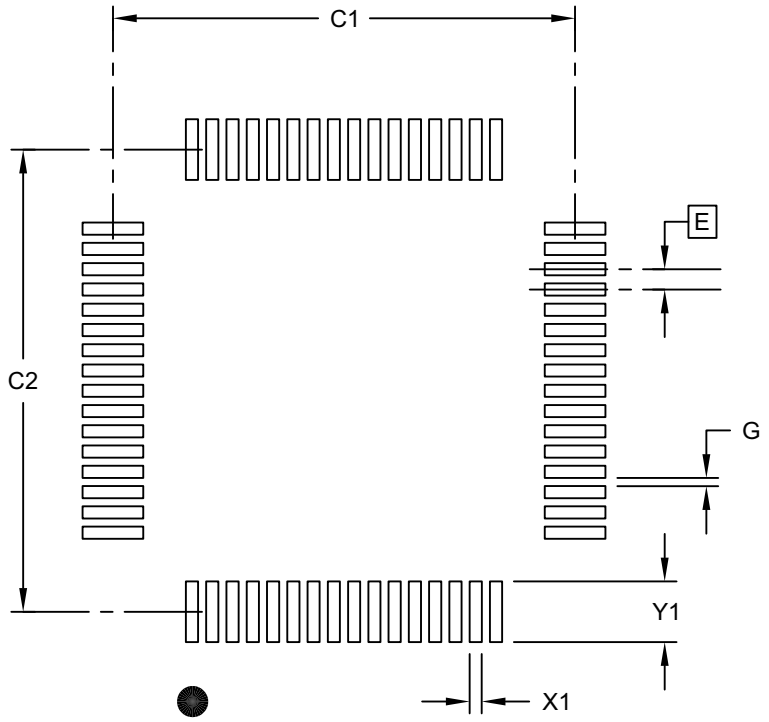
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2

## 64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E | 0.50 BSC | | |
| Contact Pad Spacing | C1 | | 11.40 | |
| Contact Pad Spacing | C2 | | 11.40 | |
| Contact Pad Width (X28) | X1 | | | 0.30 |
| Contact Pad Length (X28) | Y1 | | | 1.50 |
| Distance Between Pads | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2085B Sheet 1 of 1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# APPENDIX A: REVISION HISTORY

## Revision A (April 2011)

This is the initial released version of the document.

## Revision B (July 2011)

This revision includes minor typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-1.

**TABLE A-1: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"High-Performance, 16-bit Digital Signal Controllers and Microcontrollers"** | Changed all pin diagrams references of VLAP to TLA. |
| **Section 4.0 "Memory Organization"** | Updated the All Resets values for CLKDIV and PLLFBD in the System Control Register Map (see Table 4-35). |
| **Section 5.0 "Flash Program Memory"** | Updated "one word" to "two words" in the first paragraph of **Section 5.2 "RTSP Operation"**. |
| **Section 9.0 "Oscillator Configuration"** | Updated the PLL Block Diagram (see Figure 9-2).<br>Updated the Oscillator Mode, Fast RC Oscillator (FRC) with divide-by-N and PLL (FRCPLL), by changing (FRCDIVN + PLL) to (FRCPLL).<br>Changed (FRCDIVN + PLL) to (FRCPLL) for COSC[2:0] = 001 and NOSC[2:0] = 001 in the Oscillator Control Register (see Register 9-1).<br>Changed the POR value from 0 to 1 for the DOZE[1:0] bits, from 1 to 0 for the FRCDIV[0] bit, and from 0 to 1 for the PLLPOST[0] bit; Updated the default definitions for the DOZE[2:0] and FRCDIV[2:0] bits and updated all bit definitions for the PLLPOST[1:0] bits in the Clock Divisor Register (see Register 9-2).<br>Changed the POR value from 0 to 1 for the PLLDIV[5:4] bits and updated the default definitions for all PLLDIV[8:0] bits in the PLL Feedback Division Register (see Register 9-2). |
| **Section 22.0 "Charge Time Measurement Unit (CTMU)"** | Updated the bit definitions for the IRNG[1:0] bits in the CTMU Current Control Register (see Register 22-3). |
| **Section 25.0 "Op amp/ Comparator Module"** | Updated the voltage reference block diagrams (see Figure 25-1 and Figure 25-2). |

**TABLE A-1: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 30.0 "Electrical Characteristics"** | Removed Voltage on VCAP with respect to Vss and added Note 5 in Absolute Maximum Ratings(1).<br><br>Removed Parameter DC18 (VCORE) and Note 3 from the DC Temperature and Voltage Specifications (see Table 30-4).<br><br>Updated Note 1 in the DC Characteristics: Operating Current (IDD) (see Table 30-6).<br><br>Updated Note 1 in the DC Characteristics: Idle Current (IIDLE) (see Table 30-7).<br><br>Changed the Typical values for Parameters DC60a-DC60d and updated Note 1 in the DC Characteristics: Power-down Current (IPD) (see Table 30-8).<br><br>Updated Note 1 in the DC Characteristics: Doze Current (IDOZE) (see Table 30-9).<br><br>Updated Note 2 in the Electrical Characteristics: BOR (see Table 30-12).<br><br>Updated Parameters CM20 and CM31, and added Parameters CM44 and CM45 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).<br><br>Added the Op amp/Comparator Reference Voltage Settling Time Specifications (see Table 30-15).<br><br>Added Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).<br><br>Updated Internal FRC Accuracy Parameter F20a (see Table 30-21).<br><br>Updated the Typical value and Units for Parameter CTMUI1, and added Parameters CTMUI4, CTMUFV1, and CTMUFV2 to the CTMU Current Source Specifications (see Table 30-55). |
| **Section 31.0 "Packaging Information"** | Updated packages by replacing references of VLAP with TLA. |
| **"Product Identification System"** | Changed VLAP to TLA. |


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## Revision C (December 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

In addition, where applicable, new sections were added to each peripheral chapter that provide information and links to related resources, as well as helpful tips. For examples, see **Section 20.1 "UART Helpful Tips"** and **Section 3.6 "CPU Resources"**.

All occurrences of TLA were updated to VTLA throughout the document, with the exception of the pin diagrams (updated diagrams were not available at time of publication).

A new chapter, **Section 31.0 "DC and AC Device Characteristics Graphs"**, was added.

All other major changes are referenced by their respective section in Table A-2.

**TABLE A-2: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"16-bit Microcontrollers and Digital Signal Controllers (up to 256-Kbyte Flash and 32-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog"** | The content on the first page of this section was extensively reworked to provide the reader with the key features and functionality of this device family in an "at-a-glance" format. |
| **Section 1.0 "Device Overview"** | Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X Block Diagram (see Figure 1-1), which now contains a CPU block and a reference to the CPU diagram.<br>Updated the description and Note references in the Pinout I/O Descriptions for these pins: C1IN2-, C2IN2-, C3IN2-, OA1OUT, OA2OUT, and OA3OUT (see Table 1-1). |
| **Section 2.0 "Guidelines for Getting Started with 16-bit Digital Signal Controllers and Microcontrollers"** | Updated the Recommended Minimum Connection diagram (see Figure 2-1). |
| **Section 3.0 "CPU"** | Updated the dsPIC33EPXXXGP50X, dsPIC33EPXXXMC20X/50X, and PIC24EPXXXGP/MC20X CPU Block Diagram (see Figure 3-1).<br>Updated the Status register definition in the Programmer's Model (see Figure 3-2). |
| **Section 4.0 "Memory Organization"** | Updated the Data Memory Maps (see Figure 4-6 and Figure 4-11).<br>Removed the DCB[1:0] bits from the OC1CON2, OC2CON2, OC3CON2, and OC4CON2 registers in the Output Compare 1 Through Output Compare 4 Register Map (see Table 4-10).<br>Added the TRIG1 and TRGCON1 registers to the PWM Generator 1 Register Map (see Table 4-13).<br>Added the TRIG2 and TRGCON2 registers to the PWM Generator 2 Register Map (see Table 4-14).<br>Added the TRIG3 and TRGCON3 registers to the PWM Generator 3 Register Map (see Table 4-15).<br>Updated the second note in **Section 4.7.1 "Bit-Reversed Addressing Implementation"**. |
| **Section 8.0 "Direct Memory Access (DMA)"** | Updated the DMA Controller diagram (see Figure 8-1). |
| **Section 14.0 "Input Capture"** | Updated the bit values for the ICx clock source of the ICTSEL[12:10] bits in the ICxCON1 register (see Register 14-1). |
| **Section 15.0 "Output Compare"** | Updated the bit values for the OCx clock source of the OCTSEL[2:0] bits in the OCxCON1 register (see Register 15-1).<br>Removed the DCB[1:0] bits from the Output Compare x Control Register 2 (see Register 15-2). |

**TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"** | Updated the High-Speed PWM Module Register Interconnection Diagram (see Figure 16-2).<br>Added the TRGCONx and TRIGx registers (see Register 16-12 and Register 16-14, respectively). |
| **Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"** | Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1). |
| **Section 22.0 "Charge Time Measurement Unit (CTMU)"** | Updated the IRNG[1:0] bit value definitions and added Note 2 in the CTMU Current Control Register (see Register 22-3). |
| **Section 25.0 "Op amp/ Comparator Module"** | Updated the Op amp/Comparator I/O Operating Modes Diagram (see Figure 25-1).<br>Updated the User-programmable Blanking Function Block Diagram (see Figure 25-3).<br>Updated the Digital Filter Interconnect Block Diagram (see Figure 25-4).<br>Added **Section 25.1 "Op amp Application Considerations"**.<br>Added Note 2 to the Comparator Control Register (see Register 25-2).<br>Updated the bit definitions in the Comparator Mask Gating Control Register (see Register 25-5). |
| **Section 27.0 "Special Features"** | Updated the FICD Configuration Register, updated Note 1, and added Note 3 in the Configuration Byte Register Map (see Table 27-1).<br>Added **Section 27.2 "User ID Words"**. |
| **Section 30.0 "Electrical Characteristics"** | Updated the following Absolute Maximum Ratings:<br>• Maximum current out of $V_{SS}$ pin<br>• Maximum current into $V_{DD}$ pin<br>Added Note 1 to the Operating MIPS vs. Voltage (see Table 30-1).<br>Updated all Idle Current ($I_{IDLE}$) Typical and Maximum DC Characteristics values (see Table 30-7).<br>Updated all Doze Current ($I_{DOZE}$) Typical and Maximum DC Characteristics values (see Table 30-9).<br>Added Note 2, removed Parameter CM24, updated the Typical values Parameters CM10, CM20, CM21, CM32, CM41, CM44, and CM45, and updated the Minimum values for CM40 and CM41, and the Maximum value for CM40 in the AC/DC Characteristics: Op amp/Comparator (see Table 30-14).<br>Updated Note 2 and the Typical value for Parameter VR310 in the Op amp/ Comparator Reference Voltage Settling Time Specifications (see Table 30-15).<br>Added Note 1, removed Parameter VRD312, and added Parameter VRD314 to the Op amp/Comparator Voltage Reference DC Specifications (see Table 30-16).<br>Updated the Minimum, Typical, and Maximum values for Internal LPRC Accuracy (see Table 30-22).<br>Updated the Minimum, Typical, and Maximum values for Parameter SY37 in the Reset, Watchdog Timer, Oscillator Start-up Timer, Power-up Timer Timing Requirements (see Table 30-24).<br>The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-35) |


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**TABLE A-2: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 30.0 "Electrical Characteristics" (Continued)** | These SPI2 Timing Requirements were updated:<br>• Maximum value for Parameter SP10 and the minimum clock period value for SCKx in Note 3 (see Table 30-36, Table 30-37, and Table 30-38)<br>• Maximum value for Parameter SP70 and the minimum clock period value for SCKx in Note 3 (see Table 30-40 and Table 30-42)<br>• The Maximum Data Rate values were updated for the SPI2 Maximum Data/Clock Rate Summary (see Table 30-43)<br><br>These SPI1 Timing Requirements were updated:<br>• Maximum value for Parameters SP10 and the minimum clock period value for SCKx in Note 3 (see Table 30-44, Table 30-45, and Table 30-46)<br>• Maximum value for Parameters SP70 and the minimum clock period value for SCKx in Note 3 (see Table 30-47 through Table 30-50)<br>• Minimum value for Parameters SP40 and SP41 see Table 30-44 through Table 30-50)<br>Updated all Typical values for the CTMU Current Source Specifications (see Table 30-55).<br>Updated Note1, the Maximum value for Parameter AD06, the Minimum value for AD07, and the Typical values for AD09 in the ADC Module Specifications (see Table 30-56).<br>Added Note 1 to the ADC Module Specifications (12-bit Mode) (see Table 30-57).<br>Added Note 1 to the ADC Module Specifications (10-bit Mode) (see Table 30-58).<br>Updated the Minimum and Maximum values for Parameter AD21b in the 10-bit Mode ADC Module Specifications (see Table 30-58).<br>Updated Note 2 in the ADC Conversion (12-bit Mode) Timing Requirements (see Table 30-59).<br>Updated Note 1 in the ADC Conversion (10-bit Mode) Timing Requirements (see Table 30-60). |

## Revision D (December 2011)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

**TABLE A-3: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog"** | Removed the Analog Comparators column and updated the Op amps/Comparators column in Table 1 and Table 2. |
| **Section 21.0 "Enhanced CAN (ECAN™) Module (dsPIC33EPXXXGP/MC50X Devices Only)"** | Updated the CANCKS bit value definitions in CiCTRL1: ECAN Control Register 1 (see Register 21-1). |
| **Section 30.0 "Electrical Characteristics"** | Updated the $V_{BOR}$ specifications and/or its related note in the following electrical characteristics tables:<br>• Table 30-1<br>• Table 30-4<br>• Table 30-12<br>• Table 30-14<br>• Table 30-15<br>• Table 30-16<br>• Table 30-56<br>• Table 30-57<br>• Table 30-58<br>• Table 30-59<br>• Table 30-60 |


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## Revision E (April 2012)

This revision includes typographical and formatting changes throughout the data sheet text.

All other major changes are referenced by their respective section in Table A-3.

**TABLE A-4: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **"16-bit Microcontrollers and Digital Signal Controllers (up to 512-Kbyte Flash and 48-Kbyte SRAM) with High-Speed PWM, Op amps, and Advanced Analog"** | The following 512-Kbyte devices were added to the General Purpose Families table (see Table 1):<br>• PIC24EP512GP202<br>• PIC24EP512GP204<br>• PIC24EP512GP206<br>• dsPIC33EP512GP502<br>• dsPIC33EP512GP504<br>• dsPIC33EP512GP506<br>The following 512-Kbyte devices were added to the Motor Control Families table (see Table 2):<br>• PIC24EP512MC202<br>• PIC24EP512MC204<br>• PIC24EP512MC206<br>• dsPIC33EP512MC202<br>• dsPIC33EP512MC204<br>• dsPIC33EP512MC206<br>• dsPIC33EP512MC502<br>• dsPIC33EP512MC504<br>• dsPIC33EP512MC506<br>Certain Pin Diagrams were updated to include the new 512-Kbyte devices. |
| **Section 4.0 "Memory Organization"** | Added a Program Memory Map for the new 512-Kbyte devices (see Figure 4-4).<br>Added a Data Memory Map for the new dsPIC 512-Kbyte devices (see Figure 4-11).<br>Added a Data Memory Map for the new PIC24 512-Kbyte devices (see Figure 4-16). |
| **Section 7.0 "Interrupt Controller"** | Updated the VECNUM bits in the INTTREG register (see Register 7-7). |
| **Section 11.0 "I/O Ports"** | Added tip 6 to **Section 11.5 "I/O Helpful Tips"**. |
| **Section 27.0 "Special Features"** | The following modifications were made to the Configuration Byte Register Map (see Table 27-1):<br>• Added the column Device Memory Size (Kbytes)<br>• Removed Notes 1 through 4<br>• Added addresses for the new 512-Kbyte devices |
| **Section 30.0 "Electrical Characteristics"** | Updated the Minimum value for Parameter DC10 (see Table 30-4).<br>Added Power-Down Current (Ipd) parameters for the new 512-Kbyte devices (see Table 30-8).<br>Updated the Minimum value for Parameter CM34 (see Table 30-53).<br>Updated the Minimum and Maximum values and the Conditions for paramteer SY12 (see Table 30-22). |

### Revision F (November 2012)

Removed “Preliminary” from data sheet footer.

### Revision G (March 2013)

This revision includes the following global changes:

- changes “$\overline{\text{FLTx}}$” pin function to “FLTx” on all occurrences
- adds **Section 31.0 “High-Temperature Electrical Characteristics”** for high-temperature (+150°C) data

This revision also includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-5.

**TABLE A-5: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **Cover Section** | • Changes internal oscillator specification to 1.0%<br>• Changes I/O sink/source values to 12 mA or 6 mA<br>• Corrects 44-pin VTLA pin diagram (pin 32 now shows as 5V tolerant) |
| **Section 4.0 “Memory Organization”** | • Deletes references to Configuration Shadow registers<br>• Corrects the spelling of the JTAGIP and PTGWDTIP bits throughout<br>• Corrects the Reset value of all IOCON registers as C000h<br>• Adds footnote to Table 4-42 to indicate the absence of Comparator 3 in 28-pin devices |
| **Section 6.0 “Resets”** | • Removes references to cold and warm Resets, and clarifies the initial configuration of the device clock source on all Resets |
| **Section 7.0 “Interrupt Controller”** | • Corrects the definition of GIE as “Global Interrupt Enable” (not “General”) |
| **Section 9.0 “Oscillator Configuration”** | • Clarifies the behavior of the CF bit when cleared in software<br>• Removes POR behavior footnotes from all control registers<br>• Corrects the tuning range of the TUN[5:0] bits in Register 9-4 to an overall range ±1.5% |
| **Section 13.0 “Timer2/3 and Timer4/5”** | • Clarifies the presence of the ADC Trigger in 16-bit Timer3 and Timer5, as well as the 32-bit timers |
| **Section 15.0 “Output Compare”** | • Corrects the first trigger source for SYNCSEL[4:0] (OCxCON2[4:0]) as OCxRS match |
| **Section 16.0 “High-Speed PWM Module”** | • Clarifies the source of the PWM interrupts in Figure 16-1<br>• Corrects the Reset states of IOCONx[15:14] in Register 16-13 as ‘11’ |
| **Section 17.0 “Quadrature Encoder Interface (QEI) Module”** | • Clarifies the operation of the IMV[1:0] bits (QEICON[9:8]) with updated text and additional notes<br>• Corrects the first prescaler value for QFVDIV[2:0] (QEI1OC[13:11]), now 1:128 |
| **Section 23.0 “10-Bit/12-Bit Analog-to-Digital Converter (ADC)”** | • Adds note to Figure 23-1 that Op Amp 3 is not available in 28-pin devices<br>• Changes “sample clock” to “sample trigger” in AD1CON1 (Register 23-1)<br>• Clarifies footnotes on op amp usage in Registers 23-5 and 23-6 |
| **Section 25.0 “Op Amp/ Comparator Module”** | • Adds Note text to indicate that Comparator 3 is unavailable in 28-pin devices<br>• Splits Figure 25-1 into two figures for clearer presentation (Figure 25-1 for Op amp/ Comparators 1 through 3, Figure 25-2 for Comparator 4). Subsequent figures are renumbered accordingly.<br>• Corrects reference description in xxxxx (now ($AV_{DD}$ + $AV_{SS}$)/2)<br>• Changes CMSTAT[15] in Register 25-1 to “PSIDL” |
| **Section 27.0 “Special Features”** | • Corrects the addresses of all Configuration bytes for 512 Kbyte devices |


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**TABLE A-5: MAJOR SECTION UPDATES (CONTINUED)**

| Section Name | Update Description |
|---|---|
| **Section 30.0 "Electrical Characteristics"** | • Throughout: qualifies all footnotes relating to the operation of analog modules below VDDMIN (replaces "will have" with "may have")<br>• Throughout: changes all references of SPI timing parameter symbol "TscP" to "FscP"<br>• Table 30-1: changes VDD range to 3.0V to 3.6V<br>• Table 30-4: removes Parameter DC12 (RAM Retention Voltage)<br>• Table 30-7: updates Maximum values at 10 and 20 MIPS<br>• Table 30-8: adds Maximum IPD values, and removes all ΔIWDT entries<br>• Adds new Table 30-9 (Watchdog Timer Delta Current) with consolidated values removed from Table 30-8. All subsequent tables are renumbered accordingly.<br>• Table 30-10: adds footnote for all parameters for 1:2 Doze ratio<br>• Table 30-11:<br>- changes Minimum and Maximum values for D120 and D130<br>- adds Minimum and Maximum values for D131<br>- adds Minimum and Maximum values for D150 through D156, and removes Typical values<br>• Table 30-12:<br>- reformats table for readability<br>- changes IOL conditions for DO10<br>• Table 30-14: adds footnote to D135<br>• Table 30-17: changes Minimum and Maximum values for OS30<br>• Table 30-19:<br>- splits temperature range and adds new values for F20a<br>- reduces temperature range for F20b to extended temperatures only<br>• Table 30-20:<br>- splits temperature range and adds new values for F21a<br>- reduces temperature range for F20b to extended temperatures only<br>• Table 30-53:<br>- adds Maximum value to CM30<br>- adds footnote ("Parameter characterized...") to multiple parameters<br>• Table 30-55: adds Minimum and Maximum values for all CTMUI specifications, and removes Typical values<br>• Table 30-57: adds new footnote to AD09<br>• Table 30-58:<br>- removes all specifications for accuracy with external voltage references<br>- removes Typical values for AD23a and AD24a<br>- replaces Minimum and Maximum values for AD21a, AD22a, AD23a and AD24a with new values, split by Industrial and Extended temperatures<br>- removes Maximum value of AD30<br>- removes Minimum values from AD31a and AD32a<br>- adds or changes Typical values for AD30, AD31a, AD32a and AD33a<br>• Table 30-59:<br>- removes all specifications for accuracy with external voltage references<br>- removes Maximum value of AD30<br>- removes Typical values for AD23b and AD24b<br>- replaces Minimum and Maximum values for AD21b, AD22b, AD23b and AD24b with new values, split by Industrial and Extended temperatures<br>- removes Minimum and Maximum values from AD31b, AD32b, AD33b and AD34b<br>- adds or changes Typical values for AD30, AD31a, AD32a and AD33a<br>• Table 30-61: Adds footnote to AD51 |
| **Section 32.0 "DC and AC Device Characteristics Graphs"** | • Updates Figure 32-6 (Typical IDD @ 3.3V) with individual current vs. processor speed curves for the different program memory sizes |
| **Section 33.0 "Packaging Information"** | • Replaces drawing C04-149C (64-pin QFN, 7.15 x 7.15 exposed pad) with C04-154A (64-pin QFN, 5.4 x 5.4 exposed pad) |

## Revision H (August 2013)

This revision includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-6.

**TABLE A-6: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **Cover Section** | • Adds Peripheral Pin Select (PPS) to allow Digital Function Remapping and Change Notification Interrupts to Input/Output section<br>• Adds heading information to 64-Pin TQFP |
| **Section 4.0 "Memory Organization"** | • Corrects Reset values for ANSELE, TRISF, TRISC, ANSELC and TRISA<br>• Corrects address range from 0x2FFF to 0x7FFF<br>• Corrects DSRPAG and DSWPAG (now 3 hex digits)<br>• Changes Call Stack Frame from [15:1] to PC[15:0]<br>• Word length in Figure 4-20 is changed to 50 words for clarity |
| **Section 5.0 "Flash Program Memory"** | • Corrects descriptions of NVM registers |
| **Section 9.0 "Oscillator Configuration"** | • Removes resistor from Figure 9-1<br>• Adds Fast RC Oscillator with Divide-by-16 (FRCDIV16) row to Table 9-1<br>• Removes incorrect information from ROI bit in Register 9-2 |
| **Section 14.0 "Input Capture"** | • Changes 31 user-selectable Trigger/Sync interrupts to 19 user-selectable Trigger/Sync interrupts<br>• Corrects ICTSEL[12:10] bits (now ICTSEL[2:0]) |
| **Section 17.0 "Quadrature Encoder Interface (QEI) Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"** | • Corrects QCAPEN bit description |
| **Section 19.0 "Inter-Integrated Circuit ($I^2C$)"** | • Adds note to clarify that 100kbit/sec operation of $I^2C$ is not possible at high processor speeds |
| **Section 22.0 "Charge Time Measurement Unit (CTMU)"** | • Clarifies Figure 22-1 to accurately reflect peripheral behavior |
| **Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)"** | • Correct Figure 23-1 (changes CH123x to CH123Sx) |
| **Section 24.0 "Peripheral Trigger Generator (PTG) Module"** | • Adds footnote to Register 24-1 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled. |
| **Section 25.0 "Op Amp/ Comparator Module"** | • Adds note to Figure 25-3 (In order to operate with CVRSS=1, at least one of the comparator modules must be enabled)<br>• Adds footnote to Register 25-2 (COE is not available when OPMODE (CMxCON[10]) = 1) |
| **Section 27.0 "Special Features"** | • Corrects the bit description for FNOSC[2:0] |
| **Section 30.0 "Electrical Characteristics"** | • Corrects 512K part power-down currents based on test data<br>• Corrects WDT timing limits based on LPRC oscillator tolerance |
| **Section 31.0 "High-Temperature Electrical Characteristics"** | • Adds Table 31-5 (DC Characteristics: Idle Current ($I_{IDLE}$) |


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## Revision J (June 2020)

This revision includes minor typographical and formatting changes throughout the text.

Other major changes are referenced by their respective section in Table A-7.

**TABLE A-7: MAJOR SECTION UPDATES**

| Section Name | Update Description |
|---|---|
| **Cover Section** | • Removes "Planned" from the **"Qualification and Class B Support"** section.<br>• Adds UQFN package to Table 1 and Table 2.<br>• Adds two 36-pin UQFN pin diagrams.<br>• Changes the RD8 pin to non-5V tolerant.<br>• Adds the **"Referenced Sources"** section. |
| **Section 2.7 "Oscillator Value Conditions on Device Start-up"** | • Corrects the oscillator source frequency. |
| **Section 3.0 "CPU"** | • Changes to Note 1 here and every chapter throughout document. |
| **Section 4.0 "Memory Organization"** | • Changes to Figure 4-11 and Figure 4-16.<br>• Changes to Table 4-35. |
| **Section 5.0 "Flash Program Memory"** | • Changes to Register 5-1. |
| **Section 7.0 "Interrupt Controller"** | • Changes to Table 7-1. |
| **Section 9.0 "Oscillator Configuration"** | • Changes to Table 9-1. |
| **Section 10.0 "Power-Saving Features"** | • Replaces Example 10-1 and adds Example 10-2.<br>• Changes to **Section 10.2.1 "Sleep Mode"**. |
| **Section 11.0 "I/O Ports"** | • Changes to **Section 11.2 "Configuring Analog and Digital Port Pins"**. |
| **Section 13.0 "Timer2/3 and Timer4/5"** | • Changes to Register 13-1 and Register 13-2. |
| **Section 14.0 "Input Capture"** | • Changes to Register 14-2. |
| **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"** | • Changes to Note in **Section 16.0 "High-Speed PWM Module (dsPIC33EPXXXMC20X/50X and PIC24EPXXXMC20X Devices Only)"**.<br>• Changes to Register 16-7 and Register 16-13. |
| **Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)"** | • Changes to Register 23-8. |
| **Section 25.0 "Op Amp/ Comparator Module"** | • Changes to Figure 25-1.<br>• Changes to **Section 25.1 "Op Amp Application Considerations"**.<br>• Changes to Register 25-2 and Register 25-7. |
| **Section 27.0 "Special Features"** | • Changes to Table 27-2. |
| **Section 30.0 "Electrical Characteristics"** | • Changes to Table 30-3, Table 30-6, Table 30-11, Table 30-14 and Table 30-53. |
| **Section 31.0 "High-Temperature Electrical Characteristics"** | • Changes to Table 31-2.<br>• Adds Table 31-9, Table 31-10 and Table 31-13. |
| **Section 32.0 "DC and AC Device Characteristics Graphs"** | • Replaces Figure 32-10. |
| **Section 33.0 "Packaging Information"** | • Adds package marking diagram in **Section 33.1 "Package Marking Information"**.<br>• Adds packaging diagrams to **Section 33.2 "Package Details"**. |
| **"Product Identification System"** | • Adds M5 packaging description. |

**NOTES:**


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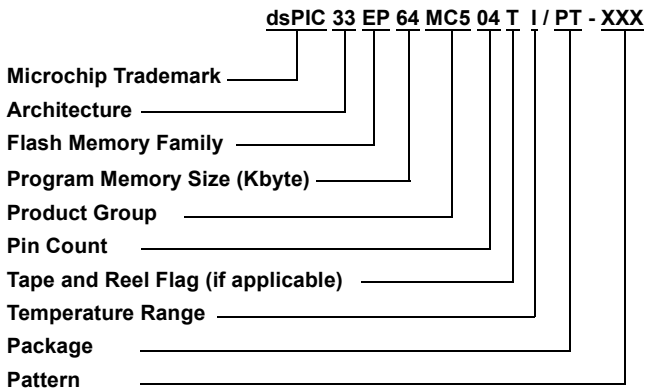


**Examples:**

dsPIC33EP64MC504-I/PT:
dsPIC33, Enhanced Performance,
64-Kbyte Program Memory,
Motor Control, 44-Pin,
Industrial Temperature,
TQFP package.

| | | | |
|---|---|---|---|
| **Architecture:** | 33 | = | 16-bit Digital Signal Controller |
| | 24 | = | 16-bit Microcontroller |
| **Flash Memory Family:** | EP | = | Enhanced Performance |
| **Product Group:** | GP | = | General Purpose family |
| | MC | = | Motor Control family |
| **Pin Count:** | 02 | = | 28-pin |
| | 03 | = | 36-pin |
| | 04 | = | 44-pin |
| | 06 | = | 64-pin |
| **Temperature Range:** | I | = | -40°C to +85°C (Industrial) |
| | E | = | -40°C to +125°C (Extended) |
| | H | = | -40°C to +150°C (High) |
| **Package:** | M5 | = | Ultra Thin Plastic Quad Flat, No Lead - (36-pin) 5x5 mm body (UQFN) |
| | ML | = | Plastic Quad, No Lead Package - (44-pin) 8x8 mm body (QFN) |
| | MM | = | Plastic Quad, No Lead Package - (28-pin) 6x6 mm body (QFN-S) |
| | MR | = | Plastic Quad, No Lead Package - (64-pin) 9x9 mm body (QFN) |
| | MV | = | Thin Quad, No Lead Package - (48-pin) 6x6 mm body (UQFN) |
| | PT | = | Plastic Thin Quad Flatpack - (44-pin) 10x10 mm body (TQFP) |
| | PT | = | Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) |
| | SO | = | Plastic Small Outline, Wide - (28-pin) 7.50 mm body (SOIC) |
| | SP | = | Skinny Plastic Dual In-Line - (28-pin) 300 mil body (SPDIP) |
| | SS | = | Plastic Shrink Small Outline - (28-pin) 5.30 mm body (SSOP) |
| | TL | = | Very Thin Leadless Array - (36-pin) 5x5 mm body (VTLA) |
| | TL | = | Very Thin Leadless Array - (44-pin) 6x6 mm body (VTLA) |

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