JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD

# SOT-23-3LK Plastic-Encapsulate Thyristors

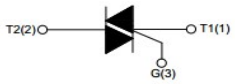
## CT401L 4Q TRIACs

### MAIN CHARACTERISTICS

| | | |
|---|---|---|
| $I_{T(RMS)}$ | | 1A |
| $V_{DRM}/V_{RRM}$ | CT401L-600T/S | 600V |
| | CT401L-800T/S | 800V |
| $V_{TM}$ | | 1.55V |

**SOT-23-3LK**

1.CATHODE
2.ANODE
3.GATE


### FEATURES

- NPNPN 5-layer Structure TRIACs
- Mesa Glass Passivated Technology
- Multi Layers Metal Electrodes
- High Junction Temperature
- Good Commutation Performance

### APPLICATIONS

- Heater Control
- Motor Speed Controller
- Mixer

### ABSOLUTE RATINGS ( $T_a$=25℃ unless otherwise noted )

| Symbol | Parameter | Test condition | | Value | | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$/ $V_{RRM}$ | Repetitive peak off-state voltage | $T_j$=25℃ | CT401L-600T/S | 600 | | V |
| | | | CT401L-800T/S | 800 | | V |
| $I_{T(RMS)}$ | RMS on-state current | SOT-23-3LK($T_C$≤60℃), Fig. 1,2 | | 1 | | A |
| $I_{TSM}$ | Non repetitive surge peak on-state current | Full sine wave, $T_j$(init)=25℃, tp=20ms; Fig. 3,5 | | 10 | | A |
| $I^2t$ | $I^2t$ value | tp=10ms | | 1.28 | | $A^2s$ |
| $dI_T/dt$ | Critical rate of rise of on-state current | $I_G$=2*$I_{GT}$, tr≤10ns, F=120Hz, $T_j$=125℃ | | Ⅰ-Ⅱ-Ⅲ | 50 | A/μs |
| | | | | Ⅳ | 10 | |
| $I_{GM}$ | Peak gate current | tp=20μs, $T_j$=125℃ | | 2 | | A |
| $P_{G(AV)}$ | Average gate power | $T_j$=125℃ | | 0.5 | | W |
| $T_{STG}$ | Storage temperature | | | -40~+150 | | ℃ |
| $T_j$ | Operating junction temperature | | | -40~+125 | | |

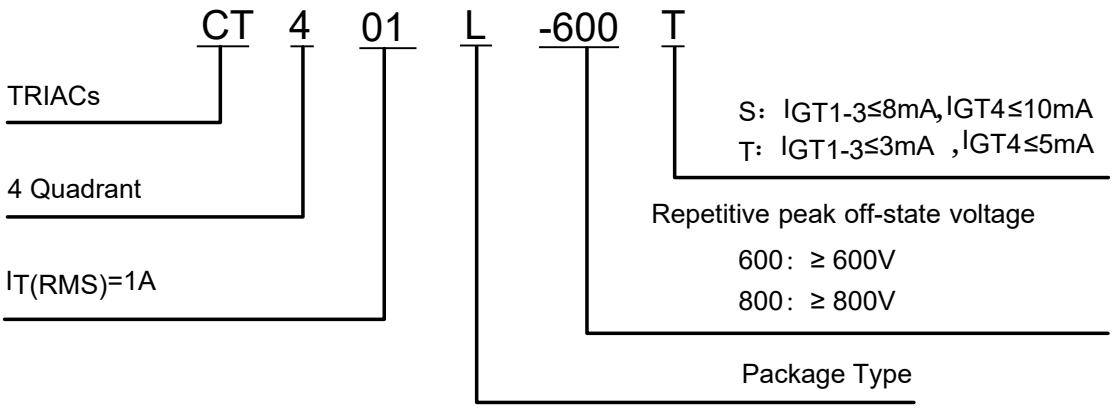
## ELECTRICAL CHARACTERISTICS ($T_a$=25℃ unless otherwise specified)

| Symbol | Parameter | Test condition | | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | T | S | |
| $I_{GT}$ | Gate trigger current | $V_D$=12V, $I_T$ =0.1A, $T_j$=25℃, Fig. 6 | Ⅰ - Ⅱ -Ⅲ | ≤3 | ≤8 | mA |
| | | | Ⅳ | ≤5 | ≤10 | |
| $V_{GT}$ | Gate trigger voltage | | Ⅰ - Ⅱ -Ⅲ - Ⅳ | ≤1.3 | | V |
| $V_{GD}$ | Non-triggering gate voltage | VD=VDRM, $T_j$=125℃ | | ≥0.2 | | V |
| $I_H$ | Holding current | $V_D$=12V, $I_{GT}$=0.1A, $T_j$=25℃, Fig. 6 | Ⅰ - Ⅱ -Ⅲ - Ⅳ | ≤5 | ≤5 | mA |
| $I_L$ | Latching current | | Ⅰ -Ⅲ- Ⅳ | ≤6 | ≤10 | mA |
| | | | Ⅱ | ≤10 | ≤15 | mA |
| $dV_D/dt$ | Critical rate of rise of off-state | $V_D$=67%$V_{DRM}$, Gate Open $T_j$=125℃ | | ≥20 | ≥50 | V/μs |
| $V_{TM}$ | On-state Voltage | $I_{TM}$=1.5A ,tp=380μs , Fig. 4 | | ≤1.55 | | V |
| $I_{DRM}$ / $I_{RRM}$ | Repetitive peak off-state current | $V_D$=$V_{DRM}$/$V_{RRM}$, $T_j$=25℃ | | ≤5 | ≤5 | μA |
| | | $V_D$=$V_{DRM}$/$V_{RRM}$,$T_j$=125℃ | | ≤0.1 | ≤0.1 | mA |

## THERMAL RESISTANCES

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| Rth (j-c) | Junction to case (AC) | SOT-23-3LK | 32 | ℃/W |
| Rth (j-a) | Junction to ambient | SOT-23-3LK | 400 | ℃/W |

## PART NUMBER



## CHARACTERISTICS CURVES

FIG.1: Maximum power dissipation versus RMS on-state current (full cycle)

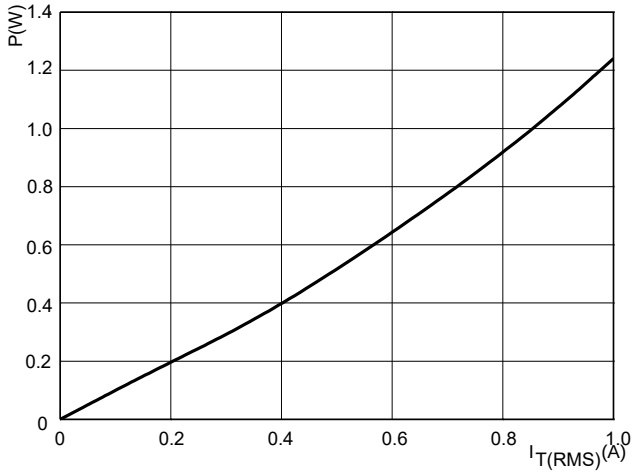



FIG.2: RMS on-state current versus case temperature (full cycle)

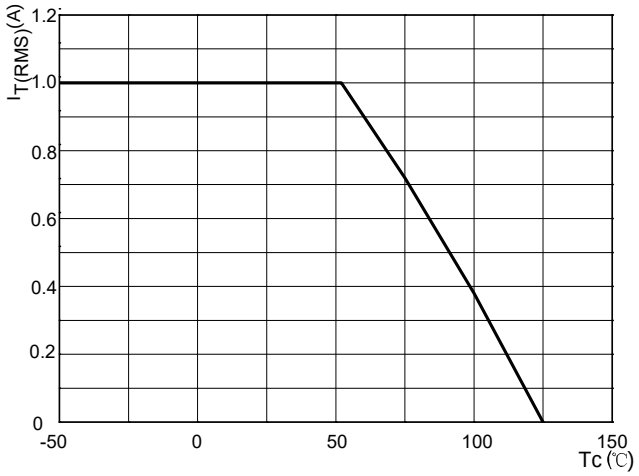



FIG.3: Surge peak on-state current versus number of cycles

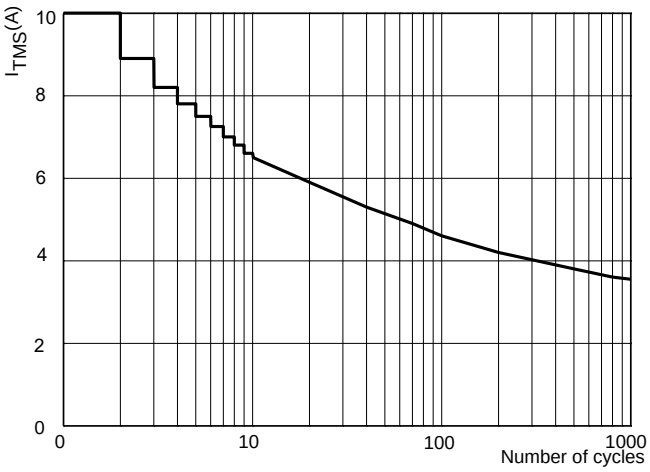



FIG.4: On-state characteristics (maximum values)

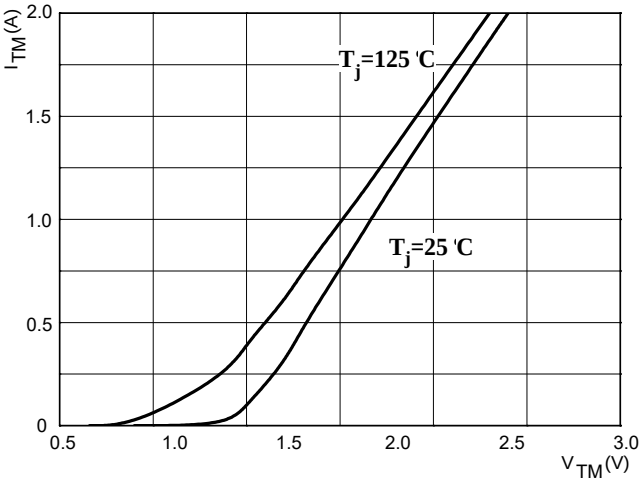



FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp < 10ms

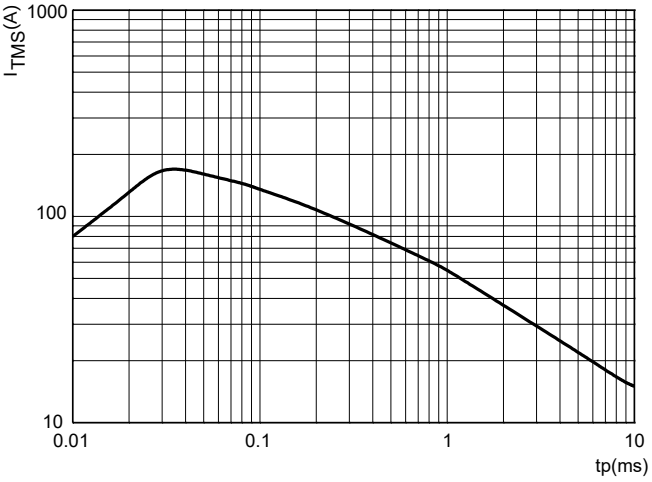
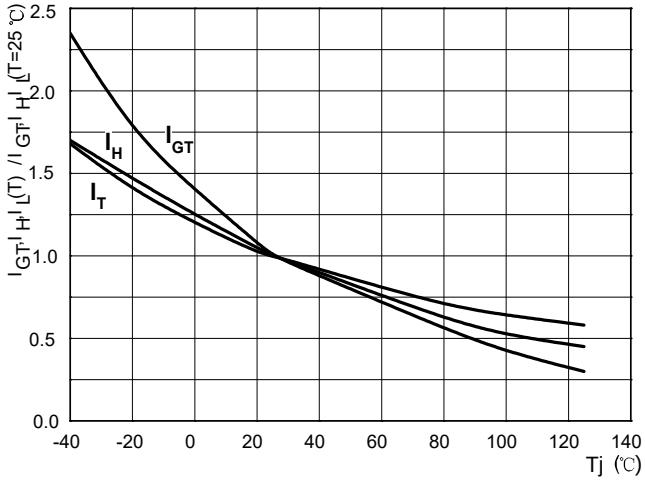
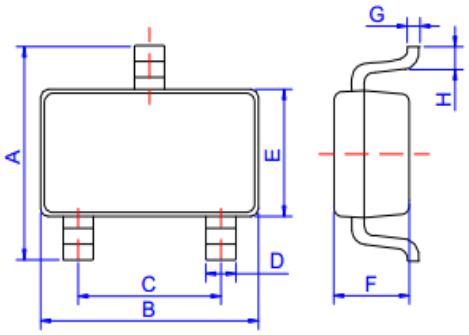



FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature (typical values)



## SOT-23-3LK PACKAGE OUTLINE DIMENSIONS




| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 2.65 | | 2.95 | 0.104 | | 0.116 |
| B | | 2.92 | | | 0.115 | |
| C | | 1.90 | | | 0.075 | |
| D | 0.34 | | 0.36 | 0.013 | | 0.014 |
| E | | 1.60 | | | 0.063 | |
| F | | 1.17 | | | 0.046 | |
| G | | 0.15 | | | 0.006 | |
| H | 0.25 | | 0.55 | 0.010 | | 0.022 |