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XD14051 XD14052 XD14053 DIP-16
XL14051 XL14052 XL14053 SOP-16

The XD14051, XD14052, and XD14053 analog multiplexers are digitally−controlled analog switches. The XD14051 effectively implements an SP8T solid state switch, the XD14052 a DP4T, and the XD14053 a Triple SPDT. All three devices feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

Features

- Triple Diode Protection on Control Inputs
- Switch Function is Break Before Make
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Analog Voltage Range (V_{DD} − V_{EE}) = 3.0 to 18 V
  Note: V_{EE} must be ≤ V_{SS}
- Linearized Transfer Characteristics
- Low−noise − 12 nV/√Cycle, f ≥ 1.0 kHz Typical
- Pin−for−Pin Replacement for XD4051, XD4052, and XD4053
- For 4PDT Switch, See XD14551
- For Lower R_{ON}, Use the XD4051, XD4052, or XD4053 High−Speed CMOS Devices
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

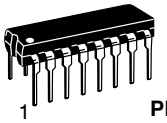
Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range (Referenced to V_{EE}, $V_{SS} \geq V_{EE}$)	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	−0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient) per Control Pin	+10	mA
I_{SW}	Switch Through Current	±25	mA
P_D	Power Dissipation per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

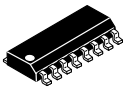
1. Temperature Derating: Plastic “P and D/DW” Packages: − 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS}, V_{EE} or V_{DD}). Unused outputs must be left open.

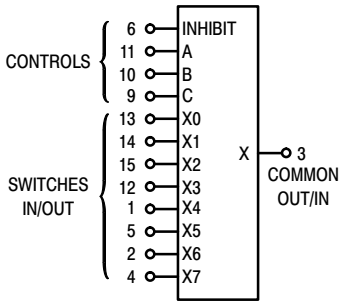


PDIP−16
P SUFFIX
CASE 648



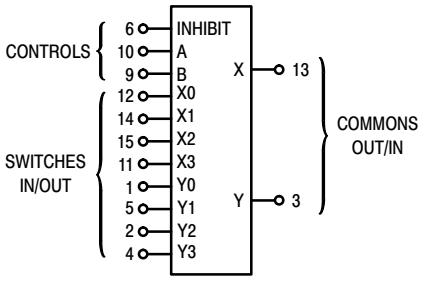
SOIC−16
D SUFFIX
CASE 751B

XD14051
8−Channel Analog Multiplexer/Demultiplexer



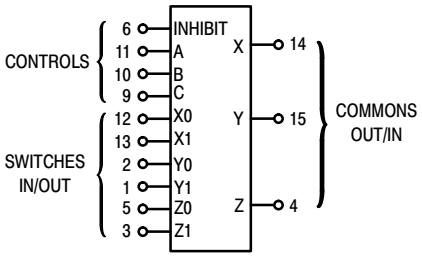
V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

XD14052
Dual 4−Channel Analog Multiplexer/Demultiplexer



V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

XD14053
Triple 2−Channel Analog Multiplexer/Demultiplexer

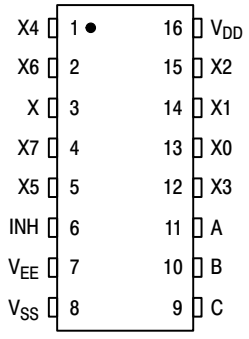


V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

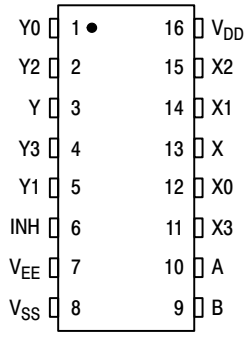
Note: Control Inputs referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be ≤ V_{SS}.

PIN ASSIGNMENT

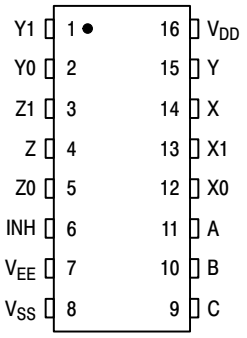
XD14051



XD14052



XD14053



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	– 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (Note 2)	Max	Min	Max	
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	–	$V_{DD} - 3.0 \geq V_{SS} \geq V_{EE}$	3.0	18	3.0	–	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: $V_{in} = V_{SS}$ or V_{DD}, Switch I/O: $V_{EE} \leq V_{I/O} \leq V_{DD}$, and $\Delta V_{switch} \leq$ 500 mV (Note 3)	– – –	5.0 10 20	– – –	0.005 0.010 0.015	5.0 10 20	– – –	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	T_A = 25°C only (The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 μA/kHz) f + I_{DD} (0.20 μA/kHz) f + I_{DD} (0.36 μA/kHz) f + I_{DD}				μA
CONTROL INPUTS — INHIBIT, A, B, C (Voltages Referenced to V_{SS})											
Low−Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	– – –	1.5 3.0 4.0	– – –	2.25 4.50 6.75	1.5 3.0 4.0	– – –	1.5 3.0 4.0	V
High−Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	– – –	3.5 7.0 11	2.75 5.50 8.25	– – –	3.5 7.0 11	– – –	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	–	± 0.1	–	±0.00001	± 0.1	–	1.0	μA
Input Capacitance	C_{in}	–		–	–	–	5.0	7.5	–	–	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y, Z (Voltages Referenced to V_{EE})											
Recommended Peak−to−Peak Voltage Into or Out of the Switch	$V_{I/O}$	–	Channel On or Off	0	V_{DD}	0	–	V_{DD}	0	V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch (Note 3) (Figure 5)	ΔV_{switch}	–	Channel On	0	600	0	–	600	0	300	mV
Output Offset Voltage	V_{OO}	–	V_{in} = 0 V, No Load	–	–	–	10	–	–	–	μV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \leq$ 500 mV (Note 3) $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} = 0 to V_{DD} (Switch)	– – –	800 400 220	– – –	250 120 80	1050 500 280	– – –	1200 520 300	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		– – –	70 50 45	– – –	25 10 10	70 50 45	– – –	135 95 65	Ω
Off−Channel Leakage Current (Figure 10)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	–	± 100	–	± 0.05	± 100	–	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	–	Inhibit = V_{DD}	–	–	–	10	–	–	–	pF
Capacitance, Common O/I	$C_{O/I}$	–	Inhibit = V_{DD} (XD14051) (XD14052) (XD14053)	 – – –	 – – –	 – – –	 60 32 17	 – – –	 – – –	 – – –	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	– –	Pins Not Adjacent Pins Adjacent	– –	– –	– –	0.15 0.47	– –	– –	– –	pF

2. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.
3. For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (Note 4) (C_L = 50 pF, T_A = 25°C) ($V_{EE} \le V_{SS}$ unless otherwise indicated)

Characteristic	Symbol	$V_{DD} - V_{EE}$ Vdc	Typ (Note 5) All Types	Max	Unit
Propagation Delay Times (Figure 6)	t_{PLH}, t_{PHL}				ns
Switch Input to Switch Output (R_L = 1 kΩ)					
XD14051					
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 26.5 ns		5.0	35	90	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 11 ns		10	15	40	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 9.0 ns		15	12	30	
XD14052					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 21.5 ns		5.0	30	75	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 8.0 ns		10	12	30	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 7.0 ns		15	10	25	
XD14053					ns
t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 16.5 ns		5.0	25	65	
t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 4.0 ns		10	8.0	20	
t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 3.0 ns		15	6.0	15	
Inhibit to Output (R_L = 10 kΩ, $V_{EE} = V_{SS}$)	t_{PHZ}, t_{PLZ},				ns
Output "1" or "0" to High Impedance, or	t_{PZH}, t_{PZL}				
High Impedance to "1" or "0" Level					
XD14051		5.0	350	700	
		10	170	340	
		15	140	280	
XD14052		5.0	300	600	ns
		10	155	310	
		15	125	250	
XD14053		5.0	275	550	ns
		10	140	280	
		15	110	220	
Control Input to Output (R_L = 1 kΩ, $V_{EE} = V_{SS}$)	t_{PLH}, t_{PHL}				ns
XD14051		5.0	360	720	
		10	160	320	
		15	120	240	
XD14052		5.0	325	650	ns
		10	130	260	
		15	90	180	
XD14053		5.0	300	600	ns
		10	120	240	
		15	80	160	
Second Harmonic Distortion (R_L = 10KΩ, f = 1 kHz) V_{in} = 5 V_{PP}	–	10	0.07	–	%
Bandwidth (Figure 7) (R_L = 50 Ω, V_{in} = 1/2 (V_{DD}–V_{EE}) p–p, C_L = 50pF 20 Log (V_{out}/V_{in}) = – 3 dB)	BW	10	17	–	MHz
Off Channel Feedthrough Attenuation (Figure 7) R_L = 1KΩ, V_{in} = 1/2 (V_{DD} – V_{EE}) p–p f_{in} = 4.5 MHz — XD14051 f_{in} = 30 MHz — XD14052 f_{in} = 55 MHz — XD14053	–	10	– 50	–	dB
Channel Separation (Figure 8) (R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}–V_{EE}) p–p, f_{in} = 3.0 MHz	–	10	– 50	–	dB
Crosstalk, Control Input to Common O/I (Figure 9) (R_1 = 1 kΩ, R_L = 10 kΩ Control $t_{TLH} = t_{THL}$ = 20 ns, Inhibit = V_{SS})	–	10	75	–	mV

4. The formulas given are for the typical characteristics only at 25°C.
5. Data labelled "Typ" is not lo be used for design purposes but In intended as an indication of the IC's potential performance.

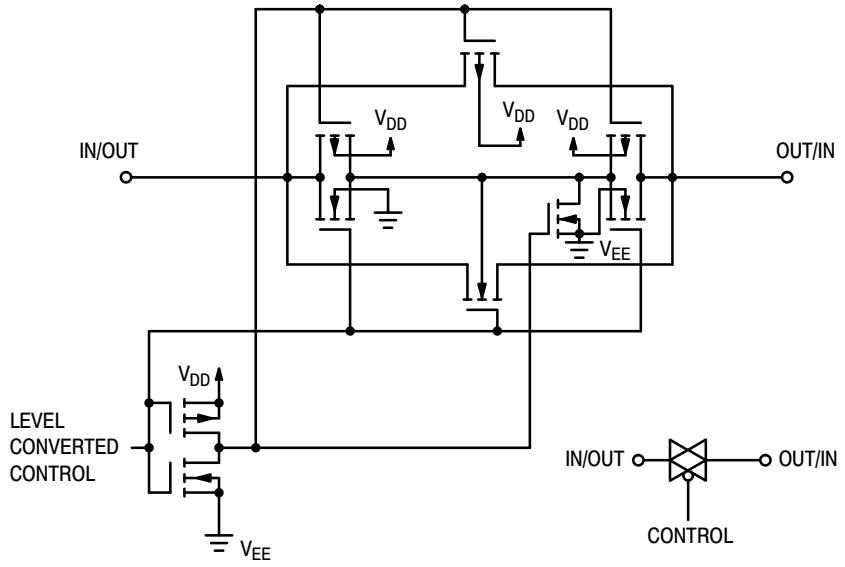


Figure 1. Switch Circuit Schematic

TRUTH TABLE

Control Inputs				ON Switches					
Inhibit	Select C*	B	A	XD14051	XD14052		XD14053		
0	0	0	0	X0	Y0	X0	Z0	Y0	X0
0	0	0	1	X1	Y1	X1	Z0	Y0	X1
0	0	1	0	X2	Y2	X2	Z0	Y1	X0
0	0	1	1	X3	Y3	X3	Z0	Y1	X1
0	1	0	0	X4			Z1	Y0	X0
0	1	0	1	X5			Z1	Y0	X1
0	1	1	0	X6			Z1	Y1	X0
0	1	1	1	X7			Z1	Y1	X1
1	x	x	x	None	None		None		

*Not applicable for XD14052
x = Don't Care

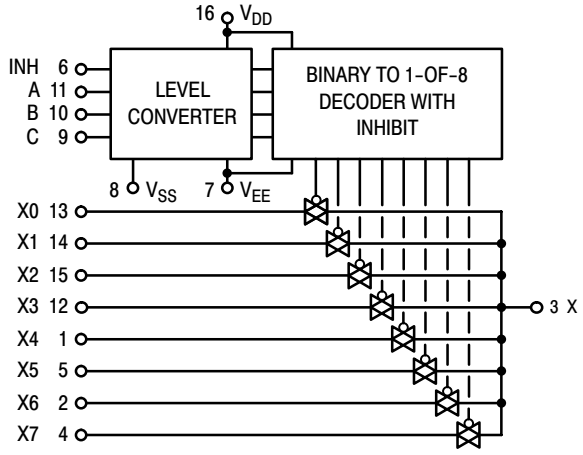


Figure 2.XD14051 Functional Diagram

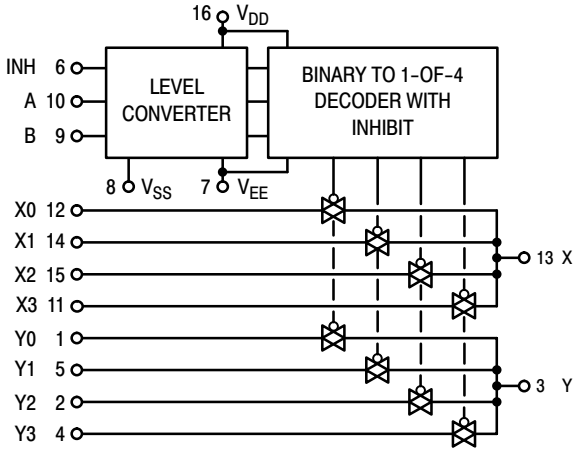


Figure 3. XD14052 Functional Diagram

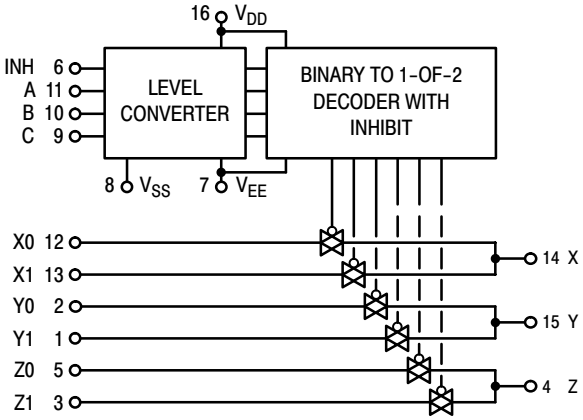


Figure 4. XD14053 Functional Diagram

TEST CIRCUITS

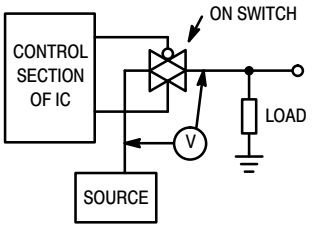


Figure 5. ΔV Across Switch

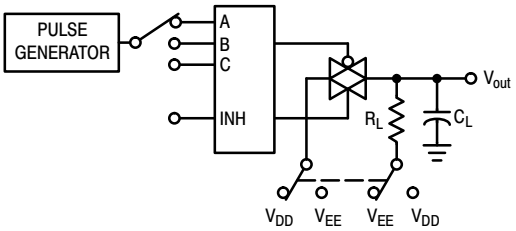


Figure 6. Propagation Delay Times, Control and Inhibit to Output

A, B, and C inputs used to turn ON or OFF the switch under test.

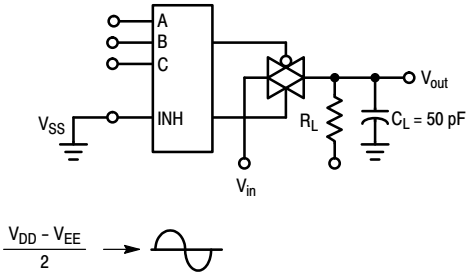


Figure 7. Bandwidth and Off−Channel Feedthrough Attenuation

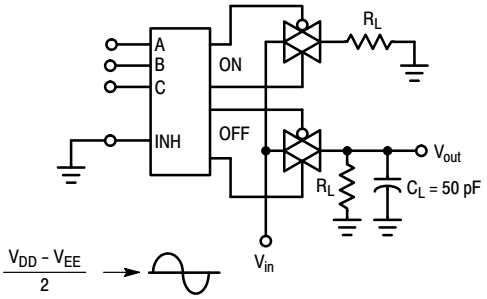


Figure 8. Channel Separation (Adjacent Channels Used For Setup)

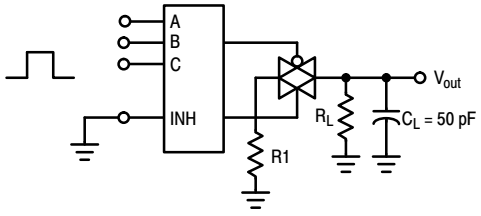


Figure 9. Crosstalk, Control Input to Common O/I

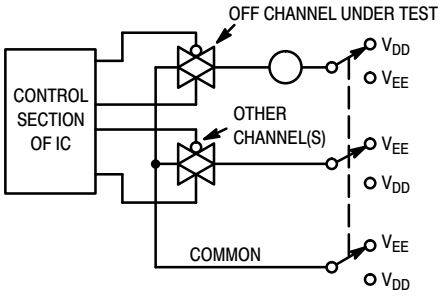


Figure 10. Off Channel Leakage

NOTE: See also Figures 7 and 8 in the XD14016 data sheet.

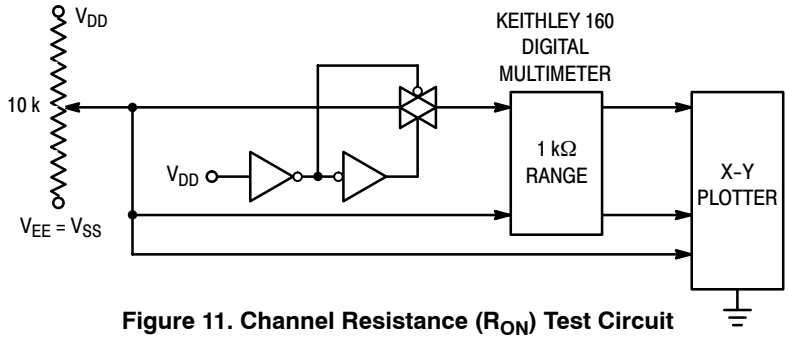


Figure 11. Channel Resistance (R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTICS

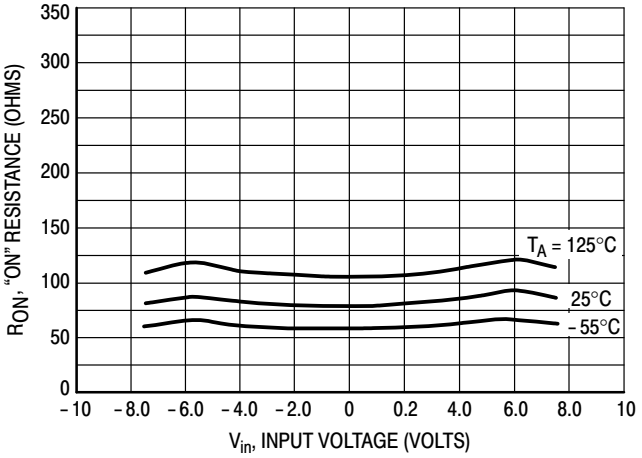


Figure 12. V_{DD} = 7.5 V, V_{EE} = − 7.5 V

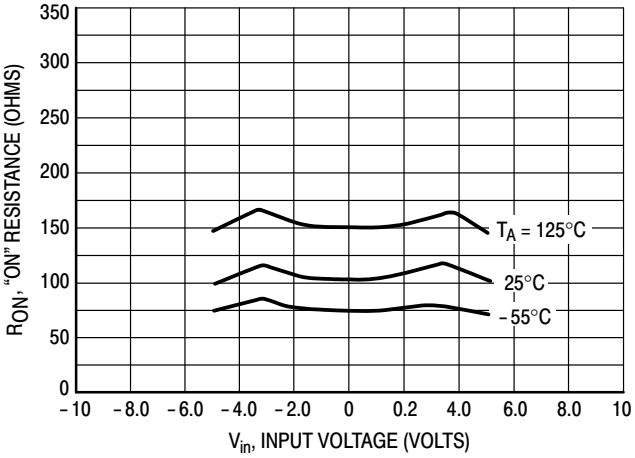


Figure 13. V_{DD} = 5.0 V, V_{EE} = − 5.0 V

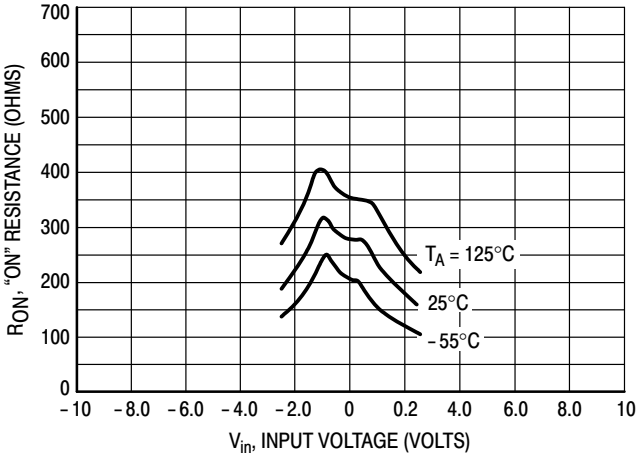


Figure 14. V_{DD} = 2.5 V, V_{EE} = − 2.5 V

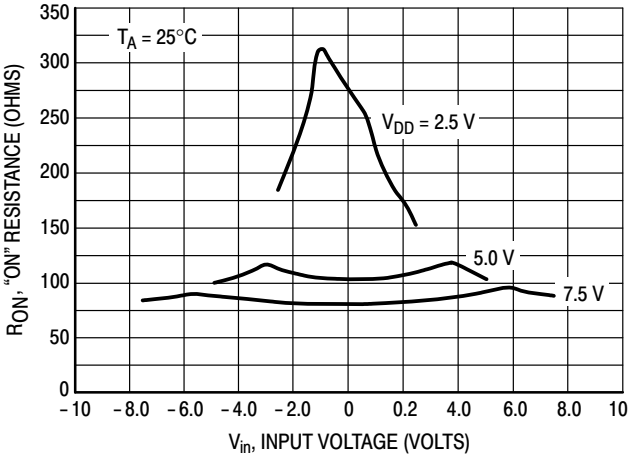


Figure 15. Comparison at 25°C, $V_{DD} = -V_{EE}$

APPLICATIONS INFORMATION

Figure A illustrates use of the on−chip level converter detailed in Figures 2, 3, and 4. The 0−to−5 V Digital Control signal is used to directly control a 9 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, V_{DD} − V_{SS} = 5 V maximum swing above V_{SS}; V_{SS} − V_{EE} = 5 V maximum swing below V_{SS}. The example shows a ± 4.5 V signal which allows a 1/2 volt margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{EE} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = + 10 V, V_{SS} = + 5 V, and V_{EE} − 3 V is acceptable. See the Table below.

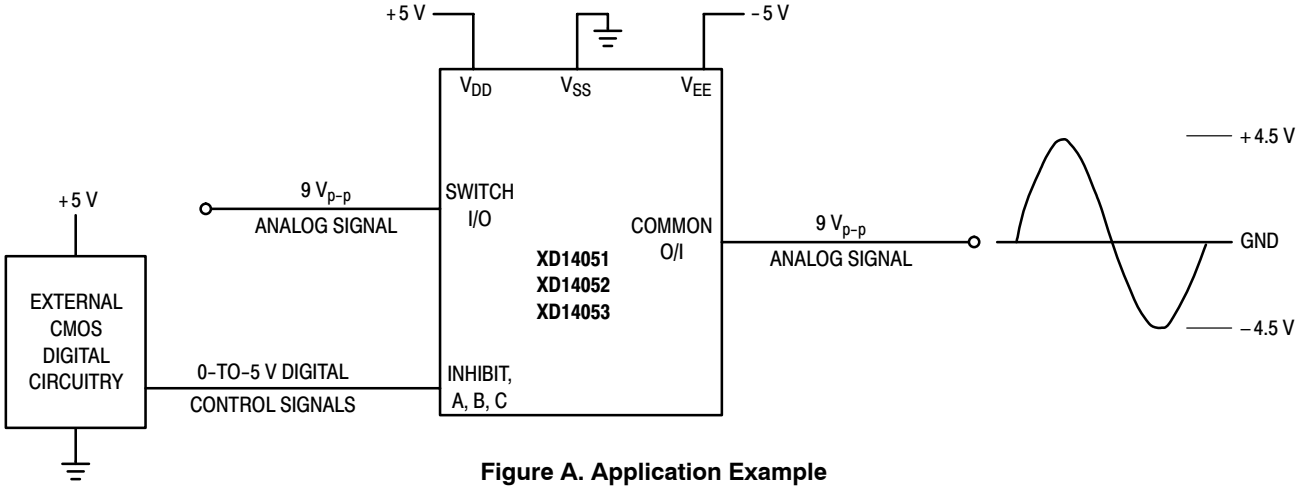


Figure A. Application Example

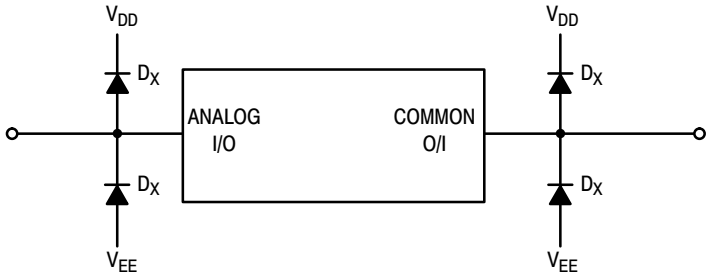
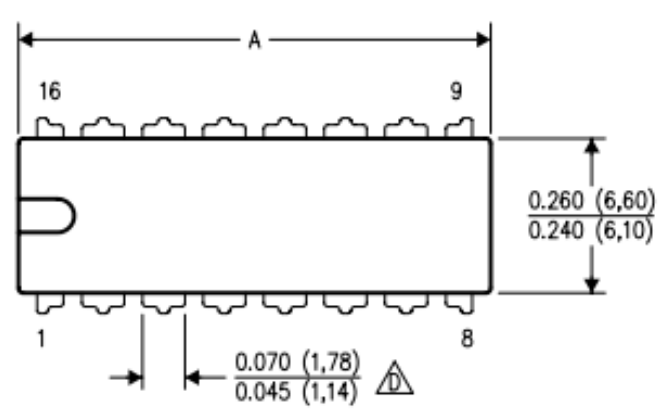


Figure B. External Germanium or Schottky Clipping Diodes

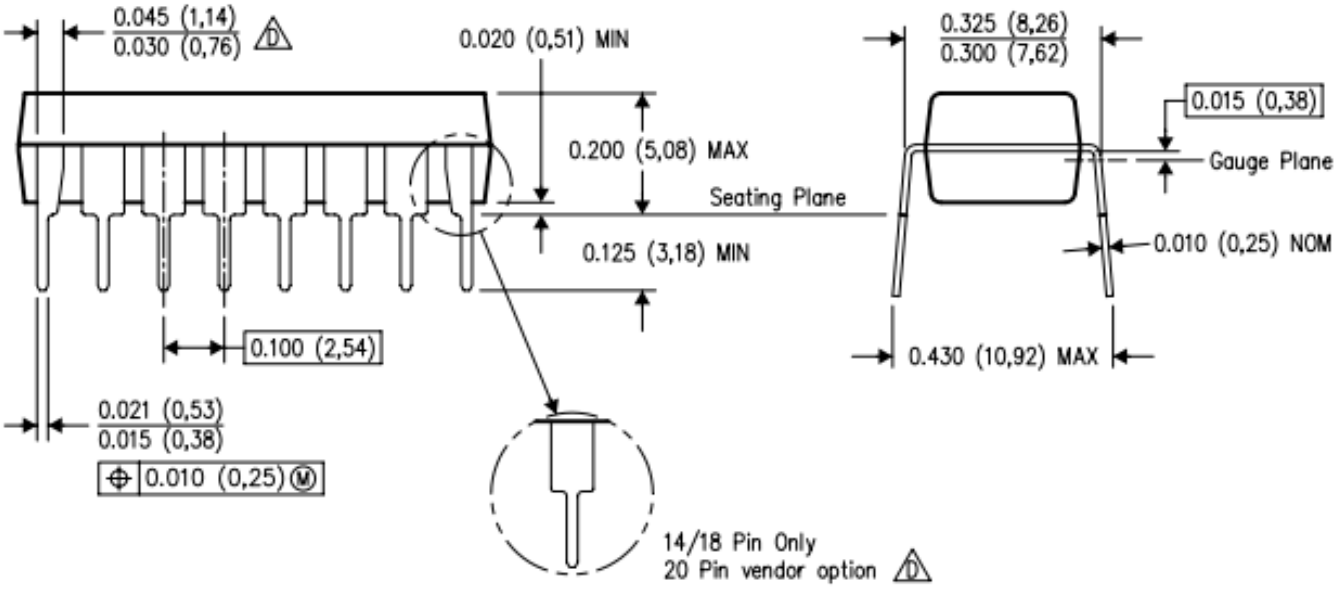
POSSIBLE SUPPLY CONNECTIONS

V_{DD} In Volts	V_{SS} In Volts	V_{EE} In Volts	Control Inputs Logic High/Logic Low In Volts	Maximum Analog Signal Range In Volts
+ 8	0	− 8	+ 8/0	+ 8 to − 8 = 16 V_{p-p}
+ 5	0	− 12	+ 5/0	+ 5 to − 12 = 17 V_{p-p}
+ 5	0	0	+ 5/0	+ 5 to 0 = 5 V_{p-p}
+ 5	0	− 5	+ 5/0	+ 5 to − 5 = 10 V_{p-p}
+ 10	+ 5	− 5	+ 10/ + 5	+ 10 to − 5 = 15 V_{p-p}



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

C



以上信息仅供参考.如需帮助联系客服人员。谢谢 XINLUDA