Dual channel N-Channel MOSFE

General Description

The LPM9031 is a dual channel MOSFET, which combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is suitable for use as a load switch or in PWM applications.

Features

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Order Information

LPM9031 □ □ □

- F: Pb-Free
- Package Type
  - SO：SOP-8
  - QV：DFN-8

Applications

- Driver for Relay, Solenoid, Motor, LED etc.
- DC-DC converter circuit
- Power Switch
- Load Switch
- Charging

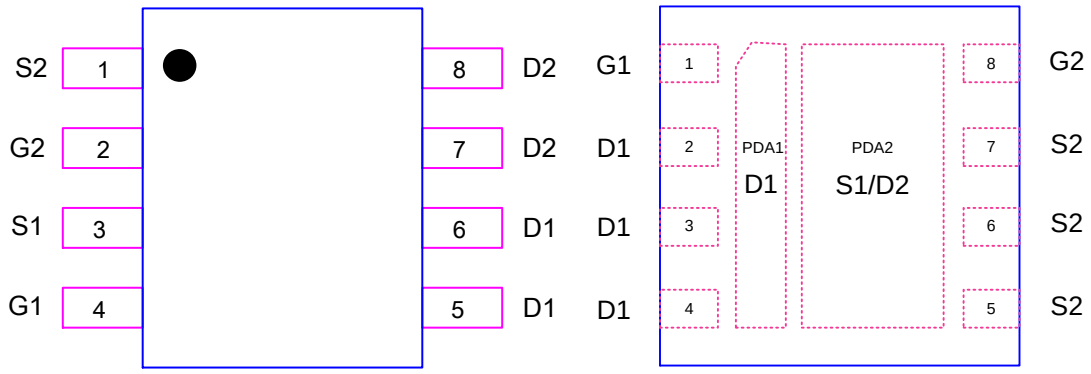
Pin Description

Pin Number		Pin Description
SOP-8	DFN_8	
1	5,6,7	S2
2	8	G2
3	PAD_2	S1
4	1	G1
5,6	2,3,4,PAD_1	D1
7,8	PAD_2	D2

Marking Information

Device	Marking	Package	Shipping
LPM9031SOF	LPS LPM9031 YWX	SOP-8	4K/REEL
LPM9031QVF	LPS 9031 YWX	DFN-8	5K/REEL
Y:Production year W:Production period X:Production batch			

Pin Configurations



SOP-8
TOP VIEW

DFN-8
TOP VIEW

Absolute Maximum Ratings

Channel 1 and channel 2 have the same maximum ratings

Parameter		Symbol	Maximum	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A=25℃	I_D	5.8	A
	T_A=70℃		4.9	
Pulsed Drain Current		I_{DM}	30	
Power Dissipation	T_A=25℃	P_D	2	W
	T_A=70℃		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal resistance ratings

Parameter		Symbol	TYP	Unit
Junction-to-Case Thermal Resistance	t ≤ 10s	$R_{\theta JA}$	48	℃/W
Junction-to-Case Thermal Resistance	Steady State		74	℃/W
Maximum Junction-to-Lead	Steady State	$R_{\theta JL}$	32	℃/W

Electrical Characteristics

Electrical Characteristics (T_J=25℃ unless otherwise noted)
Channel 1 and channel 2 have the same electrical characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	μA
		T_J=55℃			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.65	1.05	1.45	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=5.8A		18	28	mΩ
		T_J=125℃		28	39	
		V_{GS}=4.5V, I_D=5A		19	33	
		V_{GS}=2.5V, I_D=4A		24	52	
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=5.8A		33		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		630		pF
C_{oss}	Output Capacitance			75		pF
C_{rss}	Reverse Transfer Capacitance			50		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	1.5	3	4.5	Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=15V, I_D=5.8A		6		nC
Q_{gs}	Gate Source Charge			50		nC
Q_{gd}	Gate Drain Charge			3		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=2.6Ω, R_{GEN}=3Ω		3		ns
t_r	Turn-On Rise Time			2.5		ns
$t_{D(off)}$	Turn-Off DelayTime			25		ns
tf	Turn-Off Fall Time			4		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=5.8A, dI/dt=100A/μs		8.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=5.8A, dI/dt=100A/μs		2.6		nC

Typical Characteristics

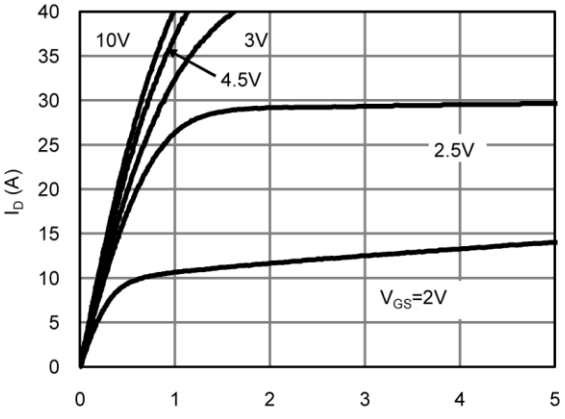


Fig 1: On-Region Characteristics

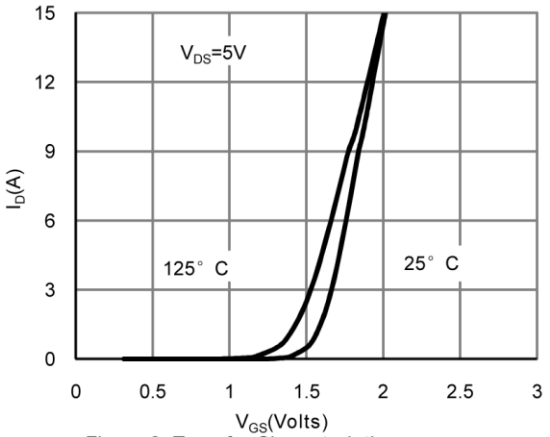


Figure 2: Transfer Characteristics

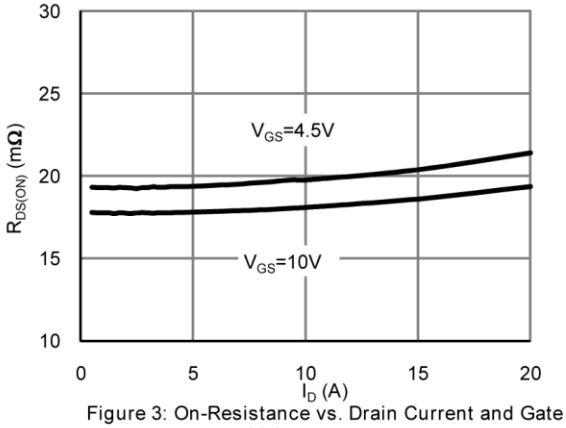


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

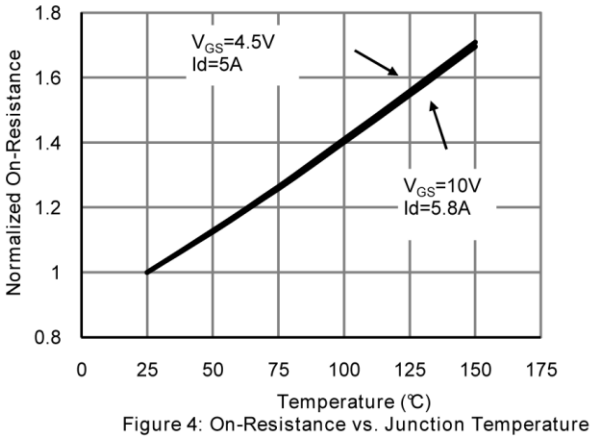


Figure 4: On-Resistance vs. Junction Temperature

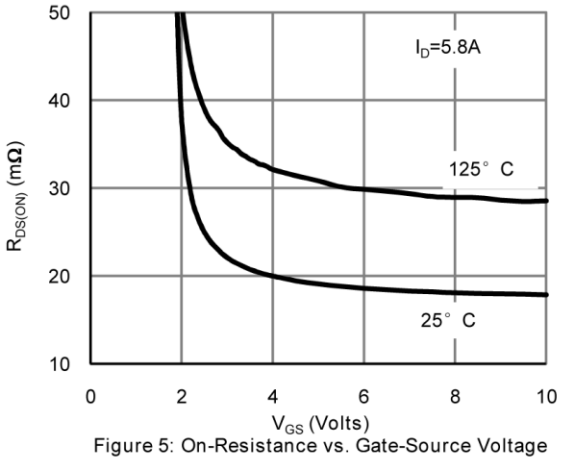


Figure 5: On-Resistance vs. Gate-Source Voltage

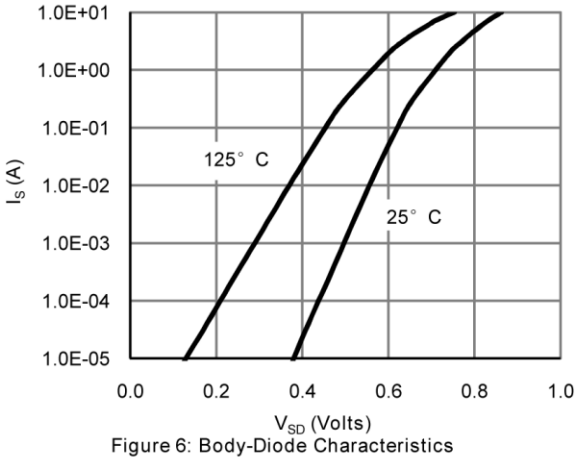


Figure 6: Body-Diode Characteristics

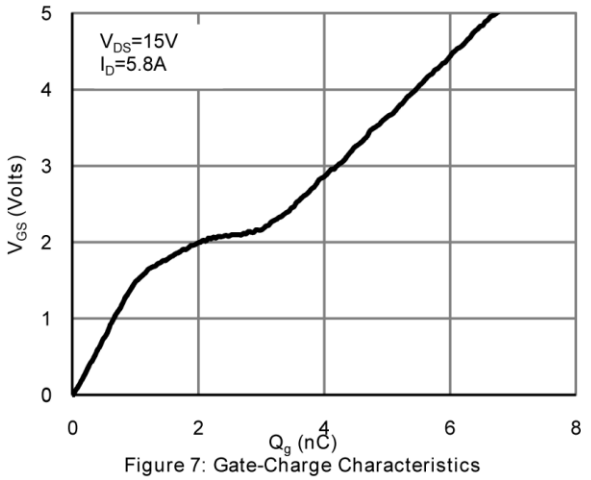


Figure 7: Gate-Charge Characteristics

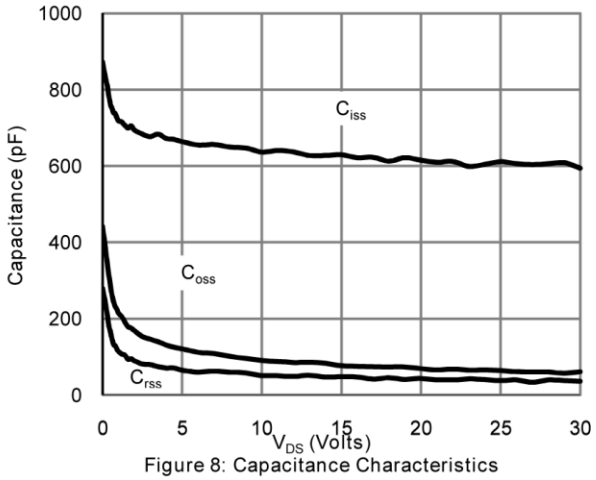


Figure 8: Capacitance Characteristics

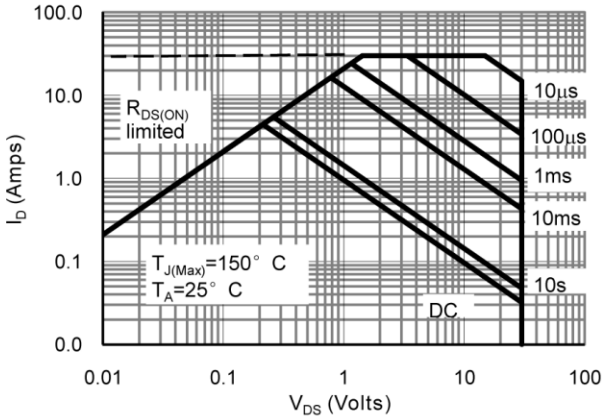


Figure 9: Maximum Forward Biased Safe Operating Area

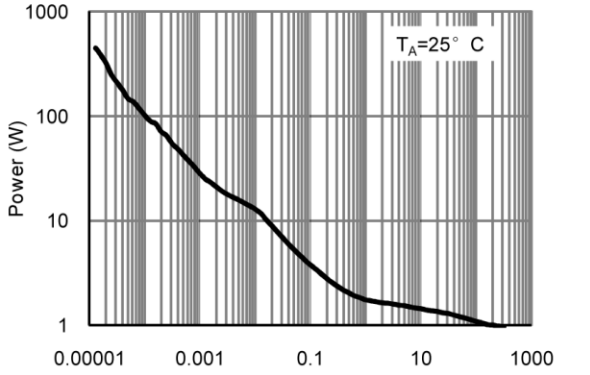


Figure 10: Single Pulse Power Rating Junction-to-Ambient

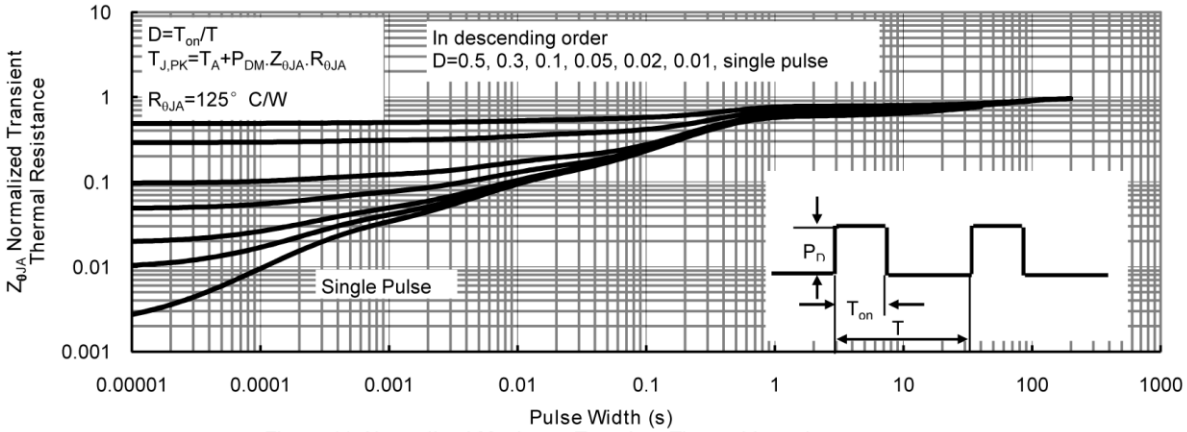
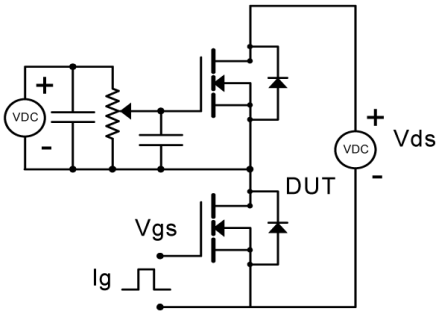
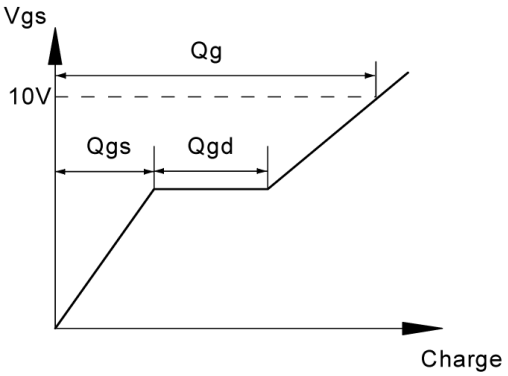


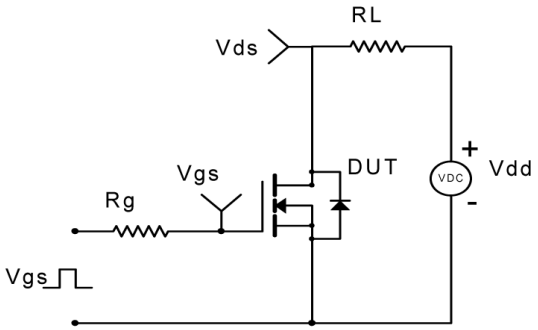
Figure 11: Normalized Maximum Transient Thermal Impedance

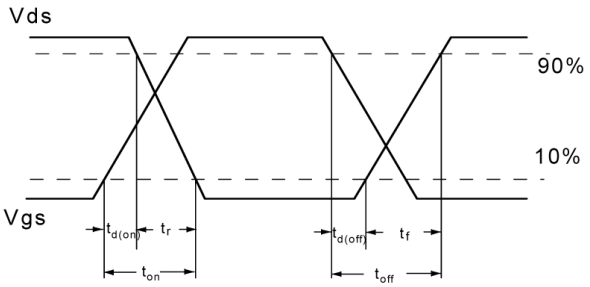
Gate Charge Test Circuit & Waveform



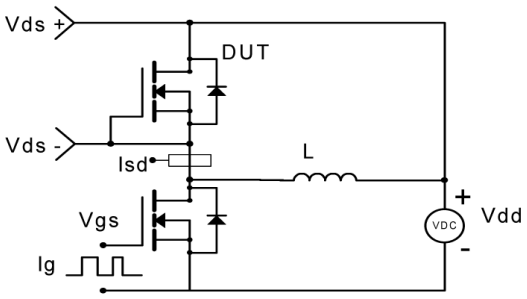


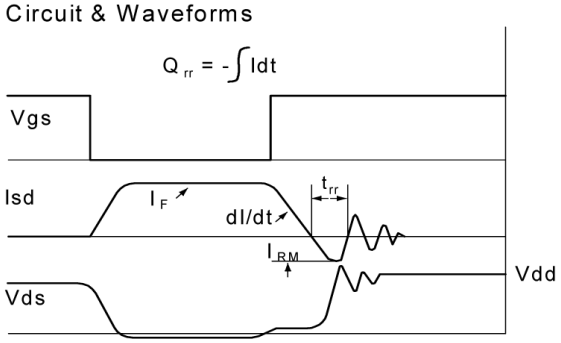
Resistive Switching Test Circuit & Waveforms





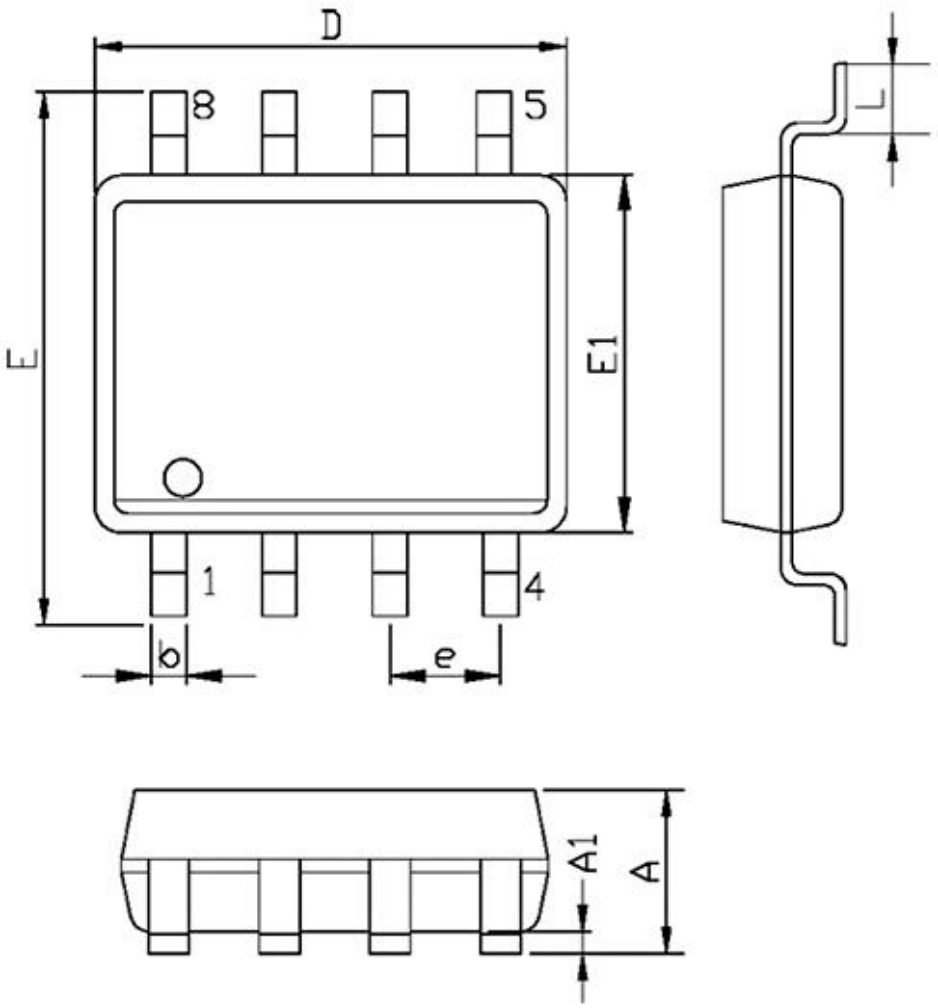
Diode Recovery Test Circuit & Waveforms





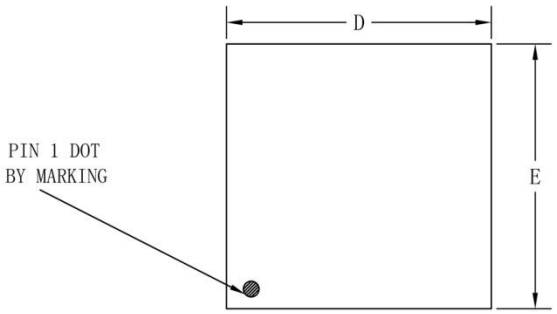
Packaging Information

SOP8

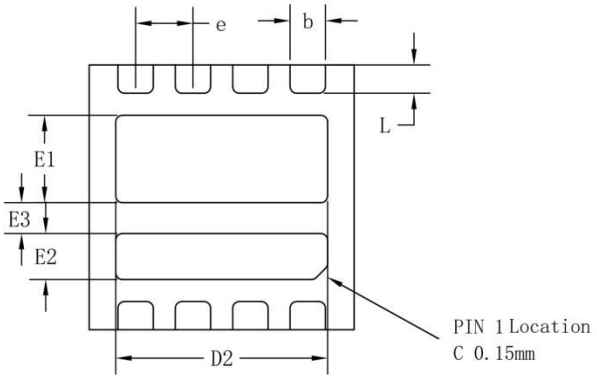


SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	4.90		0.193	
E	5.80	6.20	0.228	0.244
E1	3.90		0.153	
L	0.40	1.27	0.016	0.050
b	0.31	0.51	0.012	0.020
e	1.27		0.050	

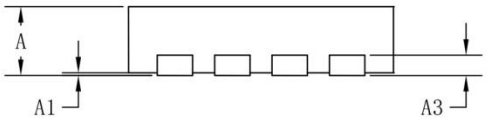
DFN8 3*3



TOP VIEW



BOTTOM VIEW



SIDE VIEW

COMMON DIMENSIONS (MM)			
PKG.	W:VERYVERY THIN		
REF.	MIN.	NOM.	MAX
A	0.70	0.75	0.80
A1	0.00	–	0.05
A3	0.20 REF.		
D	2.95	3.00	3.05
E	2.95	3.00	3.05
D2	2.30	2.40	2.50
E2	0.42	0.52	0.62
E1	0.89	0.99	1.09
E3		0.35	
b	0.35	0.40	0.45
L	0.27	0.32	0.37
e	0.65 BSC		