1000V N-ch Planar MOSFET

Lead Free Package and Finish

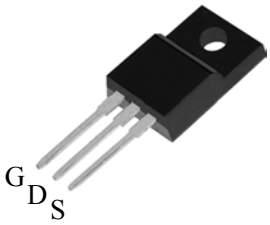
BV_{DSS}	$R_{DS(ON),typ.}$	I_D
1000V	1.2Ω	8.0A

General Features

- RoHS Compliant
- $R_{DS(ON),typ.}$=1.2 Ω @V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

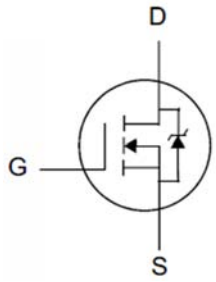
Applications

- Adaptor
- Charger
- SMPS Standby Power



TO-220F

Package No to Scale



Ordering Information

Part Number	Package	Brand
PTA08N100	TO-220F	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	PTA08N100	Unit
V_{DSS}	Drain-to-Source Voltage	1000	V
V_{GSS}	Gate-to-Source Voltage	±30	
I_D	Continuous Drain Current	8.0	A
I_{DM}	Pulsed Drain Current at V_{GS}=10V	32	
E_{AS}	Single Pulse Avalanche Energy	1000	mJ
P_D	Power Dissipation	45	W
	Derating Factor above 25℃	0.36	W/℃
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PTA08N100	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.77	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	100	

Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	1000	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=1000V, V_{GS}=0V
		--	--	100		V_{DS}=800V, V_{GS}=0V, T_J =125℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+30V, V_{DS}=0V
		--	--	-100		V_{GS}=-30V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	1.2	1.5	Ω	V_{GS}=10V, I_D=4A
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA
gfs	Forward Transconductance	--	8.0	--	S	V_{DS}=15V,ID=3A

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	2300	--	pF	V_{GS}=0V, V_{DS}=25V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	100	--		
C_{oss}	Output Capacitance	--	180	--		
Q_g	Total Gate Charge	--	62	--	nC	V_{DD}=500V, I_D=8A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	15	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	23	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	25	--	ns	V_{DD}=500V, I_D=8A, V_{GS}=10V Rg=4.7Ω
t_{rise}	Rise Time	--	33	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	58	--		
t_{fall}	Fall Time	--	36	--		

Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current[2]	--	--	8	A	Integral pn-diode in MOSFET
I_{SM}	Pulsed Source Current[2]	--	--	32		
V_{SD}	Diode Forward Voltage	--	--	1.5	V	I_S=8A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	400	--	ns	V_{GS}=0V I_F= I_S, di/dt=100A/μs
Q_{rr}	Reverse Recovery Charge	--	3.0	--	uC	

Note:

[1] T_J=+25℃ to +150℃
[2] Pulse width≤380μs; duty cycle≤2%.

Test Circuits and Waveforms

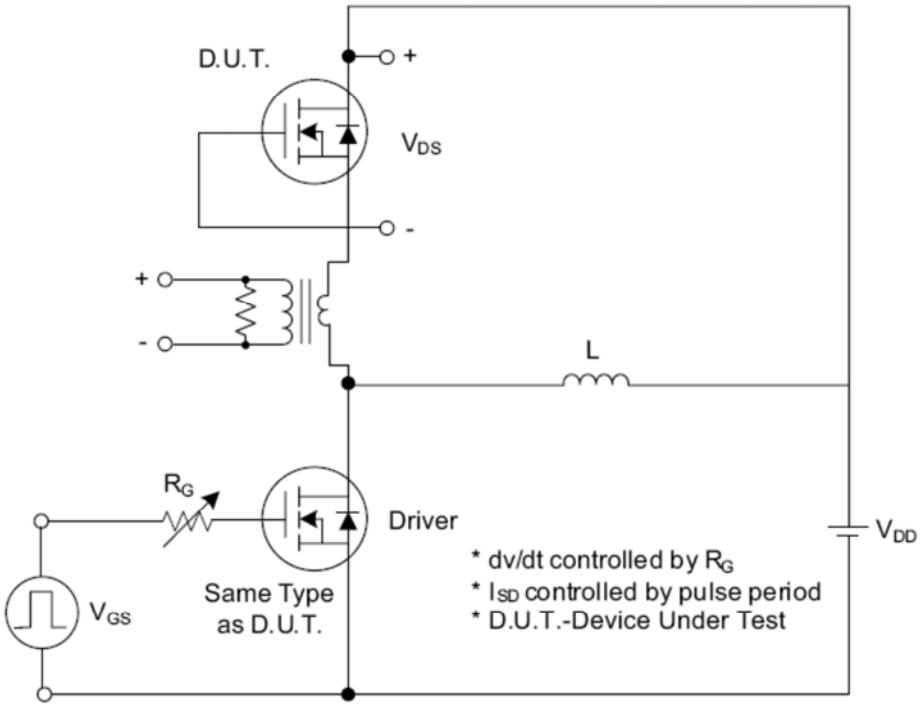


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

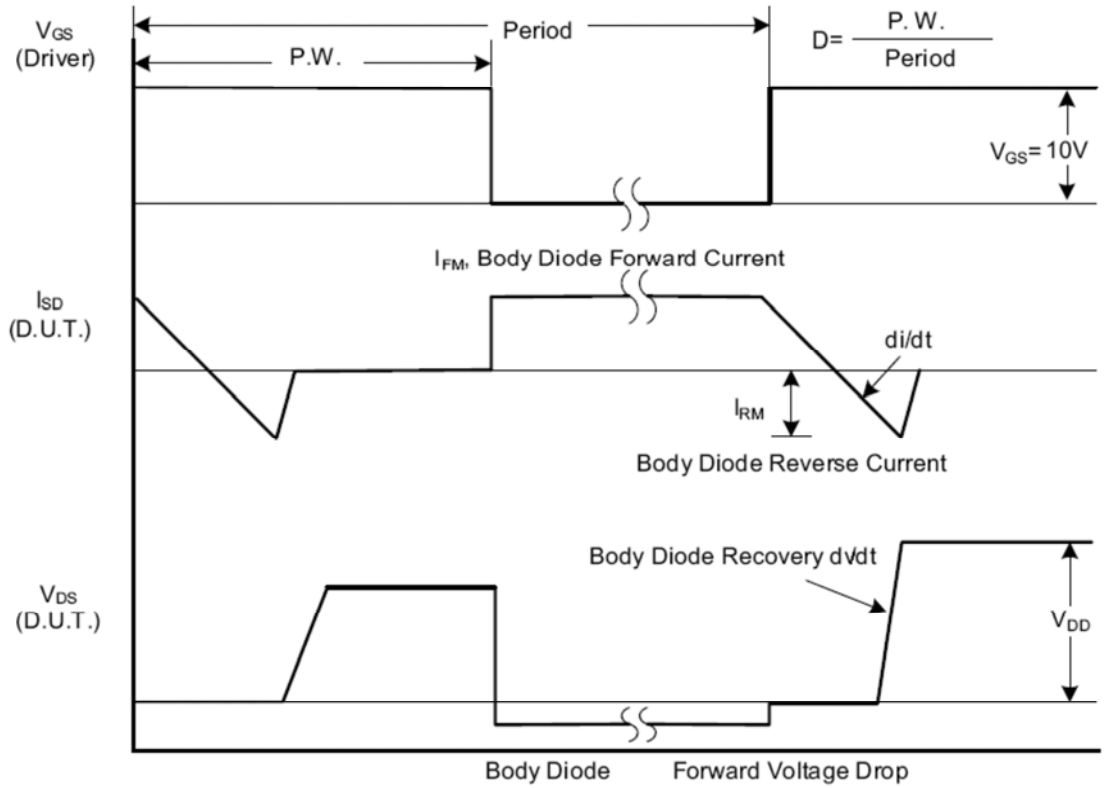


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

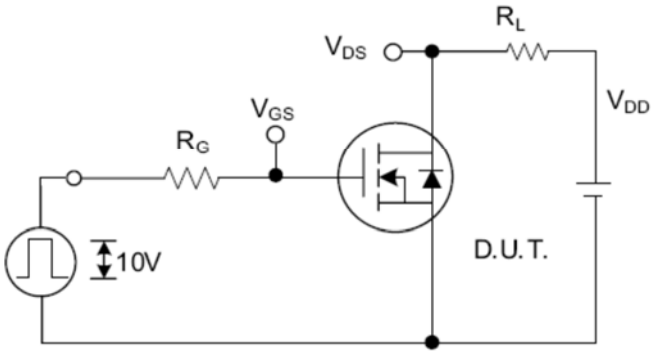


Fig. 2.1 Switching Test Circuit

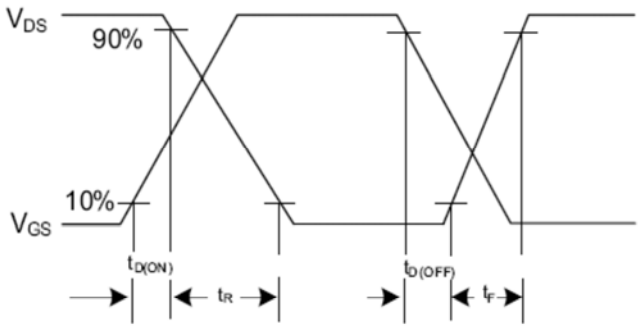


Fig. 2.2 Switching Waveforms

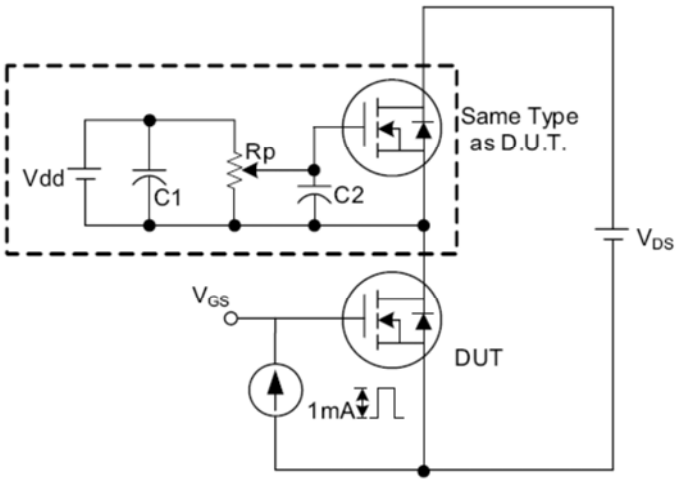


Fig. 3 . 1 Gate Charge Test Circuit

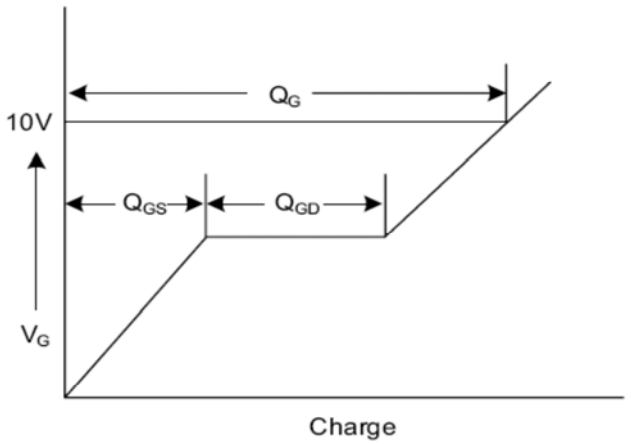


Fig. 3 . 2 Gate Charge Waveform

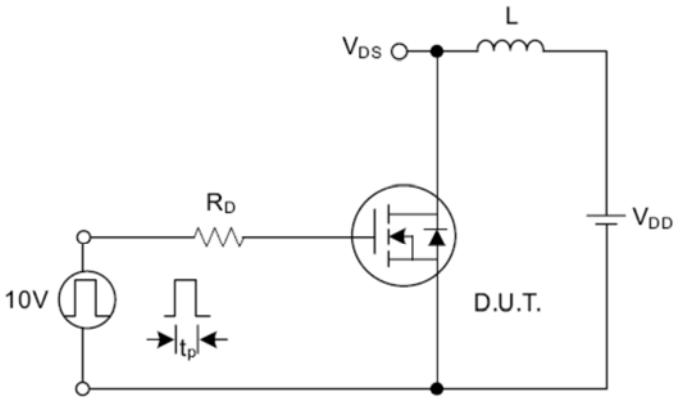


Fig. 4.1 Unclamped Inductive Switching Test Circuit

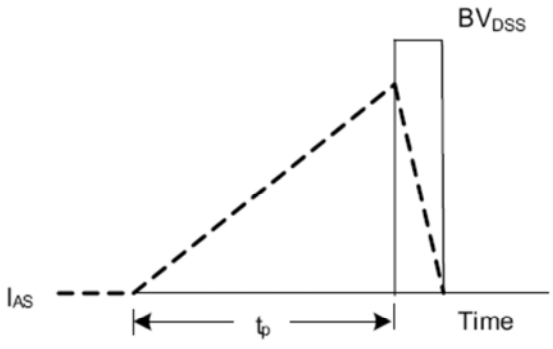


Fig. 4.2 Unclamped Inductive Switching Waveforms

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