68V N-Channel MOSFET

Lead Free Package and Finish

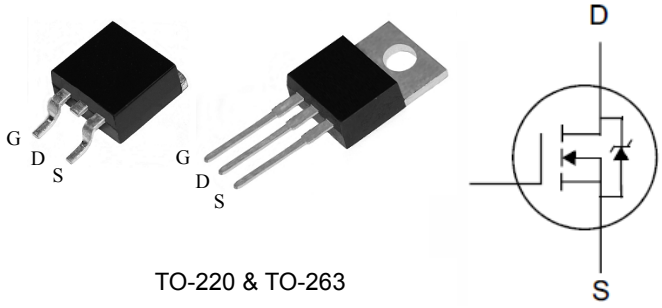
BV_{DSS}	$R_{DS(ON),typ.}$	I_D[2]
68V	6.5mΩ	95A

General Features

- Proprietary New Trench Technology
- $R_{DS(ON),typ.}$=6.5 mΩ@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

Applications

- High efficiency DC/DC Converters
- Synchronous Rectification
- UPS Inverter



TO-220 & TO-263

Package Not to Scale

Ordering Information

Part Number	Package	Brand
PTP9506E	TO-220	
PTB9506E	TO-263	

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	PTP9506E	PTB9506E	Unit
V_{DSS}	Drain-to-Source Voltage[1]	68		V
V_{GSS}	Gate-to-Source Voltage	±20		
I_D	Continuous Drain Current[2]	95		A
I_{DM}	Pulsed Drain Current at V_{GS}=10V[2,4]	380		
E_{AS}	Single Pulse Avalanche Energy	388		mJ
dv/dt	Peak Diode Recovery dv/dt[3]	5.0		V/ns
P_D	Power Dissipation @T_C = 25ºC	136		W
	Power Dissipation @T_C = 100ºC	68		
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260		℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 175		

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PTP9506E	PTB9506E	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.10		℃/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62		

Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	68	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=68V, V_{GS}=0V
		--	--	25		V_{DS}=68V, V_{GS}=0V, T_J =100℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+20V, V_{DS}=0V
		--	--	-100		V_{GS}=-20V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	6.5	7.5	mΩ	V_{GS}=10V, I_D=24A [5]
$V_{GS(TH)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=V_{GS}, I_D=250uA
gfs	Forward Transconductance	20	--	--	S	V_{DS}=5V,I_D=20A [5]

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	4200	--	pF	V_{GS}=0V, V_{DS}=30V, f=1.0MH_Z
C_{rss}	Reverse Transfer Capacitance	--	220	--		
C_{oss}	Output Capacitance	--	280	--		
Q_g	Total Gate Charge	--	70	--	nC	V_{DD}=30V, I_D=24A, V_{GS}=0 to 10V
Q_{gs}	Gate-to-Source Charge	--	20	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	18	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	15	--	nS	V_{DD}=30V, I_D=24A, V_{GS}= 10V R_G=2.5Ω
t_{rise}	Rise Time	--	95	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	45	--		
t_{fall}	Fall Time	--	35	--		

Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current[2]	--	--	95	A	Integral PN-diode in MOSFET
I_{SM}	Pulsed Source Current[2]	--	--	380		
V_{SD}	Diode Forward Voltage	--	--	1.2	V	I_S=24A, V_{GS}=0V
trr	Reverse recovery time	--	75	--	ns	V_{GS}=0V ,I_F=24A, di_F/dt=100A/μs
Qrr	Reverse recovery charge	--	50	--	nC	

Note:

[1] T_J=+25℃ to +175℃
[2] Silicon limited current only.
[3].Package limited current
[4] Repetitive rating; pulse width limited by maximum junction temperature.
[5] Pulse width≤380μs; duty cycle≤2%.

Typical Characteristics

Figure 1. Transient Thermal Impedance

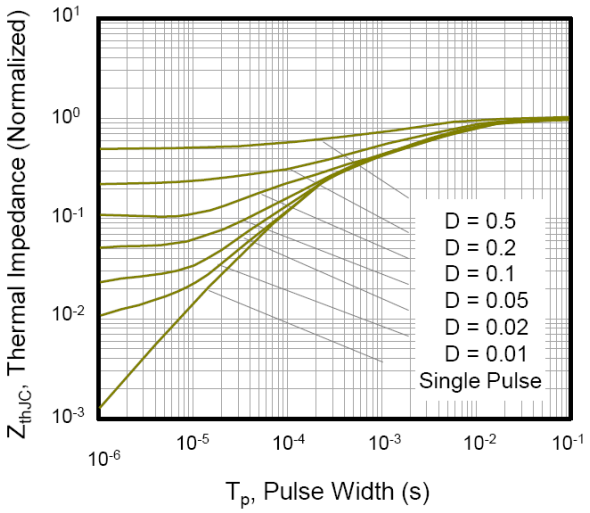


Figure 2. Safe operation area

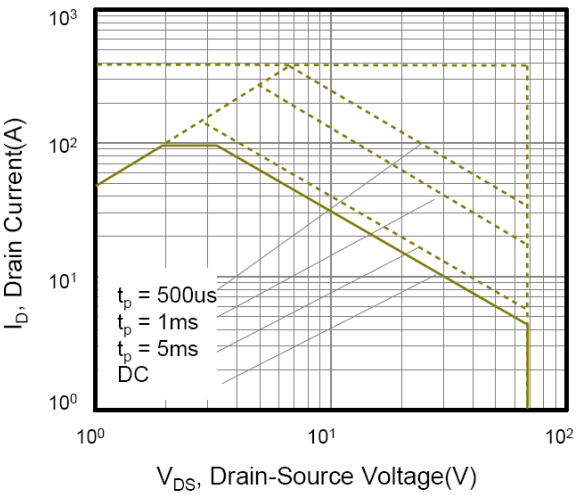


Figure 3. On-Resistance vs. Drain Current

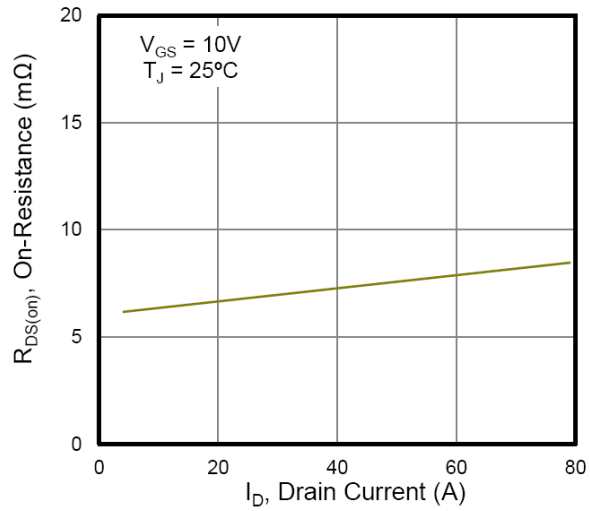


Figure 4. Capacitance

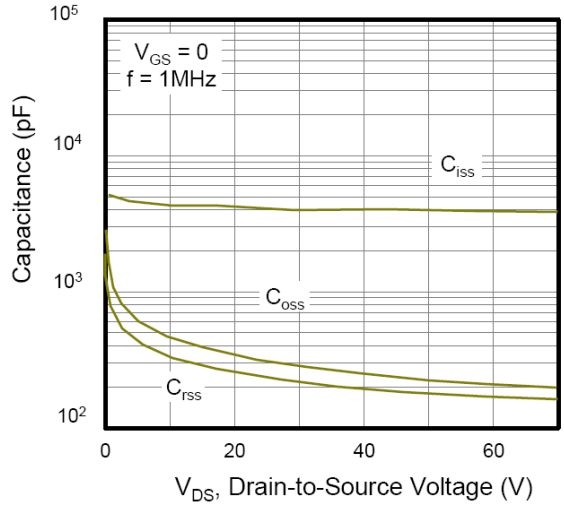


Figure 5. Gate Charge

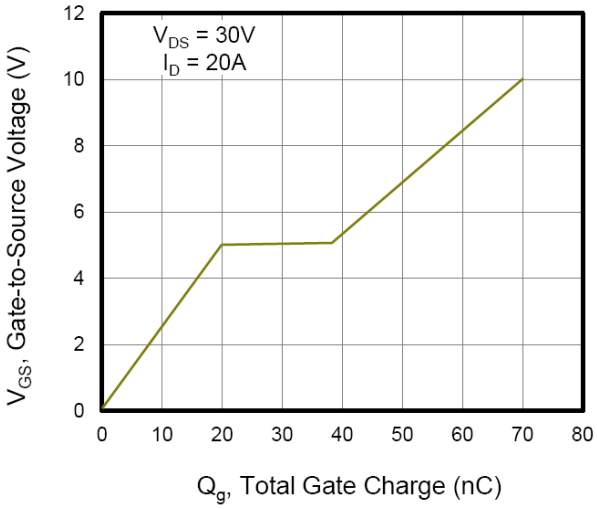
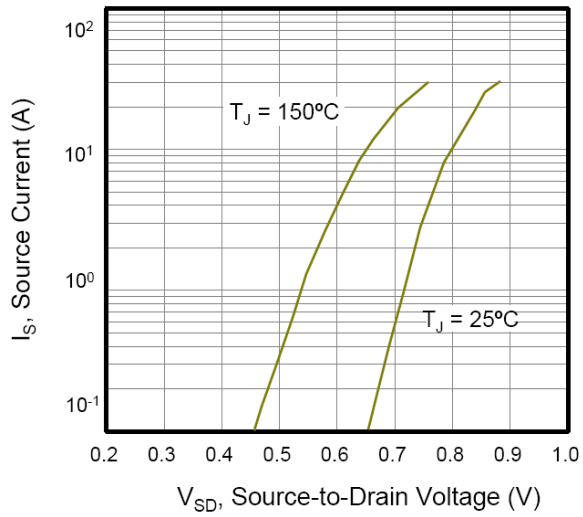


Figure 6. Body Diode Forward Voltage



Typical Characteristics(Cont.)

Figure 7. On-Resistance vs. Temperature

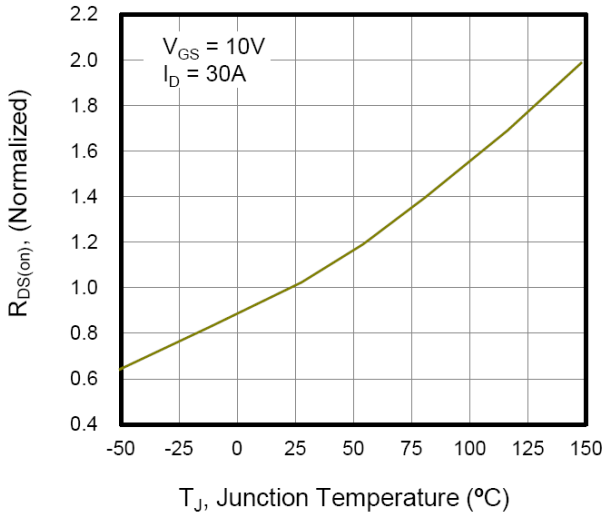


Figure 8. Threshold Voltage vs. Temperature

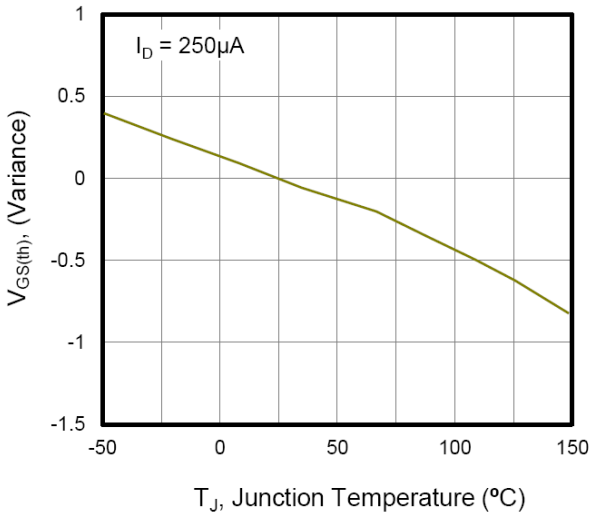


Figure 9. Output Characteristics

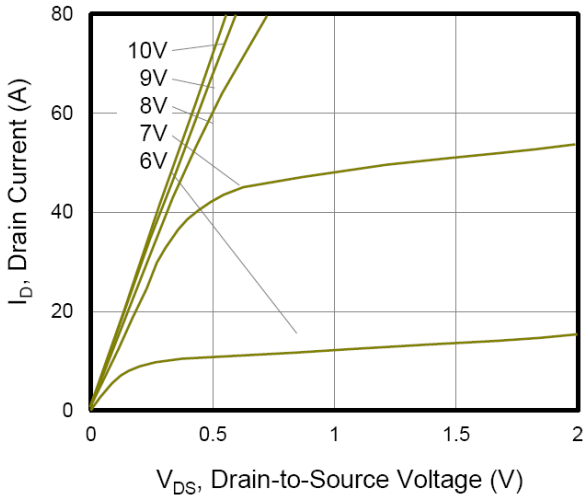
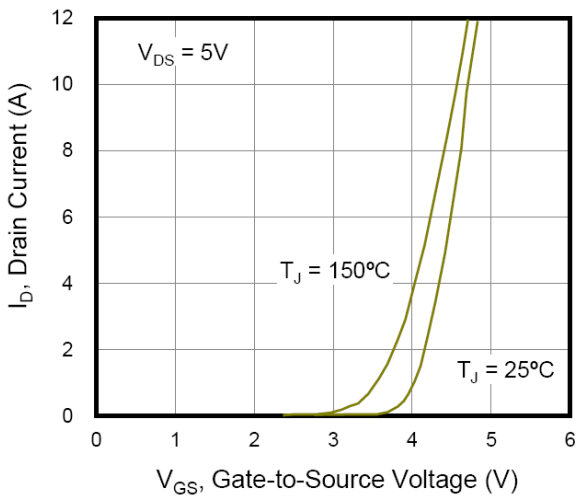


Figure 10. Transfer Characteristics



Test Circuits and Waveforms

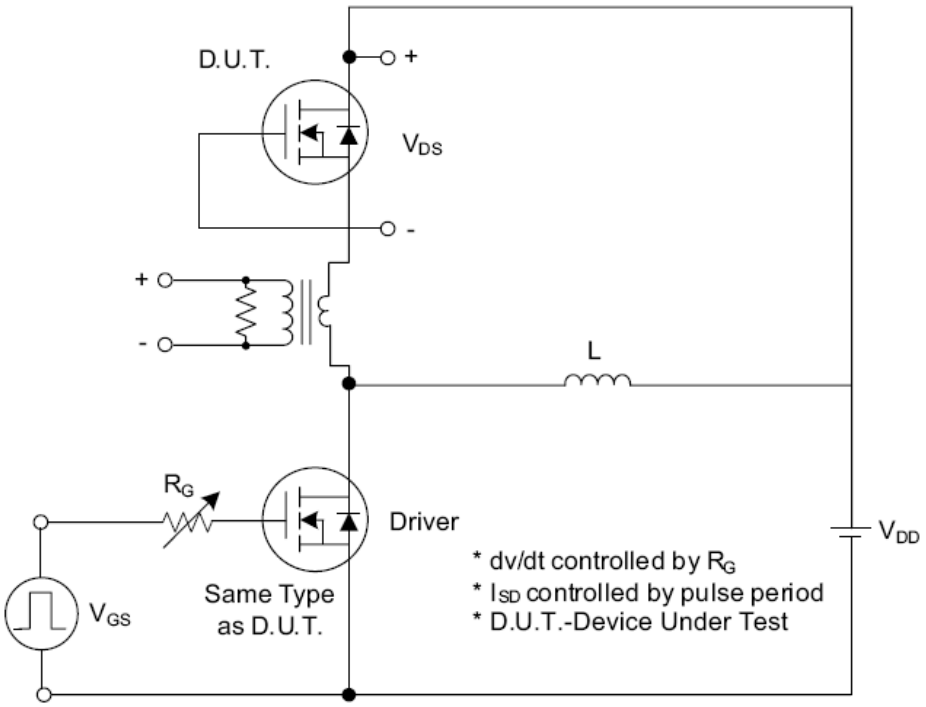


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

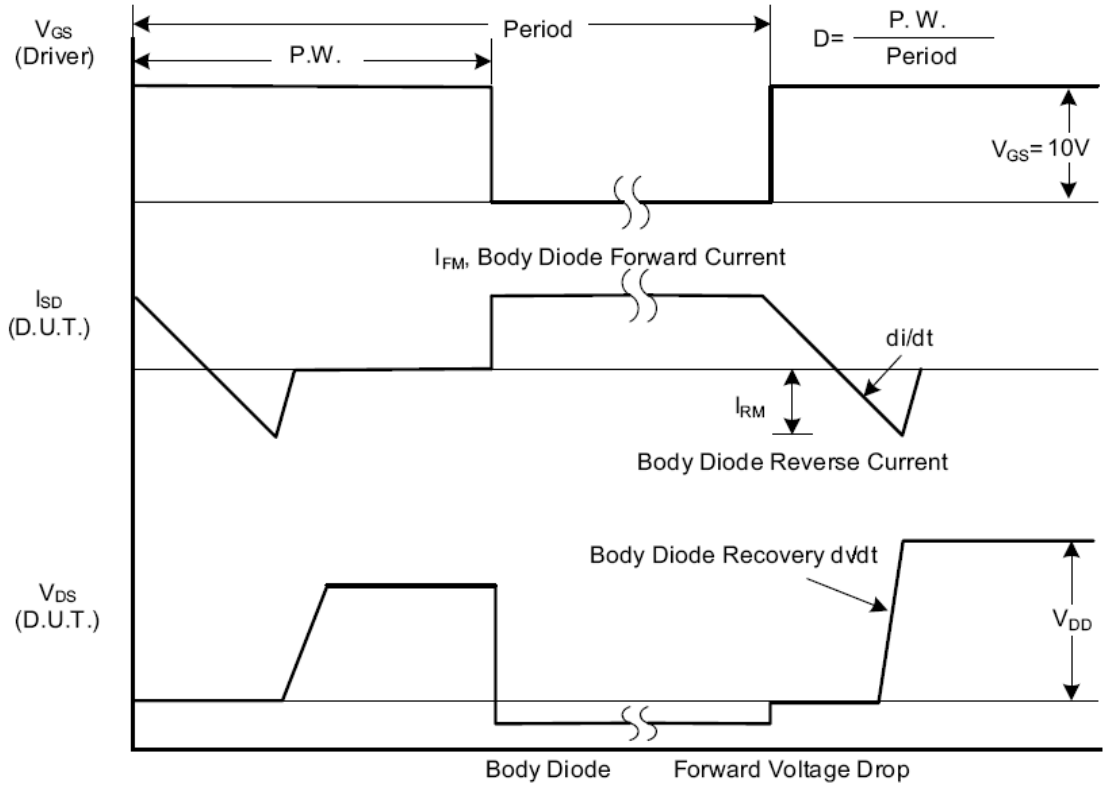


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

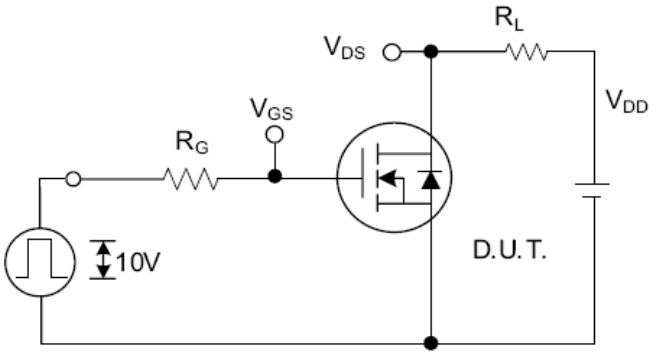


Fig. 2.1 Switching Test Circuit

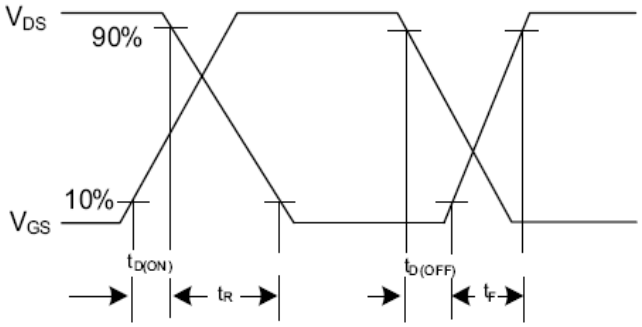


Fig. 2.2 Switching Waveforms

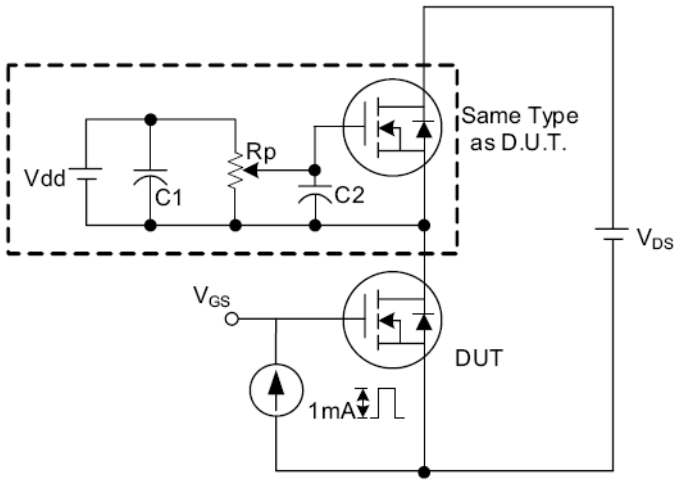


Fig. 3 . 1 Gate Charge Test Circuit

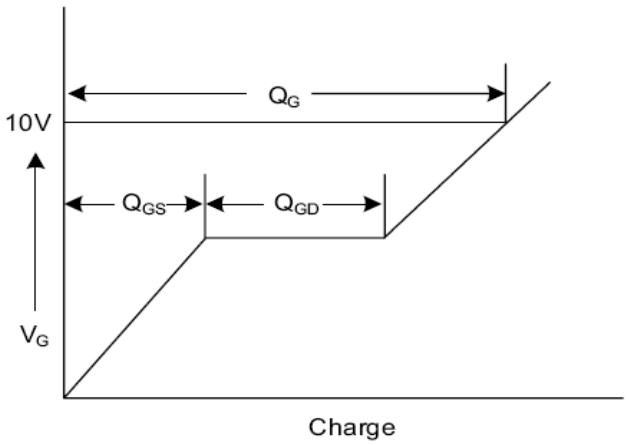


Fig. 3 . 2 Gate Charge Waveform

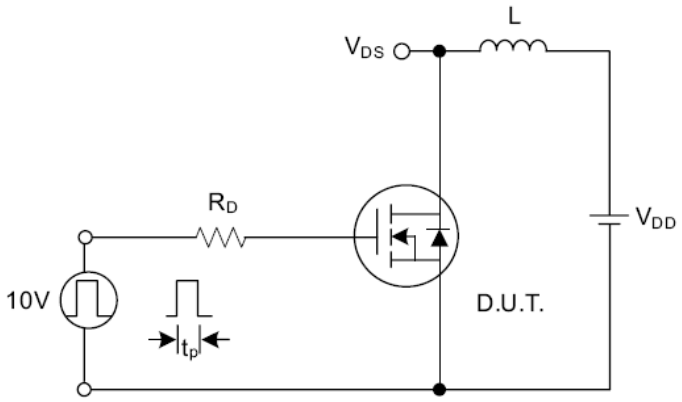


Fig. 4.1 Unclamped Inductive Switching Test Circuit

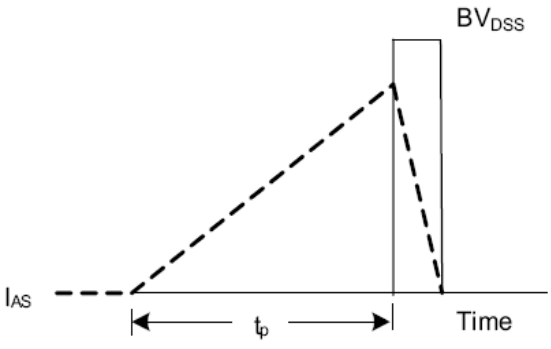


Fig. 4.2 Unclamped Inductive Switching Waveforms

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