

80V N-Channel MOSFET

General Features

- Proprietary New Trench Technology
- ightharpoonup R_{DS(ON),typ.}=4.8 m Ω @V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

Applications

- ➤ High efficiency DC/DC Converters
- Synchronous Rectification
- ▶ UPS Inverter

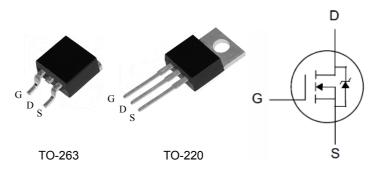
Ordering Information

Part Number	Package	Brand							
PTP14508E	TO-220	ĭ							
PTB14508E	TO-263	i							

Pb

Lead Free Package

BV _{DSS}	R _{DS(ON),typ.}	I _D ^[2]
V08	$4.8 m\Omega$	145A



Package Not to Scale

Absolute Maximum Ratings

 T_C =25 $^{\circ}$ C unless otherwise specified

Symbol	Parameter	PTB14508E	PTP14508E	Unit	
V _{DSS}	Drain-to-Source Voltage ^[1]	8	0	V	
V_{GSS}	Gate-to-Source Voltage	±2	20	V	
I _D	Continuous Drain Current ^[2]	14	15		
I _{D @ Tc =100} ℃	Continuous Drain Current @ Tc=100℃ ^[2]	10	00	Α	
I _{DM}	Pulsed Drain Current at V _{GS} =10V ^[2,4]	58	30		
E _{AS}	Single Pulse Avalanche Energy	1200		mJ	
dv/dt	Peak Diode Recovery dv/dt[3]	5.0		V/ns	
D	Power Dissipation	27	73	W	
P_D	Derating Factor above 25℃		1.82		
T _L T _{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260		$^{\circ}\! C$	
T _J & T _{STG}	Operating and Storage Temperature Range	-55 to 175			

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	PTB14508E PTP14508E		Unit
$R_{ heta JC}$	Thermal Resistance, Junction-to-Case	0.55		
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62		° M



Electrical Characteristics

OFF Characteristics T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	80			V	V _{GS} =0V, I _D =250uA
I _{DSS} Drain-to-Source Leakage Current			1		V _{DS} =80V, V _{GS} =0V	
			100	uA	V_{DS} =64V, V_{GS} =0V, T_J =125°C	
1	Cata ta Sauraa Laakaga Current			+100	nA	V _{GS} =+20V, V _{DS} =0V
I _{GSS} Gate-to	ate-to-Source Leakage Current			-100	ПА	V _{GS} =-20V, V _{DS} =0V

ON Characteristics

T_J =25 ℃ unless otherwise specified

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
R _{DS(ON)}	Static Drain-to-Source On-Resistance		4.8	5.8	mΩ	V _{GS} =10V, I _D =24A ^[5]
V _{GS(TH)}	Gate Threshold Voltage	2.0		4.0	٧	V_{DS} = V_{GS} , I_D =250uA

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
C _{iss}	Input Capacitance		8.2		nF)
C _{rss}	Reverse Transfer Capacitance		0.30			V _{GS} =0V, V _{DS} =25V,
C _{oss}	Output Capacitance		0.42			f=1.0MH _Z
Rg	Gate Series Resistance		1.2		Ω	f=1.0MH _Z
Qg	Total Gate Charge		160			
Q _{gs}	Gate-to-Source Charge		30		nC	V_{DD} =40V, I_{D} =20A, V_{GS} =0 to 10V
Q_{gd}	Gate-to-Drain (Miller) Charge		35			

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
td(ON)	Turn-on Delay Time		25			
trise	Rise Time		45		nS	V_{DD} =40V, I_{D} =20A, V_{GS} = 10V R_{G} =2.5 Ω
td(OFF)	Turn-Off Delay Time		80			
tfall	Fall Time		30			



Source-Drain Body Diode Characteristics

Symbol	Parameter	Min	Тур.	Max.	Unit	Test Conditions
I _{SD}	Continuous Source Current ^[2]		ı	145	۸	Integral PN-diode in
I _{SM}	Pulsed Source Current ^[2]			580	Α	MOSFET
V _{SD}	Diode Forward Voltage		-	1.2	V	I _S =20A, V _{GS} =0V
trr	Reverse recovery time		50		ns	V _{GS} =0V ,I _F =20A,
Qrr	Reverse recovery charge		100		nC	dir/dt=100A/μs

Note:

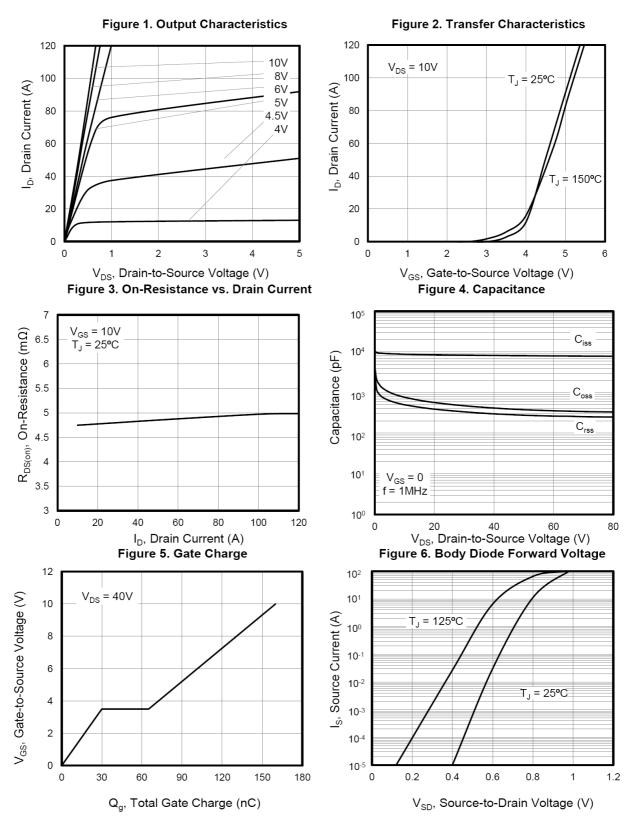
^[1] T_J=+25℃ to +175℃

^[2] Silicon limited current only. [3] Package limited current 80A

^[4] Repetitive rating; pulse width limited by maximum junction temperature. [5] Pulse width≤380µs; duty cycle≤2%.



Typical Characteristics





Typical Characteristics(Cont.)

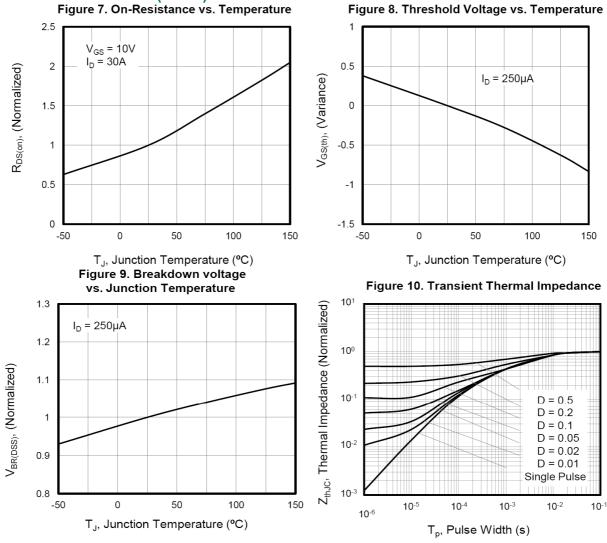


Figure 11. Safe operation area for 10³ 102 I_D, Drain Current(A) 10¹ 100 = 10us = 100us 10-= 1ms 10ms 10-2 10⁻² 10-1 **10**0 10¹ 10² 10³ V_{DS}, Drain-Source Voltage(V)



Test Circuits and Waveforms

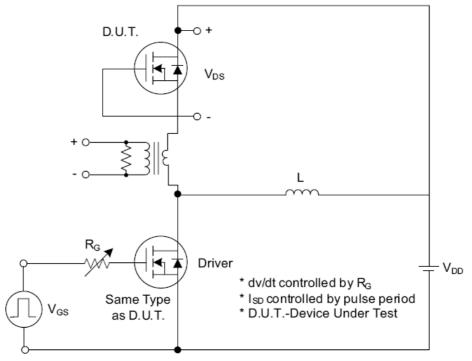


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

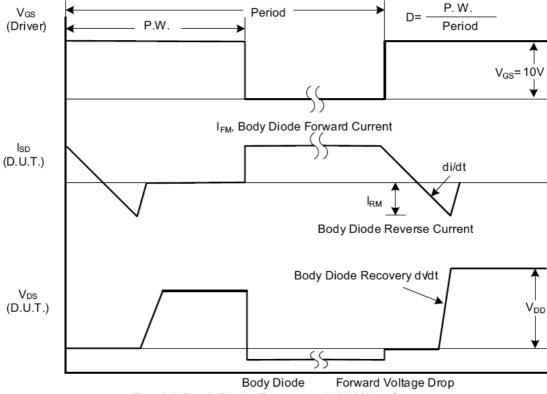


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms



Test Circuits and Waveforms (Cont.)

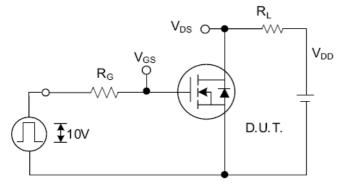


Fig. 2.1 Switching Test Circuit

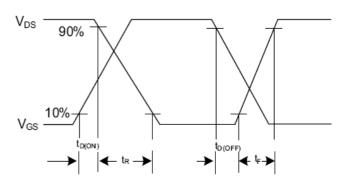


Fig. 2.2 Switching Waveforms

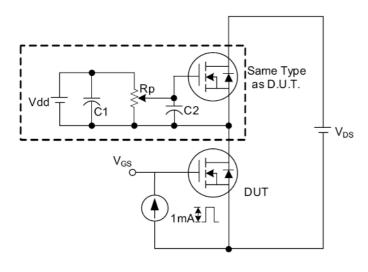


Fig. 3 . 1 Gate Charge Test Circuit

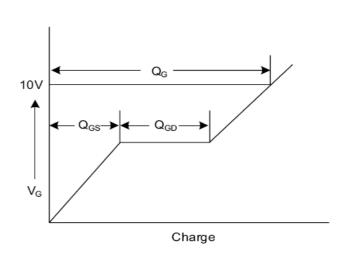


Fig. 3.2 Gate Charge Waveform

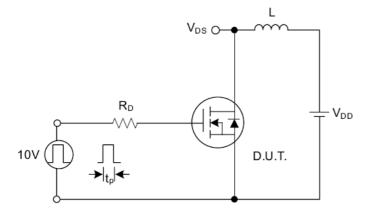


Fig. 4.1 Unclamped Inductive Switching Test Circuit

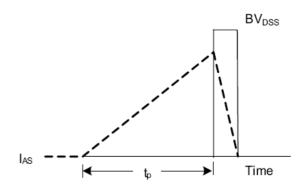


Fig. 4.2 Unclamped Inductive Switching Waveforms



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