20V N-Channel MOSFET

Lead Free Package and Finish

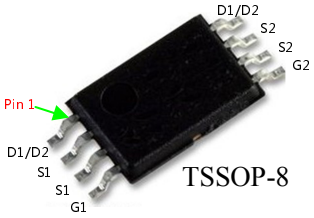
General Features

- Proprietary New Trench Technology
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

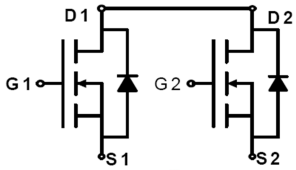
BV_{DSS}	$R_{DS(ON),max.m\Omega}$	$R_{DS(ON),typ.m\Omega}$	Test Conditions	I_D
20V	20	16	V_{GS}=10V, I_D=5.0A	7A
	22	18	V_{GS}=4.5V, I_D=4.5A	
	28	22	V_{GS}=2.5V, I_D=3.0A	

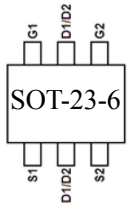
Applications

- High efficiency DC/DC Converters
- Motor Bridge Switch
- Oring FET/Load Switching



TSSOP-8





TSSOP-8 & SOT-23-6 Definition and Inner Circuit

Ordering Information

Part Number	Package	Marking	Brand
PIP8205-S8	TSSOP-8	8205	
PIP8205-Z6	SOT-23-6	8205	

Absolute Maximum Ratings T_C=25℃ unless otherwise specified

Symbol	Parameter	8205	Unit
V_{DSS}	Drain-to-Source Voltage[1]	20	V
V_{GSS}	Gate-to-Source Voltage	±12	
I_D	Continuous Drain Current T_A=25℃	7.0	A
I_{DM}	Pulsed Drain Current at V_{GS}=10V	28	
Pd	Power Dissipation T_A=25℃	1.5	W
T_L T_{PAK}	Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds	300 260	℃
T_J& T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	8205	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	110	℃/W

Electrical Characteristics

OFF Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	20	--	--	V	V_{GS}=0V, I_D=250uA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	uA	V_{DS}=20V, V_{GS}=0V
		--	--	100		V_{DS}=16V, V_{GS}=0V, T_J=125 ℃
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	V_{GS}=+12V, V_{DS}=0V
		--	--	-100		V_{GS}=-12V, V_{DS}=0V

ON Characteristics

T_J =25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	16	20	mΩ	V_{GS}=10V, I_D=5.0A
		--	18	22		V_{GS}=4.5V, I_D=4.5A
		--	22	28		V_{GS}=2.5V, I_D=3.0A
$V_{GS(TH)}$	Gate Threshold Voltage	0.5	--	1.0	V	V_{DS}=V_{GS}, I_D=250uA

Dynamic Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	900	--	pF	V_{GS}=0V, V_{DS}=10V, f=1.0MHz
C_{rss}	Reverse Transfer Capacitance	--	100	--		
C_{oss}	Output Capacitance	--	220	--		
Q_g	Total Gate Charge	--	12	--	nC	V_{DD}=10V, I_D=6A, Vgs=4.5V
Q_{gs}	Gate-to-Source Charge	--	2.3	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	1	--		

Resistive Switching Characteristics

Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	10	--	nS	V_{DD}=10V V_{GS}= 4.5V I_D=6A, R_G=6.0Ω
t_{rise}	Rise Time	--	11	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	35	--		
t_{fall}	Fall Time	--	30	--		

Source-Drain Body Diode Characteristics

T_J=25℃ unless otherwise specified

Symbol	Parameter	Min	Typ.	Max.	Unit	Test Conditions
I_{SD}	Continuous Source Current	--	--	7	A	Integral PN-diode in MOSFET
I_{SM}	Pulsed Source Current	--	--	28		
V_{SD}	Diode Forward Voltage	--	--	1.2	V	I_S=6A, V_{GS}=0V

Note:

[1] T_J=+25℃ to +150℃ .
[2] Silicon limited current only.
[3] Package limited current.
[4] Repetitive rating; pulse width limited by maximum junction temperature.
[5] Pulse width≤380μs; duty cycle≤2%.

Typical Characteristics

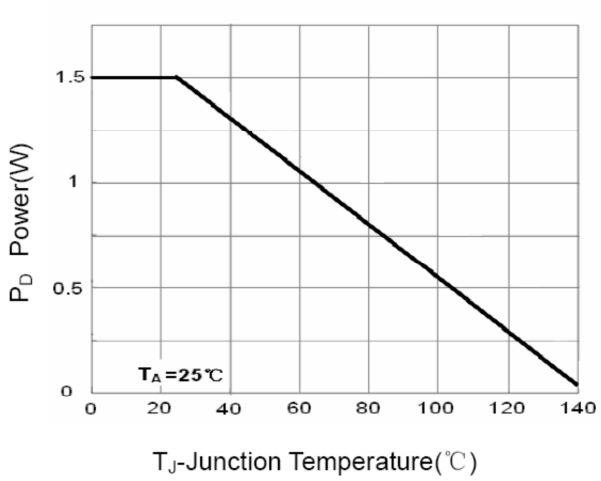


Figure 1 Power Dissipation

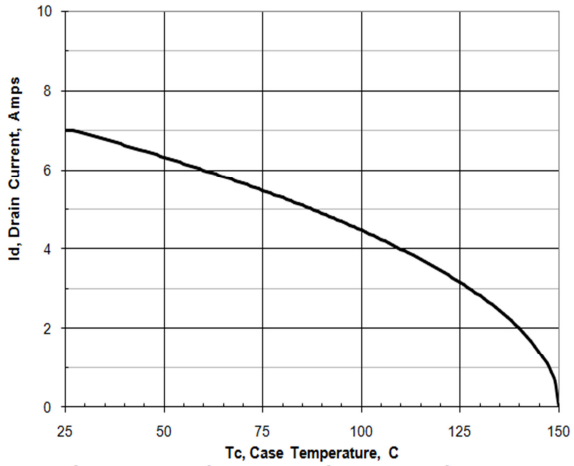


Figure 2 .Maximum Continuous Drain Current vs Case Temperature

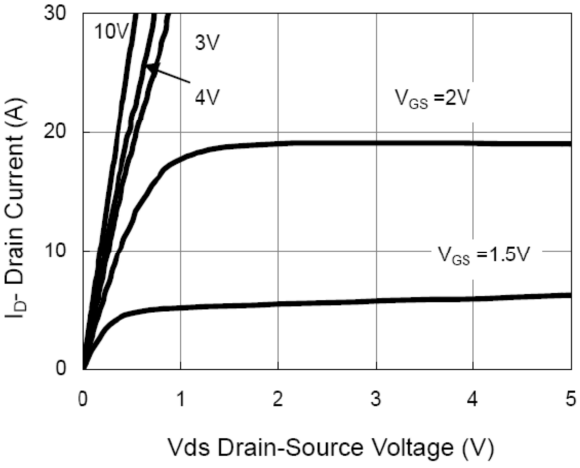


Figure 3 Output Characteristics

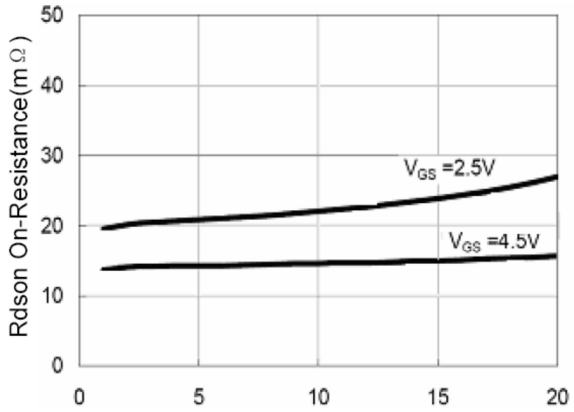


Figure 4 Drain-Source On-Resistance

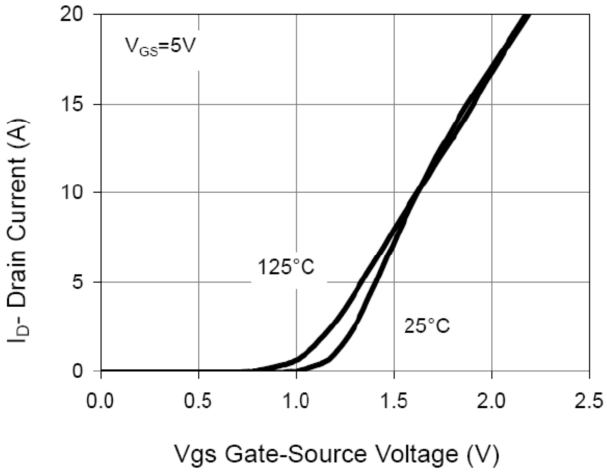


Figure 5 Transfer Characteristics

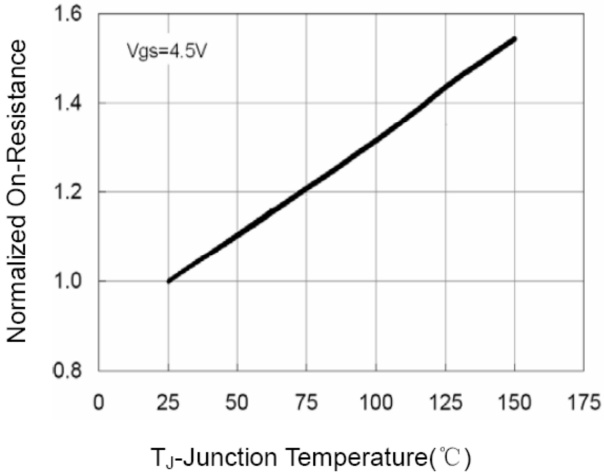


Figure 6 Drain-Source On-Resistance

Typical Characteristics

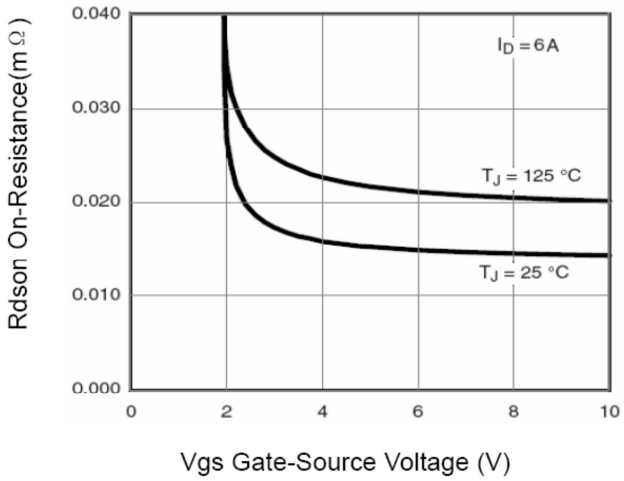


Figure 7 Rdson vs Vgs

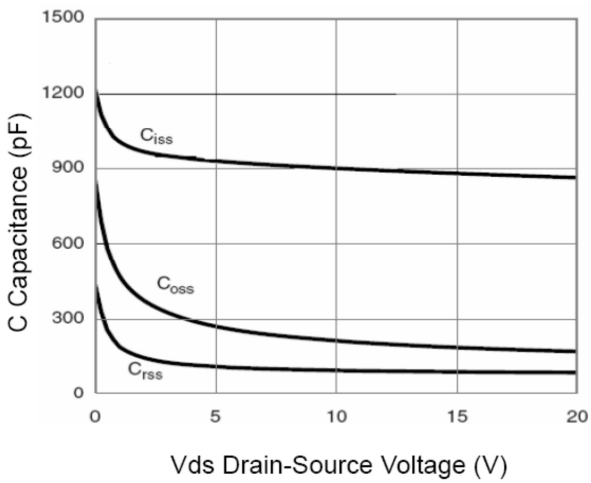


Figure 8 Capacitance vs Vds

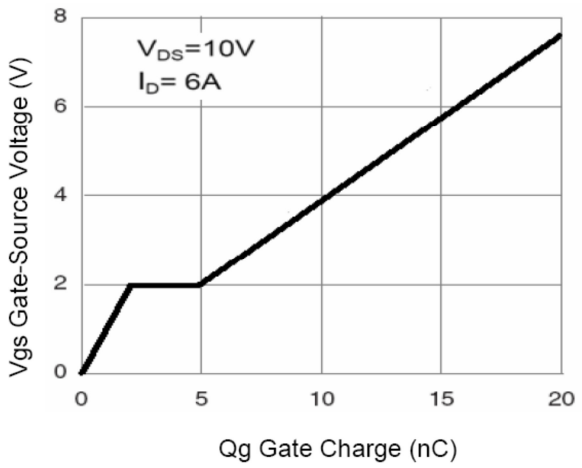


Figure 9 Gate Charge

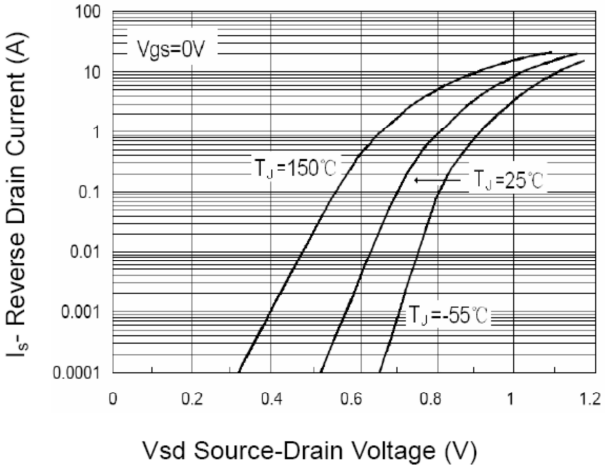


Figure 10 Source- Drain Diode Forward

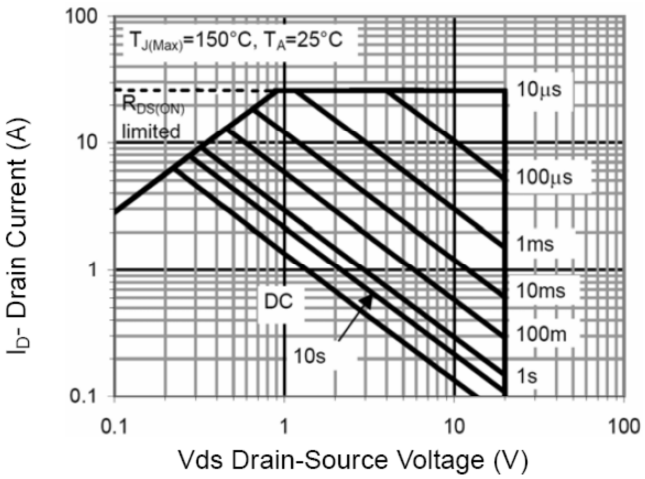


Figure 11 Safe Operation Area

Typical Characteristics

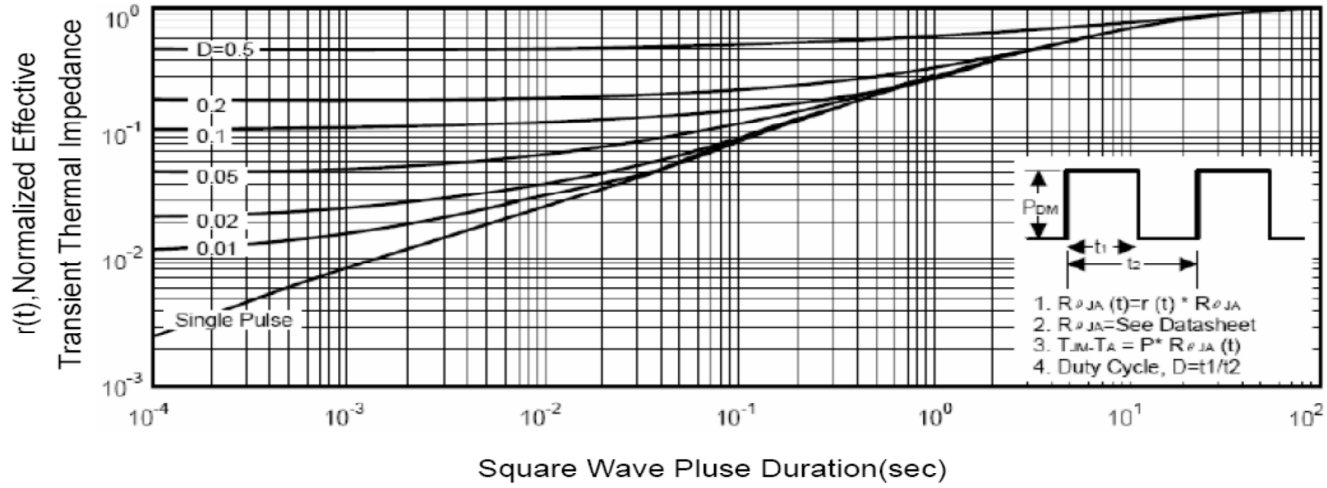


Figure 12 Normalized Maximum Transient Thermal Impedance

Test Circuits and Waveforms

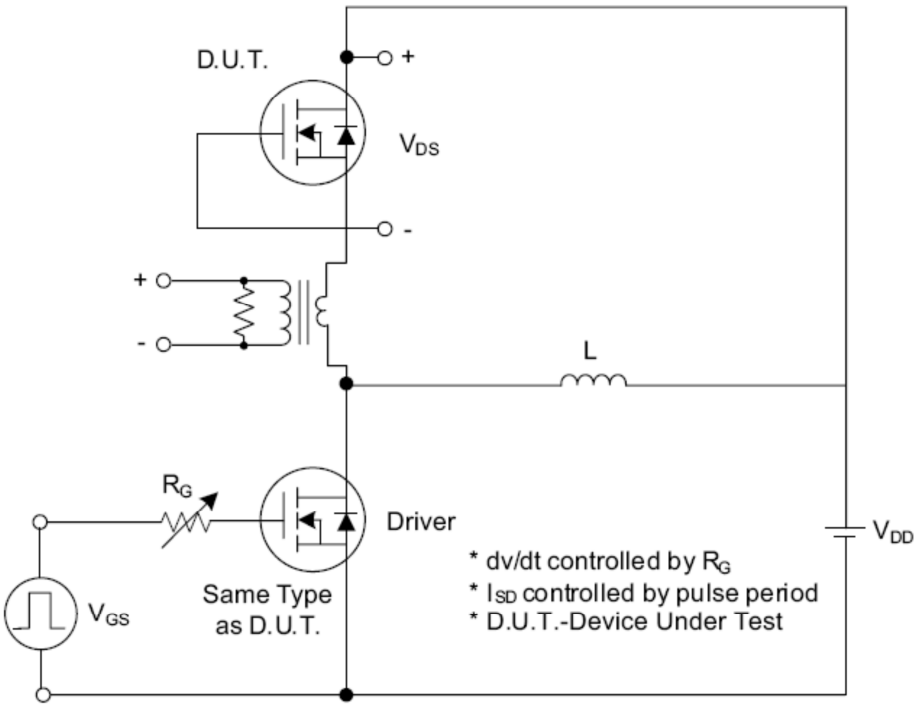


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

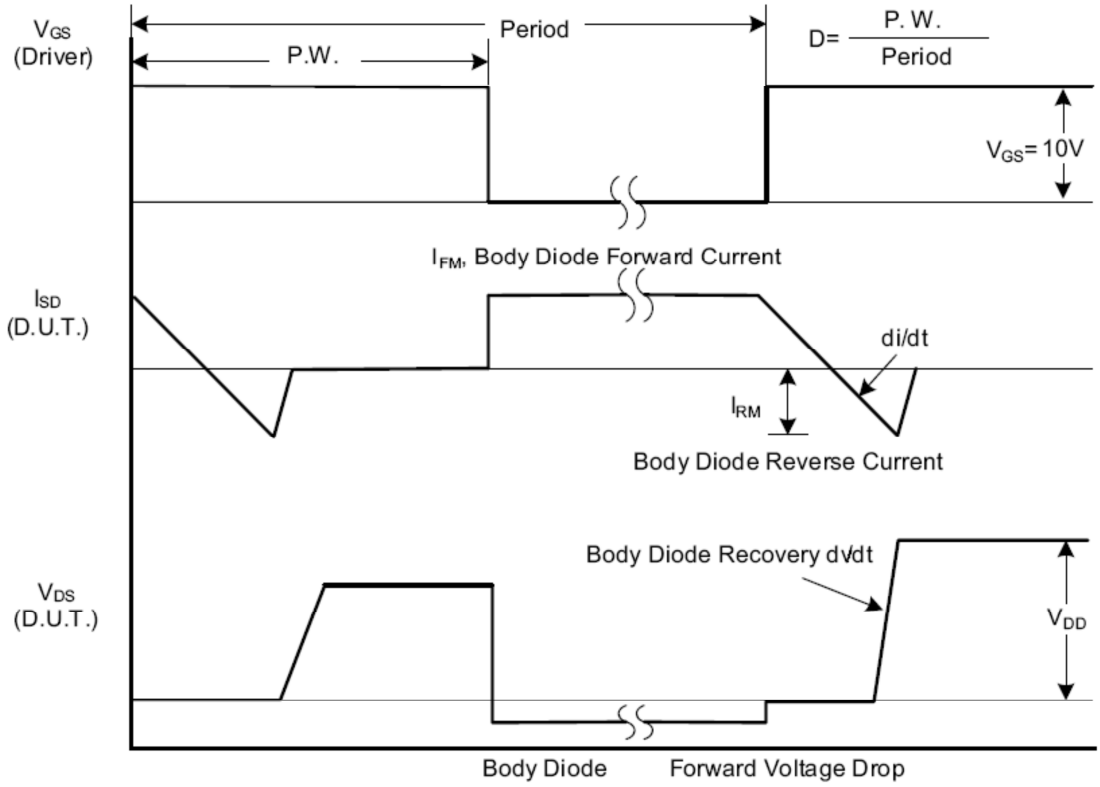


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

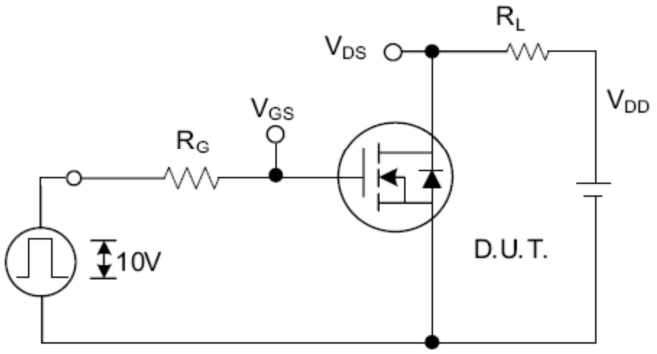


Fig. 2.1 Switching Test Circuit

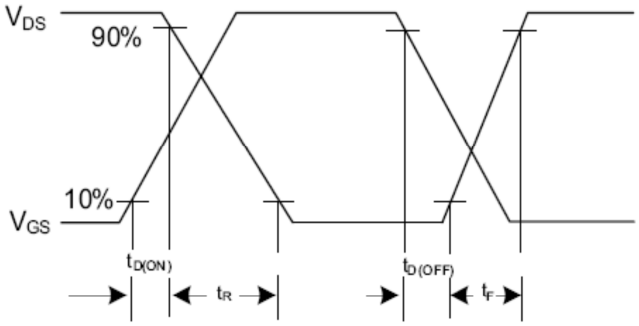


Fig. 2.2 Switching Waveforms

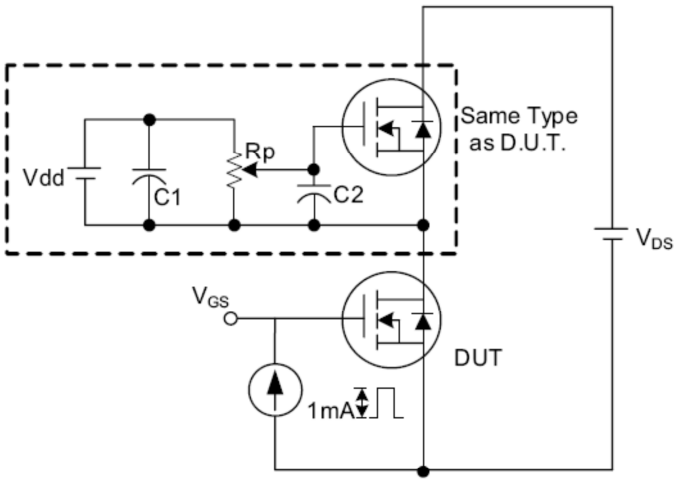


Fig. 3 . 1 Gate Charge Test Circuit

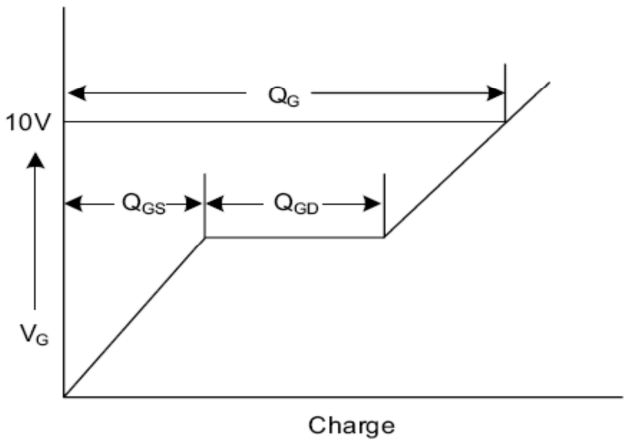


Fig. 3 . 2 Gate Charge Waveform

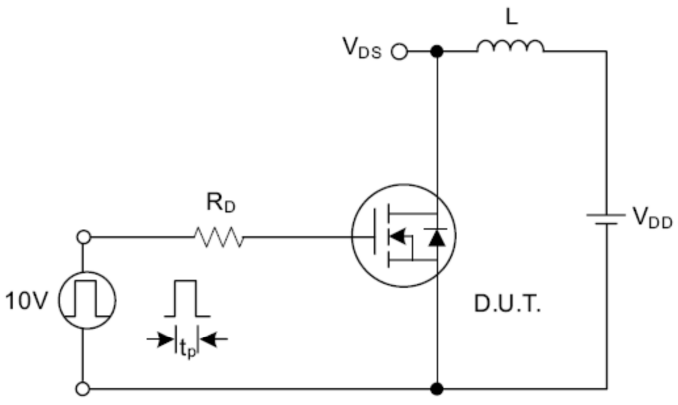


Fig. 4.1 Unclamped Inductive Switching Test Circuit

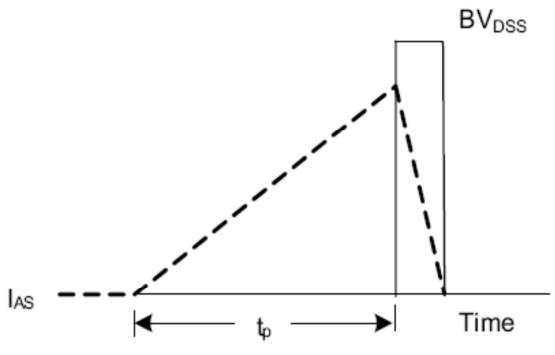


Fig. 4.2 Unclamped Inductive Switching Waveforms

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