10-Channel Level-Shift with Charge Sharing for GOP Panel

General Description

The LP6297A is a 8-CH high voltage level shifter for TV and monitor LCD applications. It converts logic level signals from Timing Controller (T-CON) to high level signals used by the LCD panel.

The outputs are switching from VGL to VGH, with capacitive loads up to 5nF.

The LP6297A also generates reset function. Once XAO reaches reset level, DIS1 and DIS2 will pulled to VGH.

Other features include thermal shutdown protection and under-voltage lockout (UVLO). The LP6297A is available in QFN-28(0.4mm pitch) package.

Features

- -20V to 40V High Output Level
- High Output Slew Rate to Drive Up to 5nF Load
- Over Temperature Protection
- Available in QFN-28 (4x4mm)
- RoHS Compliant and Halogen Free
- Pb-Free Package

Applications

- TFT for NB Using GOP/IPS Technology
- TFT for Monitors Using GOP/IPS Technology
- TFT for TV Using GOP/IPS Technology

Order Information

LP6297A □□□
- F: Green
- Package Type
  - QV: QFN-28

Marking Information

Device	Marking	Package	Shipping
LP6297A	LPS LP6297A YWX	QFN-28	3K/REEL
Y: Y is year code. W: W is week code. X: X is series number.			

Typical Application Circuit

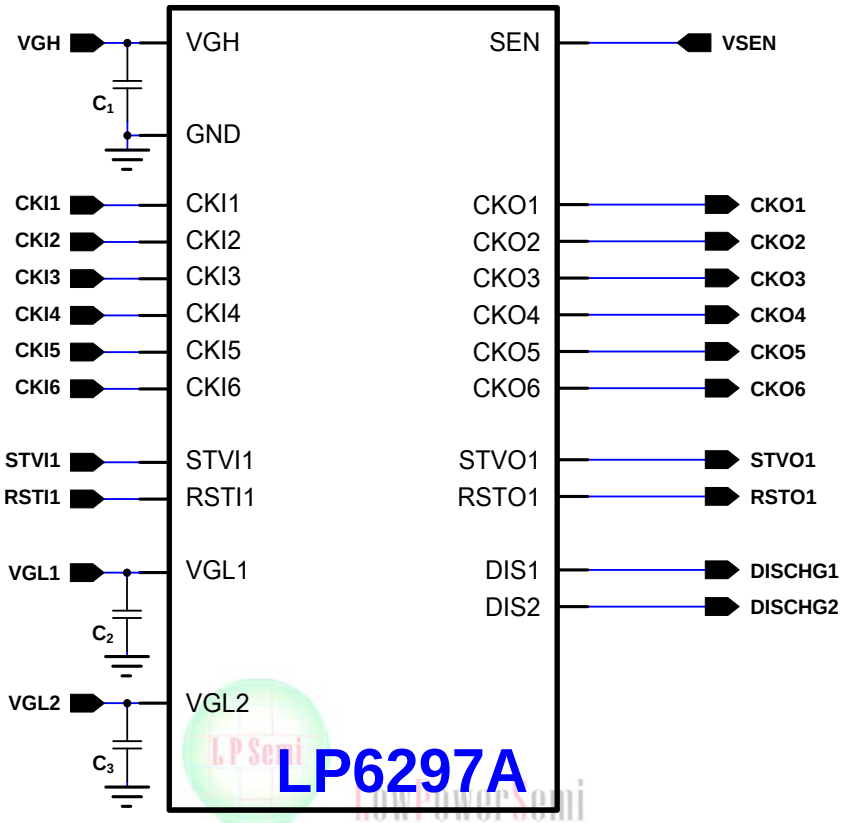


Figure 1. Typical Application Circuit of LP6297A

Pin Configuration

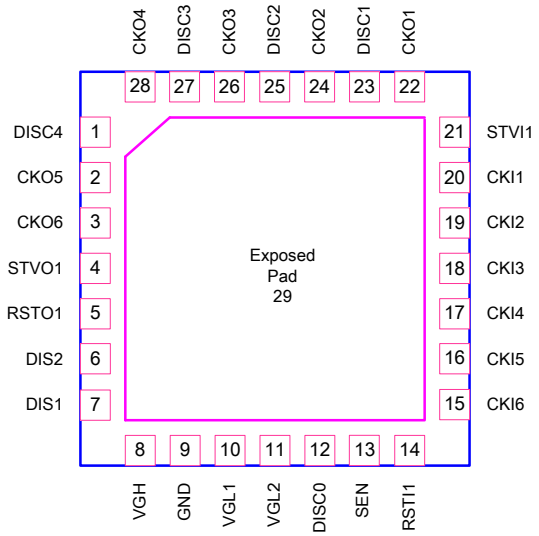


Figure 2. QFN-28 Package (4mm x 4mm) Top View of LP6297A

Function Block Diagram

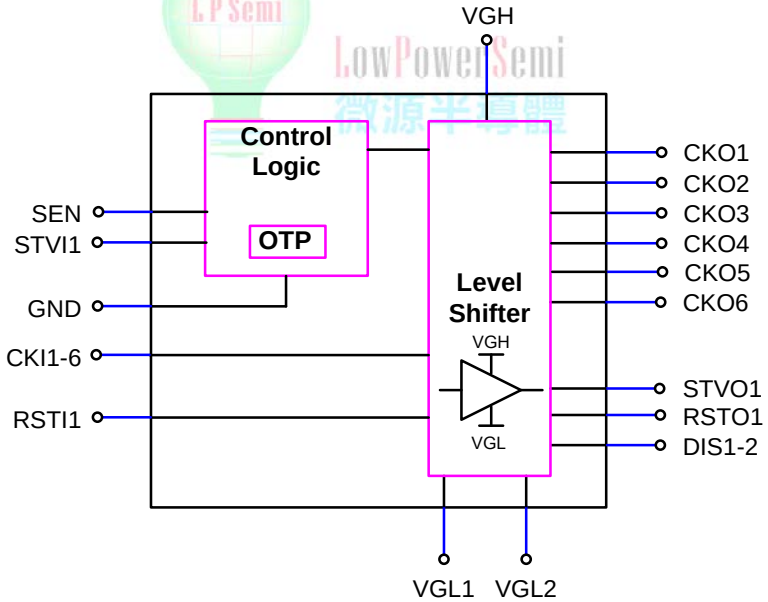


Figure 3. Function Block Diagram

Functional Pin Description

Pin NO.	Pin Name	Description
1	DISC4	Disconnected pin.
2	CKO5	Level shifter output.
3	CKO6	Level shifter output.
4	STVO1	Level shifter output.
5	RSTO1	Level shifter output.
6	DIS2	Discharge output.
7	DIS1	Discharge output.
8	VGH	Positive high supply. Connect this pin with 2.2uF ceramic capacitor to GND.
9	GND	Ground.
10	VGL1	Negative low supply 1. Connect this pin with 2.2uF ceramic capacitor to GND.
11	VGL2	Negative low supply 2. Connect this pin with 2.2uF ceramic capacitor to GND.
12	DISC0	Disconnected pin.
13	SEN	Sense Voltage pin.
14	RSTI1	Level shifter input. Internal pull-down resistance.
15	CKI6	Level shifter input. Internal pull-down resistance.
16	CKI5	Level shifter input. Internal pull-down resistance.
17	CKI4	Level shifter input. Internal pull-down resistance.
18	CKI3	Level shifter input. Internal pull-down resistance.
19	CKI2	Level shifter input. Internal pull-down resistance.
20	CKI1	Level shifter input. Internal pull-down resistance.
21	STVI1	Level shifter input. Internal pull-down resistance.
22	CKO1	Level shifter output.
23	DISC1	Disconnected pin.
24	CKO2	Level shifter output.
25	DISC2	Disconnected pin.
26	CKO3	Level shifter output.
27	DISC3	Disconnected pin.
28	CKO4	Level shifter output.
EP		Connect to VGL1. The copper area of the ground plane must be large enough to ensure adequate thermal performance.

Absolute Maximum Ratings Note 1

- ✧ STVI1, RSTI1, SEN, to GND ---------- −0.3V to +7V
- ✧ CKI1, CKI2, CKI3, CKI4, CKI5, CKI6 to GND ---------- −0.3V to +7V
- ✧ VGH to GND ---------- −0.3V to +45V
- ✧ VGL1, VGL2 to GND ---------- −20V to +0.3V
- ✧ CKO1, CKO2, CKO3, CKO4, CKO5, CKO6 to VGL1 ---------- −0.3V to +60V
- ✧ DIS1, STVO1, RSTO1 to VGL1 ---------- −0.3V to +60V
- ✧ DIS2 to VGL2 ---------- −0.3V to +60V
- ✧ Operating Junction Temperature Range (T_J) ---------- −40°C to +150°C
- ✧ Operation Ambient Temperature Range ---------- −40°C to +85°C
- ✧ Storage Temperature Range ---------- −65°C to +150°C
- ✧ Maximum Soldering Temperature (at leads, 10sec) ---------- +260°C
- ✧ Maximum Junction Temperature ---------- +150°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

- ✧ Thermal Resistance

  QFN-28 4x4, θ_{JA} ---------- 50.8°C/W

  QFN-28 4x4, θ_{JC} ---------- 19.7°C/W

Electrical Characteristics

V_{GH}=25V, V_{GL1}=V_{GL2}=-10V, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
General						
VGH Input Range	V_{GH}		16		45	V
VGL1,2 Input Range	$V_{GL1,2}$		-20		-3	V
Supply Current	I_{GH}	STVI1=RSTI1=CKIx=0V			1	mA
	I_{GL1}	STVI1=RSTI1=CKIx=0V	-0.5			mA
	I_{GL2}	STVI1=RSTI1=CKIx=0V	-0.5			mA
UVLO High Threshold	$V_{UVLO(H)}$	V_{GH} High Level	14	15	16	V
UVLO Low Threshold	$V_{UVLO(L)}$	V_{GH} Low Level	2	3.5	5	V
Thermal Shutdown Threshold	T_{SD}	Temperature Rising	130	150	170	°C
Level Shifters (STV1, RST1)						
Level Shifter Input Threshold	V_{IL}	STVI1, RSTI1 Falling			0.8	V
	V_{IH}	STVI1, RSTI1 Rising	2			
Pull Down Resistor	R_{PD}	STVI1, RSTI1	50	100	200	kΩ
High Side On Resistance	R_{DS_H}			30	60	Ω
Low Side On Resistance	R_{DS_L}			15	30	
Slew Rate	T_R	C_{OUT}=4.7nF, From 20% to 80%	20			V/us
	T_F	C_{OUT}=4.7nF, From 80% to 20%	30			
Propagation Delay	T_{R_dly}	C_{OUT}=150pF, V_{OUT} Rising		40	100	ns
	T_{F_dly}	C_{OUT}=150pF, V_{OUT} Falling		50	100	

Electrical Characteristics (Continued)

V_{GH}=25V, V_{GL1}=V_{GL2}=-10V, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Level Shifters (CKx)						
Level Shifter Input Threshold	V_{IL_CK}	CKIx Falling			0.8	V
	V_{IH_CK}	CKIx Rising	2			
Pull Down Resistor	R_{PD_CK}	CKIx	50	100	200	kΩ
High Side On Resistance	$R_{DS\_H\_CK}$			11	25	Ω
Low Side On Resistance	$R_{DS\_L\_CK}$			7	15	Ω
Slew Rate	T_{R_CK}	C_{OUT}=4.7nF, From 20% to 80%	50			V/us
	T_{F_CK}	C_{OUT}=4.7nF, From 80% to 20%	50			
Propagation Delay	T_{R_dly}	C_{OUT}=150pF, V_{OUT} Rising		40	100	ns
	T_{F_dly}	C_{OUT}=150pF, V_{OUT} Falling		50	100	
Discharge (DISx)						
Discharge Threshold Voltage	V_{SEN}	V_{SEN} Falling	1.14	1.2	1.26	V
Discharge Hysteresis	V_{SEN_HYS}	V_{SEN} Rising		50		mV
DIS1 High Side On Resistance	R_{DS1_H}			14	60	Ω
DIS1 Low Side On Resistance	R_{DS1_L}			3	10	Ω
DIS2 High Side On Resistance	R_{DS2_H}			14	60	Ω
DIS2 Low Side On Resistance	R_{DS2_L}			10	20	Ω

Timing Diagram-Power On/ Off Sequence

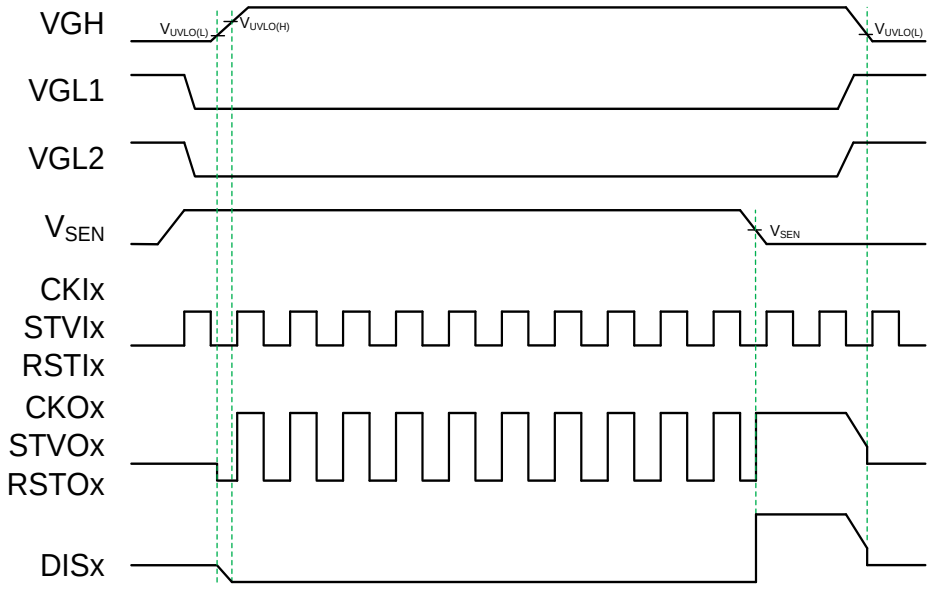


Figure 4. Power Sequence with TCON Mode

Timing Diagram-TCON Mode0

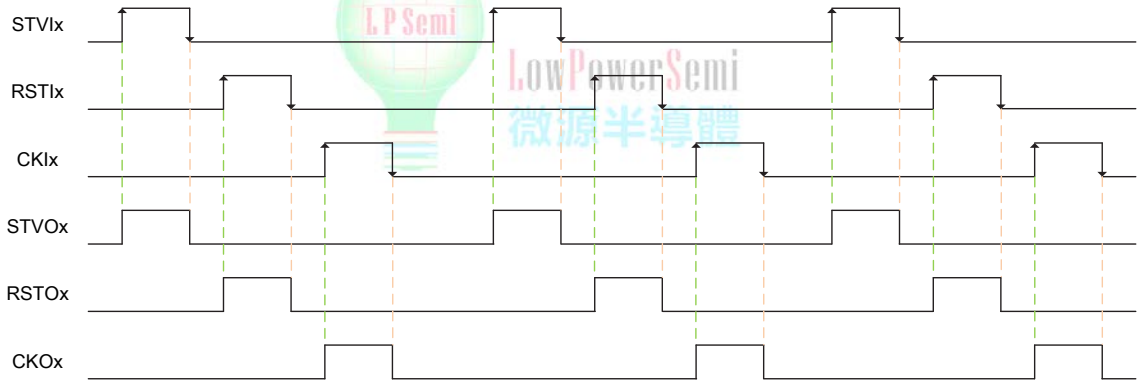


Figure 5. TCON Mode

Application Information

The LP6297A is level shifter for TFT LCD panel in GOP application. The device has six clock outputs, one STV outputs, one RST outputs. The clock output supports normal TCON application.

Under Voltage Lockout (UVLO)

The LP6297A had an UVLO internal circuit that VGH is lower than UVLO(L), the device is shutdown and all output are high-impedance. Enable the device that output follow input once the voltage on the VGH voltage exceeds the UVLO(H) threshold voltage if VSEN high level. In the case where UVLO(H) < VGH < UVLO(L), the outputs are all at VGL level.

Over Temperature Protection

The LP6297A device enters over temperature protection(OTP) if its junction temperature exceeds 150°C (Typ.). Then all the outputs will be high impedance and the IC will latch-up. VGH must be cycled to recover normal operation.

Layout Guideline

The output stages of the LP6297A are capable of sinking and sourcing high peak currents and care must be taken during PCB layout to ensure that this performance. In particular, the change of current at the rising and falling edges of each output require stray inductance to be minimized. It is easily solved by routing the output signals using short, wide PCB tracks and using a low impedance ground plane on the other side of the board to conduct return currents. Tracks between the decoupling capacitors and the corresponding power supply pins should also be keeping short and wide as possible.

1. The input capacitor should be located as closed as possible to the VGH, VGL and ground plane.

2. Minimize the distance of all traces connected to the Output node, that the traces short and wide route to obtain optimum performance.

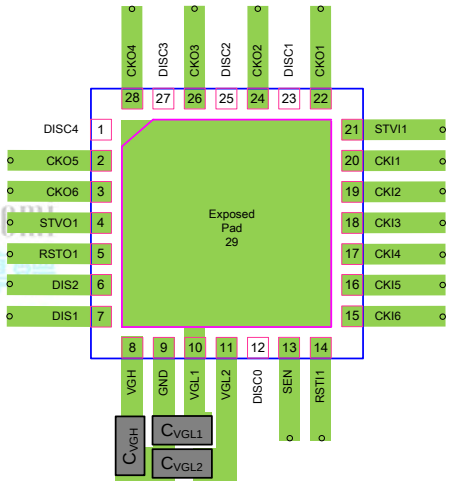
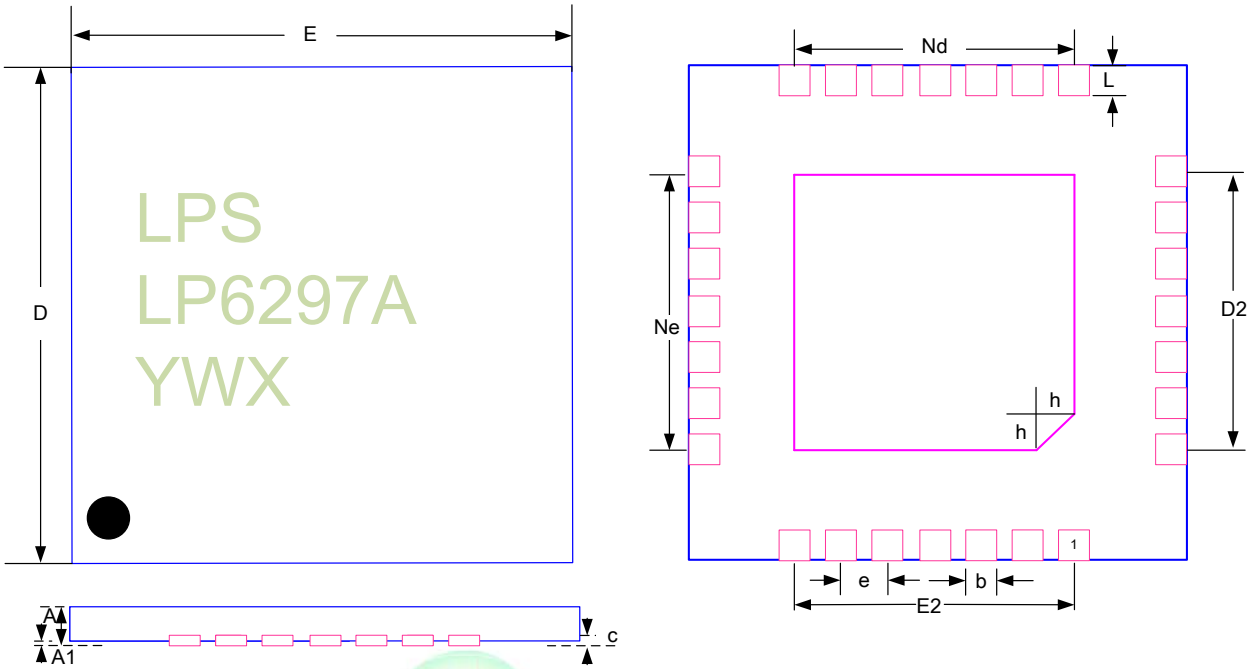


Figure 6. Recommended LP6297A PCB Layout Diagram

Outline Information

QFN-28 Package (4x4) pitch 0.4 (Unit: mm)



SYMBOL	DIMENSION IN MILLIMETER		
	MIN	NOM	MAX
A	0.700	0.750	0.800
A1	---	0.020	0.050
b	0.150	0.200	0.250
c	0.180	0.200	0.250
D	3.900	4.000	4.100
D2	2.300	2.400	2.500
E	3.900	4.000	4.100
E2	2.300	2.400	2.500
e	0.400 BSC		
Nd	2.400 BSC		
Ne	2.400 BSC		
L	0.350	0.400	0.450
h	0.300	0.350	0.400