# UTC3844D/E LINEAR INTEGRATED CIRCUIT
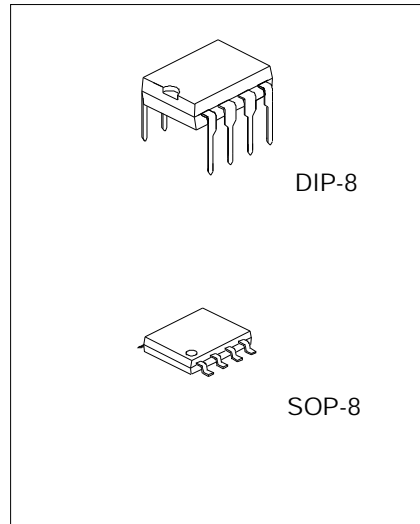
## CURRENT MODE PWM CONTROL CIRCUITS

### DESCRIPTION

The UTC3844D/E provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 0.5mA,a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control,and a totem pole output stage designed to source or sink high peak current.The output stage, suitable for driving N channel MOSFETs,is low in the off state.
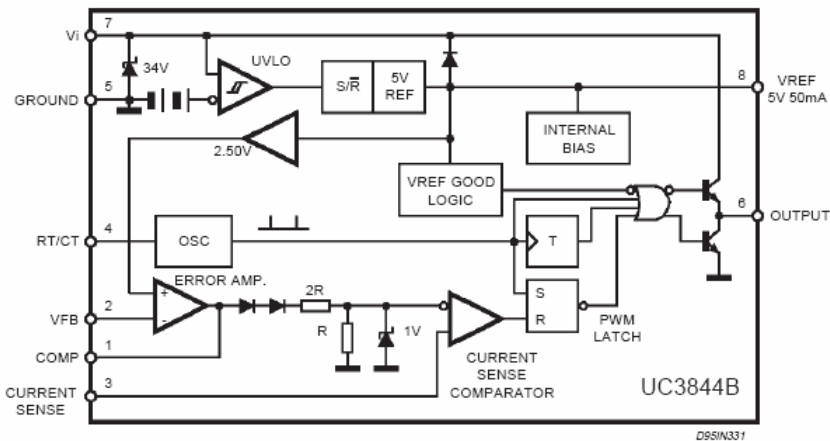
DIP-8

SOP-8

### FEATURES
*Optimized for off-line and DC to DC converts
*Low start up current(<0.5mA)
*Automatic feed forward compensation
*Pulse-by-Pulse current limiting
*Enhanced load response characteristics
*Under-voltage lockout with hysteresis
*Double pulse Suppression
*High current totem pole output
*Internally trimmed bandgap reference
*500kHz operation
*Low Ro error amp

### ORDERING INFORMATION

| Device | Package |
|--------|---------|
| UTC3844D | DIP-8-300-2.54 |
| UTC3844E | SOP-8-225-1.27 |

## BLOCK DIAGRAM

# UTC3844D/E          LINEAR INTEGRATED CIRCUIT

## ABSOLUTE MAXIMUM RATINGS(Ta=25°C)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage(Low Impedence Source) | $V_{CC}$ | 30 | V |
| Supply Voltage(Icc<30mA) | $V_{cc}$ | Self Limiting | V |
| Output Current | Io | ±1 | A |
| Output Energy(capacitive Load) | | 5 | μJ |
| Analog Inputs(pin 2,3) | $V_{I(ANA)}$ | -0.3 to +6.3 | V |
| Error Amplifier Output Sink Current | $I_{SINK(EA)}$ | 10 | mA |
| Power Dissipation | $P_D$ | at $T_{amb}$≤25°C   1.0 | W |
| Lead Temperature | Tlead | 300 | °C |
| Storage Temperature | Tstg | -65~+150 | °C |

Note 1: Ta>25°C,$P_D$ derated with 8mW/°C.

## ELECTRICAL CHARACTERISTICS

(0≤Ta≤70°C,$V_{CC}$=15V,$R_T$=10kΩ,$C_T$=3.3nF,unless otherwise specified)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Reference Section** | | | | | | |
| Output Voltage | $V_{REF}$ | Tj=25°C,Io=1mA | 4.90 | 5.00 | 5.10 | V |
| Line Regulation | $\Delta V_{REF}$ | 12≤$V_{IN}$≤25V | | 2 | 20 | mV |
| Load Regulation | $\Delta V_{REF}$ | 1≤Io=20mA | | 3 | 25 | mV |
| Temp Dtability | | (Note 2) | | 0.2 | | mV/°C |
| Total Output Variation | | Line,Load,Temp(note 2) | 4.82 | | 5.18 | μV |
| Output Noise Voltage | Vosc | 10Hz≤f≤10kHz,Tj=25°C (note 2) | | 50 | | mV |
| Long term stability | | Ta=25°C,1000Hrs(note 2) | | 5 | 25 | mV |
| Output Short Circuit | ISC | | -30 | -100 | -180 | mA |
| **Oscillator Section** | | | | | | |
| Initial Accurcy | f | Tj=25°C | 49 | 52 | 55 | kHz |
| Voltage Stability | Δf/ΔVcc | 12≤Vcc≤25V | | 0.2 | 1 | % |
| Temp stability | | Tmin≤$T_A$≤Tmax(note 2) | | 5 | | % |
| Amplitude | Vosc | Vpin 4 peak to peak | | 1.6 | | V |
| **Error Amplifier Section** | | | | | | |
| Input Voltage | $V_{I(EA)}$ | Vpin 1=2.5V | 2.42 | 2.50 | 2.58 | V |
| Input Bias current | $I_{BIAS}$ | | | -0.1 | -2 | μA |
| $A_{VOL}$ | | 2 ≤Vo≤4V | 60 | 90 | | dB |
| Unity Gain Bandwidth | | Tj=25°C (note 2) | 0.7 | 1 | | mHz |
| PSRR | | I2≤Vcc≤25V | 60 | 70 | | dB |
| Output Sink Current | Isink | Vpin 2=2.7V,Vpin 1=1.1V | 2 | 12 | | mA |
| Output Source Current | Isource | Vpin 2=2.3V,Vpin 1=5V | -0.5 | -1 | | mA |
| Vout High | $V_{OH}$ | Vpin 2=2.3V, RL=15kΩ to GND | 5 | 6.2 | | V |
| Vout Low | $V_{OL}$ | Vpin 2=2.7V,Vpin 1=1.1V | | 0.8 | 1.1 | V |
| **Current Sense section** | | | | | | |
| Gain | $G_V$ | (note 3,4) | 2.85 | 3 | 3.15 | V/V |
| Maximum Input signal | $V_{I(MAX)}$ | Vpin 1=5V( note 3) | 0.9 | 1 | 1.1 | V |
| PSRR | | 12≤Vcc≤25V | | 70 | | dB |
| Input Bias Current | $I_{BIAS}$ | | | -2 | -10 | μA |
| Delay to Output | | Vpin 3=0 to 2V | | 150 | 300 | ns |
| Output Section | | | | | | |
| Output low Level | $V_{OL}$ | Isink=20mA | | 0.1 | 0.4 | V |
| | | Isink=200mA | | 1.6 | 2.2 | V |

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(conitinued)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Output High Level | $V_{OH}$ | Isource=20mA | 13 | 13.5 | | V |
| | | Isource=200mA | 12 | 13.5 | | V |
| Rise Time | $t_R$ | Tj=25°C,CL=1nF(note 2) | | 50 | 150 | ns |
| Fall Time | $t_F$ | Tj=25°C,CL=1nF(note 2) | | 50 | 150 | ns |
| UVLO Saturation | | Vcc=5V,Isink=10mA | | 0.7 | 1.2 | V |
| **Under-Voltage Lockout Output Section** | | | | | | |
| Start Threshold | $V_{TH(ST)}$ | | 14.5 | 16 | 17.5 | V |
| Min.Operating Voltage After Turn On | $V_{OPR(min)}$ | | 8.5 | 10 | 11.5 | V |
| **PWM Section** | | | | | | |
| Maximum duty Cycle | $D_{(MAX)}$ | | 47 | 48 | 50 | % |
| Minimum Duty Cycle | $D_{(MIN)}$ | | | | 0 | % |
| **Total Standby Current** | | | | | | |
| Start-up Current | $I_{ST}$ | | | 0.3 | 0.5 | mA |
| Operating Supply Current | $I_{CC(opr)}$ | Vpin 2=Vpin 3=0V | | 12 | 17 | mA |
| Vcc Zener Voltage | $V_z$ | Icc=25mA | | 34 | | V |

note 2:These parameters,although guaranteed ,are not 100% tested in production.

note 3:Parameters measured at trip point of latch with Vpin 2=0.

note 4:Gain defined as:

$$A= \frac{\Delta Vpin\ 1}{\Delta Vpin\ 3} \quad ;0 \leq Vpin\ 3 \leq 0.8V$$

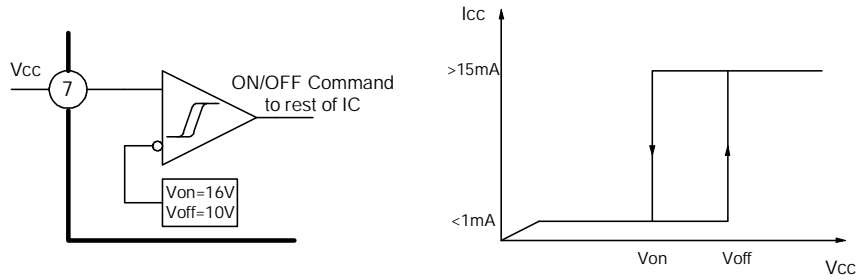note 5:Adjust Vcc above the start threshold before setting at 15V.

## OPEN-LOOP LABORATORY TEST CIRCUIT



High peak current associated with capacitive loads necessitate careful grounding techniques.Timing and bypass capacitors should be connected close to pin 5 in single point GND.The transistor and 5k$\Omega$ potentio - meter are used to sample the oscillator waveform and apply an adjustable Ramp to Pin 3.
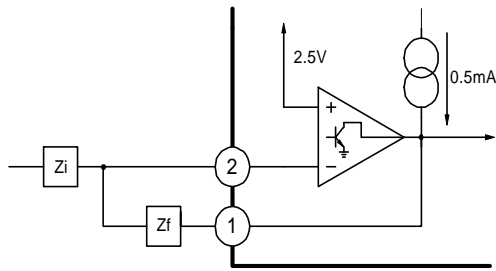
## UNDER-VOLTAGE LOCKOUT

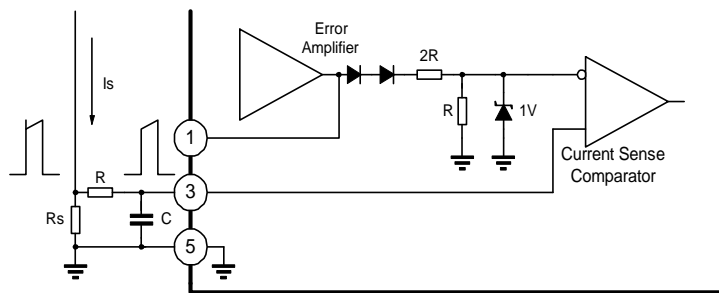During Under-Voltage Lockout, the output driver is biased to a high impedance state. Pin 6 should be shunt to GND with a bleeder resistor to prevent activating the power switch with output leakage currents.

## ERROR AMPLIFIER CONFIGURATION
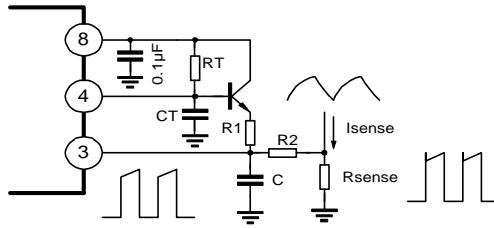
Error amplifier can source or sink up to 0.5mA

## CURRENT SENSE CIRCUIT

Peak current (Is) determined by the formula:
$$Ismax = 10V/Rs.$$
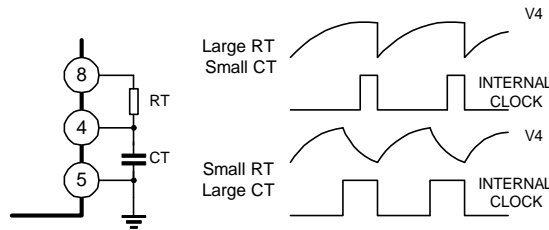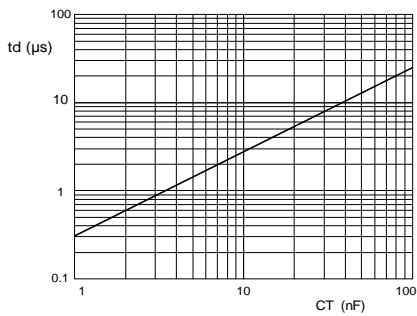A small RC filter be required to suppress switch transients.

## SLOPE COMPENSATION



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converts requiring duty cycles over 50%.Note that capacitor C, forms a filter with R2 to suppress the leading edge switch spikes.
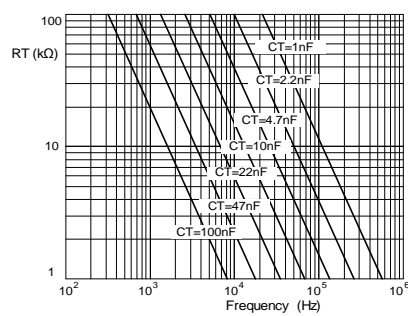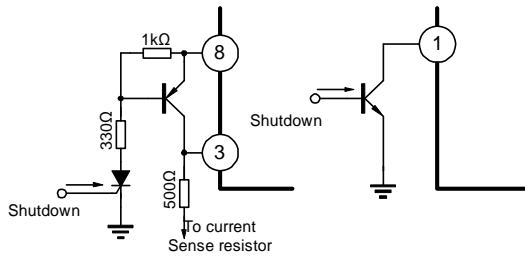
## OSCILLATOR SECTION



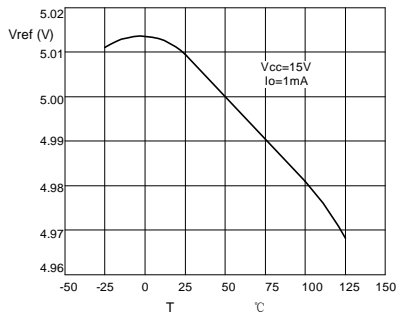Deadtime VS CT(RT>5kΩ)
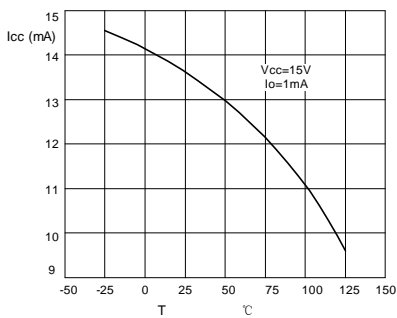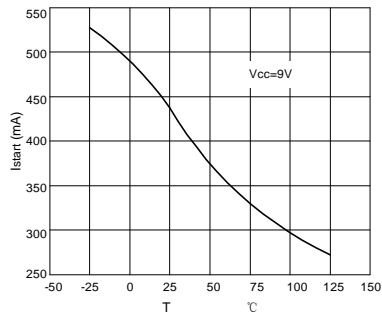


Timing Resistance Vs Frequency

## SHUTDOWN TECHNIQUES



Shutdown UTC3844D/E can be accomplished by two methods;either raise pin 3 above 1V or pull Pin 1 below a voltage two diode drops above ground.Either method caused the output of PWM comparator to be high(refer to block diagram).The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins a and/or 3 is removed .In one example, an externally latched shut - down may be accomplished by adding an SCR which be reset by cycling Vcc below the lower UVLO threshold. At this point tyhe reference turns off allowing the SCR to reset.
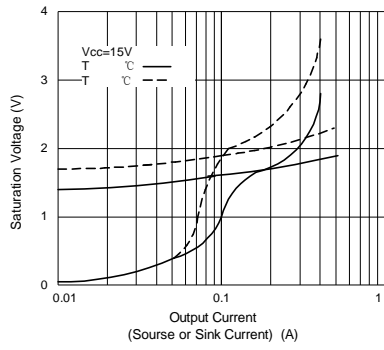
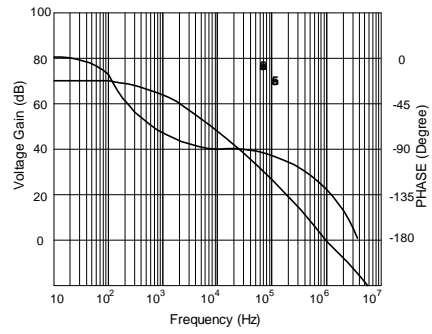## TYPICAL PERFORMANCE CHARACTERISTICS



Vref Temperature Drift



Istart Temperature Drift



Icc Temperature Drift

Output Saturation Characteristics



Error Amplifier Open-Loop
Frequency Response

# UTC3844D/E LINEAR INTEGRATED CIRCUIT

## PACKAGE DIMENSIONS

### DIP-8-300-2.54



2.54

6.35±0.25

7.62

0.25±0.05

1.52 +0.3 −0

15 degree

9.40 +0.4 −0.3

4.36MAX

0.5MIN

3.00MIN

0.46±0.08

0.89 +0.35 −0.30

### SOP-8-225-1.27



0.42

6.0±0.2

3.9±0.1

5.72

1.27

4.9±0.1

1.55±0.20