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FORESEE®

FSNAND Datasheet

FS33ND02GH2
Series

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Rev 2.5

2019-01

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Revision History:

Rev.	Date	Change	Remark
1.0	2018/02	Basic spec and architecture	
1.1	2018/07	Revise some descriptions	Spare Area (compatible)
2.0	2018/07	Revise some descriptions	Add Marketing Part Number Chart
2.4	2018/11	Revise some descriptions	Add FS33ND02GH208BFI0
2.5	2019/01	Revise some descriptions	Add Parameter page value

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1. INTRODUCTION

1.1. General Description

The FORESEE FSNAND is offered in 3.3 VCC with x8 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state application market. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data.

1.2. Flash ID

Product Family	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle
FS33ND02GH2	ADh	DAh	90h	95h	46h

1.3. Device Features

Voltage Supply
- V_{CC}: 3.3V (2.7V ~ 3.6V)

Organization
- Memory Cell Array :
  (256M + 8M) Byte or (256M + 16M) Byte
- Page Size :
  (2K + 64) Byte or (2K + 128) Byte (compatible)
- Block Erase : (128K + 4K) Byte or (128K + 8K) Byte

Automatic Program and Erase
- Page Program :
  (2K + 64) Byte or (2K+128) Byte

Page Read Operation
- Random Read: 30μs(Max.)
- Serial Access : 25ns(Min.)
- Data Transfer Rate : SDR 40Mhz

Fast Write Cycle Time
- Page Program time : 300μs(Typ.)
- Block Erase Time : 3.5ms(Typ.)

Command/Address/Data Multiplexed I/O Port
ONFI 1.0 Command Set

Hardware Data Protection
- Program/Erase Lockout During Power Transitions

Security
- OTP area
- Serial number(unique ID)
- Non-volatile protection

Operation Temperature
- Commercial Plus: -20°C to +85°C
- Industrial: -40°C to +85°C

Reliability
- Up to 100,000 P/E Cycle
- 10 Year Data retention (4bit/512byte ECC)

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1.4. Product List

[Table 1] Product List

Part Number	Density	Package Type	Organization	Package Size(mm)	VCC Range
FS33ND02GH208TFC0	2Gb	TSOP 48	x8	12*20	2.7V ~ 3.6V
FS33ND02GH208TFC1	2Gb	TSOP 48	x8	12*20	2.7V ~ 3.6V
FS33ND02GH208TFC2	2Gb	TSOP 48	x8	12*20	2.7V ~ 3.6V
FS33ND02GH208BFI0	2Gb	BGA 63	x8	9*11	2.7V ~ 3.6V

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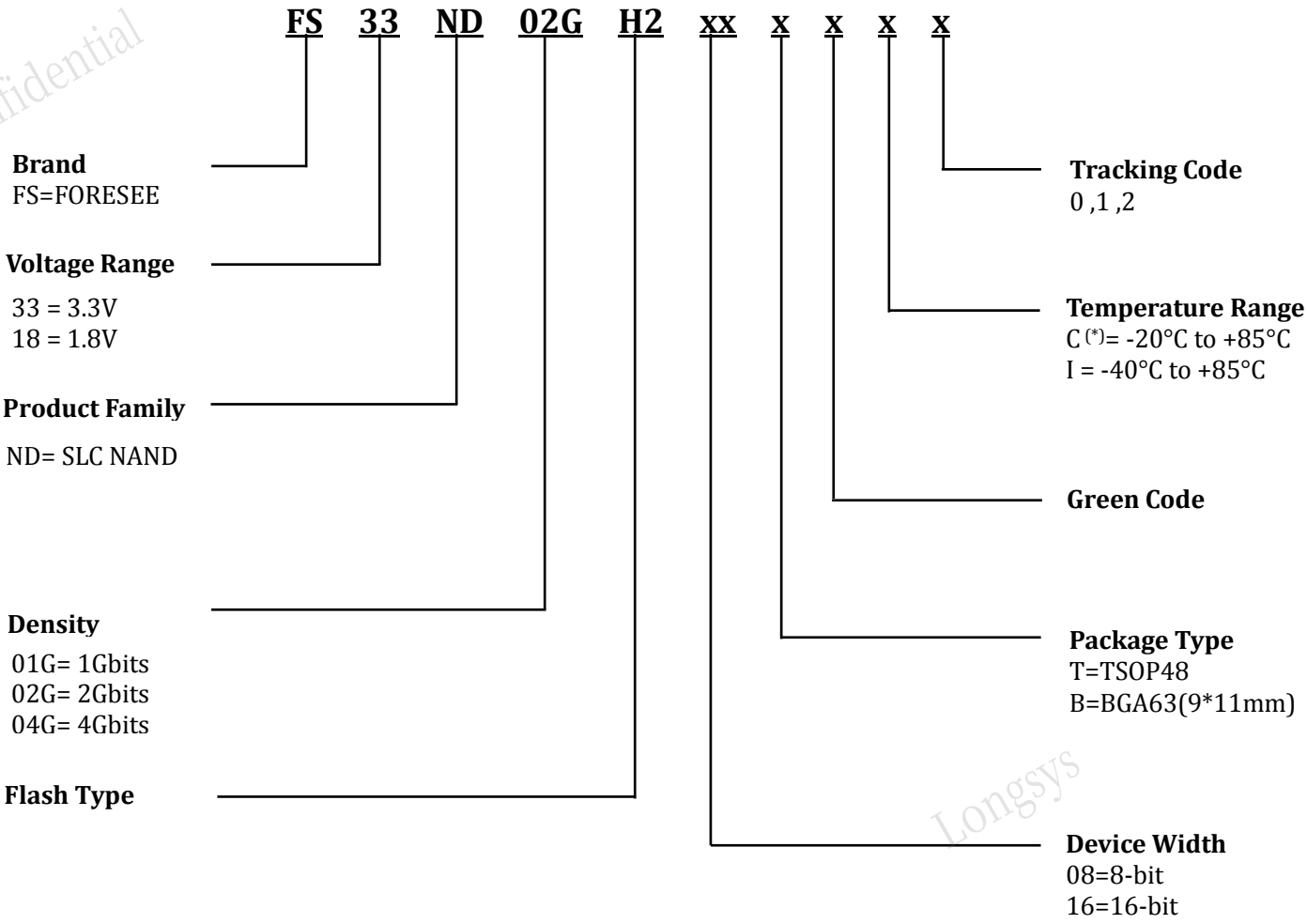
Marketing Part Number Chart



NOTE:
(*)C is Commercial Plus.

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1.5. Connection Diagram

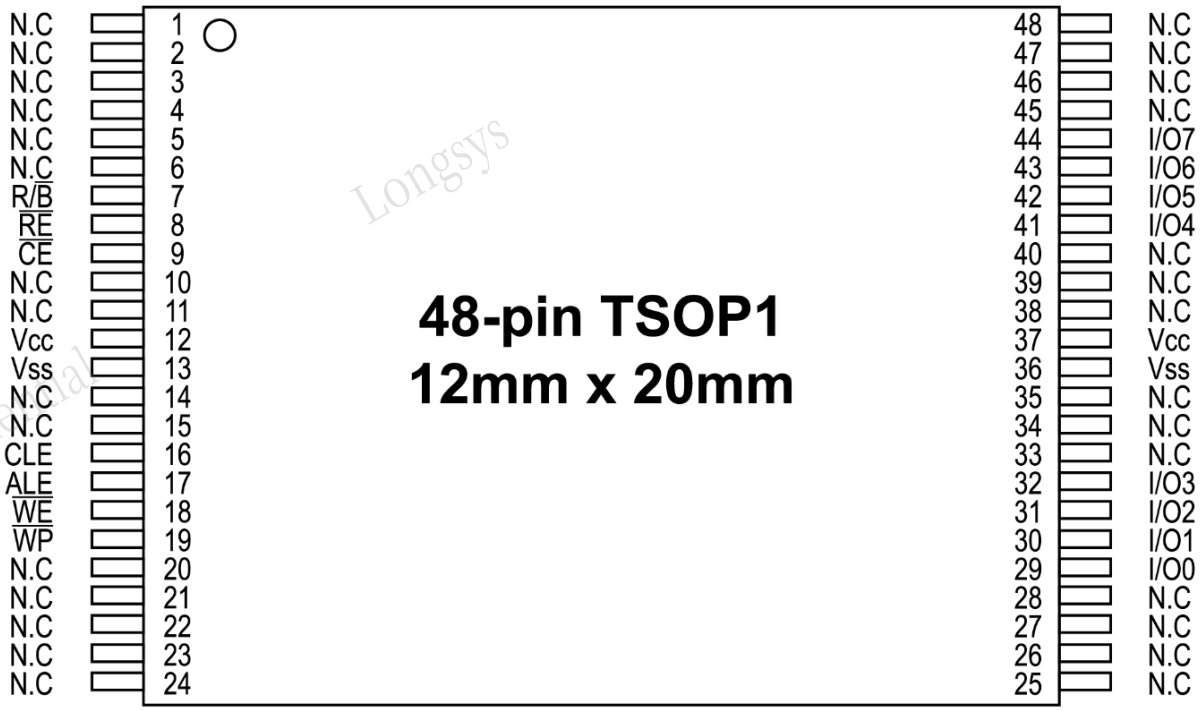

Figure 1 48-Pin TSOP1 Contact x8 Device

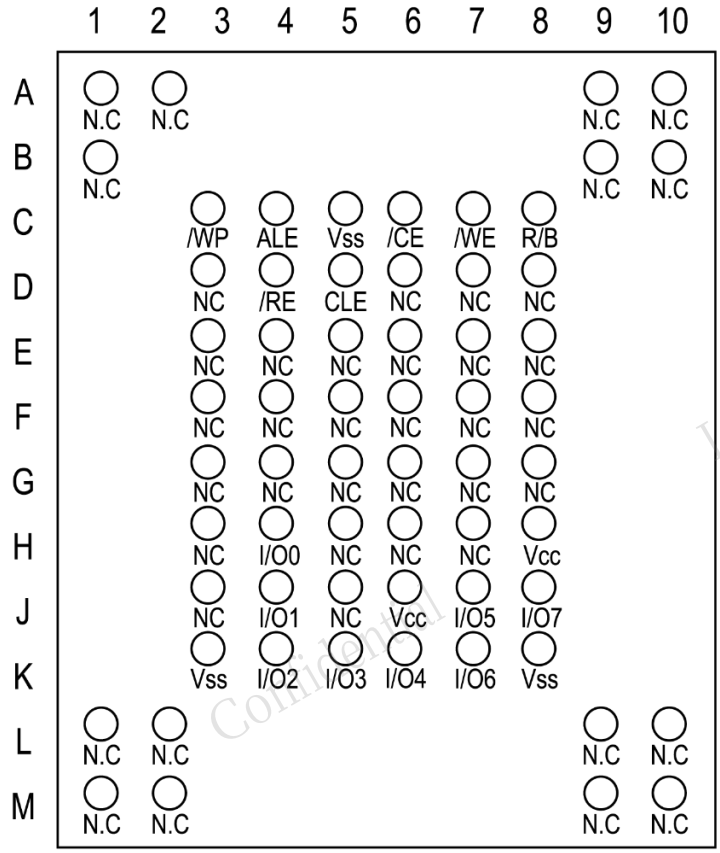

Figure 2 63-BGA Contact, x8 Device (Top View)

1.6. Pin Description

[Table 2] Pin Description

Pin Name	Pin Function
$I/O_0 \sim I/O_7$	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE# signal.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE# with ALE high.
CE#	**CHIP ENABLE** The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WE#	**WRITE ENABLE** The WE# input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	**WRITE PROTECT** The WP# pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	**READY/BUSY OUTPUT** The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER** VCC is the power supply for device.
VSS	**GROUND**
NC	**NO CONNECTION**

NOTE:
Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.
A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply.
The PCB track widths must be sufficient to carry the currents required during program and erase operations.

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1.7. System Block Diagram

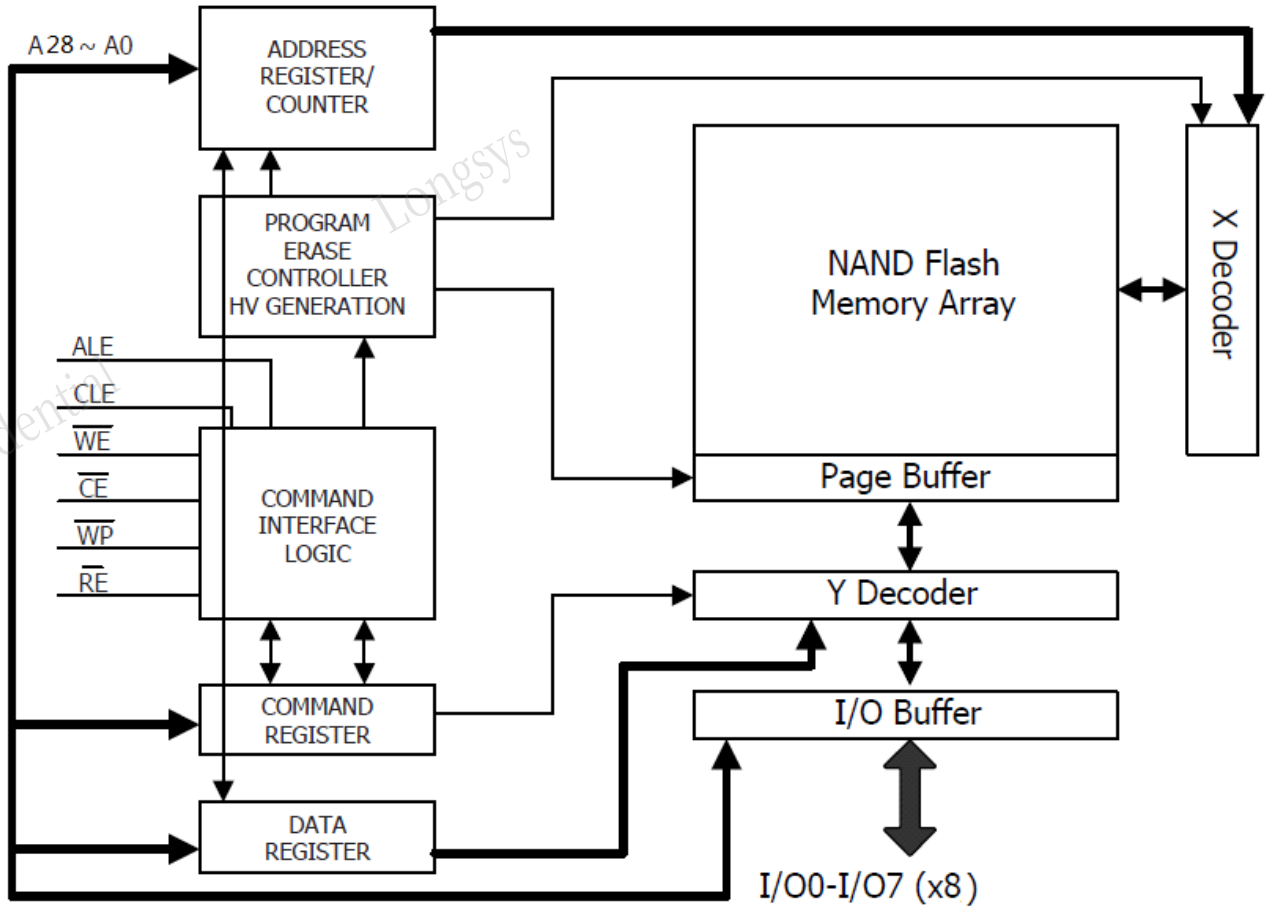
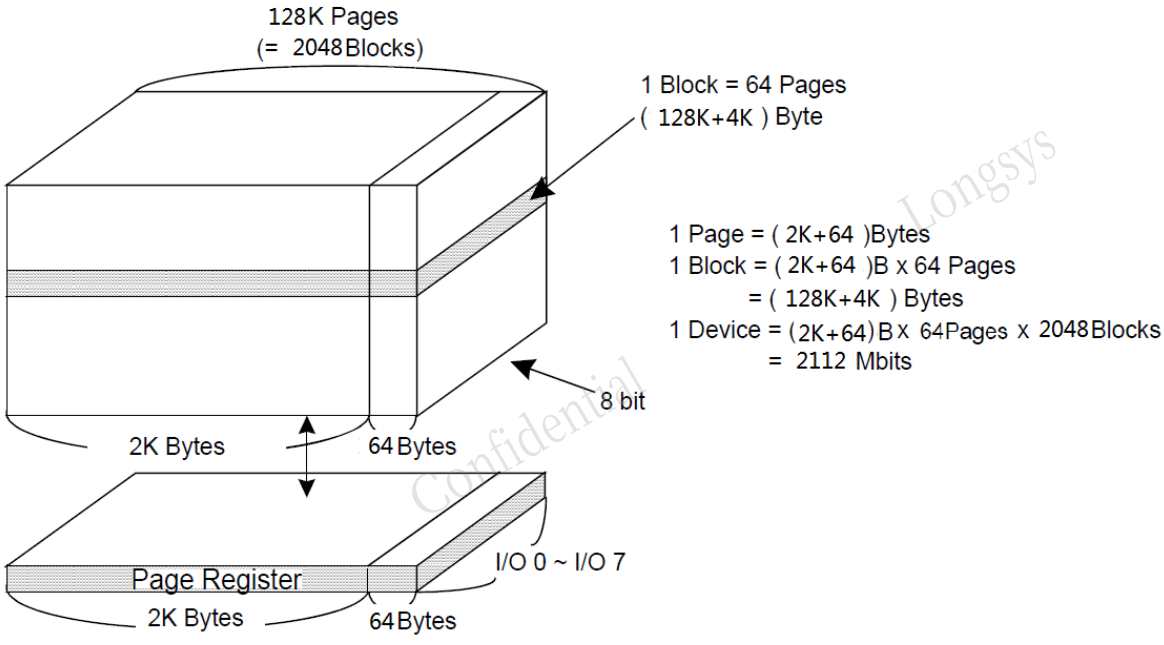
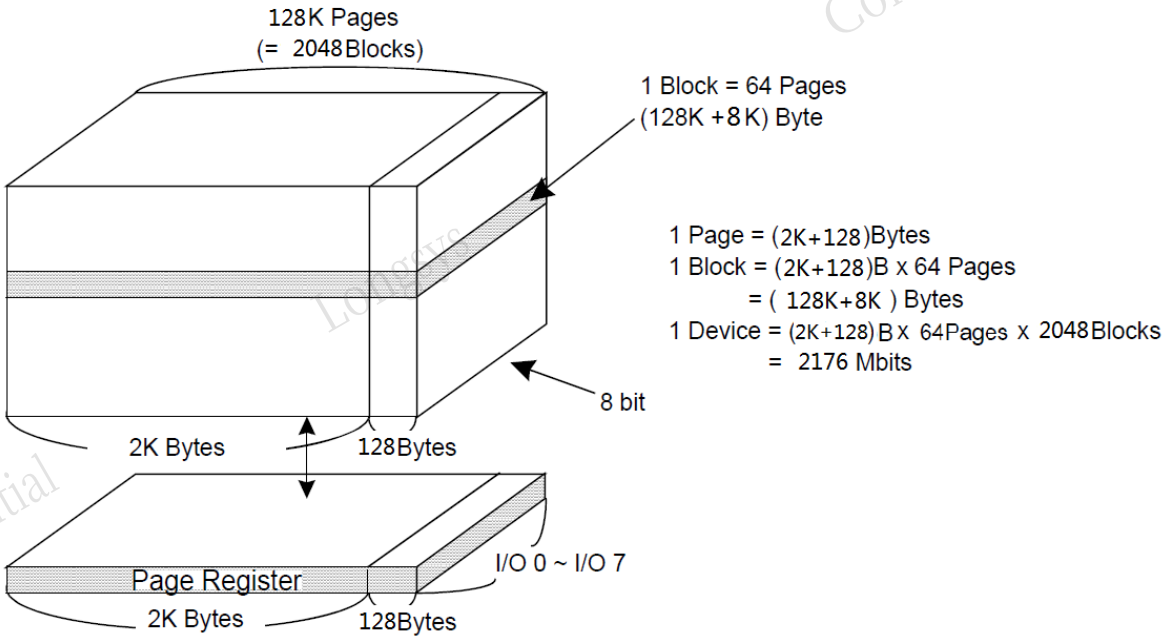


Figure 3 FSNAND Functional Block Diagram



(Page Size=(2048+64)Byte)



(Page Size=(2048+128)Byte)

Figure 4 FSNAND Array Organization

1.8. Addressing

[Table 3] Address Cycle Map

Bus cycle	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	L	L	L	L	
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	
5th Cycle	A28	L	L	L	L	L	L	L	

NOTE :
Column Address : Starting Address of the Register.
A0 - A11 : column address in the page
A12 - A17 : page address in the block
A18 : plane address (for multi-plane operations) / block address (for normal operations)
A19 – A28 : block address
L must be set to "Low".

2. DEVICE OPERATION

2.1. Command Sets

[Table 4] Command Sets

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ	00h	30h			
READ FOR COPY-BACK	00h	35h			
SPECIAL READ FOR COPY-BACK	00h	36h			
READ ID	90h	-			
RESET	FFh	-			Yes
PAGE PGM (start) / CACHE PGM (end)	80h	10h			
CACHE PGM (Start/continue)	80h	15h			
PAGE RE-PROGRAM	8Bh	10h			
COPY BACK PGM	85h	10h			
(Traditional) MULTI -PLANE PROGRAM	80h	11h	81h	10h	
ONFI MULTI-PLANE PROGRAM	80h	11h	80h	10h	
MULTI-PLANE PAGE RE-PROGRAM	8Bh	11h	8Bh	10h	
(Traditional) MULTI -PLANE CACHE PGM(start/cont)	80h	11h	81h	15h	
ONFI MULTI-PLANE CACHE PGM(start/cont)	80h	11h	80h	15h	
(Traditional)MULTI -PLANE CACHE PGM(end)	80h	11h	81h	10h	
ONFI MULTI-PLANE CACHE PGM(end)	80h	11h	80h	10h	
(Traditional) MULTI -PLANE COPY-BACK PROGRAM	85h	11h	81h	10h	
ONFI MULTI -PLANE COPY-BACK PROGRAM	85h	11h	85h	10h	
BLOCK ERASE	60h	D0h			
(Traditional) MULTI -PLANE BLOCK ERASE	60h	60h	D0h		
ONFI MULTI-PLANE BLOCK ERASE	60h	D1h	60h	D0h	
READ STATUS REGISTER	70h	-			Yes
READ STATUS ENHANCED	78h				Yes
RANDOM DATA INPUT	85h	-			
RANDOM DATA OUTPUT	05h	E0h			
READ CACHE (SEQUENTIAL)	31h				
READ CACHE ENHANCED (RANDOM)	00h	31h			
READ CACHE (END)	3Fh	-			
READ PARAMETER PAGE	ECh				

NOTE :
1) Random Data Input/Output can be executed in a page.

2.2. Page Read

This operation is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 2176 bytes (x8) of data within the selected page are transferred to the data registers in less than 30us(tR). The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns (3.3V version) cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page. After power up device is in read mode, so 00h command cycle is not necessary to start a read operation. Any operation other than read or random data output causes device to exit read mode.
Check **Figure 24** to **Figure 26** as references.

2.3. Page Program

A page program cycle consists of a serial data loading period in which up to 2176 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. **Figure 29** to **Figure 30** detail the sequence. The device is programmed basically by page, but it also allows multiple partial page programming of consecutive bytes up to 2176 (x8) in a single page program cycle.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. For example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/16byte).

2.4. Page Re-program

This command allows the re-programming of the same pattern of the last (failed) page into another memory location. The command sequence initiates with re-program setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle. See **Figure 45** for details.
On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm "10h". See **Figure 46** for details.
During page-re-program, address limitation applies as described in **Figure 31** note 1 and 2 for copy-back function.
Similarly, the multi-plane page re-program allows to re-program two pages in parallel, one per each plane. The first page must be in the first plane while the second page must be in the second plane; the multiplane page re-program operation is performed after a previously failed multi-plane page program operation. As for single page re-program case, multi-plane page re-program can be issued without any data manipulation (see **Figure 47** for details) or with data manipulation (see **Figure 48** for details).
During multi-plane page-re-program, address limitation applies as described in **Figure 40** notes 1 and 2 for multi-plane copy-back function.

2.5. Multi-plane program

Device supports multi-plane program: it is possible to program 2 pages in parallel, one per each plane. A multi-plane program cycle consists of a double serial data loading period in which up to 4352bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the five cycle address inputs and serial data for the 1st page. Address for this page must be in the 1st plane(A18=0 for x8 devices). The device supports random data input exactly same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and devices becomes busy for a short time (tDBSY).
Once it has become ready again, either the traditional "81h" or the ONFI 1.0 "80h" command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be in the 2nd plane (A18=1 for x8 devices).Program Confirm command (10h) makes parallel programming of both pages to start. **Figure 36** and **Figure 37** describe the sequences.
User can check operation status by monitoring RB# pin or reading status register commands (70h or 78h), as if it were a normal page program: read status register command is also available during Dummy Busy time (tDBSY).
In case of fail in any of 1st and 2nd page program, fail bit of status register will be set however, in order to know which page failed, ONFI 1.0 "read status enhanced" command must be issued Refer to section 3.10 for further info.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. for example, 2 times for main array (1time/512byte) and 2 times for spare array (1time/16byte).

2.6. Block Erase

The Block Erase operation is done on a block basis. Block address loading is accomplished in 3 cycles initiated by an Erase Setup command (60h). Only addresses A18 to A28 are valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify. Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register.
The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked. See **Figure 34** for details.

2.7. Multi-plane Block Erase

Multi-plane erase, allows parallel erase of two blocks in parallel, one per each memory plane. Two different command sequences are allowed in these case, traditional and ONFI 1.0.
In traditional case, Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation to start. In this case, multi-plane erase does not need any Dummy Busy Time between 1st and 2nd block insertion. See **Figure 38** for details. As an alternative, the ONFI 1.0 multi-plane command protocol can be used, with 60h erase setup followed by 1st block address and D1h first confirm, 60h erase setup followed by 2nd block address and D0h (multi-plane confirm). Between the two block-related sequences, a short busy time tIEBSY will occur. See **Figure 39** for details. Address limitation required for multi-plane program applies also to multi-plane erase. Also operation progress can be checked like in the multi-plane program through Read Status Register, or ONFI 1.0 Read Status Enhanced. As for multiplane page program, the address of the first second page must be within the first plane (A18=0 for x8 devices) and second plane (A18 = 1 for devices), respectively.

2.8. Reset

The device offers a reset feature, executed by writing FFh to the command register. If the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations.
The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. If the device is already in reset state a new reset command will not be accepted by the command register. The RB# pin transitions to low for tRST after the Reset command is written. Refer to **Figure 35** for further details.

2.9. Copy-back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block.
The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the whole 2176 bytes (x8 Device) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or copy-back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in **Figure 31** "Copy-back Program with Random Data Input". When there is a program-failure at copy-back operation, error is reported by pass/fail status. But, if copy-back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, four bit error correction is recommended for the use of copy-back operation. **Figure 31** shows the command sequence for the copy-back operation. Please note that there are two things to do during copy-back program. First, Random Data Input (with/without data) is entered before
Program Confirm command(10h) after Random Data output. Second, WP# value is don't care during Read for copy-back, while it must be set to Vcc When performing the program. During copy-back operation, address limitation applies as described in **Figure 31** notes 1 and 2.

2.10. Multi-plane copy-back Program

As for page program, device supports multi-plane copy-back program with exactly same sequence and limitations. Multi-plane copy-back program must be preceded by 2 single page read for copy-back command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane).
Multi-plane copy-back cannot cross plane boundaries : the contents of the source page of one device plane can be copied only to a destination page of the same plane.
Also in this case, two different sequences are allowed : the traditional one (85h, first plane address 11h, 81h, second plane address, 10h) represented in **Figure 40**, and ONFI 1.0 sequence (85h, first plane address 11h, 85h, second plane address, 10h) represented in **Figure 41** and **Figure 42**.
During multi-plane copy-back operation,address limitation applies as described in **Figure 40** notes1 and 2

2.11. Special read for copy-back

The device feature the "special read for copy-back".
If copy-back read (described in **sections 2.9 and 2.10**) is triggered with confirm command "36h" instead "35h", copy-back read from target page(s) will be executed with an increased internal (Vpass) voltage.
This special feature is used in order to try to recover incorrigible ECC read errors due to over-program or read disturb: it shall be used ONLY if ECC read errors have occurred in the source page using "standard read" or "standard read for copy-back" sequences..
Excluding the copy-back read confirm command, all other features described in **sections 2.9 and 2.10** for standard copy-back remain valid (including the figures referred to in those sections).

2.12. Read Status Register

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired.
RE# or CE# does not need to be toggled for updated status. Refer to "**Table 5**. Status Register Coding" for specific Status Register definitions, and **Figure 22** for specific timings requirements. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

2.13. Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation on a specific plane in case of multi-plane operations.
Figure 23 defines the Read Status Enhanced behavior and timings. The plane address must be specified in the command sequence in order to retrieve the status of the plane of interest.
Refer to **Table 5** for specific Status Register definition. The command register remains in Status Read mode until further commands are issued.
Status register is dynamic in other words, user is not required to toggle RE# / CE# to update it.

[Table 5] Status Register Coding

I/O	Page Program	Block Erase	Read	Cache Read	Cache Program/ Cache reprogram	Definition
I/O 0	Pass/Fail	Pass/Fail	Not use	Not use	Pass/Fail(N)	N Page Pass : "0" Fail : "1"
I/O 1	Not use	Not use	Not use	Not use	Pass/Fail(N-1)	N-1 Page Pass : "0" Fail : "1"
I/O 2	Not use	Not use	Not use	Not use	Not use	Don't -cared
I/O 3	Not use	Not use	Not use	Not use	Not use	Don't -cared
I/O 4	Not use	Not use	Not use	Not use	Not use	Don't -cared
I/O 5	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Active: "0" Idle: "1"
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

Notes:
1. I/O0: This bit is only valid for Program and Erase operations. During Cache Program operations, this bit is only valid when I/O5 is set to one.
2. I/O1: This bit is only valid for Cache Program operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Cache Program sequence.When Cache Program is not supported, this bit is not used.
3. I/O5: If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress. When overlapped interleaved operations or cache commands are not supported, this bit is not used.
4. I/O6: If set to one, then the device or interleaved address is ready for another command and all other bits in the status value are valid. If cleared to zero, then the last command issued is not yet complete and Status Register bits<5:0> are invalid value. When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the last operation is complete.

2.14. Cache Read (available only within a block)

The Cache Read Sequential and Cache Read Random functions permit a page to be read from the page register while another page is simultaneously read from the Flash array. A Page Read command, as defined in **table 4**, shall be issued prior to the initial Cache Read Sequential or Cache Read Random command in a Cache Read sequence. A Cache Read Sequential or Cache Read Random command shall be issued prior to a Cache Read End (3Fh) command being issued.
The Cache Read (Sequential or Random) function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Cache Read (Sequential or Random) function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Cache Read (Sequential or Random) function. Issuing an additional Cache Read (Sequential or Random) function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6]is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array. The host shall not issue a Cache Read Sequential (31h) command after the last page of the block is read. **Figure 27** defines the Cache Read behavior and timings for the beginning of the cache operations subsequent to a Read command being issued. SR[6] conveys whether the next selected page can be read from the page register.
During Cache Read operation the only acceptable commands are Read Status, Random Data Output and Reset.

2.15. Cache Program (available only within a block)

Cache Program is used to improve the program throughput by programming data using the cache register**(Figure 33**). The Cache Program operation can only be used only within one block. The cache register allows new data to be input while the previous data that was transferred to the page buffer is programmed into the memory array. After the serial data input command (80h) is loaded to the command register, followed by 5 cycles of address, a full or partial page of data is latched into the cache register. Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another Cache Program command sequence (80h-15h). The Busy time following the first sequence 80h-15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model. In case of any subsequent sequence 80h-15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete: till this moment the device will stay in a busy state (tCBSYW). Read Status commands (70h) may be issued to check the status of the different registers, and the pass/ fail status of the Cache Program operations.
More in detail:

a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data.
b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete.
c) the Cache Program error bit I/O<1> can be used to identify if the previous page(page N-1) has been successfully programmed or not in Cache Program operation. The latter can be polled upon I/O<6> status bit changing to "1" .
d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while pro-gramming page N. The latter can be polled upon I/O<5> status bit changing to "1". I/O<1> may be read together with I/O<0>. If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation. See "**table5**. Status Register Coding".

2.16. Multi-plane Cache Program

The device supports Multi-plane Cache Program, which enables high program throughput by programming two pages in parallel while exploiting the data and cache registers of both planes to implement cache.
The device supports both the traditional and ONFI 1.0 command sets.
The command sequence can be summarized as follows:
a) Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A18=0 for x8 devices). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation.
b) The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).
c) Once device returns to ready again, 81h (or 80h) command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane(A18=1 for x8 devices). The data of 2nd page other than those to be programmed do not need to be loaded.
d) Cache Program confirm command (15h) Once the cache write command (15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in Busy state for a short time (tCBSYW). After all data of the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another Cache Program command sequence.
The sequence 80h-...- 11h...-...81h...-...15h (or the corresponding ONFI 80h-...- 11h...-...80h...-...15h) can be iterated, and any new time the device will be busy for a for the tCBSYW time needed to complete cell programming of current data registers contents, and transfer from cache registers can be allowed.
The sequence to end Multi-plane Cache Program is 80h-...- 11h...-...81h...-...10h (or 80h-...- 11h...-...80h...-...10h for the ONFI 1.0 case).
Figure 43 and Figure 44 show the command sequence for the Multi-plane Cache Program operation for the two protocols.
Multi-plane Cache Program is available only within two paired blocks belonging to the two planes.
User can check operation status by R/B# pin or read status register commands (70h or 78h).
If user opts for 70h, Status register read will provide a "global" information about the operation in the two planes. More in detail:
a) I/O<6> indicates when both cache registers are ready to accept new data.
b) I/O<5> indicates when the cell programming of the current data registers is complete
c) I/O<1> identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. The latter can be polled upon I/O<6> status bit changing to "1".
d) I/O<0> identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon I/O<5> status bit changing to "1".
If the system monitor the progress of the operation only with R/B#, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.

2.17. Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.
For the FORESEE device, five read cycles sequentially output the 1st Cycle, and the device code and 3rd, 4th,5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it.

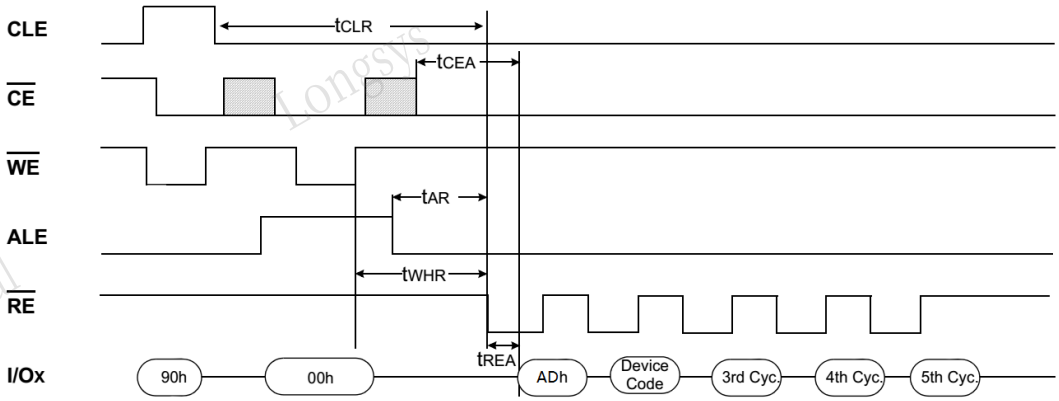


Figure 5 Read ID Sequence

[Table 6]00h Address ID cycle

Part Number	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle
FS33ND02GH2	ADh	DAh	90h	95h	46h

[Table 7]3rd ID Data

	Description	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleave Program Between multiple chips	Not Support Support		0 1						
Cache Program	Not Support Support	0 1							

[Table 8]4th ID Data

	Description	I/O_7	I/O_6	I/O_5	I/O_4	I/O_3	I/O_2	I/O_1	I/O_0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB							0 0 1 1	0 1 0 1
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 1 1	0 1 0 1				
Redundant Area Size (byte/512byte)	8 16						0 1		
Organization	x8 x16		0 1						
Serial Access Minimum	45ns 25ns Reserved Reserved	0 1 0 1				0 0 1 1			

[Table 9]5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
ECC Level	1bit/512Bytes							0	0
	2bit/512Bytes							0	1
	4bit/512Bytes							1	0
	8bit/512Bytes							1	1
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane Size (W/O redundant Area)	64Mb		0	0	0				
	128Mb		0	0	1				
	256Mb		0	1	0				
	512Mb		0	1	1				
	1Gb		1	0	0				
	2Gb		1	0	1				
	4Gb		1	1	0				
	8Gb		1	1	1				
Reserved		0							

2.18. Read ONFI Signature

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. **Figure 49** shows the operation sequence.

2.19. Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. **Figure 50** defines the Read Parameter Page behavior. This data structure enables the host processor to automatically recognize the Nand Flash configuration of a device. The whole data structure is repeated at least three times.
The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.
The Read Status command may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.
Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

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2.20. Parameter Page Data Structure Definition

For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte. Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data bytes are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use. Unused fields should be cleared to 0h.

[Table 10] Parameter Page Data Structure Definition

Byte	O/M	Description	Values
	Revision information and features block		
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"	4Fh 4Eh 46h 49h
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02h 00h
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	1Ch 00h
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache 18ntegrit 0 1 = supports Page Cache Program command	3Bh 00h
10-31		Reserved (0)	00h
	Manufacturer information block		
32-43	M	Device manufacturer (12 ASCII characters)	53h 4Bh 20h 48h 59h 4Eh 49h 58h 20h 20h 20h 20h
44-63	M	Device model (20 ASCII characters)	48h 32h 37h 55h 32h 47h 38h 46h 32h 44h 4Bh 41h 2Dh 42h 4Dh 20h 20h 20h 20h 20h
64	M	JEDEC manufacturer ID	ADh
65-66	O	Date code	00h 00h
67-79		Reserved (0)	00h
	Memory organization block		

80-83	M	Number of data bytes per page	00h 08h 00h 00h
84-85	M	Number of spare bytes per page	80h 00h
86-89	M	Number of data bytes per partial page	00h 00h 00h 00h
90-91	M	Number of spare bytes per partial page	00h 00h
92-95	M	Number of pages per block	40h 00h 00h 00h
96-99	M	Number of blocks per logical unit (LUN)	00h 08h 00h 00h
100	M	Number of logical units (LUNs)	01h
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	23h
102	M	Number of bits per cell	01h
103-104	M	Bad blocks maximum per LUN	28h 00h
105-106	M	Block endurance	05h 04h
107	M	Guaranteed valid blocks at beginning of target	01h
108-109	M	Block endurance for guaranteed valid blocks	05h 04h
110	M	Number of programs per page	04h
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00h
112	M	Number of bits ECC correctability	04h
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	01h
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	04h
115-127		Reserved (0)	00h
	Electrical parameters block		
128	M	I/O pin capacitance	0Ah
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	1Fh 00h

131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0	1Fh 00h
133-134	M	tPROG Maximum page program time (µs)	BCh 02h
135-136	M	tBERS Maximum block erase time (µs)	10h 27h
137-138	M	tR Maximum page read time (µs)	1Eh 00h
139-140	O	tCCS Minimum change column setup time(ns)	3Ch 00h
141-163		Reserved (0)	00h
	Vendor block		
164-165	M	Vendor specific Revision number	00h 00h
166-253		Vendor specific	00h
254-255	M	Integrity CRC	CCh 92h
	Redundant Parameter Pages		
256-511	M	Value of bytes 0-255	
512-767	M	Value of bytes 0-255	
768+	O	Additional redundant parameter pages	

Note:
"O" Stands for Optional, "M" for Mandatory

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3. Other Features

3.1. Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 1.8 V (3.3 V Device). WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in **Figure 6**. The two-step command sequence for program/erase provides additional software protection.

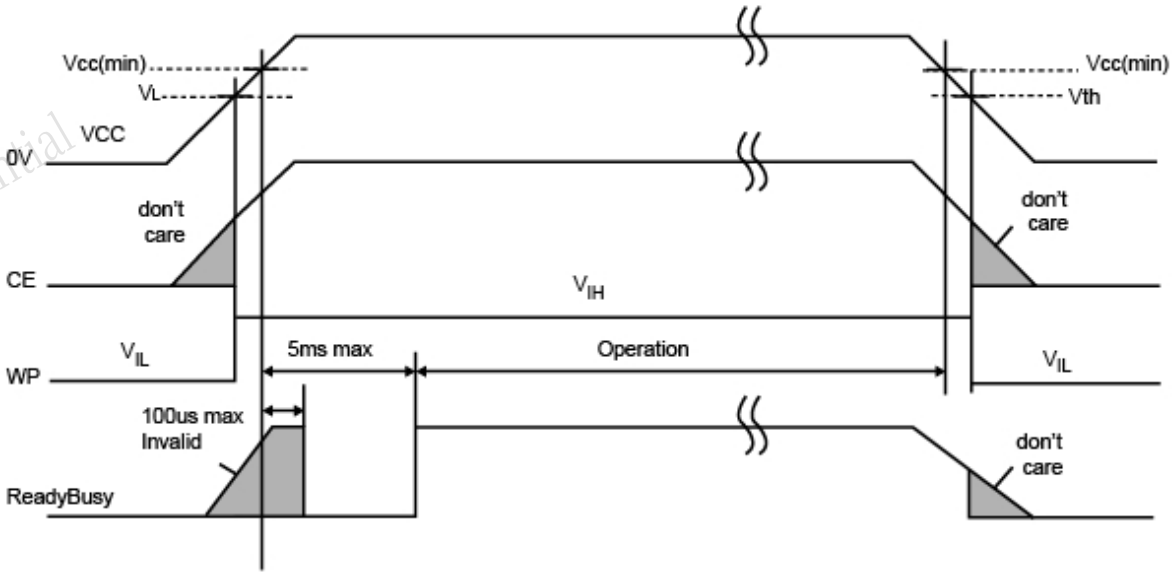


Figure 6 Data Protection & Power on/off

3.2. Ready / Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tR (R/B#) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (**Figure 7**). Its value can be determined by the following guidance.

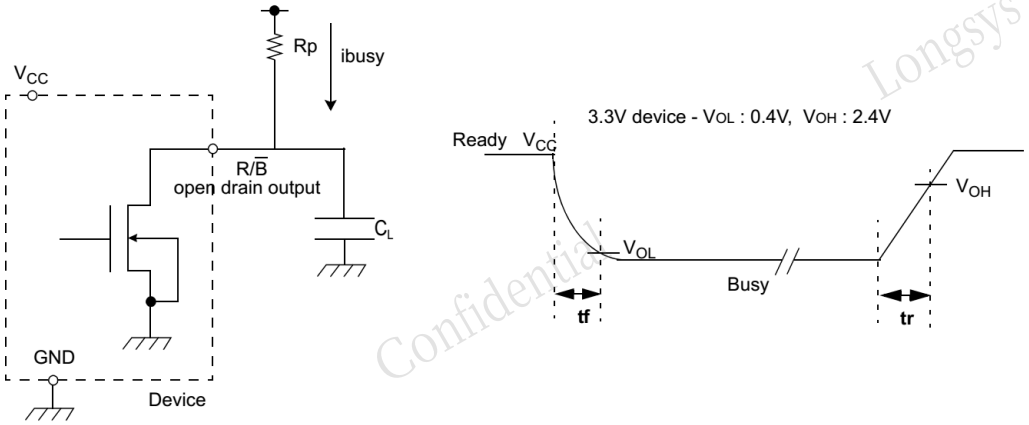
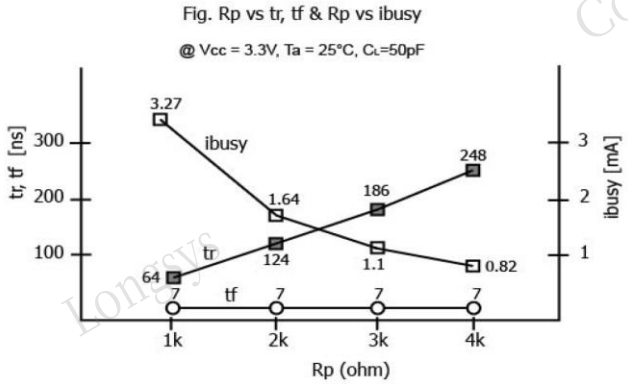


Figure 7 Rp vs tr, tf & Rp vs ibusy



Rp Value Guidence

The rise time of the R/B# signal depends on the combination of Rp and capacitive loading of the R/B# circuit.
It is approximately two times constants (Tc) between the 10% and 90% points on the R/B# waveform.
$T_C = R \times C$
Where R = Rp (Resistance of pull-up resistor), and C = C_L (Total capacitive load)
The fall time of the R/B# signal majorly depends on the output impedance of the R/B# signal and the total load capacitance.

$$\text{Rp (Min.)} = \frac{Vcc\ (Max.) - VOL\ (Max.)}{IOL + \Sigma IL}$$

Notes:
Considering of the variation of device-by-device, the above data is for reference to decide the resistor value.
Rp maximum value depends on the maximum permissible limit of tr.
IL is the total sum of the input currents of all devices tied to the R/B pin.

3.3. Write protect (#WP) handling

Erase and program operations are aborted if WP# is driven low during busy time, and kept low for about 100nsec. Switching WP# low during this time is equivalent to issuing a Reset command (FFh)
The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/B# pin will stay low for tRST (similarly to **Figure 35**). At the end of this time, the command register is ready to process the next command, and the Status Register bit IO<6> will be cleared to "1", while IO<7> value will be related to the WP# value. Refer to Table 5 for more information on device status.
Erase and program operations are enabled or disabled by setting WP# to high or low respectively prior to issuing the setup commands (80h or 60h).
The level of WP# shall be set tWW nsec prior to raising the WE# pin for the set up command, as explained in **Figure 8~11**.

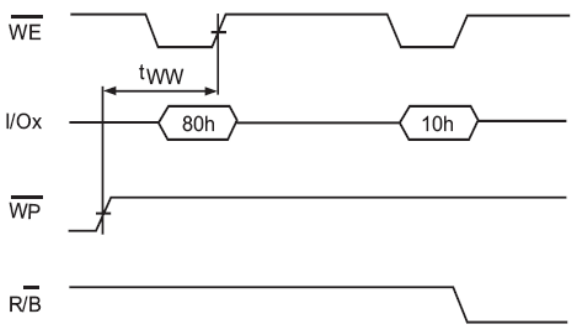


Figure 8 Enable Programming

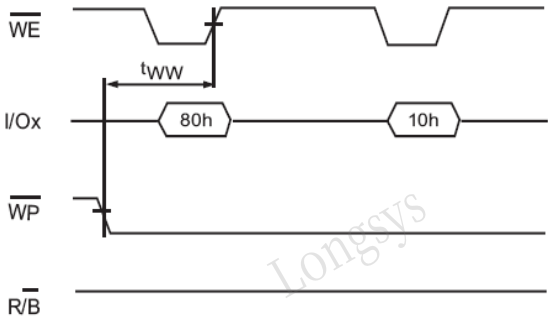


Figure 9 Disable Programming

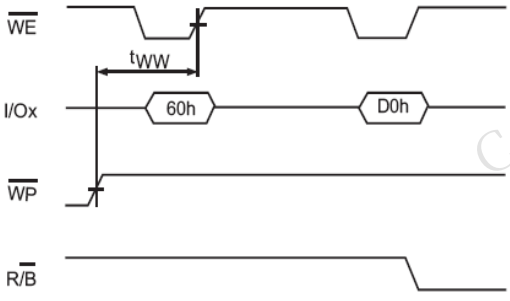


Figure 10 Enable Erasing

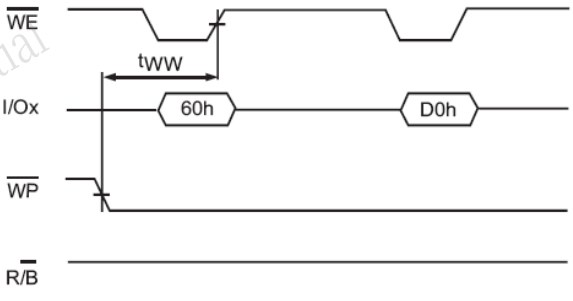


Figure 11 Disable Erasing

4. Electrical Characteristic

4.1. Valid Block

[Table 11] The Number of Valid Block

Parameter	Symbol	Min	Typ.	Max	Unit
FS33ND02GH2	NVB	2,008	-	2,048	Blocks

4.2. Recommended Operating Conditions

[Table 12] Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Power Supply Voltage	VCC	2.7	3.3	3.6	V
Ground Supply Voltage	VSS	0	0	0	V

Notes:
1. The 1st block is guaranteed to be a valid block at the time of shipment.
2. Invalid blocks are one that contains one or more bad bits. The device may contain bad blocks upon shipment.

4.3. Absolute Maximum DC Ratings

[Table 13] Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to VSS	VCC	-0.6 to + 4.6	V
	VIN	-0.6 to + 4.6	
	VI/O	-0.6 to VCC + 0.3 (< 4.6V)	
Ambient Operating Temperature	TA	Commercial Plus: -20 to +85	℃
		Industrial: -40 to +85	

NOTE :
Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns.
Maximum DC voltage on input/output pins is VCC+0.3V which, during transitions, may overshoot to VCC+2.0V for periods <20ns.
Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this datasheet.
Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4.4. DC Operating Characteristics

[Table 14] DC & Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Access Operation Current	ICC1	tRC=25ns CE#=VIL, IOUT=0mA	-	15	30	mA
Program Operation Current	ICC2	Normal	-	-	30	
		Cache		-	40	
Erase Operation Current	ICC3	-	-	15	30	
Stand-by Current (TTL)	ICC4	CE#=VIH, WP#=0V/VCC	-	-	1	
Stand-by Current (CMOS)	ICC5	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	µA
Input Leakage Current	ILI	VIN=0 to VCC(max)	-	-	±10	
Output Leakage Current	ILO	VOUT=0 to VCC(max)	-	-	±10	
Input High Voltage	VIH1)	-	0.8xVCC	-	VCC+0.3	V
Input Low Voltage, All inputs	VIL1)	-	-0.3	-	0.2xVCC	
Output High Voltage Level	VOH	IOH=-400µA	2.4	-	-	
Output Low Voltage Level	VOL	IOL=2.1mA	-	-	0.4	
Output Low Current (R/B#)	IOL(R/B#)	VOL=0.4V	8	10	-	mA

NOTE :
VIL can undershoot to -0.4V and VIH can overshoot to VCC +0.4V for durations of 20ns or less.
Typical value is measured at VCC=3.3V, TA=25℃. Not 100% tested.

4.5. Input / Output Capacitance (TA=25℃, VCC=3.3V, f=1.0Mhz)

[Table 15] Input / Output Capacitance

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

NOTE :
Capacitance is periodically sampled and not 100% tested.

4.6. Read / Program / Erase Characteristics

[Table 16] NAND Read / Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Cell to Register	tR	-		30	µs
Read Cache busy time	tCBSYR	-	5	tR	µ s
Program Time	tPROG	-	300	700	µs
Cache Program short busy time	tCBSYW	-	5	tPROG	µs
Cache Program busy time (ONFI)	tPCBSY	-	5	tPROG	µs
Multi-plane Erase busy time	tIEBSY	-	500	1000	ns
Multi-plane Program busy time (traditional)	tDBSY	-	500	1000	ns
Multi-plane Program busy time (ONFI)	tIPBSY	-	500	1000	ns
Number of Partial Program Cycles	Nop	-	-	4	cycles
Block Erase Time	tBERS	-	3.5	10	ms

NOTE :
Typical value is measured at VCC=3.3V, T_A=25℃. Not 100% tested.
Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V VCC and 25℃ temperature.

4.7. AC Timing Parameters Table

[Table 17] AC Timing Characteristics

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS[1)]	12	-	ns
CLE Hold Time	tCLH	5	-	ns
CE# Setup Time	tCS[1)]	20	-	ns
CE# Hold Time	tCH	5	-	ns
WE# Pulse Width	tWP	12	-	ns
ALE Setup Time	tALS[1)]	12	-	ns
ALE Hold Time	tALH	5	-	ns
Data Setup Time	tDS[1)]	12	-	ns
Data Hold Time	tDH	5	-	ns
Write Cycle Time	tWC	25	-	ns
WE# High Hold Time	tWH	10	-	ns
Address to Data Loading Time	tADL[2)]	70	-	ns
ALE toRE# Delay	tAR	10	-	ns
CLE to RE# Delay	tCLR	10	-	ns
Ready to RE# Low	tRR	20	-	ns
RE# Pulse Width	tRP	12	-	ns
WE# High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	25	-	ns
RE# Access Time	tREA	-	20	ns
RE# High to Output Hi-Z	tRHZ	-	100	ns
CE# High to Output Hi-Z	tCHZ	-	30	ns
CE# High to ALE or CLE Don't Care	tCSD	10	-	ns
RE# High to Output Hold	tRHOH	15	-	ns
RE# Low to Output Hold	tRLOH	5		ns
Data Hold Time after CE# Disable	tCOH	15	-	ns
RE# High Hold Time	tREH	10	-	ns
Output Hi-Z to RE# Low	tIR	0	-	ns
RE# High to WE# Low	tRHW	100	-	ns
WE# High to RE# Low	tWHR	60	-	ns
CE# low to RE# low	tCR	10		
Device Resetting Time (Read/Program/Erase)	tRST	-	5/10/500 [1)]	µs
Write protection time	tWW	100		

NOTE :
1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.
2. In case of first reset after initial powering up, it takes max 5ms.

5. NAND FLASH TECHNICAL NOTES

5.1. Initial Invalid Block(s)

The initial invalid blocks are included in the device while it gets shipped called. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. During the time of using the device, the additional invalid blocks might be increasing; therefore, it is recommended to check the invalid block marks and avoid using the invalid blocks. Furthermore, please read out the initial invalid block and the increased invalid block information before any erase operation since it may be cleared by any erase operation.

5.2. Identifying Initial Invalid Block(s)

While the device is shipped, the value of all data bytes of the good blocks are FFh. The initial invalid block(s) status is defined by the 1st byte in the spare area. Longsys makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048.
Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart (Figure 16). The erase operation at the invalid block is not recommended.

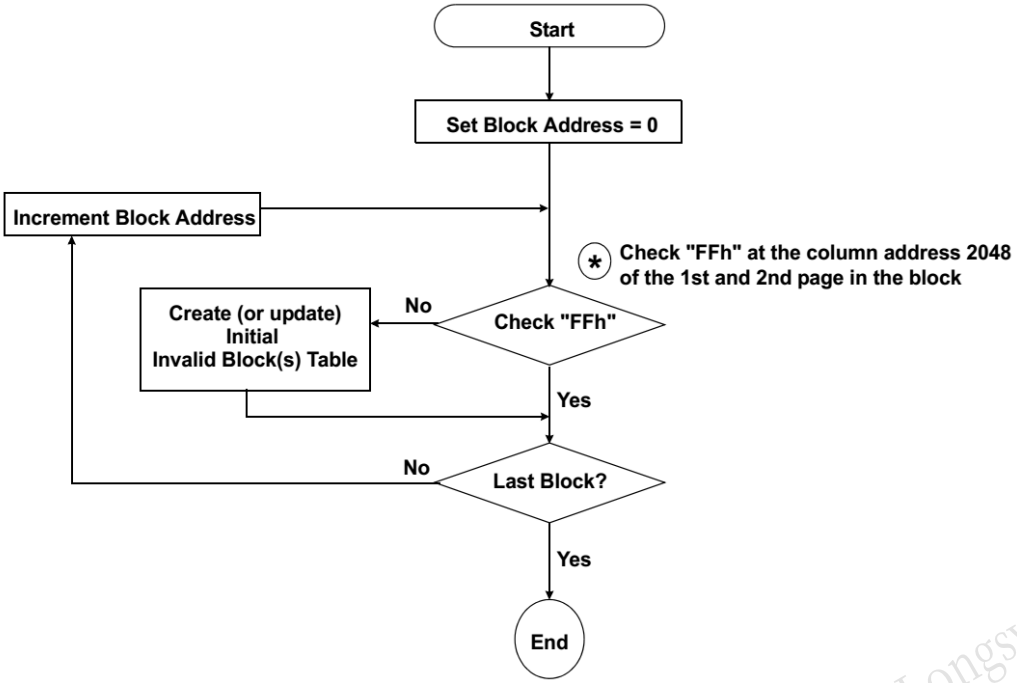


Figure 12 Flow Chart to Create Initial Invalid Block Table

5.3. Error in Write or Read Operation

The device may fail during a Read, Program or Erase operation. The following possible failure modes should be considered when implementing a highly reliable system.Block replacement should be done while status read failure after erase or program. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

[Table 18] Failure Cases

	Failure Mode	Detection and Countermeasure Sequence
Write	Erase Failure	Read Status after Erase --> Block Replacement
	Program Failure	Read Status after Program --> Block Replacement
Read	Single bit Failure	Verify ECC -> ECC Correction

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ECC:

Error Correcting Code --> Hamming Code etc.
Example) 1bit correction & 2bit detection

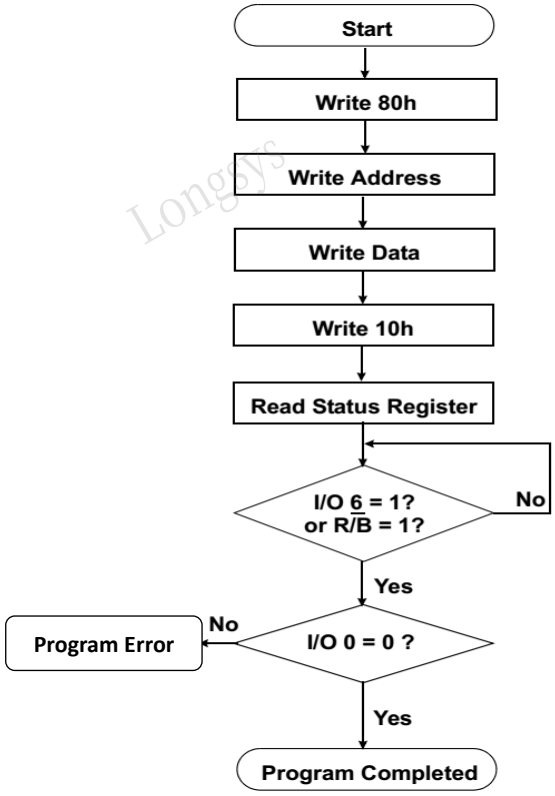
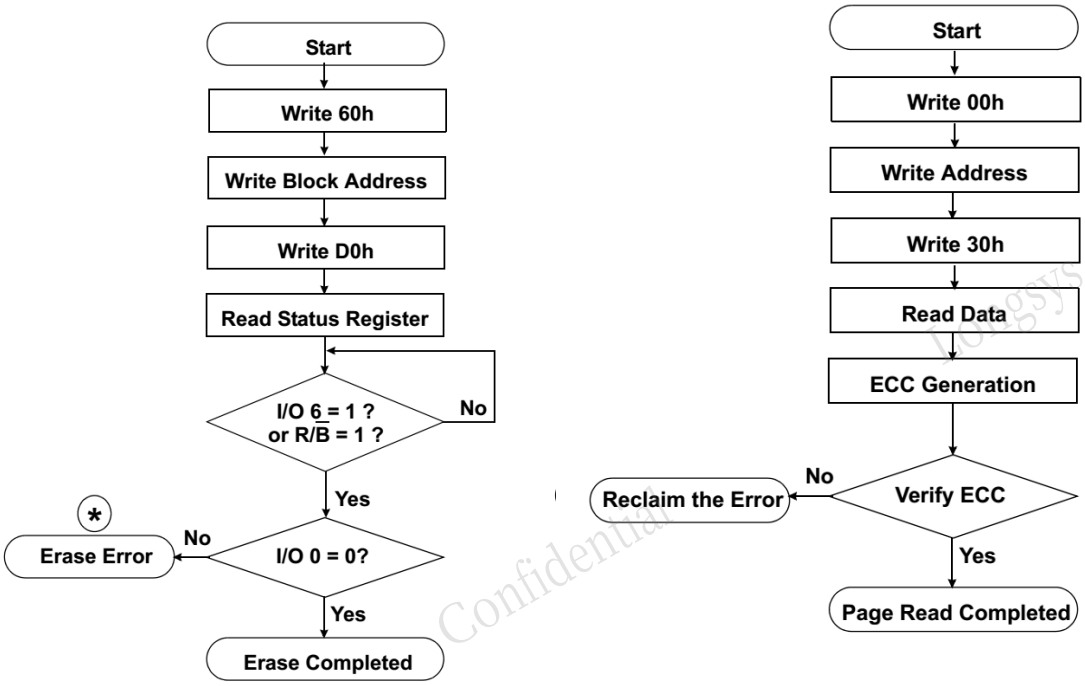


Figure 13 Program Flow Chart

If program operation results in an error, map out the block including the page in error and copy the target data to another block.



*If erase operation results in an error, map out the failing block and replace it with another block.

Figure 14 Erase Flow Chart& Read Flow Chart

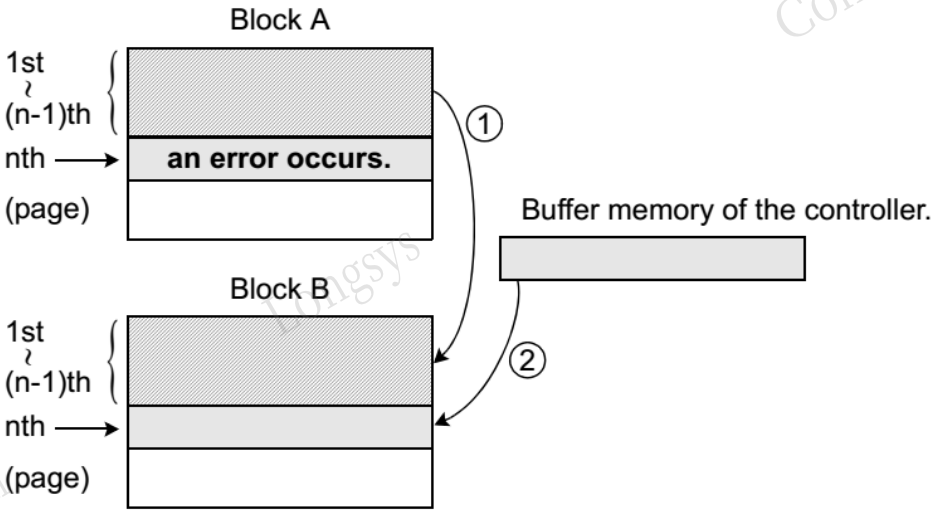


Figure 15 Block Replacement

1.When an error happens in the nth page of the Block 'A' during erase or program operation.
2.Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block'B')
3. Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block'B'.
4. Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

5.4. Addressing for Program Operation

Within a block, The page program operation in a block should start from the low address to high address. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.

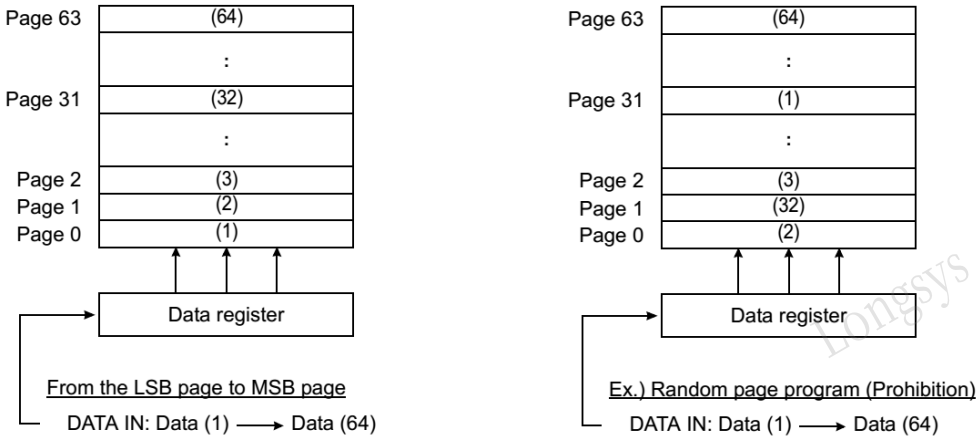


Figure16 Addressing for Program Operation

6. Timing

6.1. Data Protection & Power Up Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below about 2V(3.3V device). WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences as shown in Figure 23. The two step command sequence for program/erase provides additional software protection.

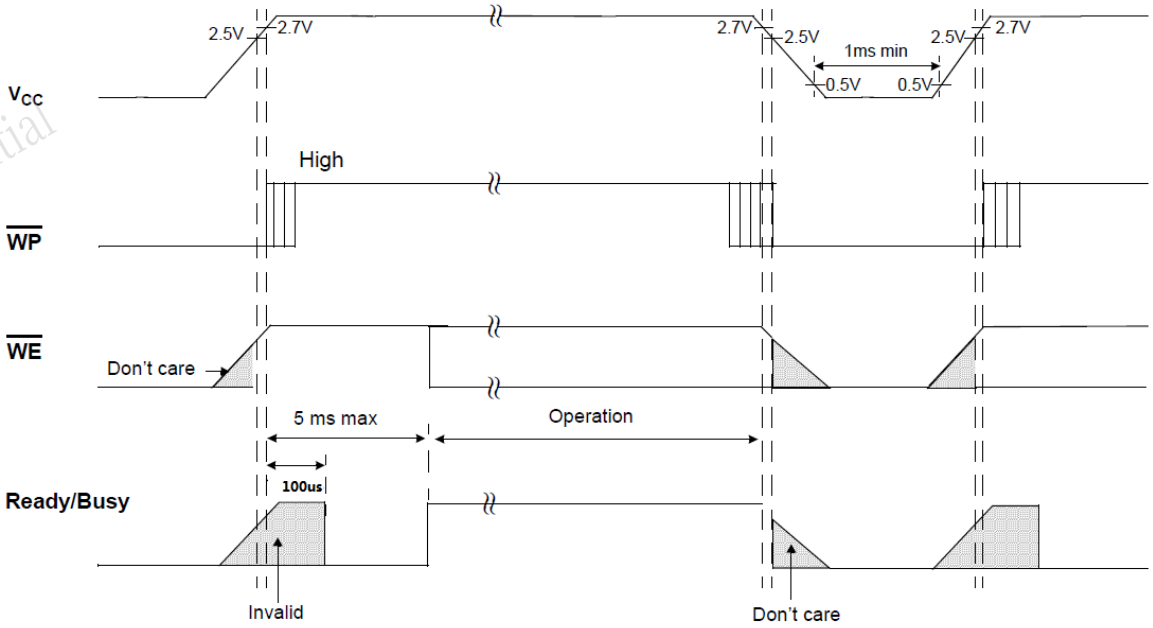


Figure 17 AC Waveforms for Power Transition

NOTE :
1) During the initialization, the device consumes a maximum current of 30mA (ICC1).
2) Once Vcc drops under 2.5V, Vcc is recommended that it should be driven down to 0.5V and stay low under 0.5V for at least 1ms before Vcc power up.

6.2. Mode Selection

[Table 19]Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input(5cycles)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input(5cycles)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X[1)]	X	X	X	L	Write Protect	
X	X	H	X	X	0V/VCC[2)]	Stand-by	

NOTE :
1) X can be VIL or VIH.
2) WP should be biased to CMOS high or CMOS low for standby.

6.3. Command Latch Cycle

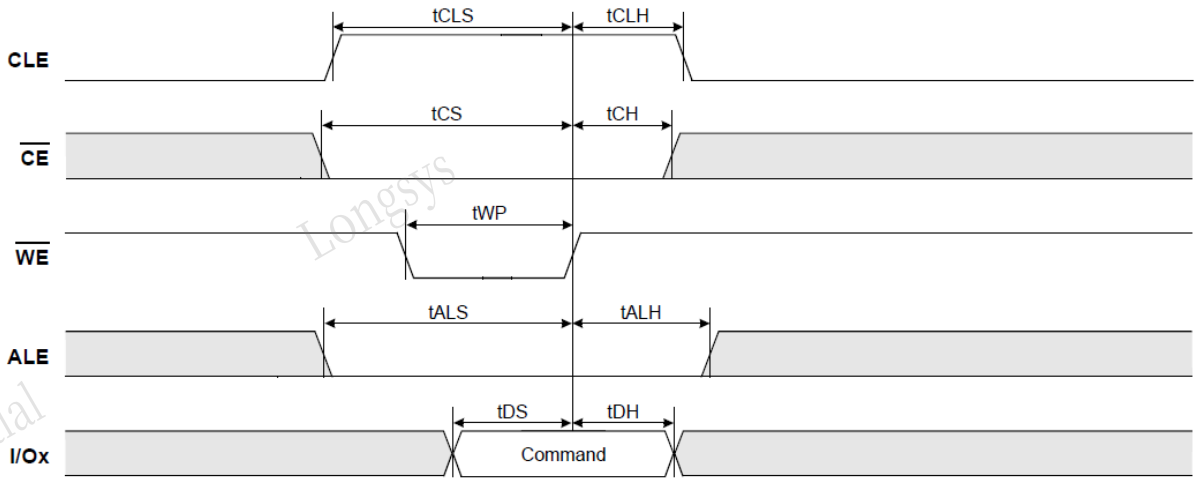


Figure 18 Command Latch Cycle

6.4. Address Latch Cycle

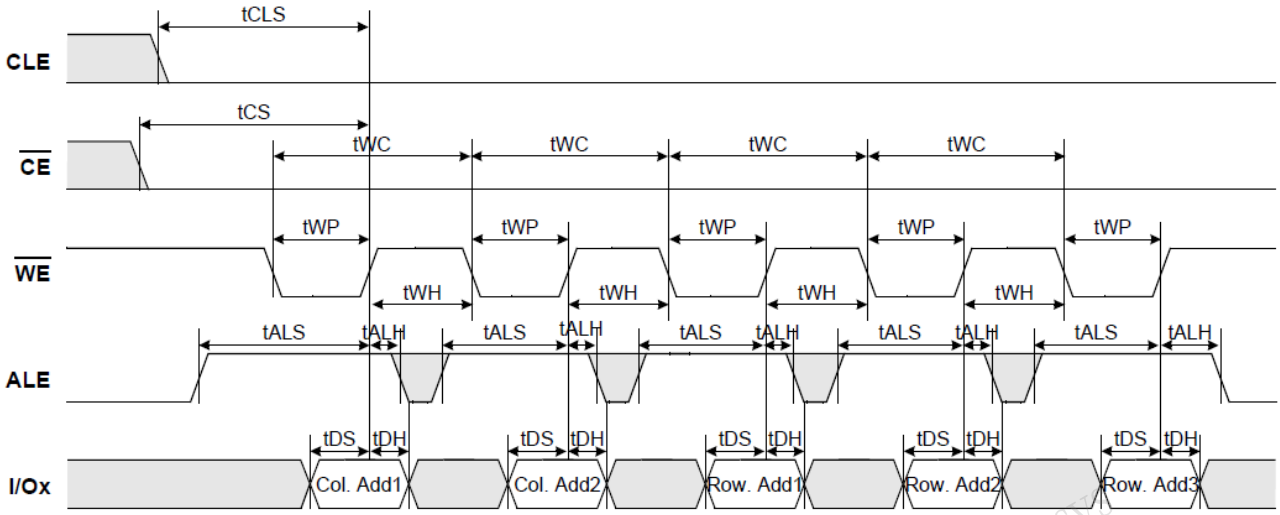


Figure 19 Address Latch Cycle

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6.5. Input Data Latch Cycle

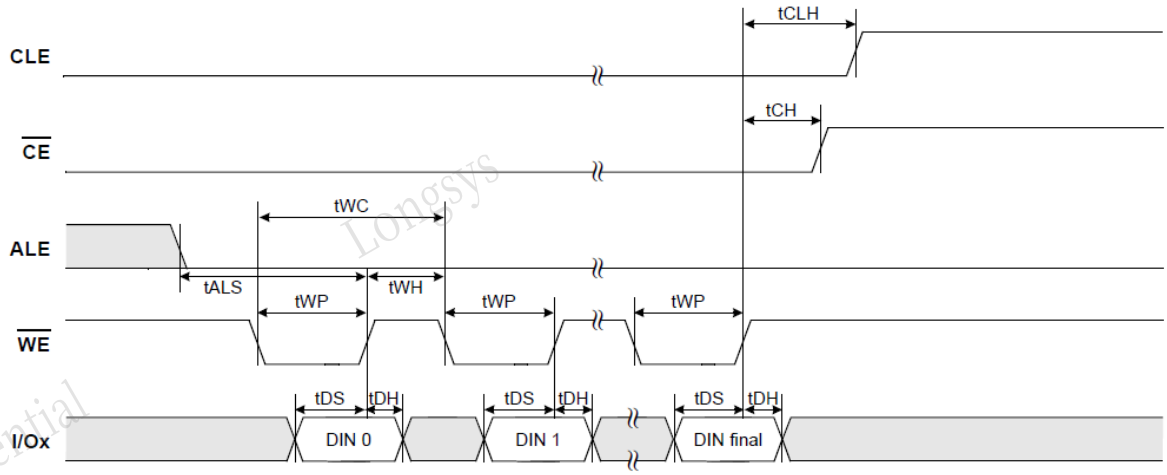

Figure 20 Input Data Latch Cycle

Note:
Data Input cycle is accepted to data register on the rising edge of WE#, when CLE and CE# and ALE are low, and device is not Busy state.

6.6. Data Output Cycle Timings (CLE=L, WE#=H, ALE=L)

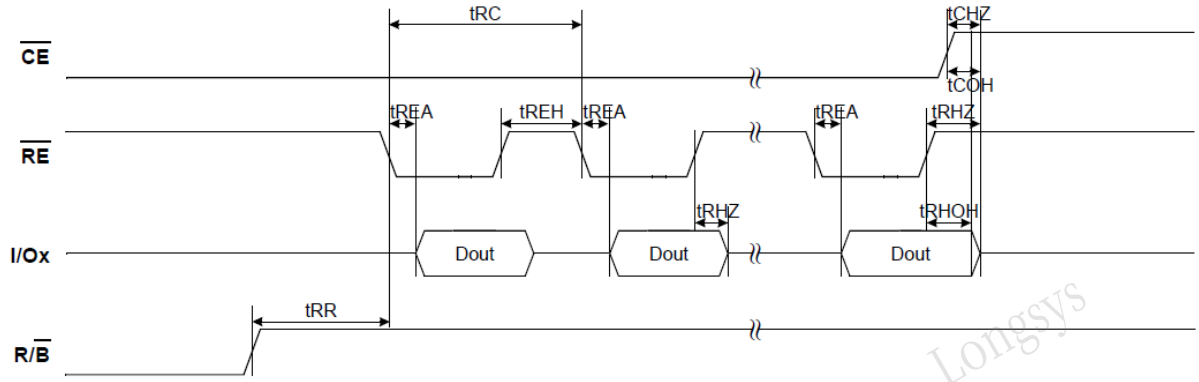

Figure 21 Serial Access Cycle after Read (CLE=L, WE#=H, ALE=L)

NOTE :
1) Transition is measured at 200mV from steady state voltage with load. This parameter is sampled and not 100% tested.
2) tRHOH starts to be valid when frequency is lower than 33Mhz.

6.7. Read Status Cycle

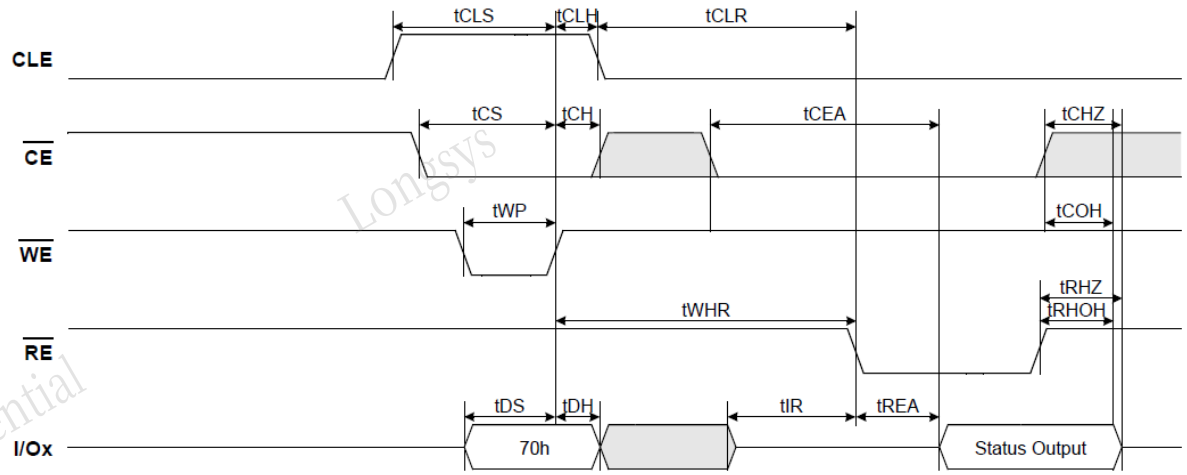

Figure 22 Read Status Cycle

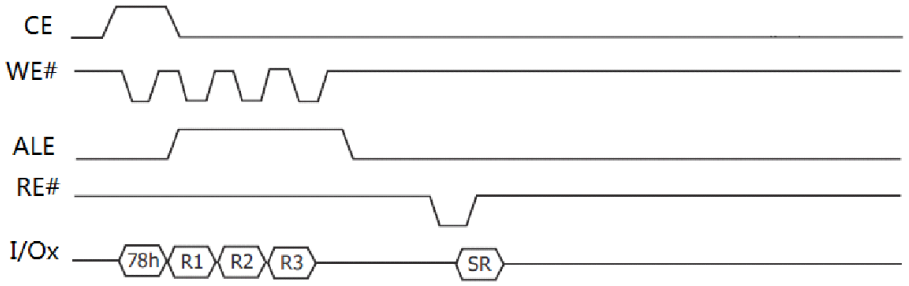

Figure 23 : Read Status Enhanced cycle

6.8. Read Operation

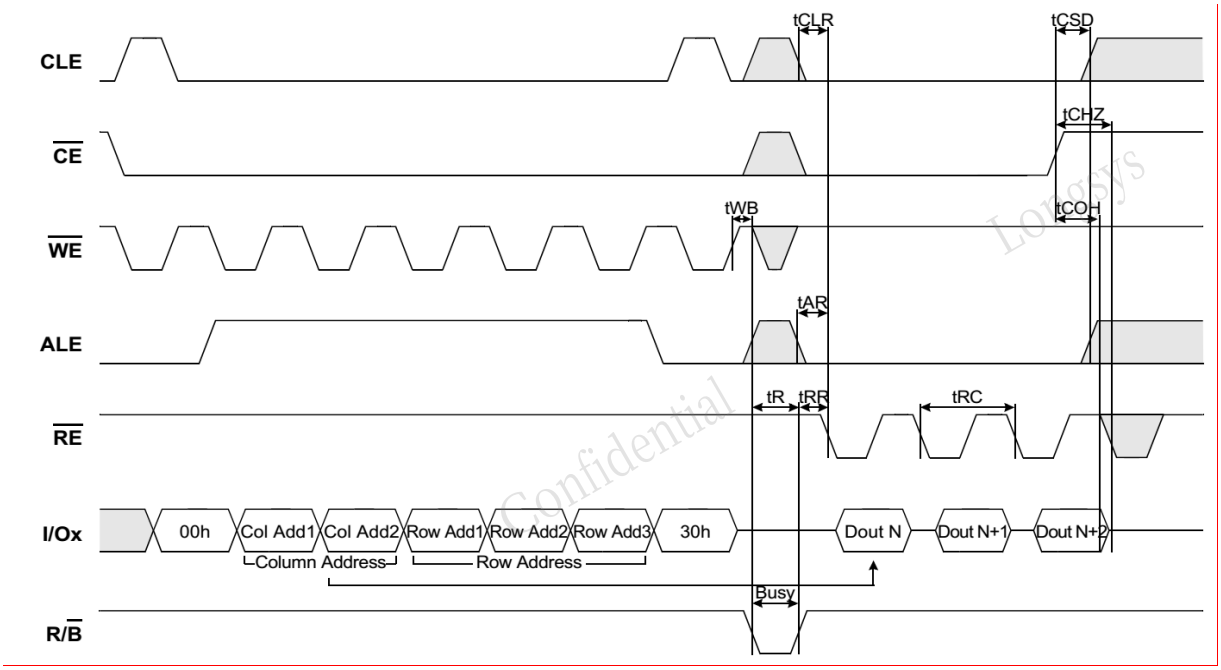

Figure 24 Read Operation

6.9. Page Read Operation Timings with CE# don't care

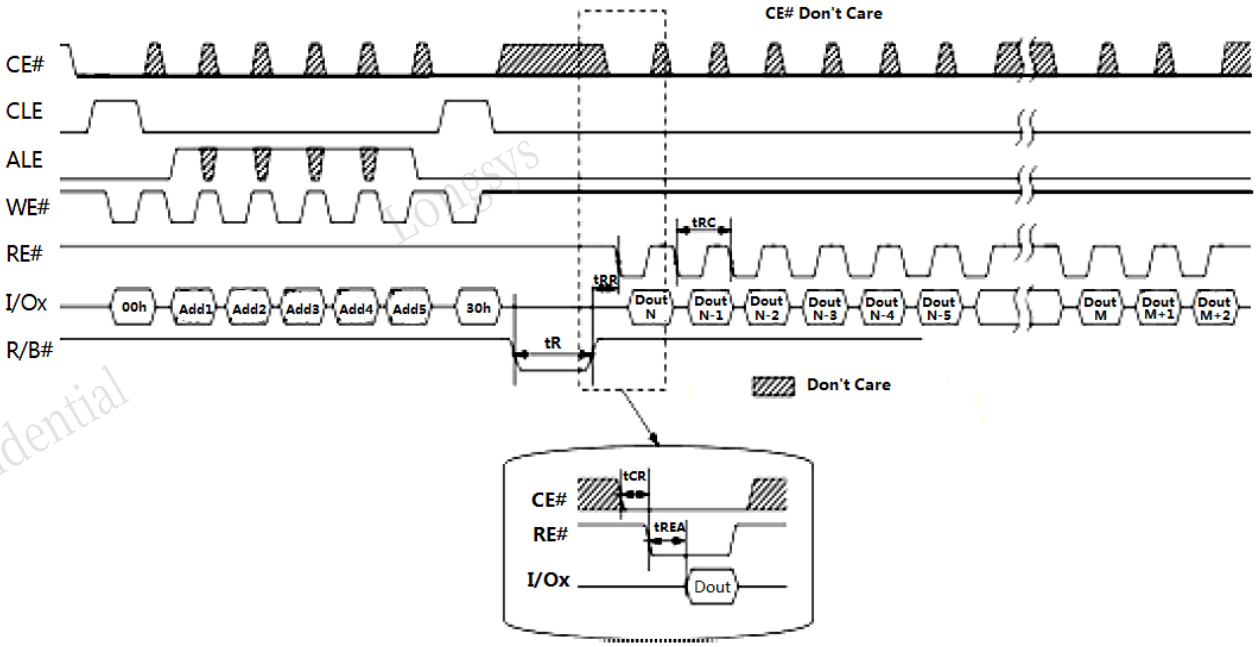

Figure 25 Page Read Operation Timings with CE# don't care

6.10. Random Data Output In a Page Operation

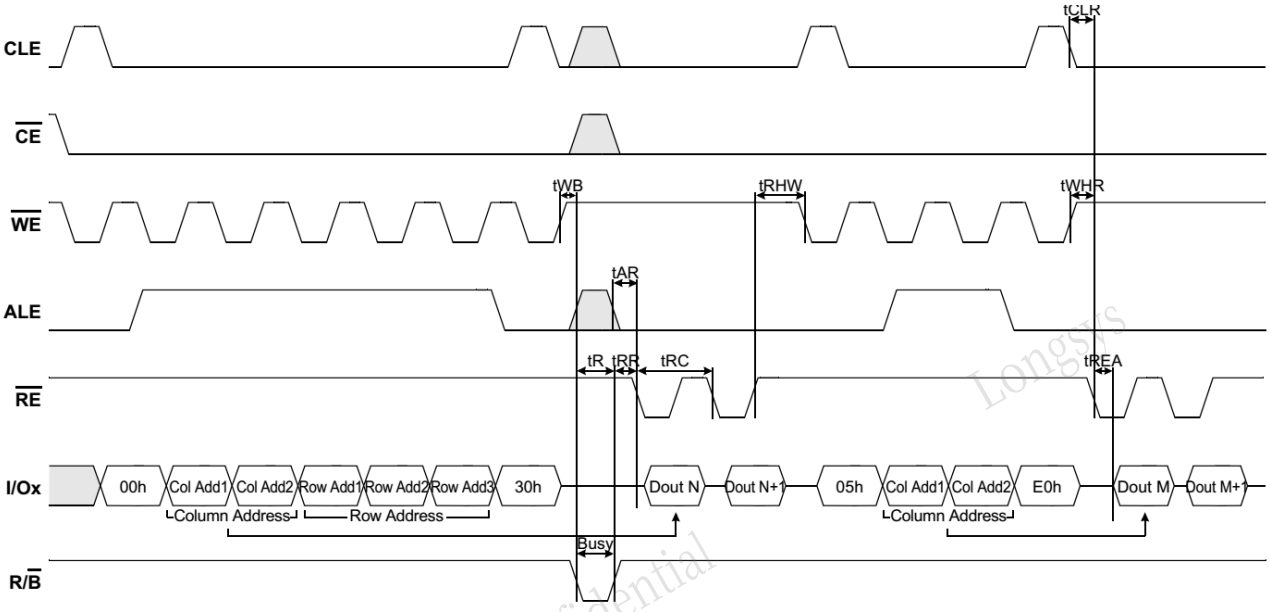

Figure 26 Random Data Output In a Page Operation

6.11. Cache Read Operation Timings

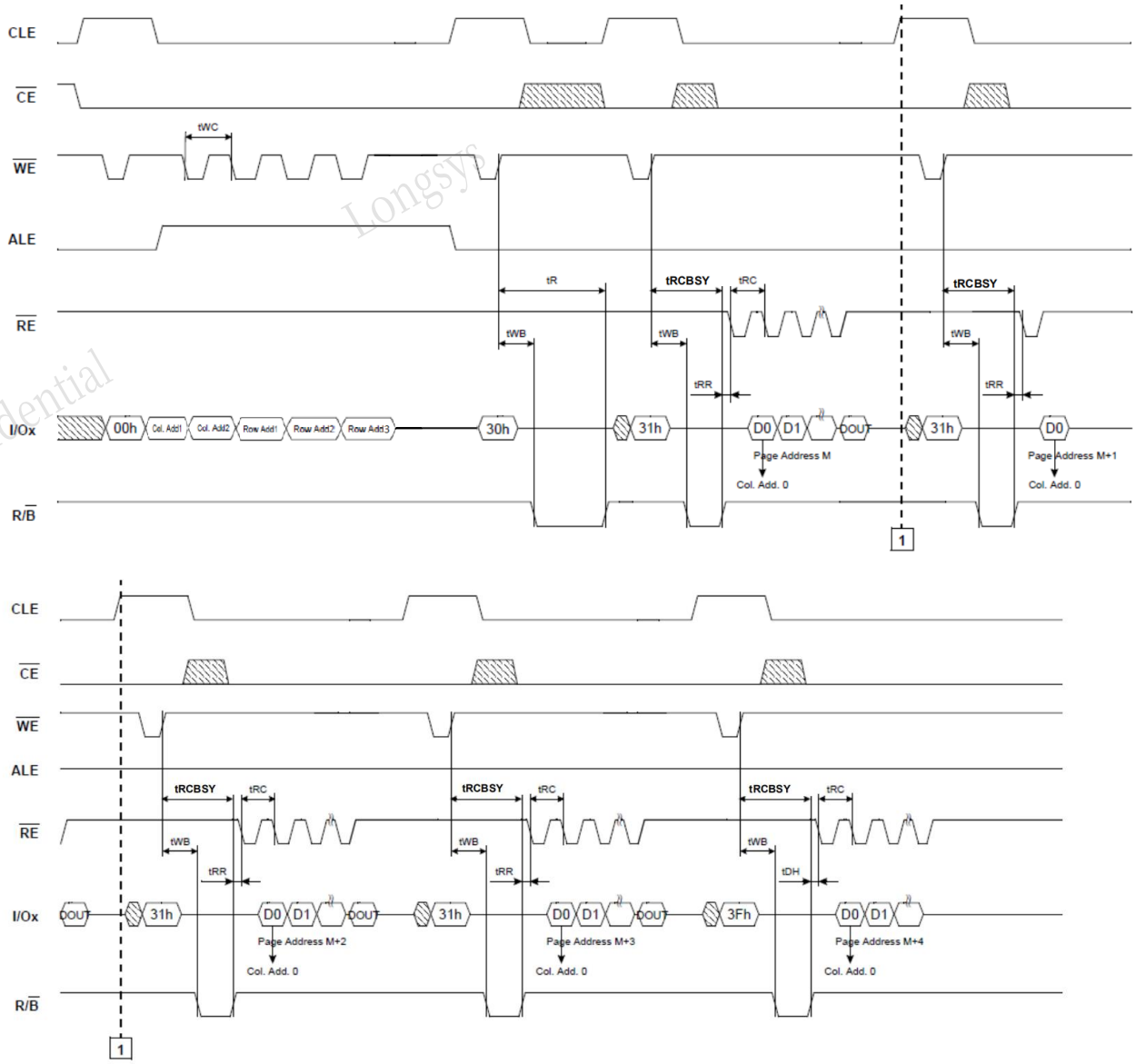

Figure 27 Cache Read Operation Timings

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6.12. Read ID Operation

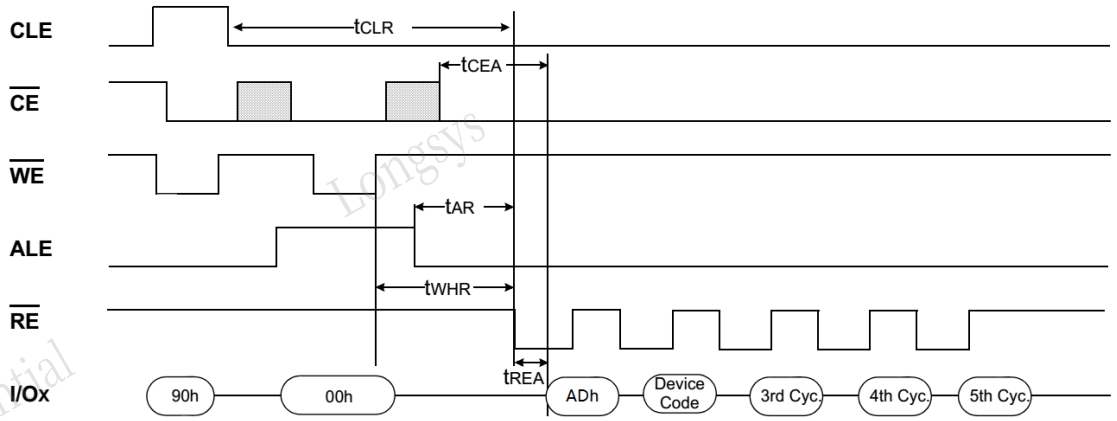

Figure 28 Read ID Operation

6.13. Page Program Operation

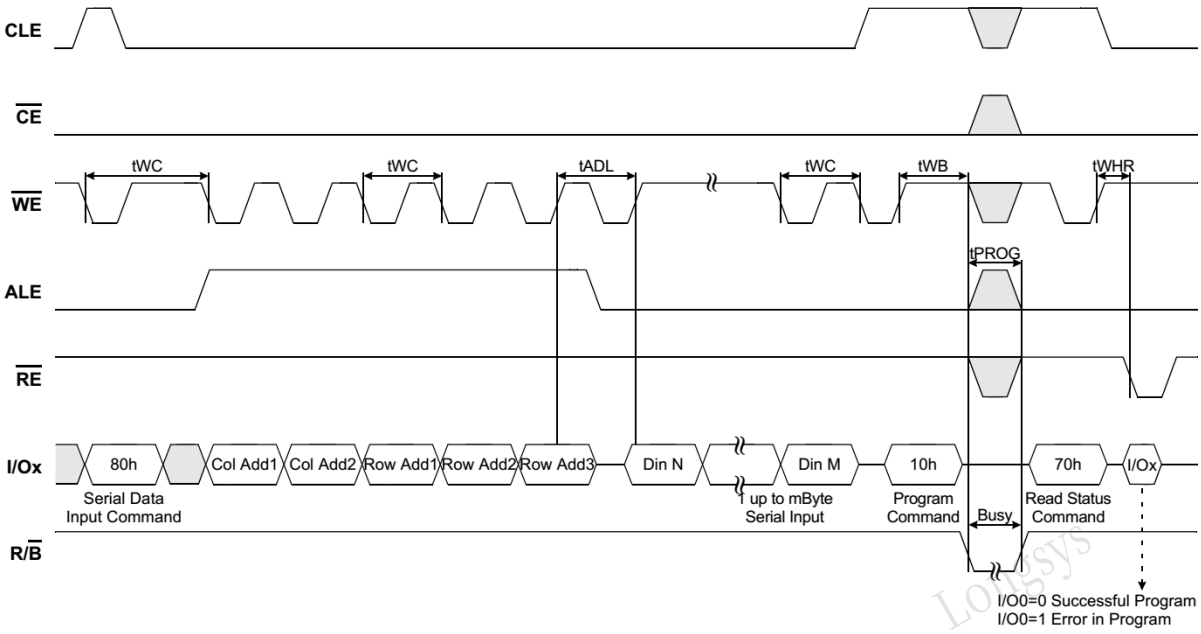

Figure 29 Page Program Operation

NOTE :
tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

6.14. Random Data Input Timings

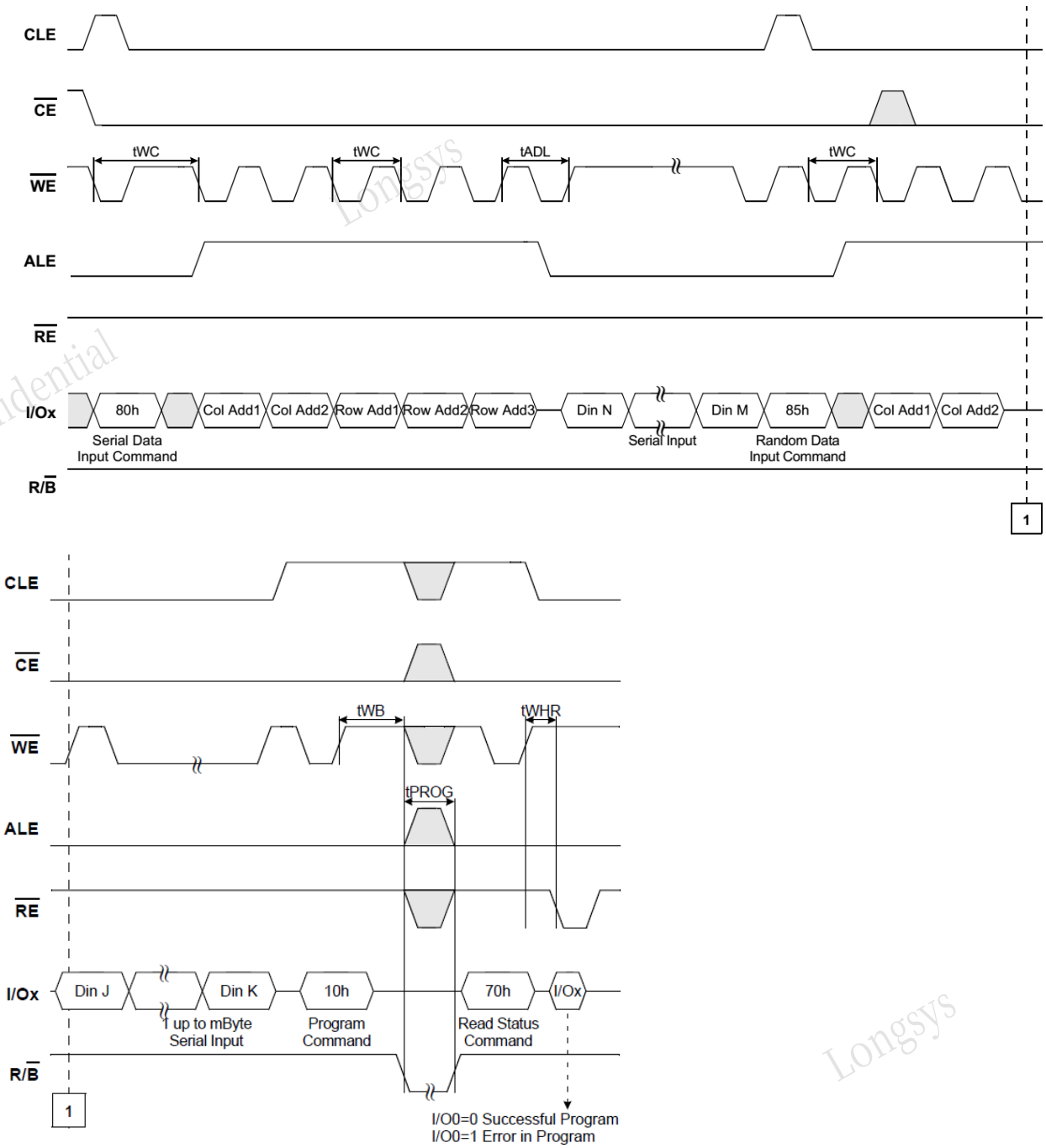

Figure 30 Random Data Input Timings

Notes:
1. tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.
2. Random data input can be performed in a page.

6.15. Copy-Back Program Operation Timings with Random Data Input

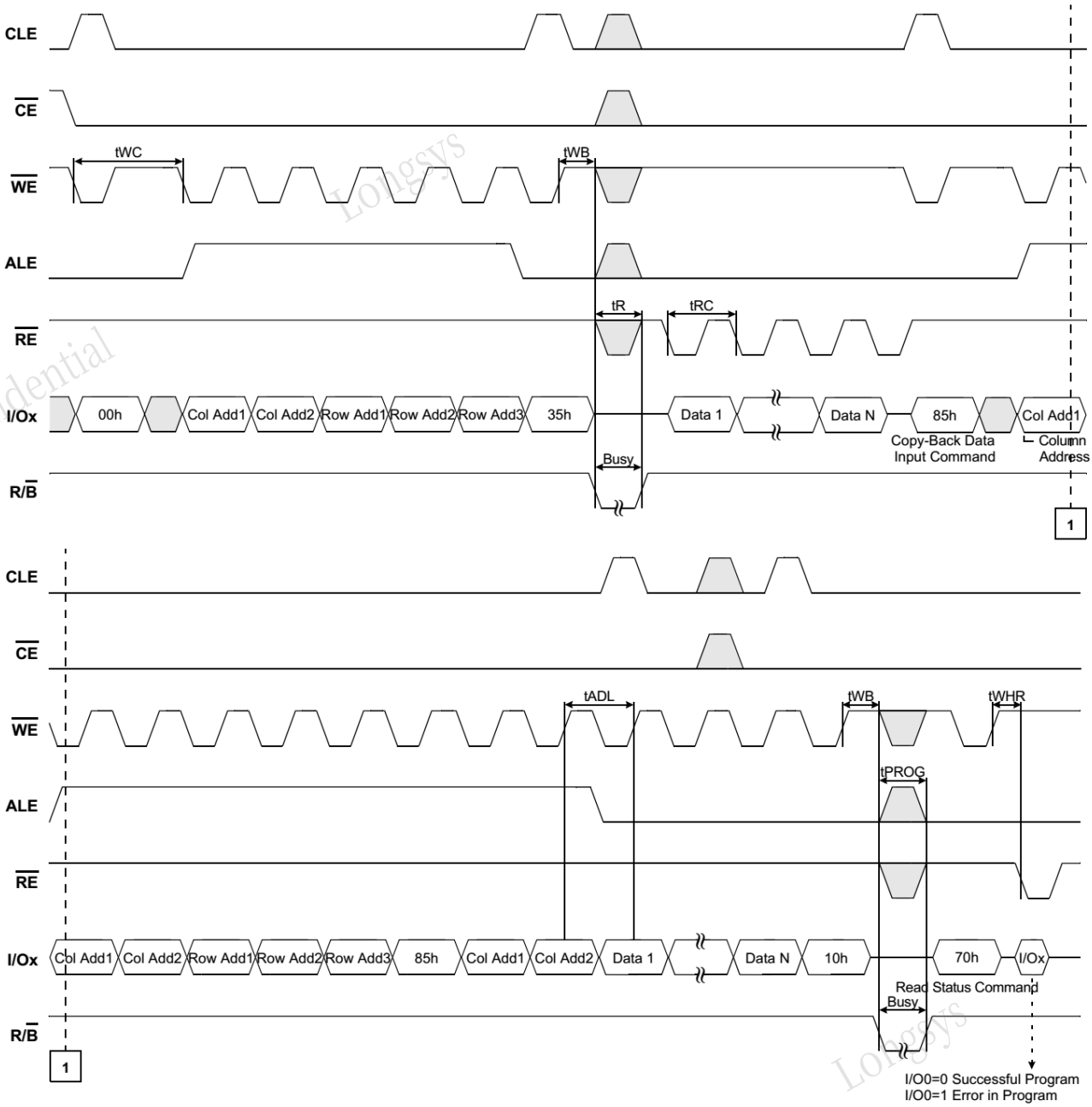

Figure 31 Copy-Back Program Operation Timings with Random Data Input

Notes:
1. Copy-Back Program operation is allowed only within the same memory plane.
2. On the same plane, It's prohibited to operate copy-back program from an odd address page(source page) to an even address page(target page) or from an even address page(source page) to an odd address page(target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.
3. tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

6.16. Page Program Operation Timings with CE# don't care

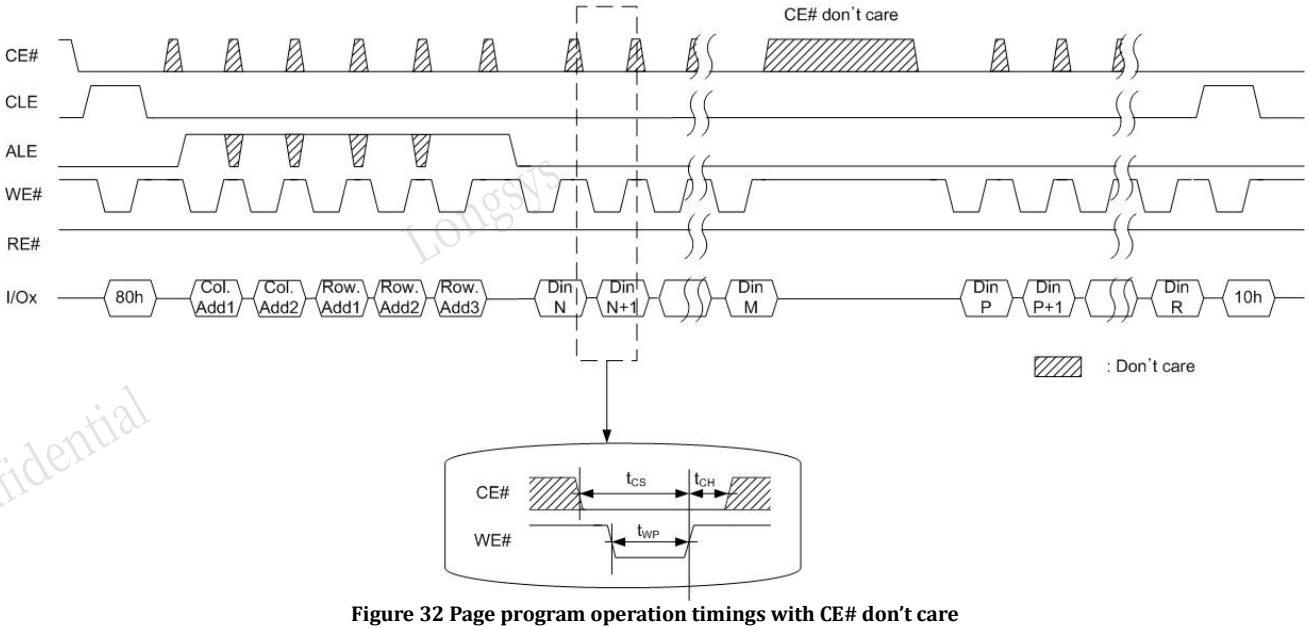

Figure 32 Page program operation timings with CE# don't care

Note:
tADL is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

6.17. Cache Program Operation Timings

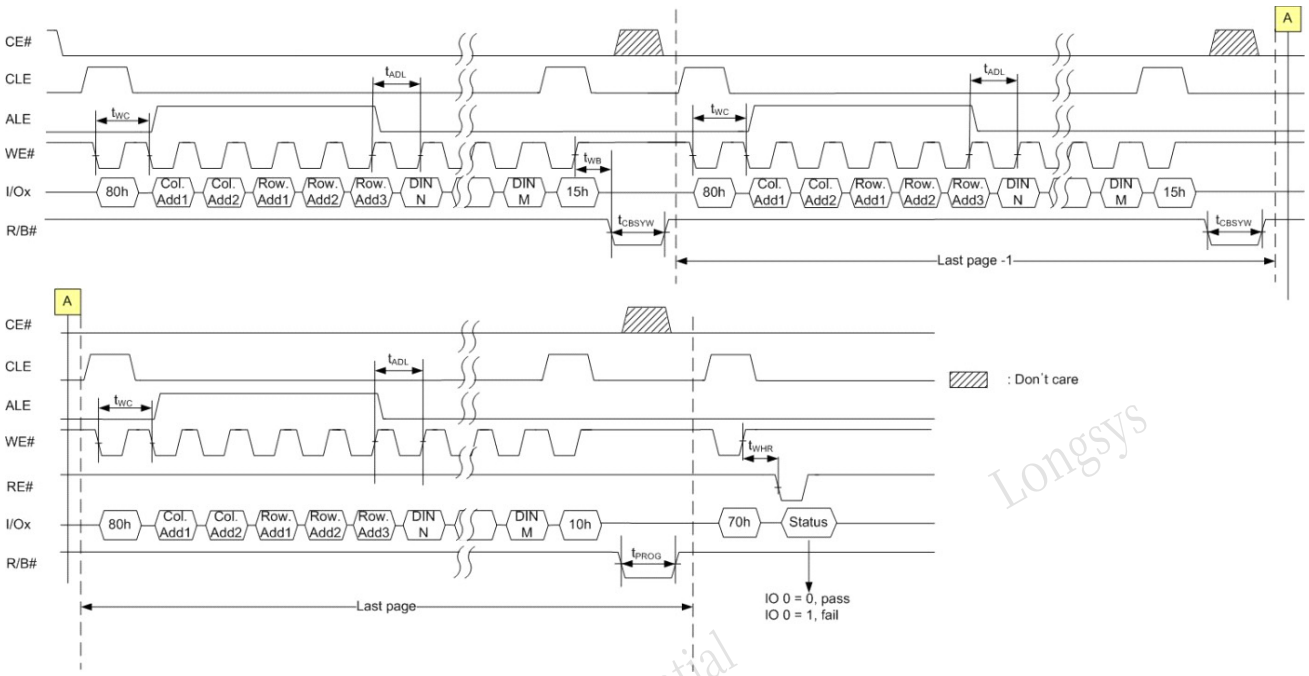

Figure 33 Cache Program Operation

Note:
tPROG = Program time for the last page + Program time for the (last -1)th page- (command input cycle time + address input cycle time + Last page data loading time)

6.18. Block Erase Operation

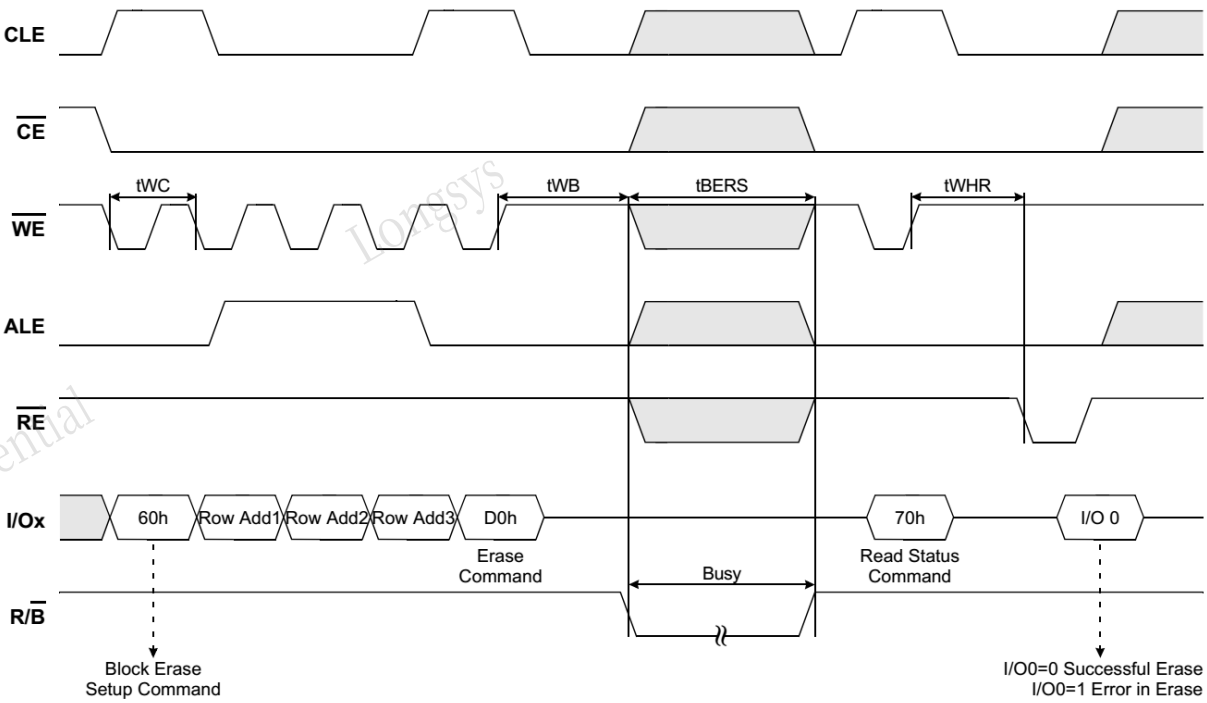

Figure 34 Block Erase Operation

6.19. Reset

Figure 35 Reset

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6.20. Multi-plane program

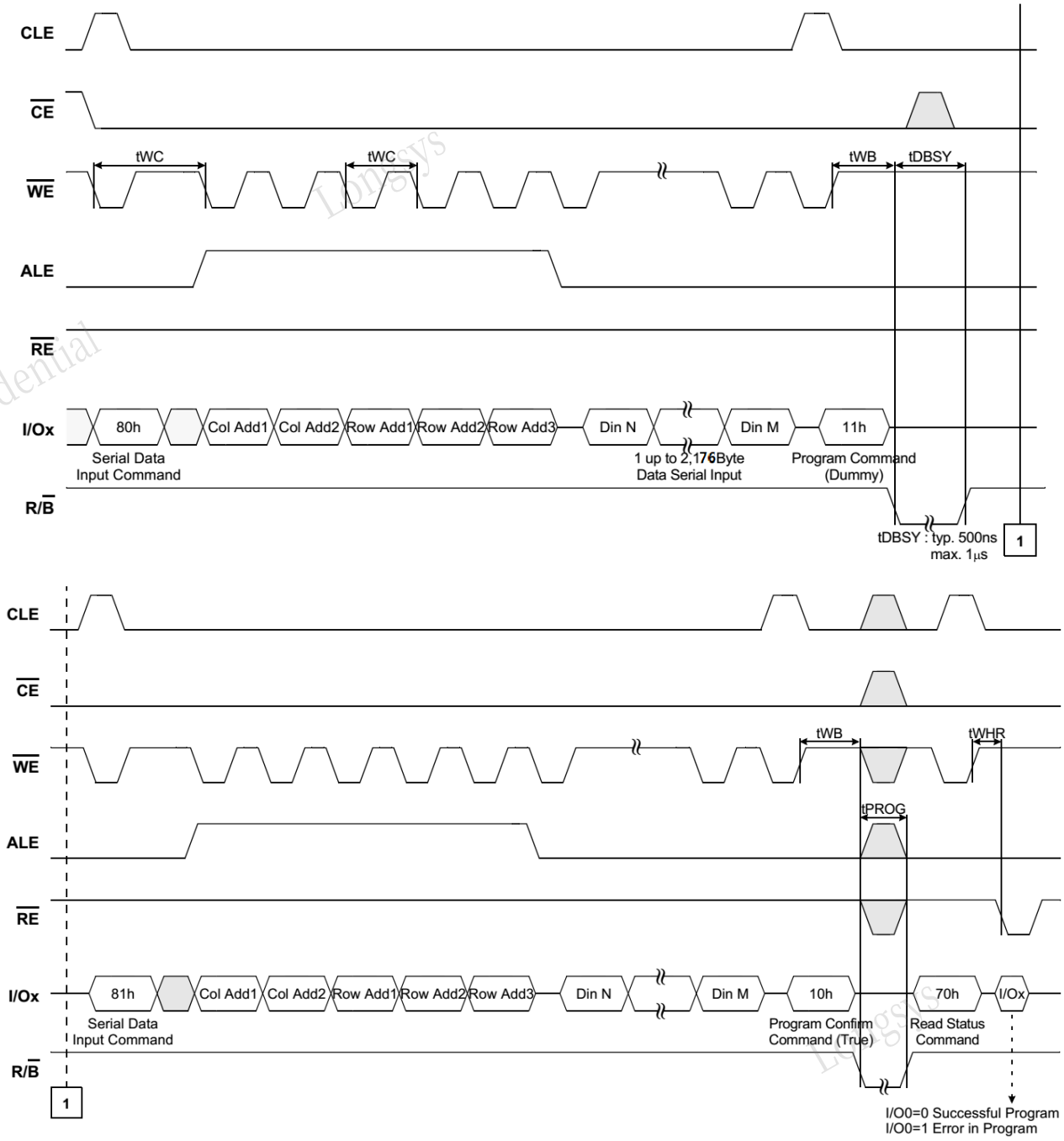

Figure 36 Multi-plane program

Notes:
Any command between 11h and 81h is prohibited except 70h, 78h and FFh

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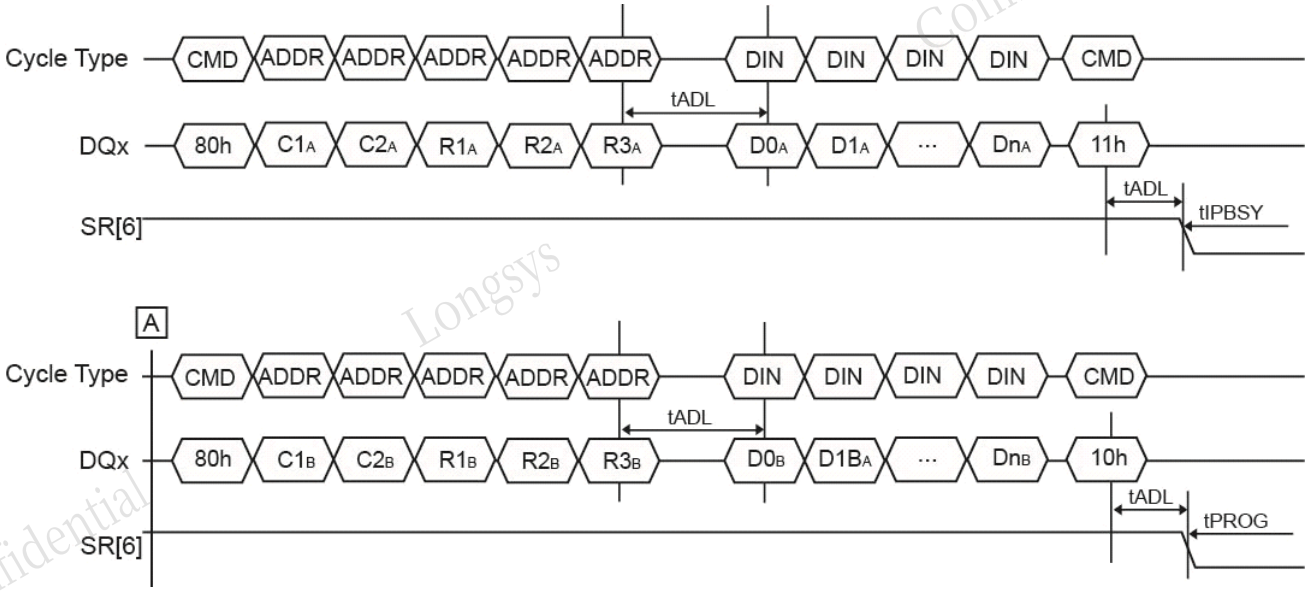
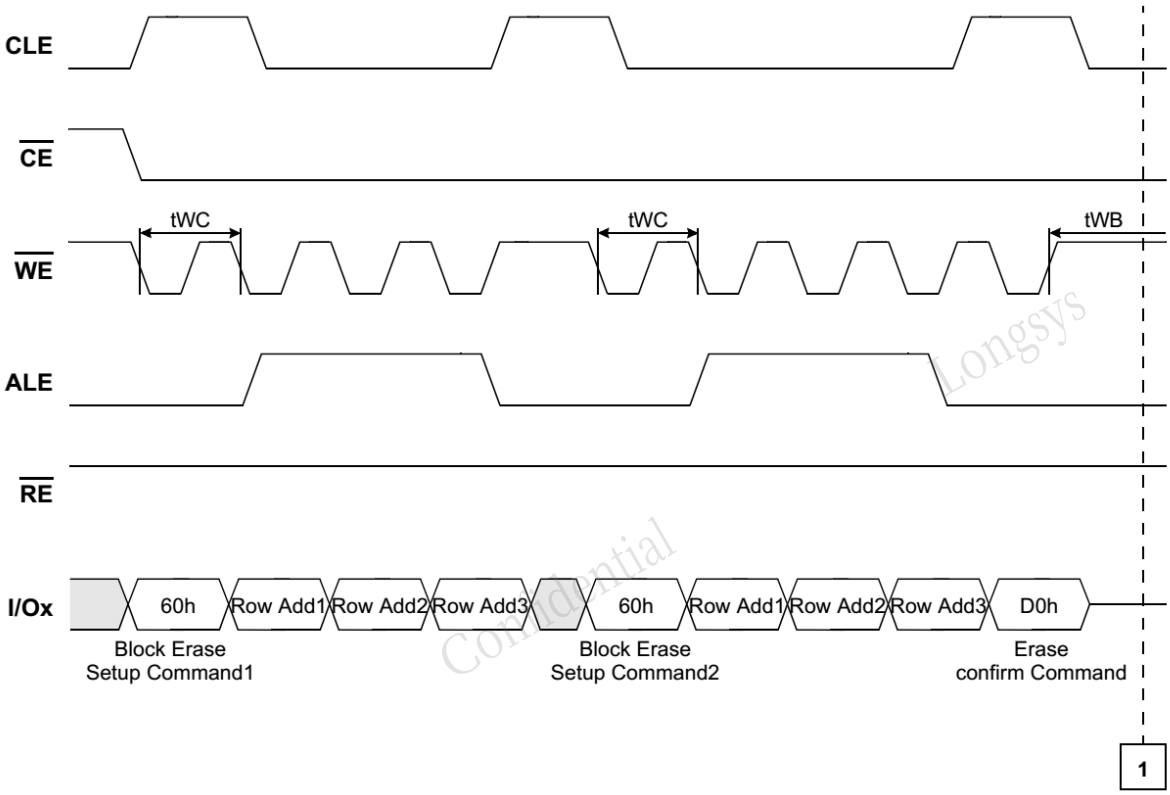


Figure 37 : Multi-plane page program (ONFI 1.0 protocol)

Notes:
C1A-C2A Column address for page A. C1A is the least significant byte.
R1A-R3A Row address for page A. R1A is the least significant byte.
D0A-DnA Data to program for page A.
C1B-C2B Column address for page B. C1B is the least significant byte.
R1B-R3B Row address for page B. R1B is the least significant byte.
D0B-DnB Data to program for page B.
Same restrictions on address of pages A and B, and allowed commands as **Figure 36** apply

6.21. Multi-plane Block Erase



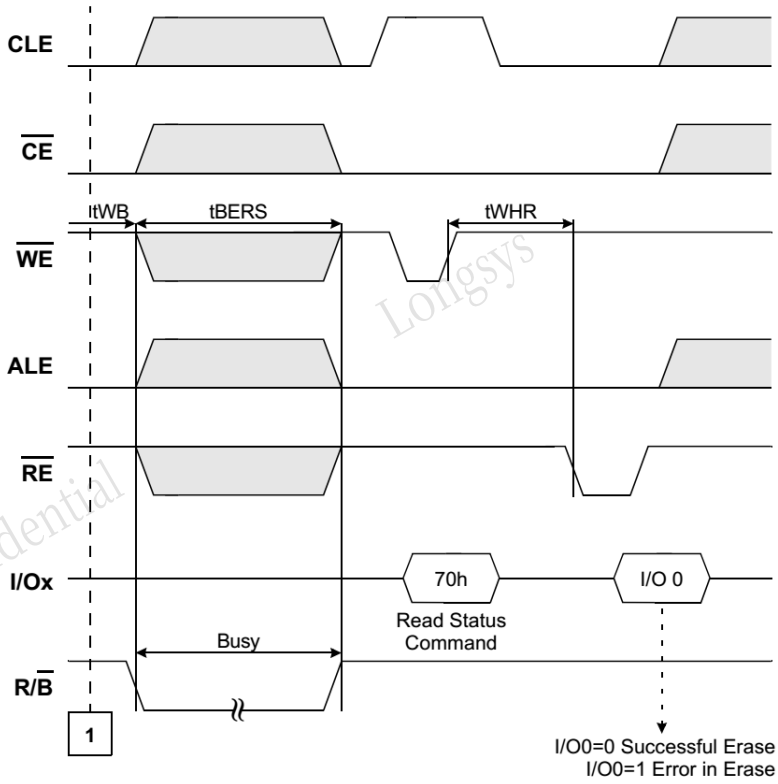


Figure 38 : Multi-plane block erase (traditional protocol)

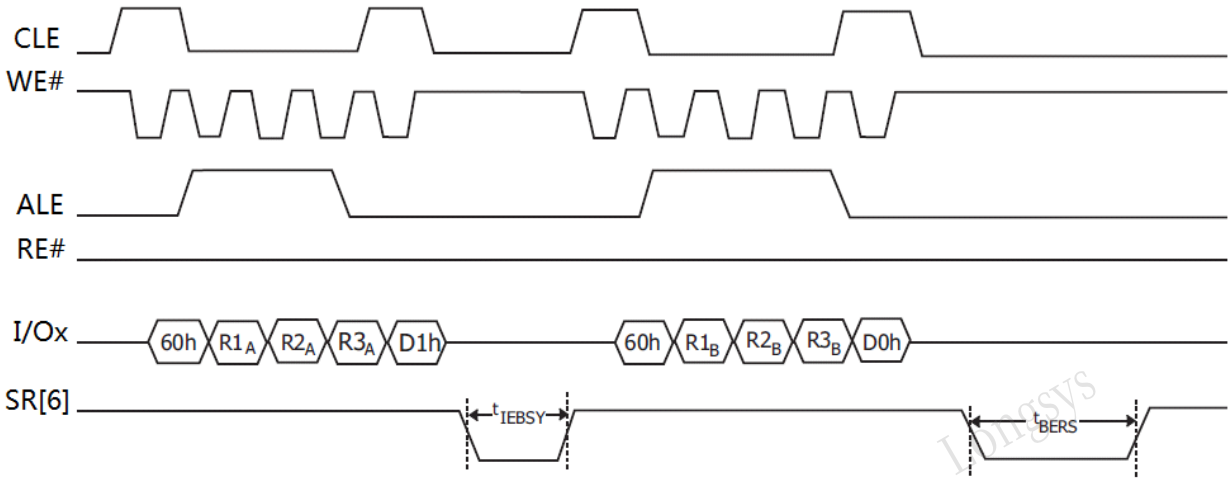


Figure 39 : Multi-plane block erase (ONFI 1.0 protocol)

Notes:
R1A-R3A Row address for block on plane 0. R1A is the least significant byte.
R1B-R3B Row address for block on plane 1. R1B is the least significant byte.
Same restrictions on address of blocks on plane 0(A) and 1(B) and allowed commands as **Figure 40** apply

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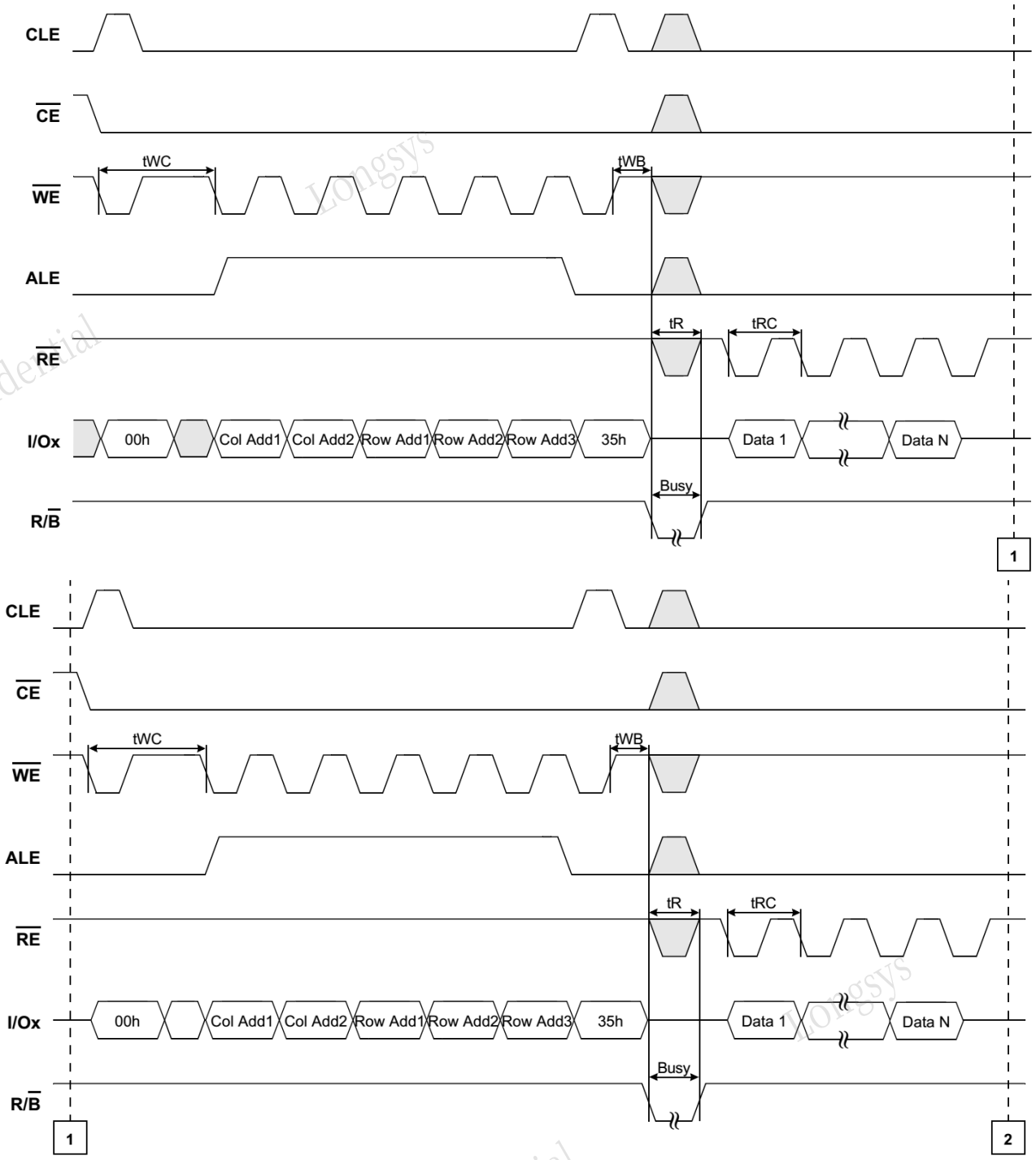
6.22. Multi-plane copy-back Program



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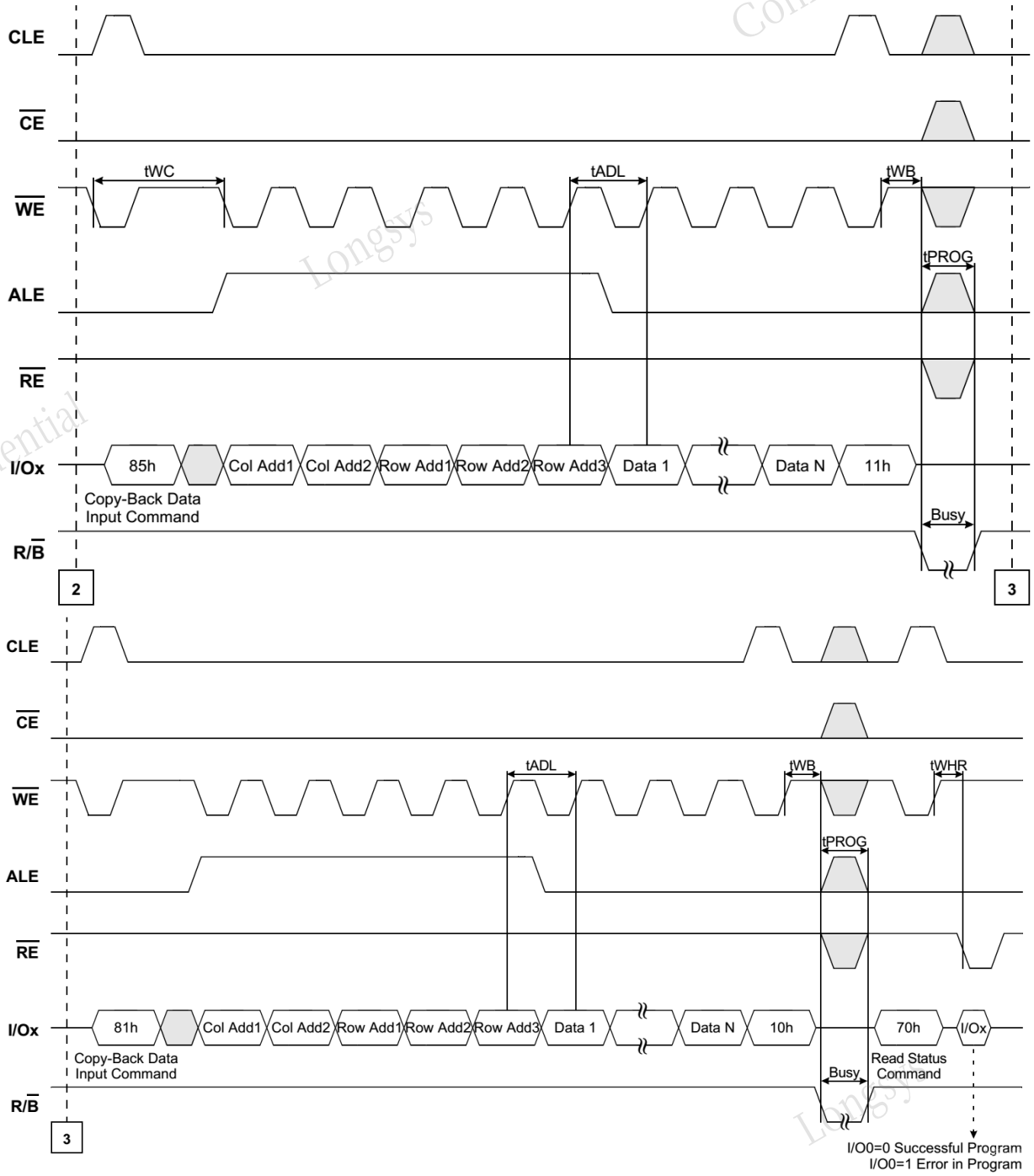

Figure 40 : Multi-plane copy-back program (traditional protocol)

Notes:
1. Copy-back program operation is allowed only within the same memory plane.
2. On the same plane it is prohibited to operate copy-back program from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page). Therefore, the copy-back program is permitted just between odd address pages or even address pages.
3. Any command between 11h and 81 h is prohibited except 70h and FFh.

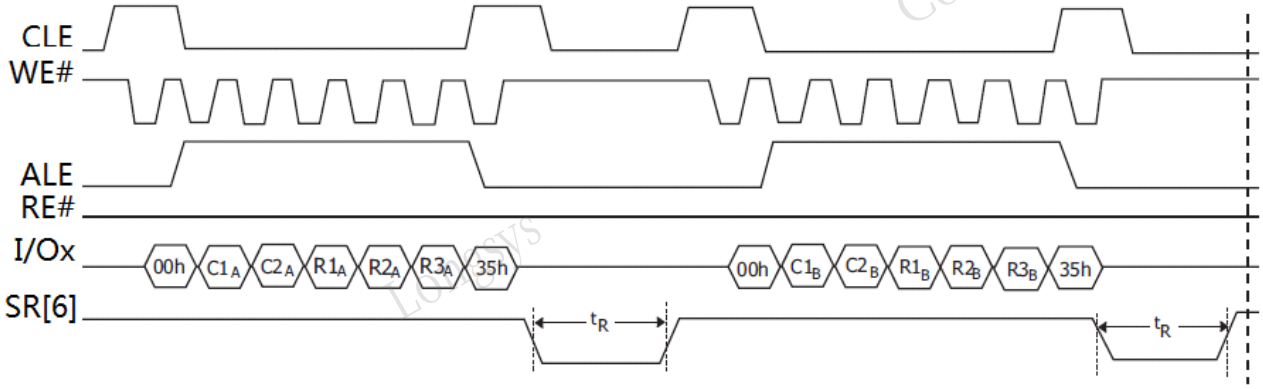

Figure 41 : Multi-plane copy-back read (ONFI 1.0 protocol)

Notes:
C1A-C2A Column address for page A. C1A is the least significant byte.
R1A-R3A Row address for page A. R1A is the least significant byte.
C1B-C2B Column address for page B. C1B is the least significant byte.
R1B-R3B Row address for page B. R1B is the least significant byte.

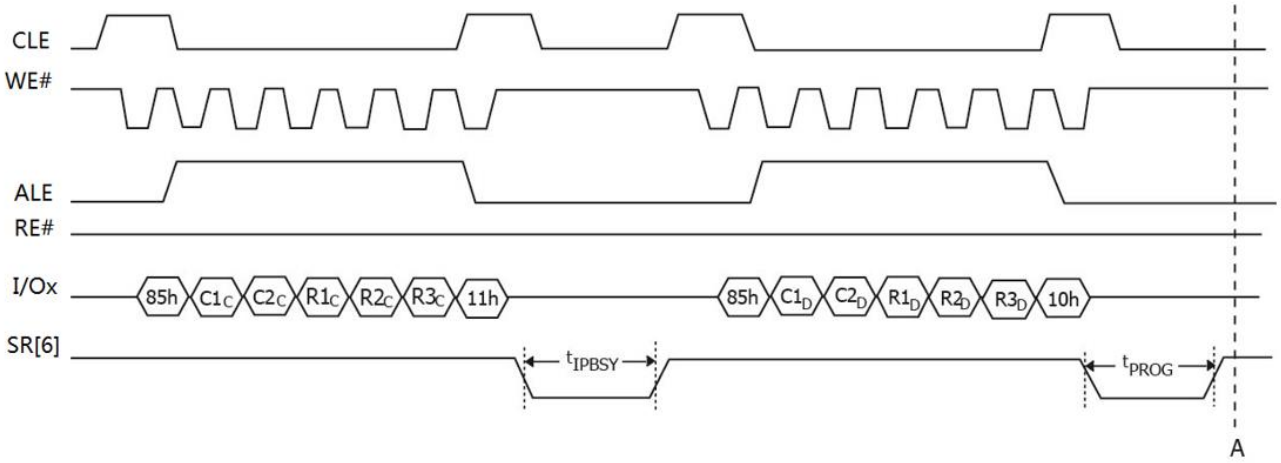

Figure 42 : Multi-plane copy-back program (ONFI 1.0 protocol)

Notes:
C1C-C2C Column address for page C. C1A is the least significant byte.
R1C-R3C Row address for page C. R1A is the least significant byte.
D0C-DnC Data to program for page C.
C1D-C2D Column address for page D. C1B is the least significant byte.
R1D-R3D Row address for page D. R1B is the least significant byte.
D0D-DnD Data to program for page D.
Same restrictions on address of pages C and D, and allowed commands as **Figure 28** apply

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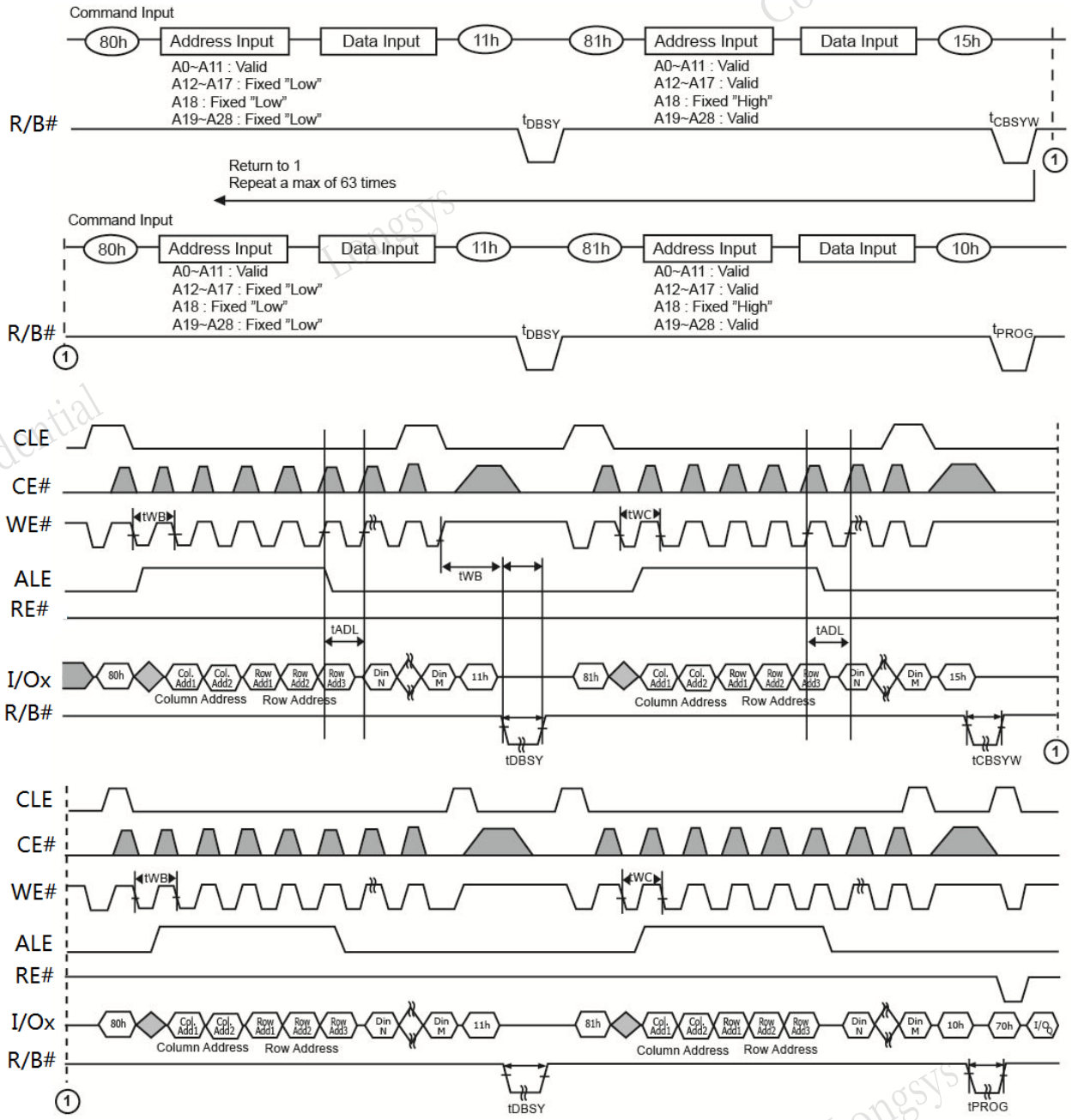

Figure 43 : Multi-plane cache program (traditional protocol)

Notes:
Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.

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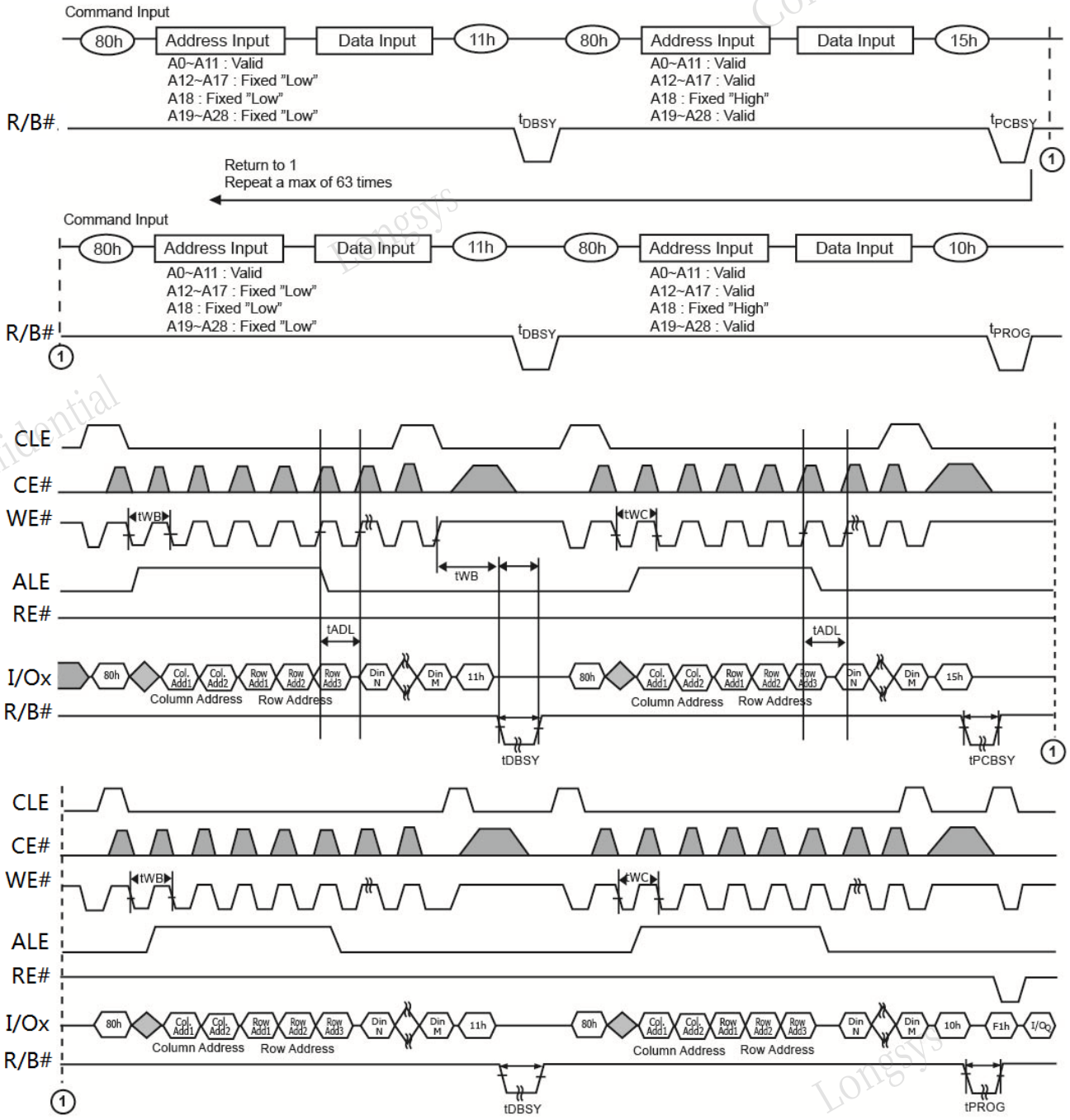

Figure 44 : Multi-plane cache program (ONFI protocol)

Notes:
Read Status register (70h) is used in the figure. Read Status Enhanced (78h) can be also used.

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6.23. Page Re-program

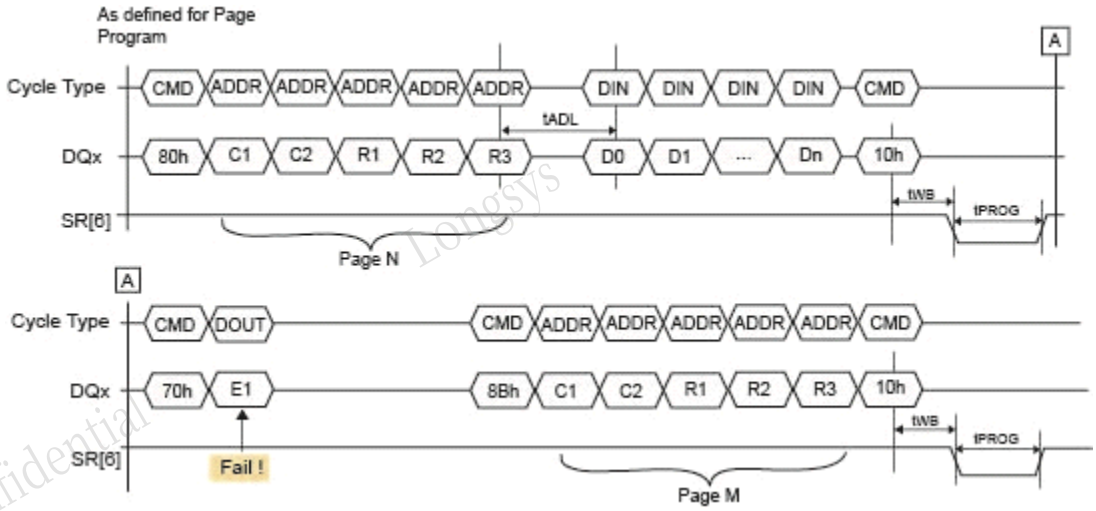

Figure 45 : Page Re-program

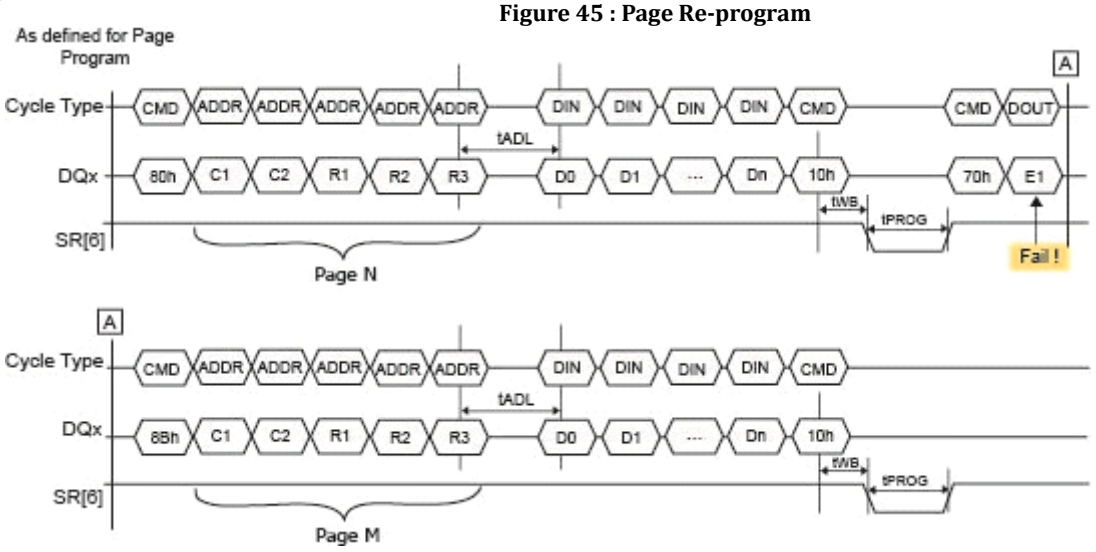

Figure 46 : Page Re-program with data manipulation

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6.24. Multi-plane Page Re-program

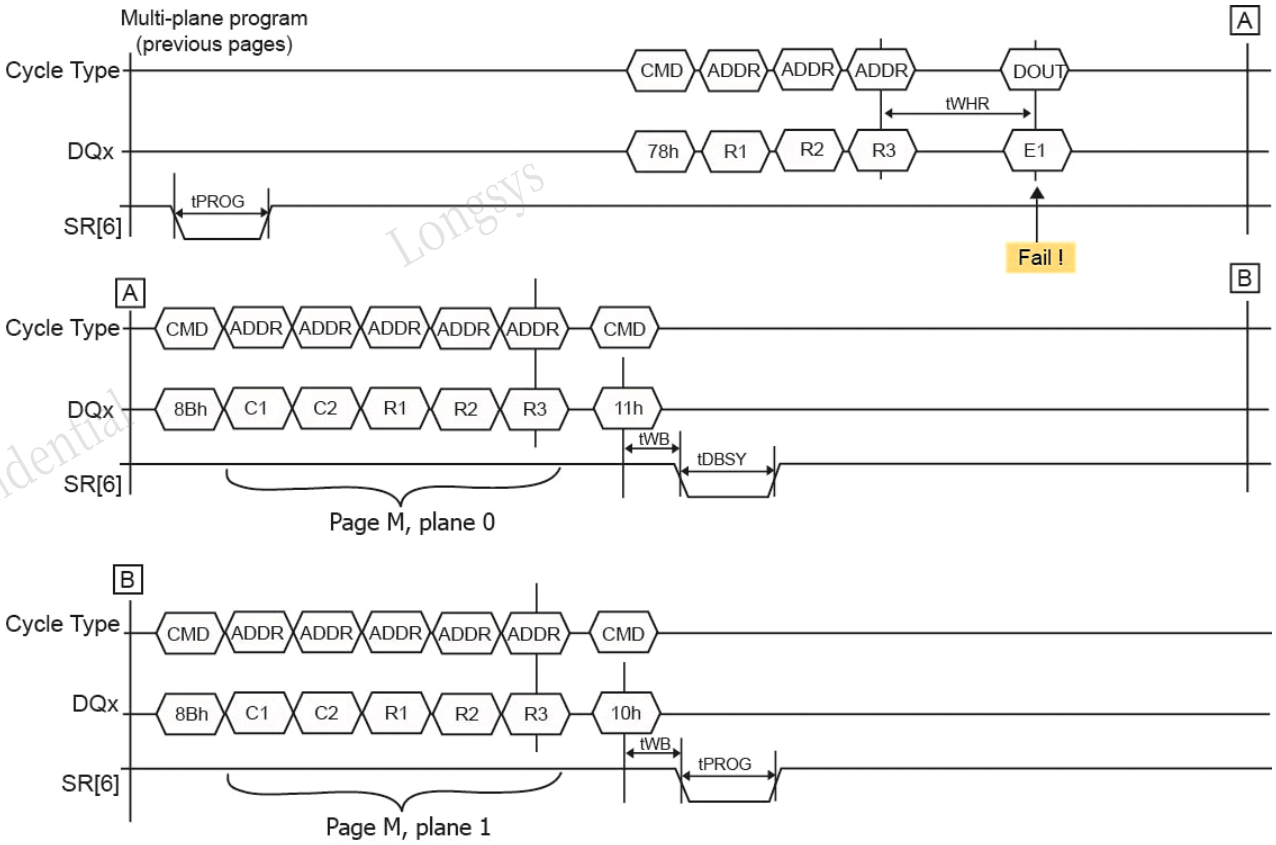

Figure 47 : Multi-plane Page Re-program

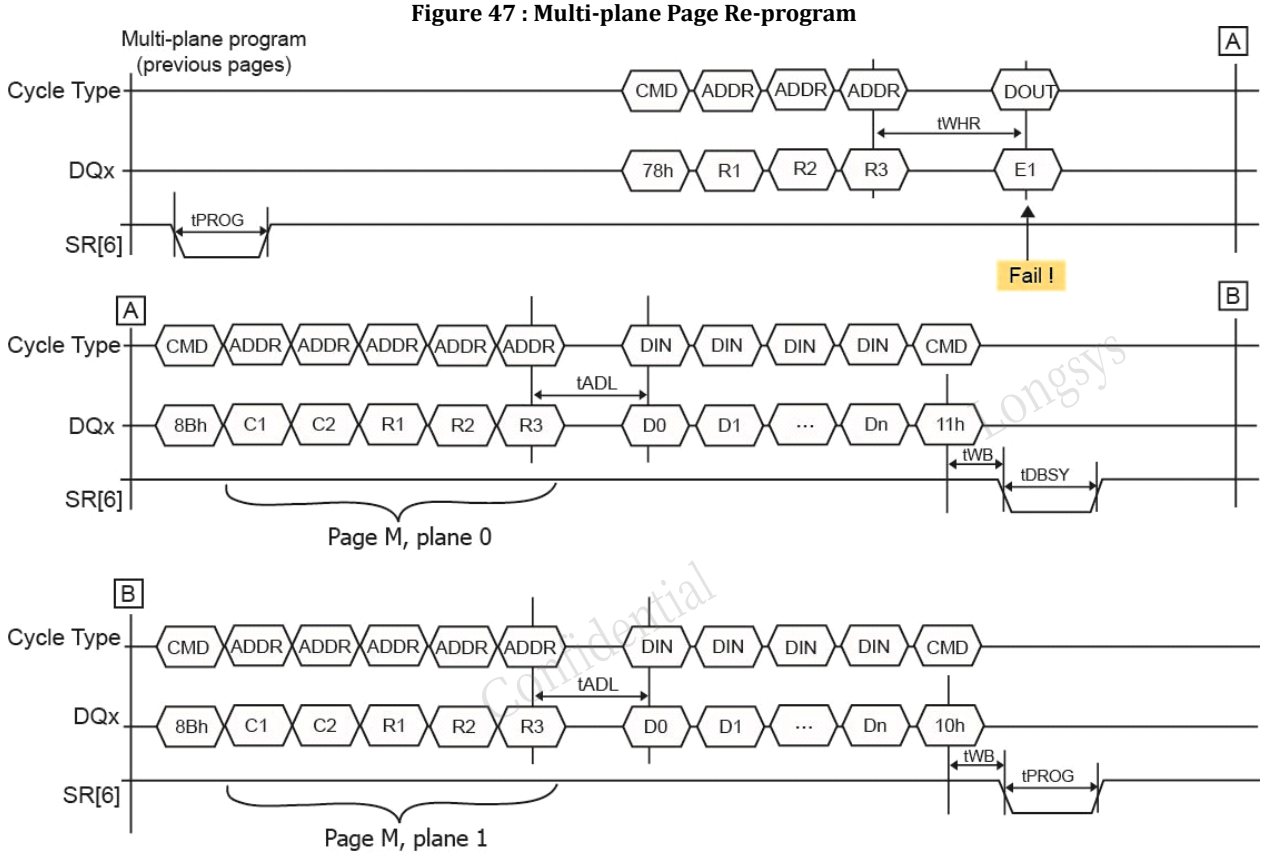

Figure 48: Multi-plane Page Re-program with data manipulation

6.25. ONFI signature timing

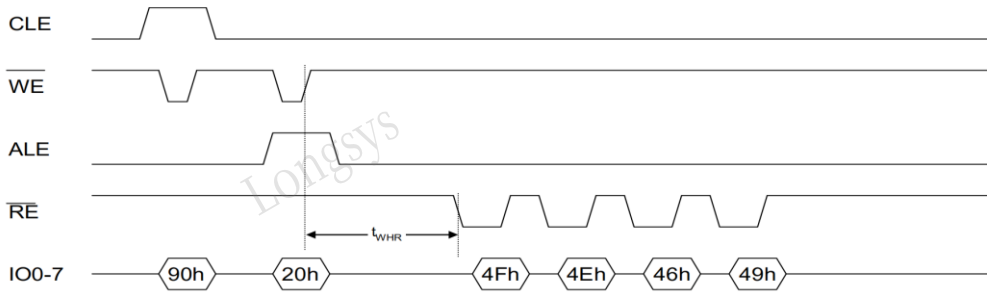

Figure 49 : ONFI signature timing

6.26. Read Parameter Page timings signature timing

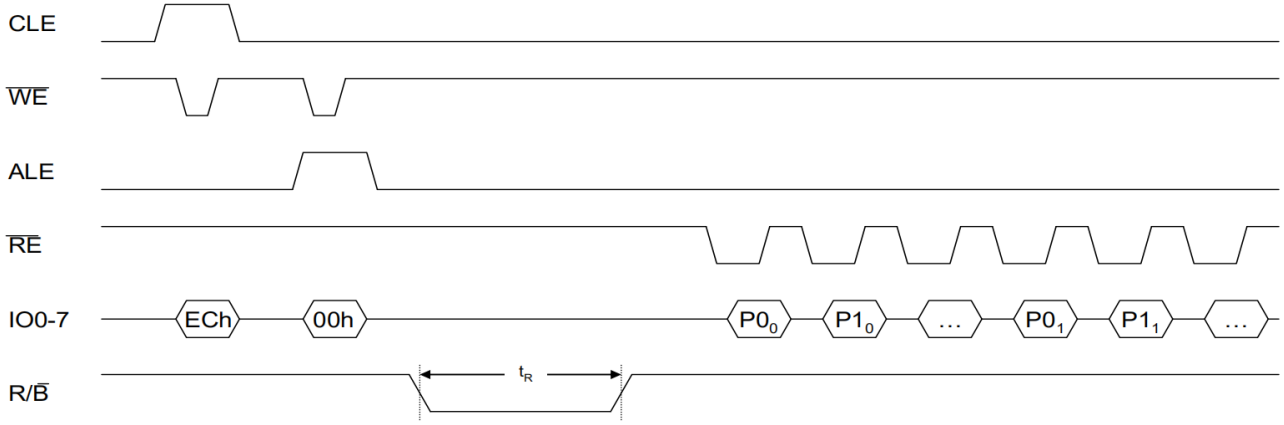

Figure 50 : Read Parameter Page timings

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7. Physical Diagram

7.1. 48-Pin Thin Small Outline Package(TSOP)

Unit :mm/Inch

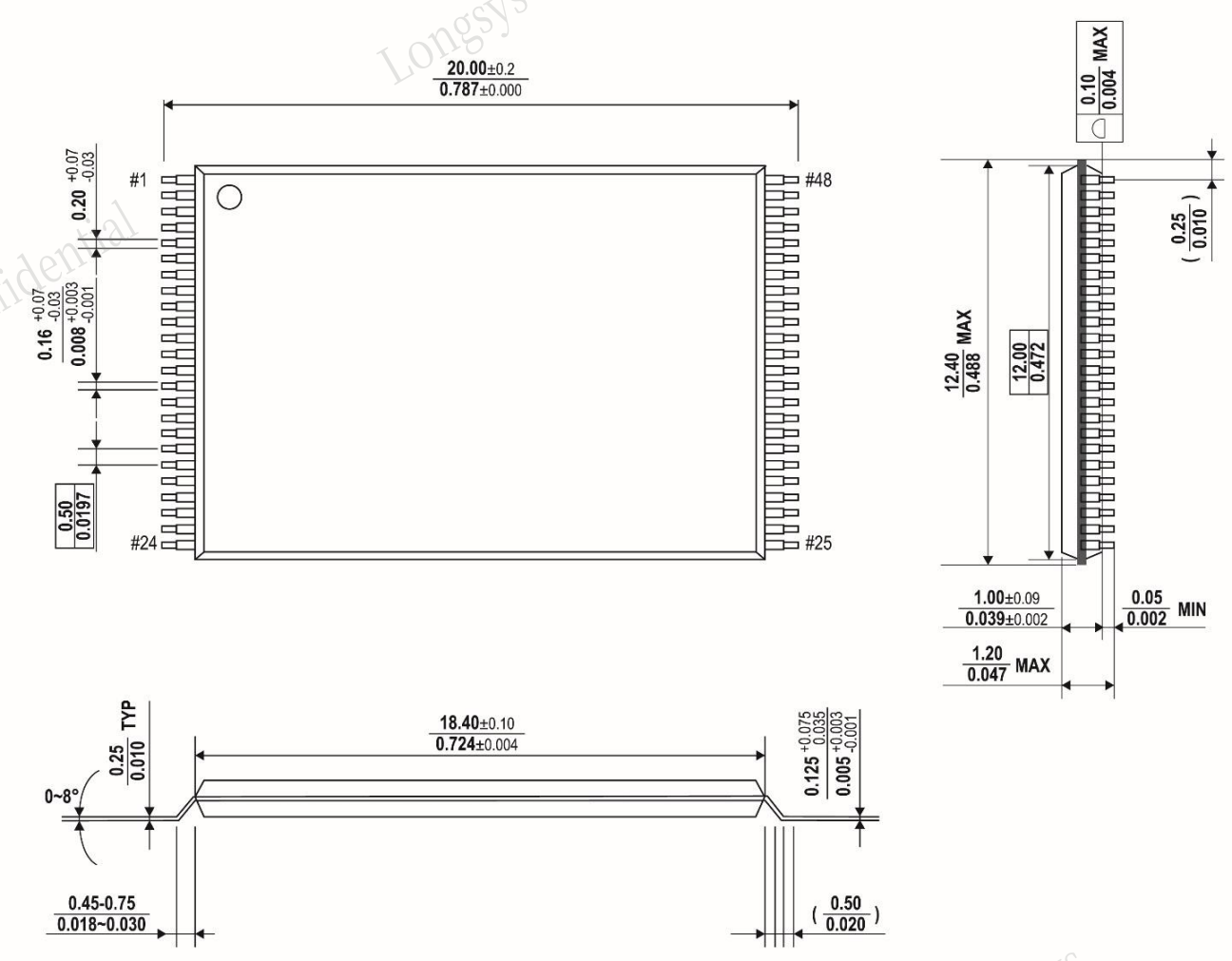

Figure 51 48-Pin Thin Small Outline Package

7.2. 63-Pin Ball Grid Array (BGA)

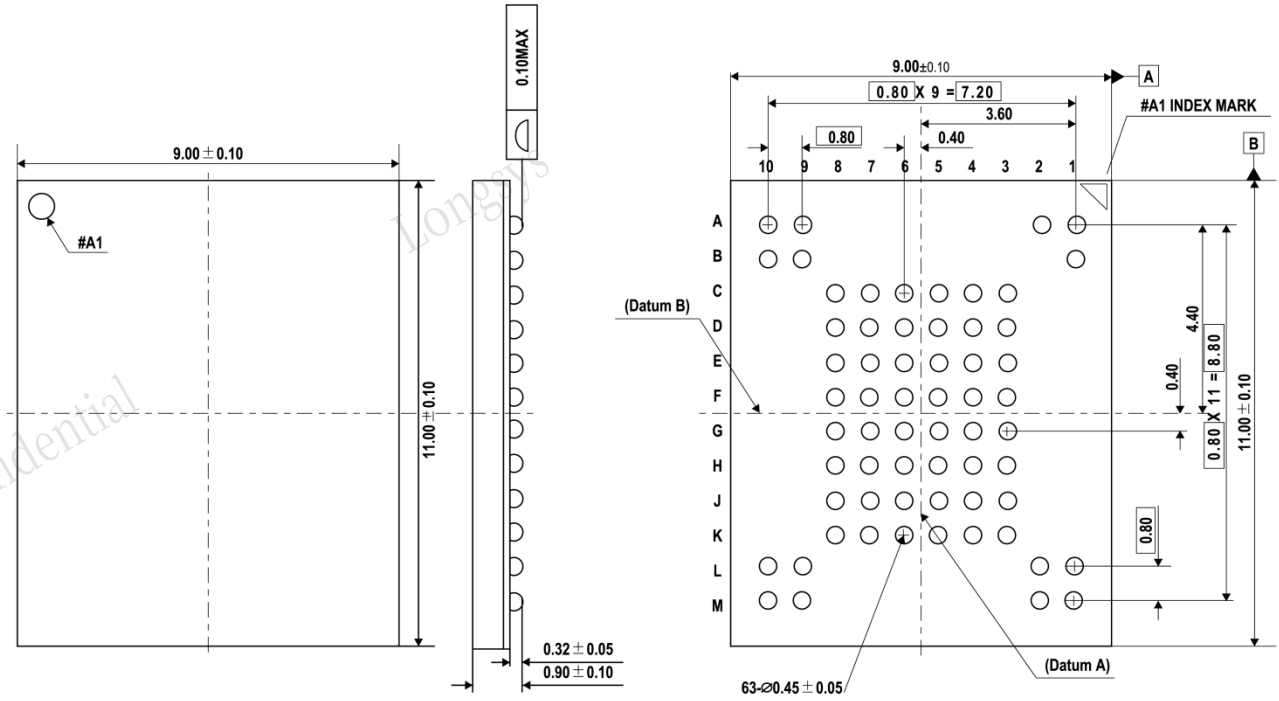

Figure 52 63-Pin Ball Grid Array

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