LMH32401 500MHz 可编程增益、差分输出跨阻放大器

1 特性

- 集成的可编程增益：2kΩ 或 20kΩ
- 性能：增益 = 2kΩ、C_{PD} = 1pF：
  - 带宽：500MHz
  - 输入参考噪声：250nA$_{RMS}$
  - 上升、下降时间：0.7ns
- 性能：增益 = 20kΩ、C_{PD} = 1pF：
  - 带宽：250MHz
  - 输入参考噪声：49nA$_{RMS}$
  - 上升、下降时间：1.25ns
- 集成式环境光消除
- 集成式 100mA 保护钳位
- 集成式输出多路复用器
- 宽输出摆幅：1.5V$_{PP}$
- 静态电流：30mA
- 温度范围：-40 至 +125°C

2 应用

- 机械扫描激光雷达
- 固态扫描激光雷达
- 激光测距仪
- 光学 ToF 位置传感器
- 无人机视觉
- 工业机器人激光雷达
- 移动机器人激光雷达
- 扫地机器人激光雷达

3 说明

LMH32401 是一款可编程增益、单端、输入转差分输出跨阻放大器，适用于光探测和测距 (LIDAR) 应用 和激光测距系统。可以为 LMH32401 配置 2kΩ 或 20kΩ 增益。LMH32401 具有 1.5V$_{PP}$ 的输出摆幅，可驱动 100Ω 负载。

LMH32401 集成了一个 100mA 钳位，可以为放大器提供保护并允许器件迅速从过载输入状况中恢复。LMH32401 还 具有 一个集成式环境光消除电路，可取代光电二极管与放大器之间的交流耦合，从而节省布板空间和系统成本。当需要直流耦合时，可以禁用环境光消除电路。

当不使用放大器时，可以使用 $\overline{EN}$ 引脚将 LMH32401 置于低功耗模式，以节省能源。将放大器置于低功耗模式会使其输出引脚进入高阻抗状态。此功能允许多个 LMH32401 放大器多路复用到单个 ADC 中，$\overline{EN}$ 控制引脚将用作多路复用器选择功能。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMH32401	VQFN (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

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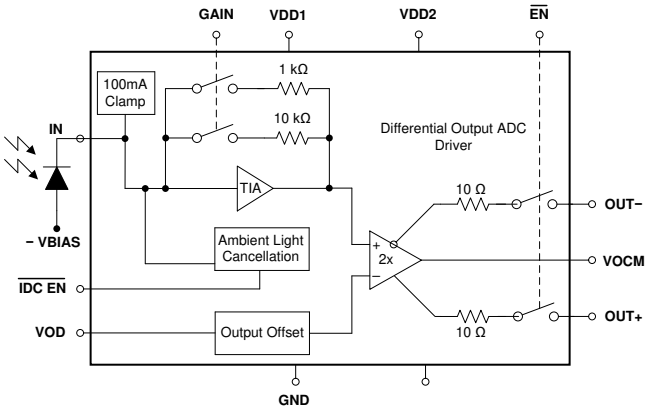
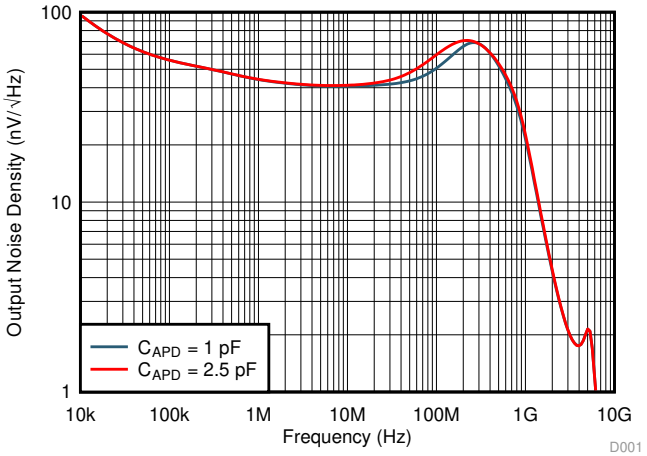
简化框图



输出噪声密度（增益 = 20kΩ）



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2019 年 10 月	*	初始发行版。

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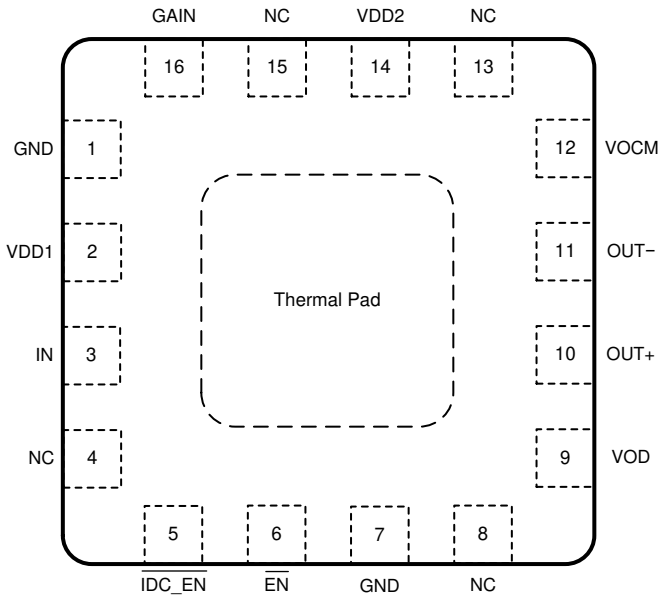
5 Pin Configuration and Functions

RGT Package
16-Pin VQFN With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	6	I	Device enable pin. $\overline{EN}$ = logic low = normal operation (default)(1); $\overline{EN}$ = logic high = power off mode.
GAIN	16	I	Gain setting. GAIN = low = 2 kΩ (default)(1); GAIN = high = 20 kΩ.
GND	1, 7	I	Amplifier ground.
$\overline{IDC_EN}$	5	I	Ambient light cancellation loop enable. $\overline{IDC_EN}$ = logic low = enable DC cancellation (default)(1); $\overline{IDC_EN}$ = logc high = disable DC cancellation.
IN	3	I	Transimpedance amplifier input.
NC	4, 8, 13, 15	—	No connect
OUT–	11	O	Inverting amplifier output. When light is incident on the photodiode the output pin transitions in a negative direction from the no light condition.
OUT+	10	O	Noninverting amplifier output. When light is incident on the photodiode the output pin transitions in a positive direction from the no light condition.
VDD1	2	I	Positive power supply for the transimpedance amplifier stage.
VDD2	14	I	Positive power supply for the differential amplifier stage. Tie VDD1 and VDD2 to the same power supply with independent power-supply bypassing.
VOCM	12	I	Differential amplifier common-mode output setting.
VOD	9	I	Differential amplifier differential output offset setting.
Thermal pad		—	Connect the thermal pad to GND or the most negative power supply of the device under test (DUT).

(1) TI recommends driving a digital pin with a low-impedance source rather than leaving the pin floating because fast-moving transients can couple into the pin and inadvertently change the logic level.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD1}, V_{DD2}	Total supply voltage, V_{DD}(2)		3.55	V
	Voltage at output pins	–1	V_{DD} + 1	V
	Voltage at logic pins	–1	V_{DD} + 1	V
I_{IN}	Continuous current into IN		25	mA
I_{OUT}	Continuous output current		25	mA
T_J	Junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VDD1 and VDD2 should always be tied to the same supply and have separate power-supply bypass capacitors.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Total supply voltage	3	3.3	3.45	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMH32401 RGT (VQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	31.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics: Gain = 2 kΩ

V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, GAIN = 0 V, $\overline{IDC_EN}$ = 3.3 V, R_L = 100 Ω, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 100 mV_{PP}		500		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		475		MHz
t_R, t_F	Rise and fall time	V_{OUT} = 100 mV_{PP}, Pulse width = 10 ns		0.7		ns
	Slew rate (2)	V_{OUT} = 1 V_{PP}, Pulse width = 10 ns		1100		V/µs
	Overload recovery time (1% settling)	I_{IN} = 100 mA, Pulse width = 10 ns		5		ns
	Overload pulse extention (3)	I_{IN} = 100 mA, Pulse width = 10 ns		4		ns
i_N	Integrated input current noise	f = 500 MHz		250		nA_{RMS}
DC PERFORMANCE						
Z_{21}	Small-signal transimpedance gain (4)		1.75	2	2.25	kΩ
V_{OD}	Differential output offset voltage ($V_{OUT-} – V_{OUT+}$)		–12	3.5	12	mV
$\Delta V_{OD}/\Delta T_A$	Differential output offset voltage drift			4.5		µV/°C
INPUT PERFORMANCE						
V_{IN}	Default input bias voltage	Input pin floating	2.42	2.47	2.52	V
$\Delta V_{IN}/\Delta T_A$	Default input bias voltage drift	Input pin floating		1.1		mV/°C
I_{IN}	DC input current range	Z_{21} < 3-dB degradation from I_{IN} = 50 µA	600	705		µA

(1) Input capacitance of photodiode.
(2) Average of rising and falling slew rate.
(3) Pulse width extension measured at 50% of pulse height of a square wave.
(4) Gain measured at the amplifier output pins when driving a 100-Ω resistive load. At higher resistor loads the gain increases.

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6.6 Electrical Characteristics: Gain = 20 kΩ

V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, GAIN = 3.3 V, $\overline{IDC_EN}$ = 3.3 V, R_L = 100 Ω, and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 100 mV_{PP}		250		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		250		MHz
t_R, t_F	Rise and fall time	V_{OUT} = 100 mV_{PP}, Pulse width = 10 ns		1.25		ns
	Slew rate (2)	V_{OUT} = 1 V_{PP}, Pulse width = 10 ns		700		V/µs
	Overload recovery time (1% settling)	I_{IN} = 100 mA, Pulse width = 10 ns		9		ns
	Overload pulse extension (3)	I_{IN} = 100 mA, Pulse width = 10 ns		4		ns
i_N	Integrated input current noise	f = 250 MHz		49		nA_{RMS}
DC PERFORMANCE						
Z_{21}	Small-signal transimpedance gain (4)		17	20	22.5	kΩ
V_{OD}	Differential output offset voltage ($V_{OUT-} – V_{OUT+}$)		–15	5	15	mV
$\Delta V_{OD}/\Delta T_A$	Differential output offset voltage			±17.5		µV/°C
INPUT PERFORMANCE						
V_{IN}	Default input bias voltage	Input pin floating	2.42	2.47	2.52	V
$\Delta V_{IN}/\Delta T_A$	Default input bias voltage drift	Input pin floating		1.1		mV/°C
I_{IN}	DC input current range	Z_{21} < 3-dB degradation from I_{IN} = 5 µA	60	72		µA

(1) Input capacitance of photodiode.
(2) Average of rising and falling slew rate.
(3) Pulse width extension measured at 50% of pulse height of a square wave.
(4) Gain measured at the amplifier output pins when driving a 100-Ω resistive load. At higher resistor loads the gain increases.

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6.7 Electrical Characteristics: Both Gains

V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, GAIN = 0 V / 3.3 V, $\overline{IDC_EN}$ = 3.3 V, R_L = 100 Ω, and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT PERFORMANCE						
V_{OH}	Single-sided output voltage swing (high) (2)	T_A = 25°C	2.87	2.9		V
V_{OL}	Single-sided output voltage swing (low) (2)	T_A = 25°C		0.36	0.39	V
I_{OUT}	Linear output drive (sink and source)	T_A = 25°C, I_{IN} = 50 µA, Gain = 20 kΩ, R_L = 25 Ω	24	26.6	32	mA
		T_A = –40°C, I_{IN} = 50 µA, Gain = 20 kΩ, R_L = 25 Ω		27.1		
		T_A = 125°C, I_{IN} = 50 µA, Gain = 20 kΩ, R_L = 25 Ω		25.1		
I_{SC}	Output short-circuit current (differential) (3)			70		mA
Z_{OUT}	DC output impedance (amplifier enabled)	Differential impedance	18	21	24	Ω
Z_{OUT}	DC output impedance in shutdown	Differential impedance	2.8	3.3		kΩ
OUTPUT COMMON-MODE CONTROL (V_{OCM}) PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OCM} = 100 mV_{PP} at VOCM pin		285		MHz
LSBW	Large-signal bandwidth	V_{OCM} = 1 V_{PP} at VOCM pin		100		MHz
e_N	Output common-mode noise	f = 10 MHz, 1-nF capacitor to GND on VOCM pin		17.8		nV/√Hz
A_V	Gain, ($\Delta V_{OCM}/\Delta$VOCM)	IN floating, VOCM = 1.1 V (driven)		1		V/V
	Gain error	T_A = 25°C, VOCM = 0.7 V to 2.3 V	–2%	0.5%	2%	
		T_A = –40°C to 125°C, VOCM = 0.7 V to 2.3 V		±1%		
	Input impedance			17		kΩ
VOCM	VOCM pin default offset from 1.1 V	VOCM floating, (VOCM measured - 1.1 V)	–2.5	6.5	15	mV
	V_{OCM} error vs Input current [1- (V_{OCM} @ 50 µA/V_{OCM} @ 5 µA)]	I_{IN} = 5 µA, 50 µA (Gain = 20 kΩ), VOCM = 1.1 V (driven)	–0.05 %	0.01%	0.05%	
V_{OCM}	Output common-mode voltage, (V_{OUT+} + V_{OUT-})/2	T_A = 25°C, VOCM pin floating	1.05	1.1	1.15	V
	Output common-mode voltage drift, ($\Delta V_{OCM}/\Delta T_A$)	T_A = –40°C to 125°C, VOCM pin floating		70		µV/°C
V_{OCM}	Output common-mode voltage, (V_{OUT+} + V_{OUT-})/2	T_A = 25°C, VOCM pin driven to 1.1 V	1.05	1.1	1.15	V
	Output common-mode voltage drift, ($\Delta V_{OCM}/\Delta T_A$)	T_A = –40°C to 125°C, VOCM pin driven to 1.1 V		–14		µV/°C

(1) Input capacitance of photodiode.
(2) Output levels achieved by adjusting VOCM, VOD, and input current.
(3) Device cannot withstand continuous short-circuit between the differential outputs.

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Electrical Characteristics: Both Gains (continued)

V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, GAIN = 0 V / 3.3 V, $\overline{IDC_EN}$ = 3.3 V, R_L = 100 Ω, and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT DIFFERENTIAL OFFSET (V_{OD}) PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OD} = 100 mV_{PP} at VOD pin		45		MHz
LSBW	Large-signal bandwidth	V_{OD} = 1 V_{PP}		19.5		MHz
V_{OS_D}	Differential output offset, V_{OUT} = (V_{OUT-} –V_{OUT+})	IN floating, VOD = 0.5 V	490	510	530	mV
	Differential output offset drift, $\Delta V_{OS_D}/\Delta T_A$	IN floating, VOD = 0.5 V		0.03		mV/℃
V_{OS_D}	Differential output offset, V_{OUT} = (V_{OUT-} –V_{OUT+})	IN floating, VOD floating	490	510	530	mV
	Differential output offset drift, $\Delta V_{OS_D}/\Delta T_A$	IN floating, VOD floating		0.04		mV/℃
A_V	Gain, ($\Delta V_{OUT}/\Delta VOD$), where V_{OUT} = (V_{OUT-} –V_{OUT+})	IN floating, VOCM = 1.1 V (driven)		1.01		V/V
	Gain error	T_A = 25℃, VOD = 0 V to 1.2 V	–5%	±0.8%	5%	
		T_A = –40℃ to 125℃, VOD = 0 V to 1.2 V		±1.5%		
	Input impedance			2.5		kΩ
AMBIENT LIGHT CANCELLATION PERFORMANCE (IDC_EN = 0 V) (4)						
	Settling time (1% (2 mV) of settled V_{OS})	I_{IN} = 0 µA → 100 µA, GAIN = 2 kΩ		18		µs
		I_{IN} = 0 µA → 10 µA, GAIN = 20 kΩ		3		
		I_{IN} = 100 µA → 0 µA, GAIN= 2 kΩ		21		
		I_{IN} = 10 µA → 0 µA, GAIN = 20 kΩ		12		
	Ambient light current cancellation range	Differential output offset (V_{OUT-} – V_{OUT+}) shift from I_{DC} = 10 µA < ±10 mV	2	3		mA
POWER SUPPLY						
I_Q	Quiescent current, total	T_A = 25°C	24	28.9	33.5	mA
		T_A = 125°C		32		
		T_A = –40°C		27		
PSRR+	Positive power-supply rejection ratio, VDD1 = VDD2		54	66		dB
SHUTDOWN						
I_Q	Disabled quiescent current ($\overline{EN}$ = V_{DD})	T_A = 25°C	2.6	3.2	3.8	mA
		T_A = –40°C		2.3		
		T_A = 125°C		5.2		
	Disable pin input bias current	T_A = 25°C		65	80	µA

(4) Enabling the ambient light cancellation loop adds noise to the system.

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6.8 Electrical Characteristics: Logic Threshold and Switching Characteristics

V_{DD} = 3.3 V, V_{OCM} = Open, V_{OD} = 0 V, C_{PD} (1) = 1 pF, $\overline{EN}$ = 0 V, GAIN = 0 V / 3.3 V, $\overline{IDC_EN}$ = 3.3 V, R_L = 100 Ω, and T_A = 25℃. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC THRESHOLD PERFORMANCE						
	High gain enable, threshold voltage	Amplifier in high gain above this voltage		1.8	2	V
	Low gain enable, threshold voltage	Amplifier in low gain below this voltage	0.8	1		V
	$\overline{EN}$ control, disable threshold voltage	Amplifier disabled above this voltage		1.8	2	V
	$\overline{EN}$ control, enable threshold voltage	Amplifier enabled below this voltage	0.8	1		V
	$\overline{IDC_EN}$ control, disable threshold voltage	Ambient light cancellation loop disabled above this voltage		1.8	2	V
	$\overline{IDC_EN}$ control, enable threshold voltage	Ambient light cancellation loop enabled below this voltage	0.8	1		V
GAIN CONTROL TRANSIENT PERFORMANCE						
	High gain to low gain transition-time, (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP} (Initial condition), I_{DC} = 0 µA		90		ns
	Low gain to high gain transition-time, (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP} (Final condition), I_{DC} = 0 µA		750		ns
	High gain to low gain transition-time, (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP} (Initial condition), I_{DC} = 100 µA		4		µs
	Low gain to high gain transition-time, (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP} (Final condition), I_{DC} = 100 µA		4		µs
PD CONTROL TRANSIENT PERFORMANCE						
	Enable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA, GAIN = 2 kΩ		125		ns
	Disable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA, GAIN = 2 kΩ		3		ns
	Enable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA, GAIN = 20 kΩ		850		ns
	Disable transition-time (1% settling)	Ambient loop disabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 0 µA, GAIN = 20 kΩ		3		ns
	Enable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA, GAIN = 2 kΩ		10		µs
	Disable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA, GAIN = 20 kΩ		3.5		ns
	Enable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA, GAIN = 20 kΩ		4		µs
	Disable transition-time (1% settling)	Ambient loop enabled, f_{IN} = 25 MHz, V_{OUT} = 1 V_{PP}, I_{DC} = 100 µA, GAIN = 2 kΩ		3		ns

(1) Input capacitance of photodiode

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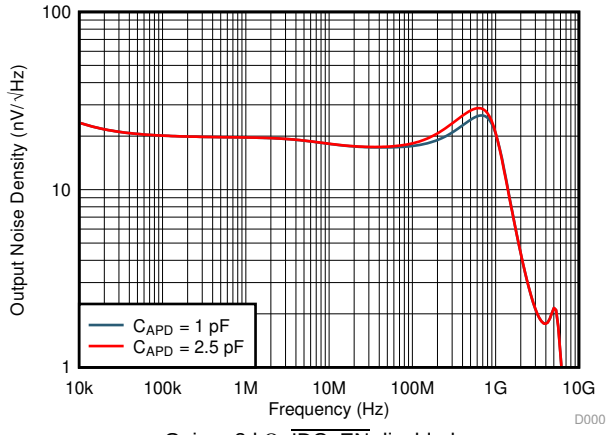
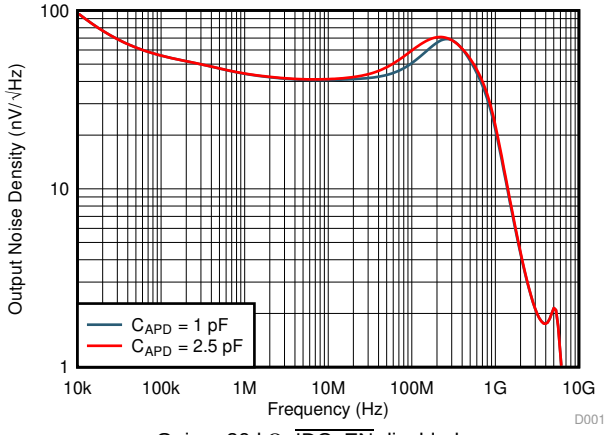
6.9 Typical Characteristics

at V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted)



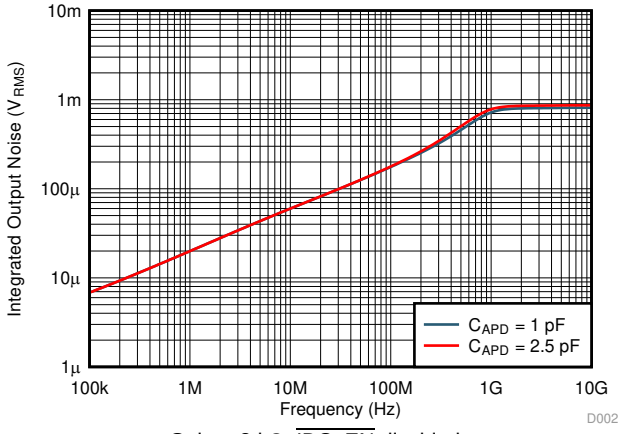
Gain = 2 kΩ, $\overline{IDC_EN}$ disabled

图 1. Output Noise Density vs Frequency



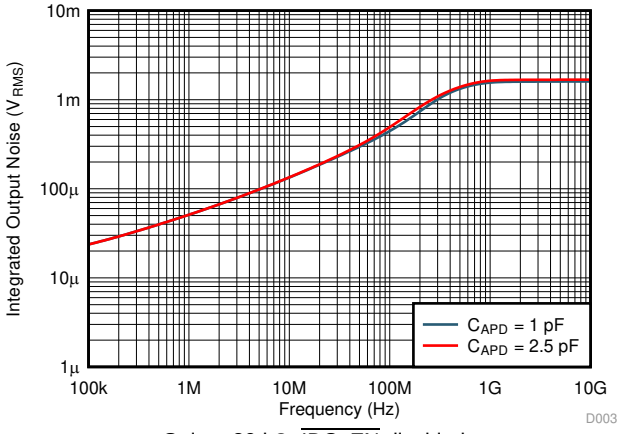
Gain = 20 kΩ, $\overline{IDC_EN}$ disabled

图 2. Output Noise Density vs Frequency



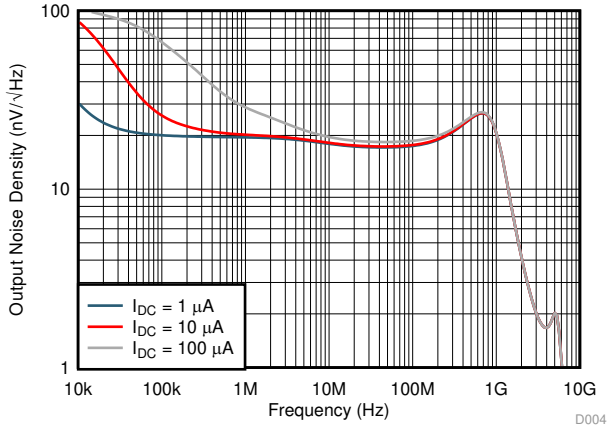
Gain = 2 kΩ, $\overline{IDC_EN}$ disabled

图 3. Integrated Output Noise vs Frequency



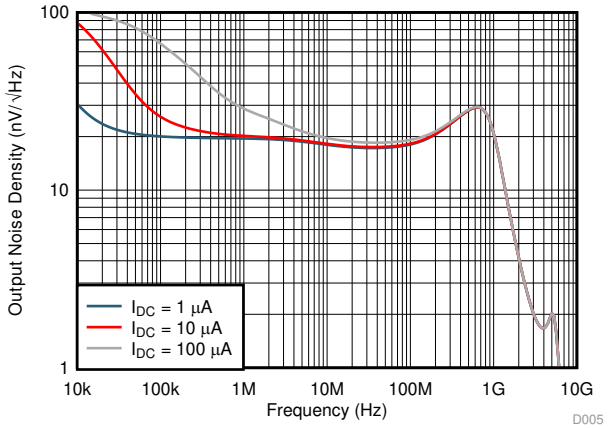
Gain = 20 kΩ. $\overline{IDC_EN}$ disabled

图 4. Integrated Output Noise vs Frequency



Gain = 2 kΩ, C_{APD} = 1 pF, $\overline{IDC_EN}$ enabled

图 5. Output Noise Density vs Frequency Over Input DC Current



Gain = 2 kΩ, C_{APD} = 2.5 pF, $\overline{IDC_EN}$ enabled

图 6. Output Noise Density vs Frequency Over Input DC Current

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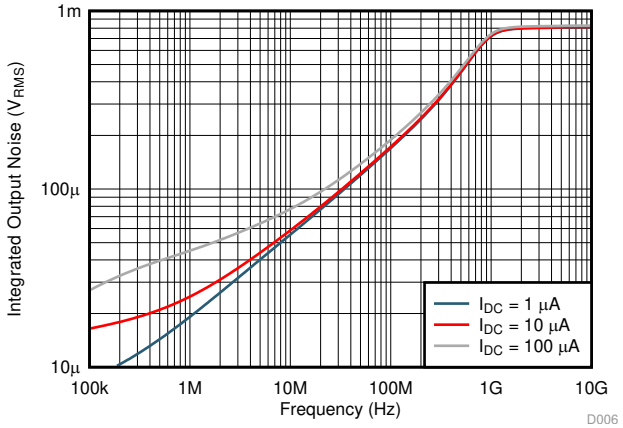
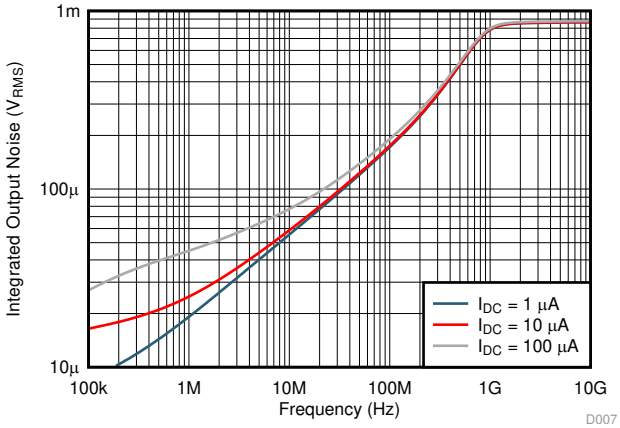
Typical Characteristics (接下页)

at V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted)



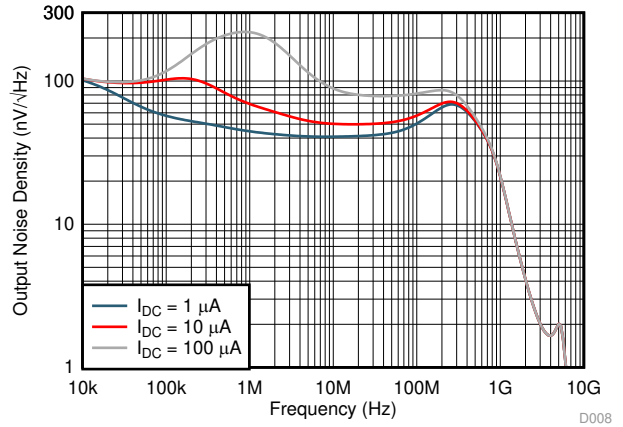
Gain = 2 kΩ, C_{APD} = 1 pF, $\overline{IDC_EN}$ enabled

图 7. Integrated Output Noise vs Frequency Over Input DC Current



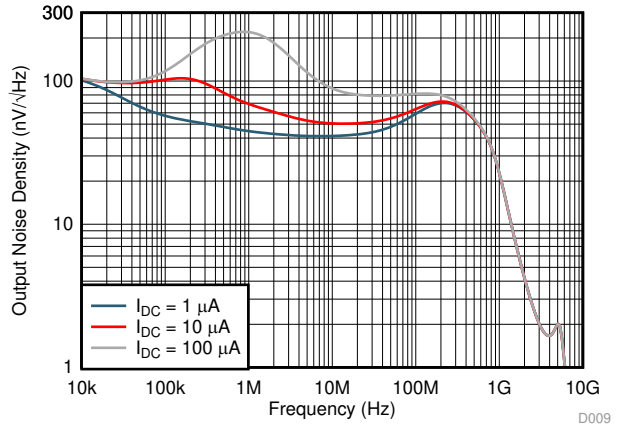
Gain = 2 kΩ, C_{APD} = 2.5 pF, $\overline{IDC_EN}$ enabled

图 8. Integrated Output Noise vs Frequency Over Input DC Current



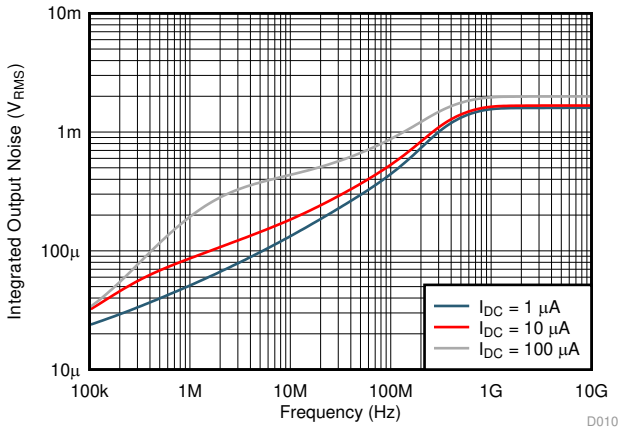
Gain = 20 kΩ, C_{APD} = 1 pF, $\overline{IDC_EN}$ enabled

图 9. Output Noise Density vs Frequency Over Input DC Current



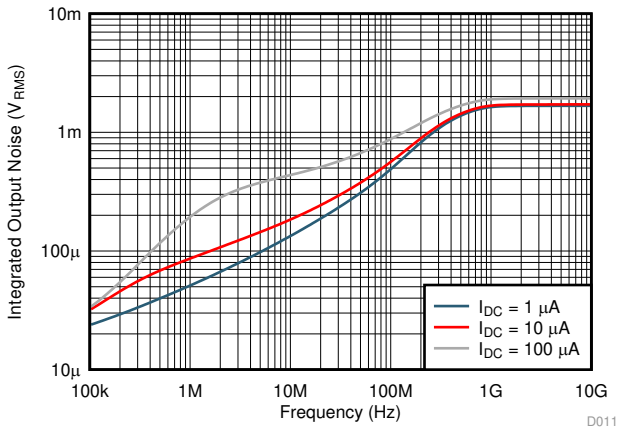
Gain = 20 kΩ, C_{APD} = 2.5 pF, $\overline{IDC_EN}$ enabled

图 10. Output Noise Density vs Frequency Over Input DC Current



Gain = 20 kΩ, C_{APD} = 1 pF, $\overline{IDC_EN}$ enabled

图 11. Integrated Output Noise vs Frequency Over Input DC Current



Gain = 20 kΩ, C_{APD} = 2.5 pF, $\overline{IDC_EN}$ enabled

图 12. Integrated Output Noise vs Frequency Over Input DC Current

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Typical Characteristics (接下页)

at V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted)

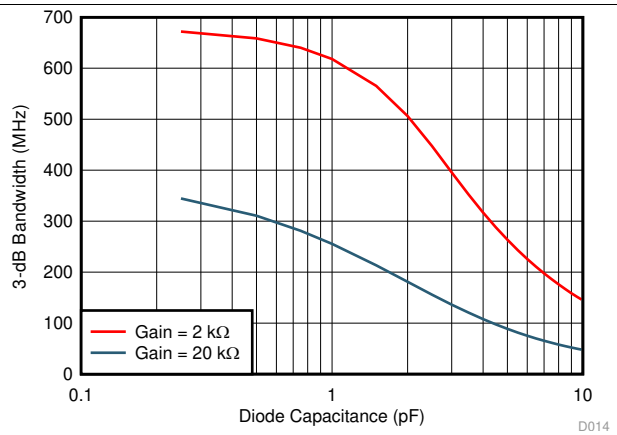
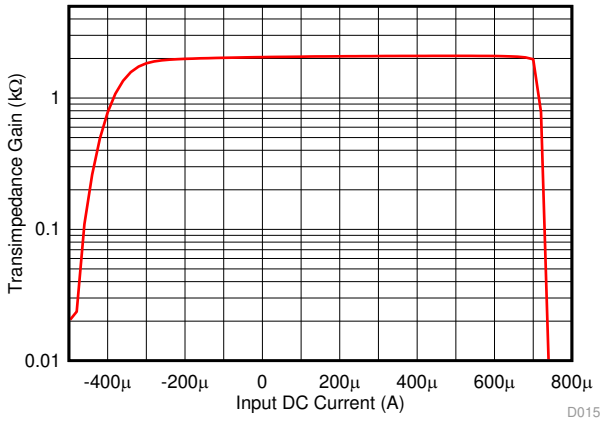
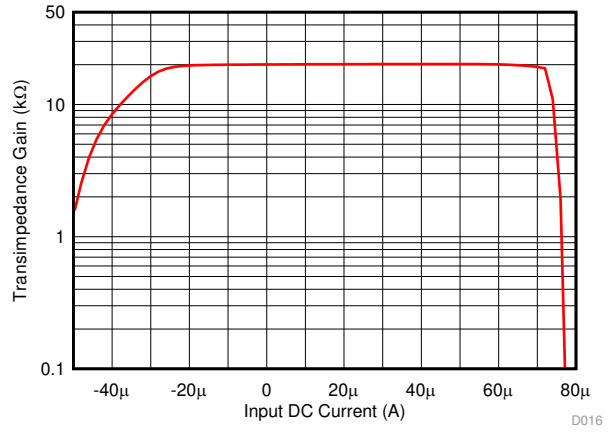


图 13. Bandwidth vs Photodiode Capacitance



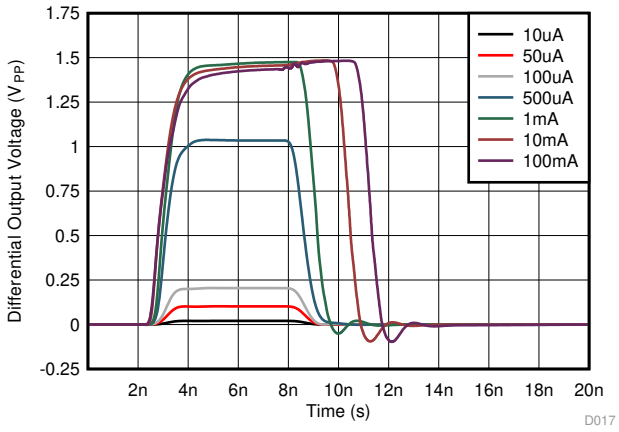
Gain = 2 kΩ, positive current flows out of the amplifier input pin

图 14. Transimpedance Gain vs Input Signal Current



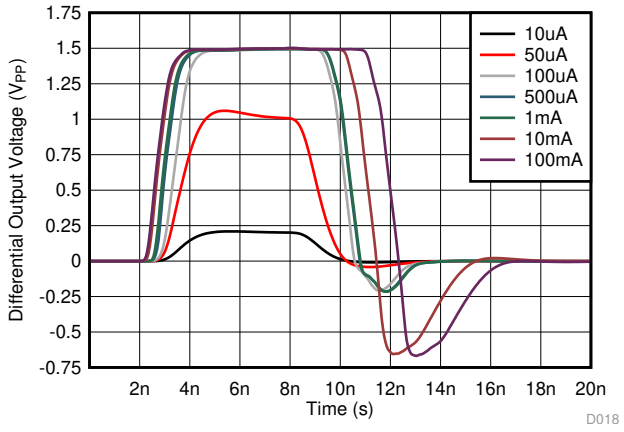
Gain = 20 kΩ, positive current flows out of the amplifier input pin

图 15. Transimpedance Gain vs Input Signal Current



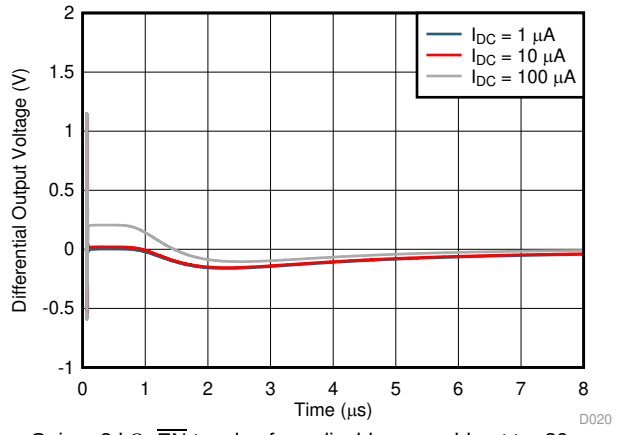
Gain = 2 kΩ

图 16. Pulse Response Over Input Signal Current



Gain = 20 kΩ

图 17. Pulse Response Over Input Signal Current



Gain = 2 kΩ, $\overline{EN}$ toggles from disable → enable at t = 30 ns

图 18. Ambient Light Cancellation Loop Settling Time Over Input DC Current

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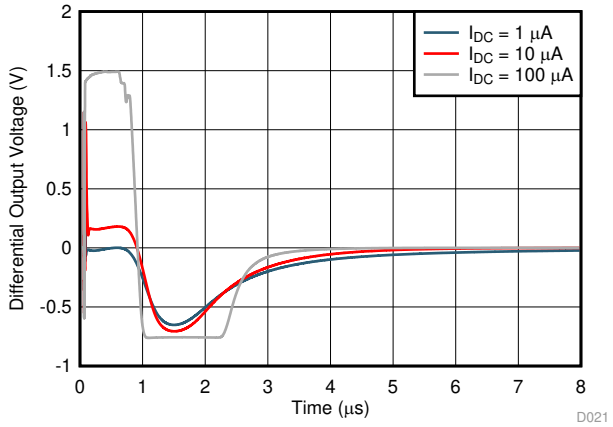
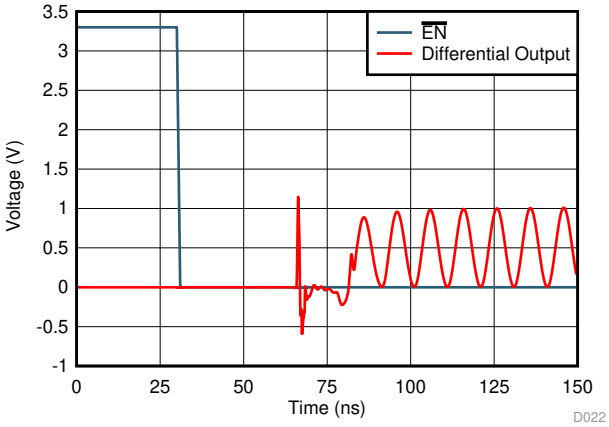
Typical Characteristics (接下页)

at V_{DD} = 3.3 V, V_{OCM} = open, V_{OD} = 0 V, C_{PD} = 1 pF, $\overline{EN}$ = 0 V (enabled), $\overline{IDC_EN}$ = 3.3 V (disabled), R_L = 100 Ω (differential load between OUT+ and OUT–), and T_A = 25°C (unless otherwise noted)



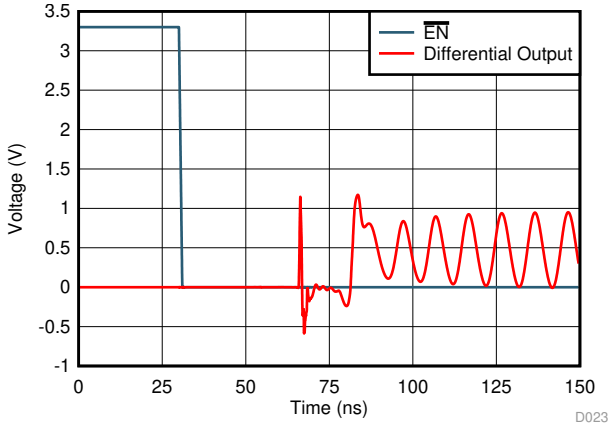
Gain = 20 kΩ, $\overline{EN}$ toggles from disable → enable at t = 30 ns

图 19. Ambient Light Cancellation Loop Settling Time Over Input DC Current



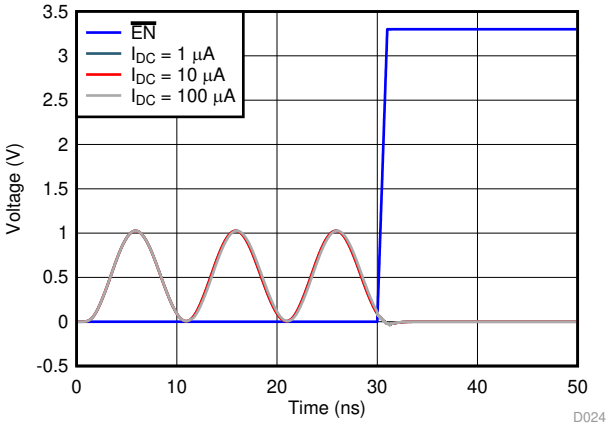
Gain = 2 kΩ, $\overline{IDC_EN}$ = high , VOD = 0 V, VOCM = 1 V

图 20. Amplifier Enable Settling Time



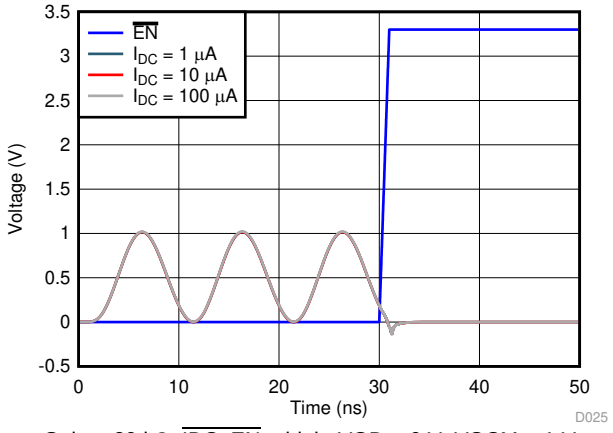
Gain = 20 kΩ, $\overline{IDC_EN}$ = high, VOD = 0 V, VOCM = 1 V

图 21. Amplifier Enable Settling Time



Gain = 2 kΩ, $\overline{IDC_EN}$ = high, VOD = 0 V, VOCM = 1 V

图 22. Amplifier Disable Settling Time Over Input DC Current



Gain = 20 kΩ, $\overline{IDC_EN}$ = high, VOD = 0 V, VOCM = 1 V

图 23. Amplifier Disable Settling Time Over Input DC Current

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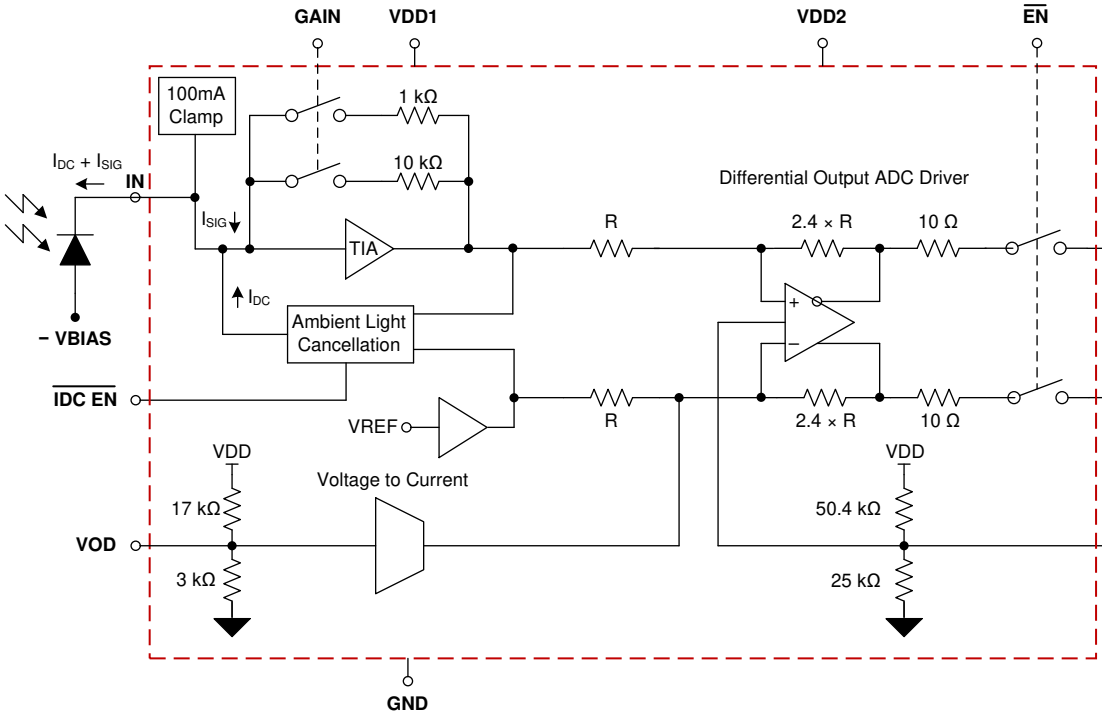
7 Detailed Description

7.1 Overview

The LMH32401 is a single-channel, differential output, high-speed transimpedance amplifier (TIA) and features several integrated functions geared towards light detection and ranging (LIDAR) and pulsed time-of-flight (ToF) systems. The LMH32401 is designed to work with photodiodes (PDs) whose anodes are biased to a negative voltage and cathodes tied to the amplifier input so that the amplifier sources the photocurrent. The LMH32401 is offered in a space-saving 3-mm × 3-mm, 16-pin VQFN package and is rated over a temperature range from –40°C to +125°C.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Switched Gain Transimpedance Amplifier

The LMH32401 features a programmable gain transimpedance amplifier (TIA) stage followed by a fixed-gain, single-ended input to differential output amplifier stage. The closed-loop bandwidth and noise of a TIA are affected by the transimpedance gain and photodiode capacitance. For a given value of photodiode capacitance, the LMH32401 has higher bandwidth in its low-gain configuration compared to the high-gain configuration. Increasing the gain of the TIA stage by a factor of *X* increases the output signal by a factor *X* but the noise contribution from the resistor only increases by $\sqrt{X}$. The input-referred noise density of the low-gain configuration is therefore higher than the input-referred noise density of the high-gain configuration.

The TIA stage is followed by a buffer stage that level shifts the TIA DC offset from 2.6 V (approximately) to 1.65 V (V_{DD} = 3.3 V). The importance of the level-shift buffer stage is explained in subsequent sections.

The gain of the TIA stage is controlled by the GAIN pin. Setting this pin low places the TIA in its low-gain configuration, whereas setting the pin high places the TIA in a high-gain configuration. The LMH32401 defaults to its high-gain configuration when the GAIN pin is left floating.

7.3.2 Clamping and Input Protection

The LMH32401 is configured to work with PDs whose anode is tied to a large negative voltage with its cathode tied to the amplifier input. In this configuration, the PD sinks a current when light is incident. Stray reflections from nearby objects with high reflectivity can produce large output current pulses from the PD. The linear input range of the LMH32401 is approximately 65 µA in the high-gain configuration and 650 µA in the low-gain configuration. Input currents in excess of the linear current range cause the internal nodes of the amplifier to saturate, which increases the amplifier recovery time. The end result is a broadening of the output pulse leading to blind zones in the system. To protect against this condition, the LMH32401 features an integrated clamp that absorbs and diverts the excess current to the positive supply (V_{DD1}) when the amplifier detects its nodes entering a saturated condition. The integrated clamp minimizes the pulse extension to less than 3 ns for input pulses up to 100 mA. The power-supply pins (VDD1 and VDD2) must each have their own bypass capacitors to prevent large input pulses from affecting the differential output stage. When the amplifier is in low-power mode, the clamp circuitry is still active, thereby protecting the TIA input.

7.3.3 ESD Protection

All LMH32401 pins have an internal electrostatic discharge (ESD) protection diode to the positive and negative supply rails to protect the amplifier from ESD events.

7.3.4 Differential Output Stage

The differential output stage of the LMH32401 performs two functions that are common across all differential amplifiers. This stage:

1. Converts the single-ended output from the TIA stage to a differential output
2. Performs a common-mode output shift to match the specified ADC input common-mode voltage

The differential output stage has two 10-Ω series resistors on its output to isolate the amplifier output stage transistors from the package bond-wire inductance and printed circuit board (PCB) capacitance. The net gain of the LMH32401 (TIA + output stage) is 2 kΩ (low gain) and 20 kΩ (high gain) when driving an external 100-Ω resistor. When the external load resistor is increased above 100 Ω, the effective gain from the IN pin to the differential output pin increases. Consequently, when the external load resistor is decreased to less than 100 Ω, the effective gain from the IN pin to the differential output pin decreases as a result of the larger voltage drop across the two internal 10-Ω resistors. When there is no load resistor between the OUT+ and OUT– pins, the effective TIA gain is 2.4 kΩ and 24 kΩ in the low- and high-gain configurations, respectively.

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Feature Description (接下页)

The output common-mode voltage of the LMH32401 can be set externally through the VOCM pin. A resistor divider internal to the amplifier, between VDD2 and ground sets the default voltage to 1.1 V. The internal resistors generate common-mode noise that is typically rejected by the CMRR of the subsequent ADC stage. To maximize the amplifier SNR, place an external noise bypass capacitor to ground on the VOCM pin. In single-ended signal chains, such as ToF systems that use time-to-digital converters (TDCs), only a single output of the LMH32401 is needed. In such situations, terminate the unused differential output in the same manner as the used output to maintain balance and symmetry. The signal swing of the single-ended output is half the available differential output swing. Additionally, the common-mode noise of the output stage, which is typically rejected by the differential input ADC, is now added to the total noise, further degrading SNR.

The output stage of the LMH32401 has an additional VOD input that sets the differential output between OUT– and OUT+. When the photodiode output current is zero and the VOD input is set to 0 V, as shown in 图 24, each output pin of the LMH32401 is at the voltage set by the VOCM pin (default = 1.1 V). When the VOD pin is driven to a voltage of *X* volts, the two output pins are separated by *X* volts when the photodiode current is zero. The average voltage is still equal to VOCM. For example, if VOCM is set to 1.1 V and VOD is set to 0.4 V, as shown in 图 25, then OUT– = 1.1 V + 0.2 V = 1.3 V and OUT+ = 1.1 V – 0.2 V = 0.9 V.

The VOD output offset feature is included in the LMH32401 because the output current of a photodiode is unipolar. Depending on the reverse bias configuration, the photodiode can either sink or source current, but cannot do both at the same time. With the anode connected to a negative bias and the cathode connected to the TIA stage input, the photodiode can only sink current, which implies that the TIA stage output swings in a positive direction above its default input bias voltage. Subsequently, OUT– only swings below VOCM and OUT+ only swings above VOCM. With VOD = 0 V, the LMH32401 only uses half its output swing range ($V_{OUT} = V_{OUT+} – V_{OUT–}$) as shown in 图 24, because one output never swings below VOCM and the other output never goes above VOCM. The signal dynamic range in this case is 0.4 V_{PP} – 0 V = 0.4 V_{PP}.

The VOD pin voltage allows OUT– to be level-shifted above VOCM and OUT+ to be level-shifted below VOCM, as shown in 图 25, to maximize the output swing capabilities of the amplifier. The signal dynamic range in this case is 0.4 V_{PP} – (–0.4 V_{PP}) = 0.8 V_{PP}.

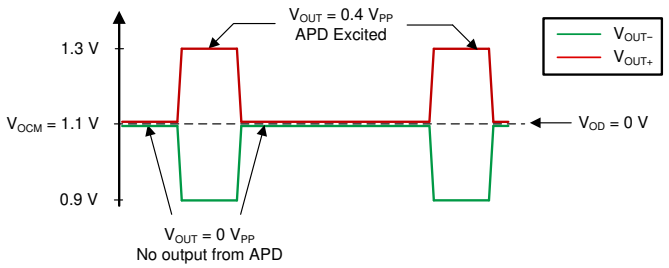

图 24. Single-Ended Outputs With VOD = 0 V

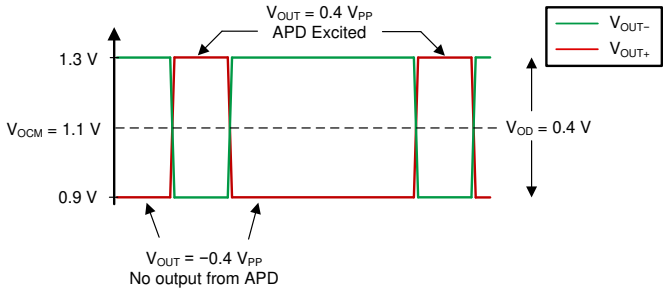

图 25. Single-Ended Outputs With VOD = 0.4 V

When the LMH32401 drives a 100-Ω load, the voltage set at the VOD pin is equal to the differential output offset ($V_{OUT} = V_{OUT+} – V_{OUT–}$) when the input signal current is zero. Use 公式 1 to calculate the differential output offset under other load conditions.

$$V_{OD} = 1.2 \times VOD \times \frac{R_L}{\left(R_L \times 20\ \Omega\right)}, \text{ where} \quad (1)$$

where

- VOD = Voltage applied at pin 9
- $V_{OD} = (V_{OUT–} – V_{OUT+})$
- R_L = External load resistance

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7.4 Device Functional Modes

7.4.1 Ambient Light Cancellation Mode

The LMH32401 has an integrated DC cancellation loop that can used to cancel any voltage offsets resulting from ambient light. The DC cancellation loop is enabled by setting $\overline{IDC_EN}$ low. The cancellation loop senses the low-frequency DC offset at the output of the TIA and compares this offset against an internal reference voltage. If the photodiode produces a DC output current resulting from ambient light, the output of the level-shift buffer stage is offset from the reference voltage. The cancellation loop detects this offset and produces an output DC current that cancels the photodiode output current. The loop has a high-pass cutoff frequency of 100 kHz. The ambient light cancellation loop is disabled when the amplifier is placed in power-down mode.

The shot noise current introduced by the DC cancellation loop increases the overall amplifier noise, so if the ambient light level is negligible disable the loop to improve SNR. The cancellation loop helps save PCB space and system costs by eliminating the need for external AC coupling passive components. Additionally, the extra trace inductance and PCB capacitance introduced by using external AC coupling components degrades the LMH32401 dynamic performance.

7.4.2 Power-Down Mode (Multiplexer Mode)

The LMH32401 can be placed in low-power mode by setting $\overline{EN}$ high, which helps in saving system power. Enabling low-power mode puts the outputs of the internal amplifiers in the LMH32401, including the differential outputs, in a high-impedance state. If a system consists of several photodiode and amplifier channels multiplexed to a single ADC channel, this device feature eliminates the need for a discrete high-speed multiplexer, further saving board space and cost. The disabled channel outputs are not an ideal open circuit so as the number of multiplexed channels increases the disabled channels begin to load down the enabled channel. Multiplexing more than four channels in parallel degrades the performance of the enabled channel. When the amplifier is in its low-power mode, the clamp circuitry is still active thereby protecting the TIA input. The ambient light cancellation loop is disabled when the amplifier is placed in power-down mode. When the LMH32401 is brought out of power-down operation the ambient light cancellation loop requires several time constants to settle. The time constant is based on the 100-kHz cutoff frequency of the loop.

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8 Application and Implementation

> **注**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The differential outputs of the LMH32401 can directly drive a high-speed differential input ADC. When driving an ADC with a 100-Ω differential input impedance, as shown in 图 26 (R_{ADC_IN} = 50 Ω), the effective signal gain between the TIA input and the ADC input is 2 kΩ or 20 kΩ depending on the gain configuration. 公式 2 gives the effective signal gain between the TIA input and the ADC input when driving an ADC with any other value of differential input impedance ($R_{ADC_IN} \neq 50\ \Omega$).

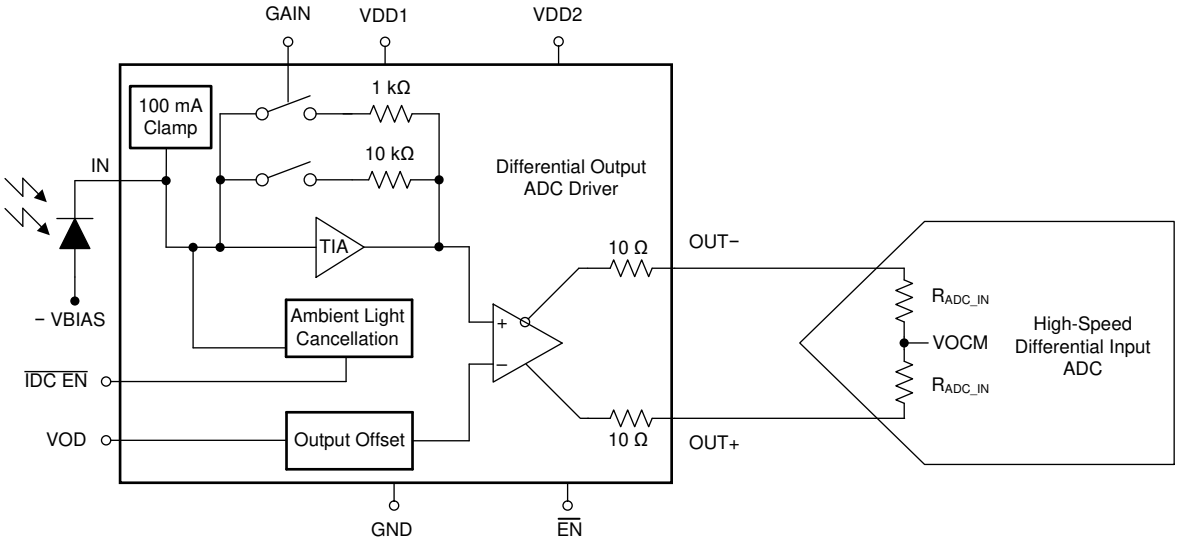

图 26. LMH32401 to ADC Interface

$$A_V = 2\ k\Omega\ (\text{or } 20\ k\Omega) \times 1.2 \times \frac{2 \times R_{ADC_IN}}{(2 \times R_{ADC_IN} + 20\ \Omega)}, \text{ where}$$

where

- A_V = Differential gain from the TIA input to the ADC input
- R_{ADC_IN} = Input resistance of the ADC (2)

As shown in 图 27, in some designs a matching resistor network can be inserted between the LMH32401 output and the ADC inputs. 公式 3 gives the effective gain from the TIA input to the ADC input when using a matching resistor network.

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Application Information (接下页)

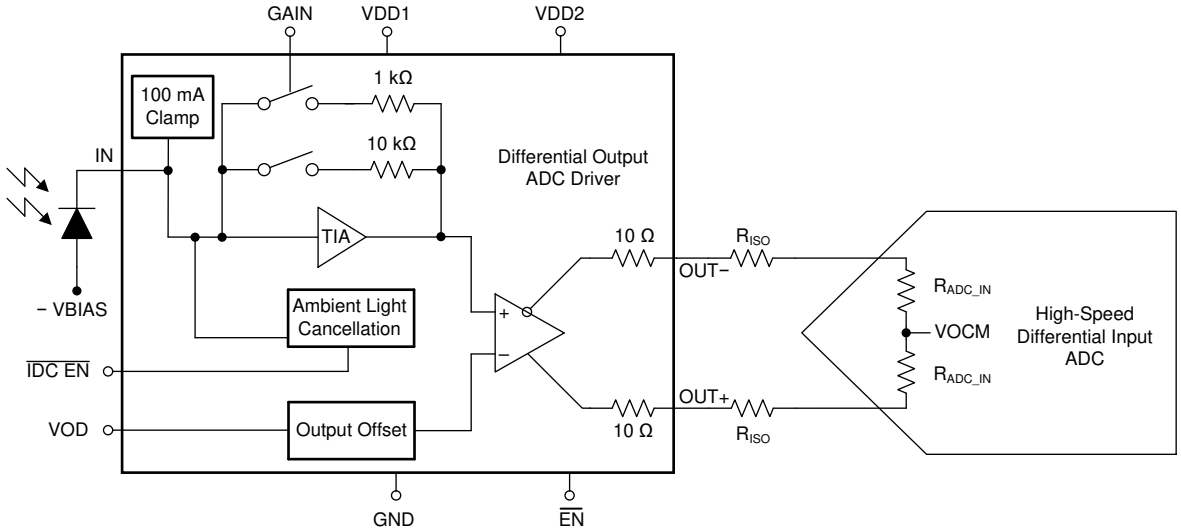

图 27. LMH32401 to ADC Interface With a Matching Resistor Network

$$A_V = 2\ k\Omega\ (\text{or } 20\ k\Omega) \times 1.2 \times \frac{2 \times R_{ADC_IN}}{(2 \times R_{ADC_IN} + 2 \times R_{ISO} + 20\ \Omega)}, \text{ where}$$

where

- A_V = Gain from the TIA input to the ADC input
- R_{ADC_IN} = Differential input resistance of the ADC
- R_{ISO} = Series resistance between the TIA and ADC (3)

公式 4 gives the voltage to be applied at the VOD pin (pin 9) if a certain differential offset voltage (V_{OD}) is needed at the ADC input for the circuit in 图 27.

$$VOD = V_{OD} \times \left(\frac{1}{1.2}\right) \times \frac{(2 \times R_{ADC_IN} + 2 \times RISO + 20\ \Omega)}{(2 \times R_{ADC_IN})}, \text{ where}$$

where

- VOD = Voltage applied at pin 9
- V_{OD} = Desired differential offset voltage at the ADC input
- R_{ADC_IN} = Differential input resistance of the ADC
- R_{ISO} = Series resistance between the TIA and ADC (4)

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8.2 Typical Application

图 28 shows the circuit used to test the LMH32401 with a voltage source.

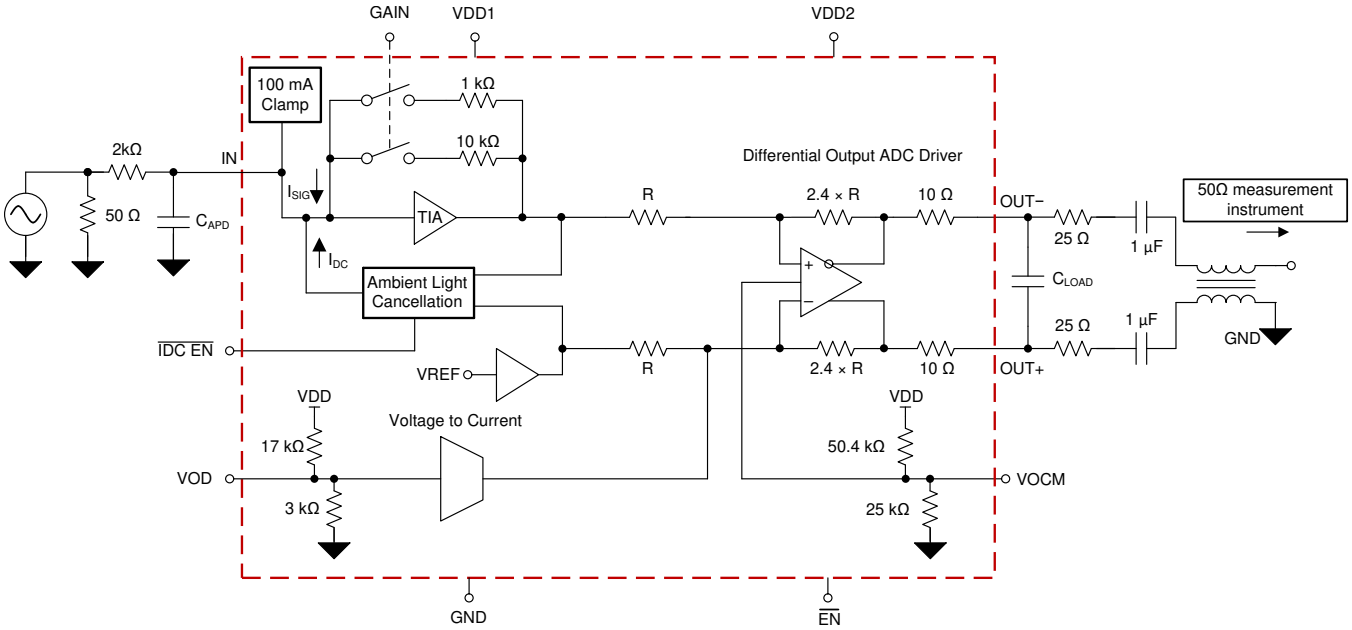

图 28. LMH32401 Test Circuit

8.2.1 Design Requirements

The objective is to design a low-noise, wideband differential output transimpedance amplifier. The design requirements are:

- Amplifier supply voltage: 3.3 V
- Transimpedance gain: 20 kΩ
- Photodiode capacitance: C_{APD} = 1 pF
- Target bandwidth: 250 MHz
- Integrated input-referred noise: 50 nA_{RMS} (noise bandwidth = 250 MHz)

8.2.2 Detailed Design Procedure

图 28 shows the LMH32401 test circuit used to measure its bandwidth and transient pulse response. The voltage source is DC biased close to the input bias voltage of the LMH32401 (approximately 2.45 V). The LMH32401 internal design is optimized to only source current out of the input pin (pin 3). If the voltage input from the source exceeds 2.45 V, the LMH32401 input sinks current, resulting in degraded bandwidth. When testing the LMH32401 with a network analyzer or sinusoidal source, set the DC bias such that sum of the input AC and DC component does not result in a sourcing current into the amplifier input. Only use the LMH32401 with avalanche photodiodes (APDs) that sink current. An anode-biased APD satisfies this requirement.

The bandwidth of a transimpedance amplifier strongly depends on the APD capacitance (C_{APD}). The larger the capacitance, the lower the closed loop bandwidth. 图 29 shows the measured results when the C_{APD} is swept from 0 pF to 2 pF. The estimated PCB capacitance is approximately 1 pF. For the frequency response in 图 29 the output load capacitor (C_{LOAD}) was uninstalled. 图 30 compares the frequency response with C_{LOAD} not installed and C_{LOAD} = 2.7 pF. The extra output loading extends the bandwidth of the LMH32401 by close to 30% without additional output peaking. C_{APD} was not populated for the measurements in 图 30.

图 31 shows the pulsed output response of the LMH32401 when the input current is increased past the amplifier linear input range. The internal clamp of the LMH32401 turns on when the input current exceeds the linear range. This feature enables the LMH32401 to recover from a saturated condition in less than 2 ns.

图 32 shows the input-referred noise spectral density of the LMH32401 with C_{APD} = 1 pF. The input-referred current noise in a noise bandwidth of 250 MHz (brickwall filter) was measured to be 48 nA_{RMS}.

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Typical Application (接下页)

图 33 shows the turn-on time of the LMH32401 when the $\overline{EN}$ pin is toggled from off to on. The input source is constantly driving a 10-MHz input sine wave. When the amplifier is off, the output is in a high-impedance state. When the amplifier turns on, the output settles and starts tracking the input within approximately 125 ns.

8.2.3 Application Curves

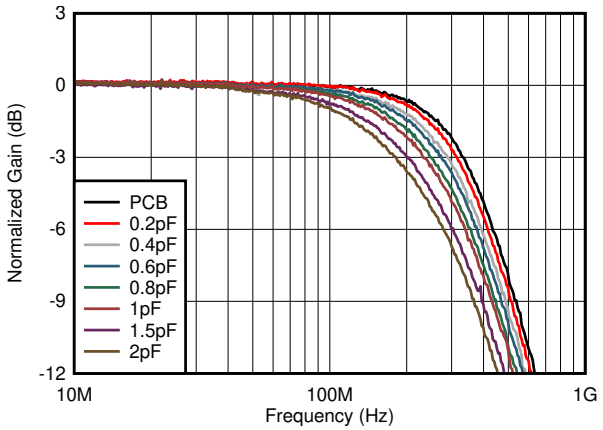

图 29. Bandwidth vs Input Capacitance

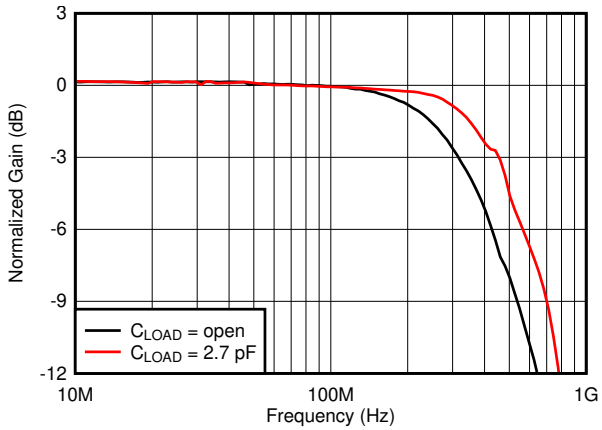

图 30. Bandwidth vs Capacitive Load

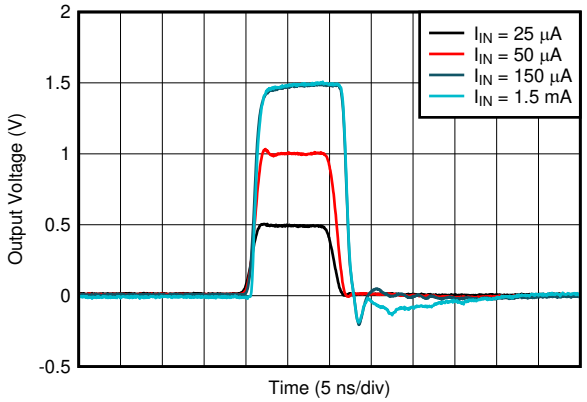

图 31. Output Response vs Input Current

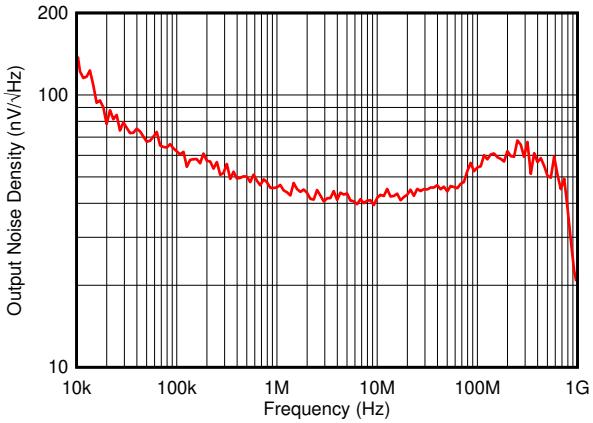

图 32. Output Noise Spectral Density

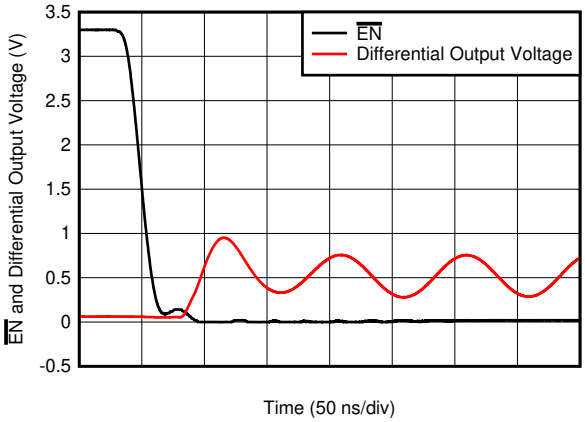

图 33. Turn-On Response

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9 Power Supply Recommendations

The LMH32401 operates on 3.3-V supplies. The VDD1 and VDD2 pins must always be driven from the same supply source and individually bypassed. A low power-supply source impedance must be maintained across frequency so use multiple bypass capacitors in parallel. Place the bypass capacitors as close to the supply pins as possible. Place the smallest capacitor on the same side of the PCB as the LMH32401. Placing the larger valued bypass capacitors on the same side of the PCB is preferable as well, however if there are space constraints the capacitors can be moved to the opposite side of the PCB using multiple vias to reduce the series inductance resulting from the vias. The LMH32401 can be run on bipolar supplies by connecting pins 1 and 7 to the negative supply. The thermal pad must always be connected to the most negative supply. The digital pin threshold voltages must be appropriately level shifted as they are referred to voltages at pins 1 and 7.

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10 Layout

10.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the LMH32401 requires careful attention to board layout parasitics and external component types. Recommendations that optimize performance include:

- **Minimize parasitic capacitance from the signal I/O pins to ac ground.** Parasitic capacitance on the output pins can cause instability whereas parasitic capacitance on the input pin reduces the amplifier bandwidth. To reduce unwanted capacitance, cut out the power and ground traces under the signal input and output pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.
- **Minimize the distance from the power-supply pins to high-frequency bypass capacitors.** Use high-quality, 100-pF to 0.1-µF, C0G and NPO-type decoupling capacitors with voltage ratings at least three times greater than the amplifiers maximum power supplies. Place the smallest value capacitors on the same side as the DUT. If space constraints force the larger value bypass capacitors to be placed on the opposite side of the PCB, use multiple vias on the supply and ground side of the capacitors. This configuration makes sure that there is a low-impedance path to the amplifiers power-supply pins across the amplifiers gain bandwidth specification. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors that are effective at lower frequency must be used on the supply pins. Place these decoupling capacitors further from the device. Share the decoupling capacitors among several devices in the same area of the printed circuit board (PCB).

10.2 Layout Example

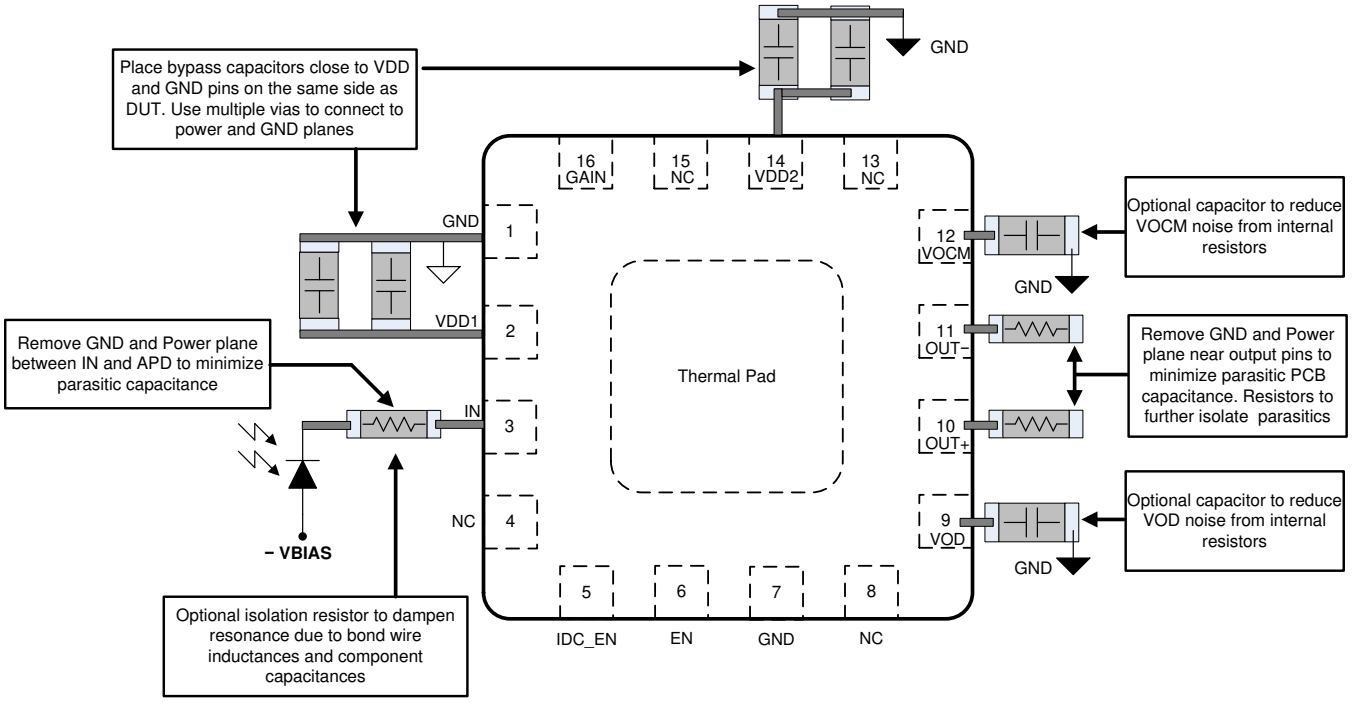

图 34. Layout Recommendation

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11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

- 德州仪器 (TI)，*《光学前端系统参考设计》* 设计指南
- 德州仪器 (TI)，*《使用高速数据转换器的激光雷达脉冲飞行时间参考设计》* 设计指南
- 德州仪器 (TI)，*《激光雷达脉冲飞行时间参考设计》* 设计指南

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《LMH32401IRGT 评估模块》* 用户指南
- 德州仪器 (TI)，*《高速放大器跨阻注意事项》* 应用报告
- 德州仪器 (TI)，*《跨阻放大器须知 - 第 1 部分》* 博客
- 德州仪器 (TI)，*《跨阻放大器须知 - 第 2 部分》* 博客
- 德州仪器 (TI)，*“培训视频：如何设计跨阻放大器电路”*
- 德州仪器 (TI)，*“培训视频：高速跨阻放大器设计流程”*
- 德州仪器 (TI)，*“培训视频：如何将 TINA-TI 模型转换为通用 SPICE 模型”*

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 机械、封装和可订购信息

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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH32401IRGTR	PREVIEW	VQFN	RGT	16	3000	TBD	Call TI	Call TI	-40 to 125		
LMH32401IRGTT	PREVIEW	VQFN	RGT	16	250	TBD	Call TI	Call TI	-40 to 125		
XLMH32401IRGTT	ACTIVE	VQFN	RGT	16	250	TBD	Call TI	Call TI	-40 to 125		Samples

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(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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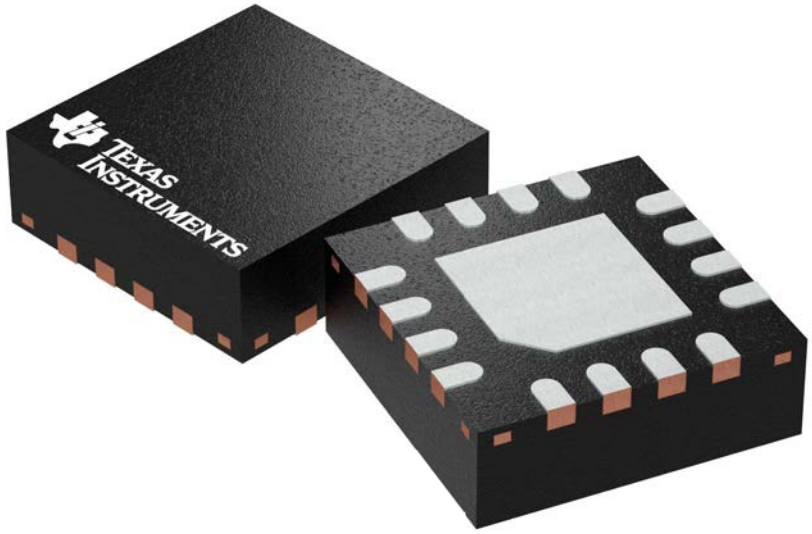
RGT 16

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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