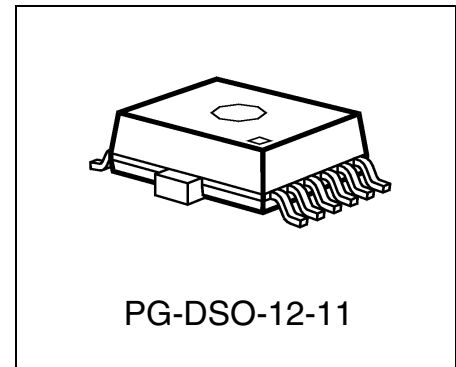




### Features

- Stand-by output 190 mA; 5 V  $\pm$  2%
- Main output: 300 mA, 5 V tracked to the stand-by output
- Low quiescent current consumption
- Disable function separately for both outputs
- Wide operation range: up to 42 V
- Very low dropout voltage
- 2 independent reset circuits
- Watchdog
- Output protected against short circuit
- Wide temperature range: -40 °C to 150 °C
- Overtemperature protection
- Overload protection
- Green product (RoHS compliant)
- AEC qualified



### Functional Description

The TLE 4473 is a monolithic integrated voltage regulator with two low dropout outputs, a main output Q1 for loads up to 300 mA and a stand by output Q2 providing a maximum of 190 mA. The stand-by regulator transforms an input voltage  $V_I$  in the range of 5.6 V  $\leq V_I \leq$  42 V to an output voltage of  $V_{Q2} = 5.0$  V ( $\pm$ 2%). The main output is tracked to the stand by output voltage and provides also 5 V. A versions of this device with 5 V/3.3 V and 5 V/2.6 V are also available, please refer to the data sheet TLE 4473 G V53/ TLE 4473 G V52. The Inhibit input INH1 disables the output Q1 only, whereas Inhibit input INH2 disables both, Q1 and Q2 output. The quiescent current then is 1  $\mu$ A.

The TLE 4473 is designed to supply microprocessor systems and sensors under the severe conditions of automotive applications and therefore is equipped with additional protection functions against overload, short circuit and overtemperature. The device operates in the wide junction temperature range of -40 °C to 150 °C.

Type	Package	Marking
TLE 4473 GV55-2	PG-DSO-12-11 (RoHS compliant)	TLE4473 GV55-2

The device features a reset with adjustable power on delay for each of the outputs. In addition the output for the microcontroller supply comes up with a watchdog in order to supervise a connected microcontroller

### Reset and Watchdog Behavior

The reset output RO2 is in high-state if the voltage on the delay capacitor  $C_{D2}$  is greater or equal  $V_{DU2}$ . The delay capacitor  $C_{D2}$  is charged with the current  $I_{DC2}$  for output voltages greater than the reset threshold  $V_{RT2}$ . If the output voltage gets lower than  $V_{RT2}$  ('reset condition') a fast discharge of the delay capacitor  $C_{D2}$  sets in and as soon as  $V_{D2}$  gets lower than  $V_{DL2}$  the reset output RO2 is set to low-level. The time for the delay capacitor charge is the reset delay time. For the power-on case the charging process of  $C_{D2}$  starts from 0 V, which leads to the equation:

$$t_{D, on} = \frac{C_{D2} \times V_{DU2}}{I_{DC2}} \quad (1)$$

for the power-on reset delay time.

When the voltage on the delay capacitor has reached  $V_{DU2}$  and reset was set to high, the watchdog circuit is enabled and discharges  $C_{D2}$  with the constant current  $I_{DD2}$ .

If there is no rising edge observed at the watchdog input,  $C_{D2}$  will be discharge down to  $V_{DL2}$ . Then reset output RO2 will be set to low and  $C_{D2}$  will be charged again with the current  $I_{DC2}$  until  $V_{D2}$  reaches  $V_{DU2}$  and reset will be set high again.

If the watchdog pulse (rising edge at watchdog input WI) occurs during the discharge period  $C_{D2}$  is charged again and the reset output stays high. After  $V_{D2}$  has reached  $V_{DU2}$ , the periodical cycle starts again.

The watchdog timing is shown in **Figure 1**. The maximum duration between two watchdog pulses corresponds to the minimum watchdog trigger time  $T_{WI, tr}$ . Higher capacitances on pin D2 result in longer watchdog trigger times:

$$T_{WI, tr} |_{max} = 0.34 \text{ ms/nF} \times C_{D2} \quad (2)$$

If the output voltage Q1 decreases below  $V_{RT1}$  (typ. 4.65 V), the external capacitor  $C_{D1}$  is discharged by the reset generator of the main output. If the voltage on this capacitor drops below  $V_{DL1}$ , a reset signal is generated on pin 2 (RO1). If the output voltage rises above the reset threshold,  $C_{D1}$  will be charged with the constant current  $I_{DC1}$ . After the power-on-reset time the voltage on the capacitor reaches  $V_{DU1}$  and the reset output will be set high again. The value of the power-on-reset time can be set within a wide range depending of the capacitance of  $C_{D1}$  using the above given equation (1) analogous for Q1.

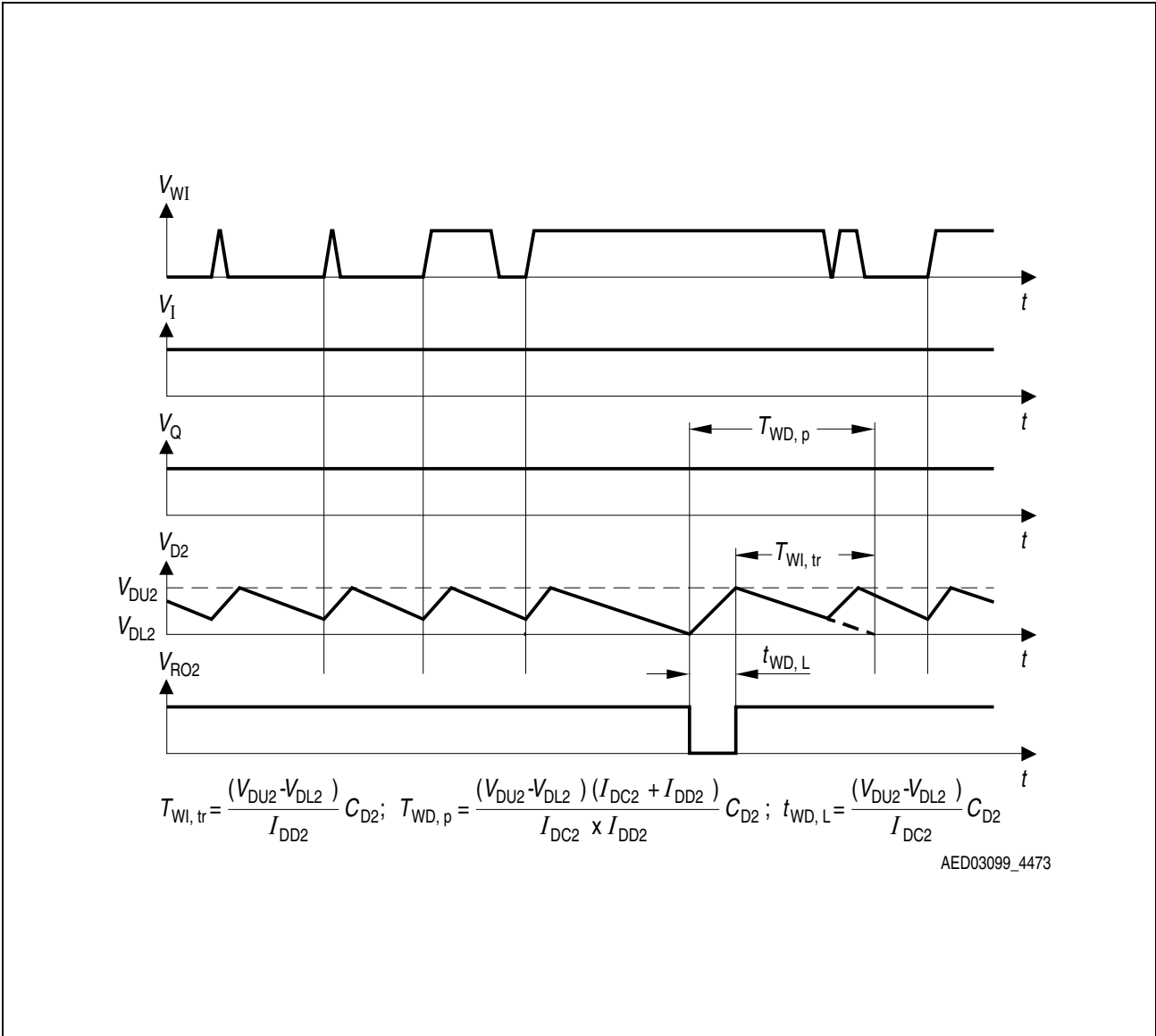


Figure 1 Watchdog Timing Schedule

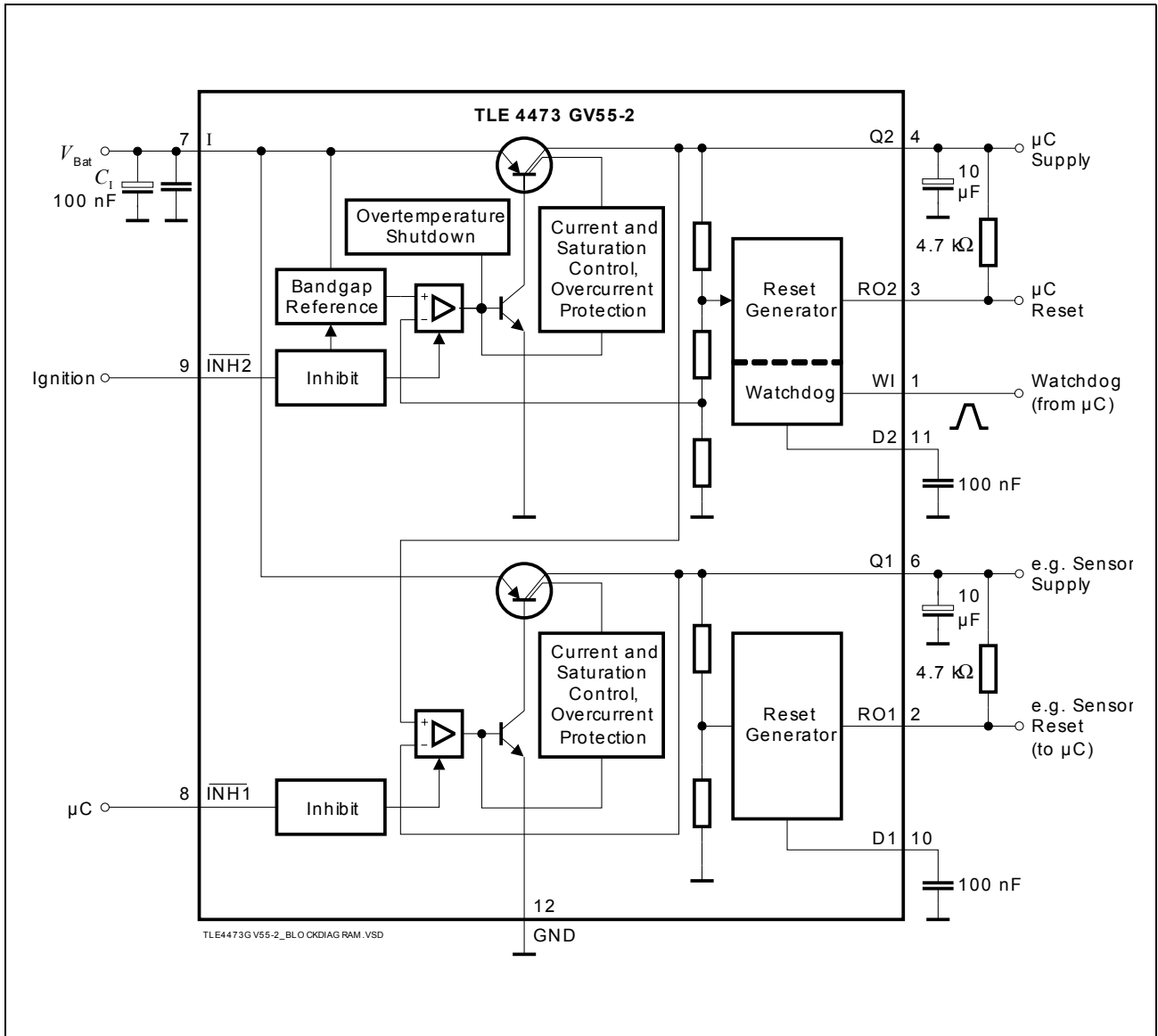


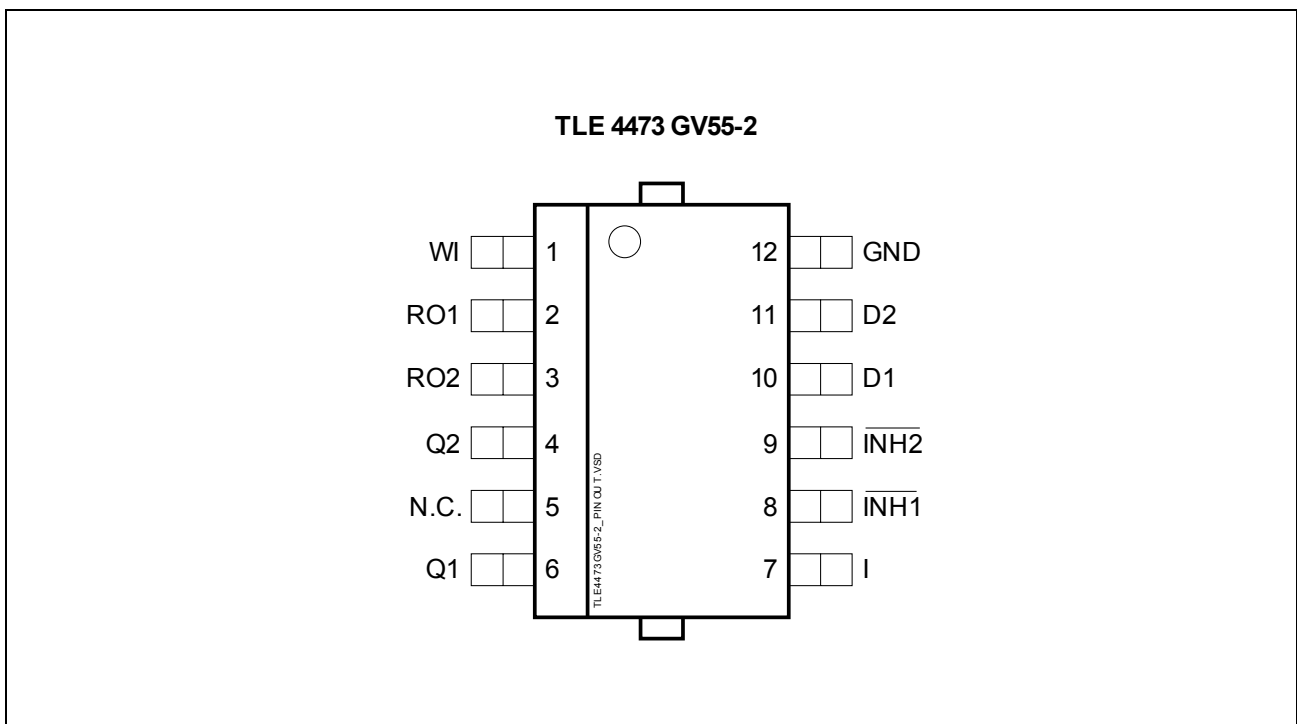
Figure 2 Block Diagram with Typical External Components

### Application Information

The output voltage is divided by a voltage divider and compared to an internal reference voltage. A regulation loop controls the Q2 output in order to achieve a stable output voltage at the Q2 pin. A second regulation loop controls the Q1 output. The reference voltage for the Q1 is the regulated Q2 potential (tracking regulator).

**Figure 2** includes the components needed for a typical application. Maintaining the stability of the regulation loops requires a capacitor of 10  $\mu\text{F}$  both outputs. A maximum ESR of 5  $\Omega$  is permissible for the Q2 output, while the Q1 output requires a capacitor with a maximum ESR of 3  $\Omega$ . For both output blocking capacitors it is recommended to use tantalum types in order to stay in the permissible ESR range over the full operating temperature range.

At the input of the regulator a capacitor is necessary for compensating line influences. A minimum of 100 nF (ceramic capacitor) is recommended. In addition for compensation of long input lines of several meters an electrolytic input capacitor of 47  $\mu\text{F}$  ... 220  $\mu\text{F}$  should be placed at the input.



**Figure 3** Pin Configuration (top view)

**Table 1 Pin Definitions and Functions**

Pin No.	Symbol	Function
1	WI	<b>Watchdog input;</b> input for watchdog pulses, positive edge triggered.
2	RO1	<b>Reset and watchdog output for Q1;</b> open collector output. Connect to pull-up resistor.
3	RO2	<b>Reset output 2;</b> open collector output. Connect to pull-up resistor.
4	Q2	<b>Stand-by regulator output voltage;</b> block to GND with a capacitor $C_{Q2} \geq 10 \mu\text{F}$ , $\text{ESR} < 5 \Omega$ at 10 kHz.
5	N.C.	<b>Internally not connected;</b> connect to GND.
6	Q1	<b>Main regulator output voltage;</b> output voltage tracked to Q2 voltage; block to GND with a capacitor $C_{Q1} \geq 10 \mu\text{F}$ , $\text{ESR} < 3 \Omega$ at 10 kHz
7	I	<b>Input voltage;</b> block to ground directly at the IC with a ceramic capacitor.
8	$\overline{\text{INH1}}$	<b>Inhibit input 1;</b> low level disables Q1, integrated pull-down resistor.
9	$\overline{\text{INH2}}$	<b>Inhibit input 2;</b> low level at $\overline{\text{INH2}}$ and $\overline{\text{INH1}}$ disables Q2 and Q1, integrated pull-down resistor.
10	D1	<b>Reset Delay 1;</b> connect to ground via a capacitor to set reset delay for Q1.
11	D2	<b>Reset Delay 2;</b> connect to ground via a capacitor to set reset delay and watchdog timing for Q2.
12	GND	<b>Ground;</b> connect to heatslug.
Heatslug		Interconnect with PCB heatsink area and GND.

**Table 2 Absolute Maximum Ratings**
 $-40\text{ °C} < T_j < 150\text{ °C}$ 

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
<b>Input I</b>					
Voltage	$V_I$	-42	45	V	–
Current	$I_I$	–	–	mA	Internally limited
<b>Stand-by Output Q2</b>					
Voltage	$V_{Q2}$	-0.3	18	V	–
Current	$I_{Q2}$	–	–	mA	Internally limited
<b>Main Output Q1</b>					
Voltage	$V_{Q1}$	-0.3	18	V	–
Current	$I_{Q1}$	–	–	mA	Internally limited
<b>Inhibit Input <math>\overline{\text{INH1}}</math></b>					
Voltage	$V_{\overline{\text{INH1}}}$	-42	45	V	–
Current	$I_{\overline{\text{INH1}}}$	-2	2	mA	–
<b>Inhibit Input <math>\overline{\text{INH2}}</math></b>					
Voltage	$V_{\overline{\text{INH2}}}$	-42	45	V	–
Current	$I_{\overline{\text{INH2}}}$	-2	2	mA	–
<b>Reset Output RO1</b>					
Voltage	$V_{\text{RO1}}$	-0.3	18	V	–
Current	$I_{\text{RO1}}$	–	–	mA	Internally limited
<b>Reset Output RO2</b>					
Voltage	$V_{\text{RO2}}$	-0.3	18	V	–
Current	$I_{\text{RO2}}$	–	–	mA	Internally limited
<b>Reset Delay D1</b>					
Voltage	$V_{\text{D1}}$	-0.3	7	V	–
Current	$I_{\text{D1}}$	-5	5	mA	–
<b>Reset Delay D2</b>					
Voltage	$V_{\text{D}}$	-0.3	7	V	–
Current	$I_{\text{D}}$	-5	5	mA	–

**Table 2 Absolute Maximum Ratings (cont'd)**
 $-40\text{ °C} < T_j < 150\text{ °C}$ 

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
<b>Watchdog Input WI</b>					
Voltage	$V_{\text{RADJ}}$	-0.3	7	V	–
Current	$I_{\text{RADJ}}$	-5	5	mA	–
<b>Temperatures</b>					
Junction temperature	$T_j$	-50	150	°C	–
Storage temperature	$T_{\text{stg}}$	-50	150	°C	–

**Table 3 Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	$V_I$	5.6	42	V	–
Junction temperature	$T_j$	-40	150	°C	–

**Thermal Resistances PG-DSO-12-11**

Junction pin	$R_{\text{thj-pin}}$	–	4	K/W	–
Junction ambient	$R_{\text{thj-a}}$	–	115	K/W	PCB Heat Sink Area 0 mm <sup>2</sup> 1)
Junction ambient	$R_{\text{thj-a}}$	–	100	K/W	PCB Heat Sink Area 100 mm <sup>2</sup> 1)
Junction ambient	$R_{\text{thj-a}}$	–	60	K/W	PCB Heat Sink Area 300 mm <sup>2</sup> 1)
Junction ambient	$R_{\text{thj-a}}$	–	48	K/W	PCB Heat Sink Area 600 mm <sup>2</sup> 1)

1) Package mounted on PCB 80 × 80 × 1.5 mm<sup>3</sup>; 35μ Cu; 5μ Sn; zero airflow.

*Note: In the operating range the functions given in the circuit description are fulfilled. Integrated protection functions are designed to prevent IC destruction under fault conditions. Protection functions are not designed for continuous repetitive operation.*



**Table 4 Electrical Characteristics**
 $V_{I1} = 13.5 \text{ V}; V_{INH1} = V_{INH2} = 5 \text{ V}; -40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C};$  unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		

**Stand-by Regulator**
**Output Q2**

Output voltage	$V_{Q2}$	4.90	5.0	5.10	V	$1 \text{ mA} < I_{Q2} < 190 \text{ mA};$ $6 \text{ V} < V_1 < 28 \text{ V}$
Output current limitation	$I_{Q2}$	200	300	650	mA	$V_{Q2} = 4.5 \text{ V}$
Output drop voltage; $V_{DRQ1} = V_{I1} - V_{Q1}$	$V_{DRQ2}$	–	200	600	mV	$I_{Q2} = 100 \text{ mA}^{1)}$
Load regulation	$\Delta V_{Q2,Lo}$	–	15	50	mV	$1 \text{ mA} < I_{Q2} < 190 \text{ mA}$
Line regulation	$\Delta V_{Q2,Li}$	–	5	20	mV	$I_{Q2} = 1 \text{ mA};$ $6 \text{ V} < V_1 < 28 \text{ V}$
Power Supply Ripple Rejection	$PSRR$	–	65	–	dB	$f_r = 100 \text{ Hz};$ $V_r = 1 \text{ V}_{pp}$

**Current Consumption**

Quiescent current; stand-by $I_q = I_1 - I_{Q2}$	$I_q$	–	170	220	$\mu\text{A}$	$I_{Q2} = 500 \mu\text{A}; T_j = 25 \text{ }^\circ\text{C};$ $V_{INH1} < V_{INH1 \text{ OFF}} \text{ (Q1 off)}$
		–	–	245	$\mu\text{A}$	$I_{Q2} = 500 \mu\text{A}; T_j = 85 \text{ }^\circ\text{C};$ $V_{INH1} < V_{INH1 \text{ OFF}} \text{ (Q1 off)}$
		–	–	280	$\mu\text{A}$	$I_{Q2} = 500 \mu\text{A};$ $V_{INH1} < V_{INH1 \text{ OFF}} \text{ (Q1 off)}$
		–	4.5	5	mA	$I_{Q2} = 100 \text{ mA};$ $V_{INH1} < V_{INH1 \text{ OFF}} \text{ (Q1 off)}$
Quiescent current; inhibited	$I_q$	–	0.1	1	$\mu\text{A}$	$V_{INH1} = V_{INH2} = 0 \text{ V};$ $T_j < 85 \text{ }^\circ\text{C}$
		–	0.1	20	$\mu\text{A}$	$V_{INH1} = V_{INH2} = 0 \text{ V}$

**Table 4 Electrical Characteristics (cont'd)**
 $V_{I1} = 13.5 \text{ V}; V_{INH1} = V_{INH2} = 5 \text{ V}; -40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C};$  unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		

**Inhibit Input  $\overline{INH2}$** 

Turn-on Voltage	$V_{\overline{INH2} \text{ ON}}$	–	–	2.3	V	$V_{Q2}$ on
Turn-off Voltage	$V_{\overline{INH2} \text{ OFF}}$	0.65	–	–	V	$V_{Q2}$ off
H-input current	$I_{\overline{INH2} \text{ ON}}$	-1	3.2	6	$\mu\text{A}$	$V_{INH2} = 5.0 \text{ V}$ (see <a href="#">Page 13</a> )
L-input current	$I_{\overline{INH2} \text{ OFF}}$	-1	0.1	1	$\mu\text{A}$	$0 \text{ V} < V_{INH2} < 0.8 \text{ V}$

**Watchdog and Reset Timing D2**

Charge current	$I_{DC2}$	6.5	9.0	14.0	$\mu\text{A}$	$V_{D2} = 1 \text{ V}$
Discharge current	$I_{DD2}$	2.0	3.5	5.0	$\mu\text{A}$	$V_{D2} = 1 \text{ V}$
Upper timing threshold	$V_{DU2}$	1.5	1.85	2.4	V	–
Lower timing threshold	$V_{DL2}$	0.3	0.45	0.6	V	–
Saturation Voltage	$V_{D2, \text{SAT}}$	–	–	100	mV	$V_{Q2} < V_{RT2}$
Watchdog trigger time	$T_{WI, \text{tr}}$	34	42	51	ms	$C_{D2} = 100 \text{ nF}$
Reset delay time	$T_{RD2}$	15	20	25	ms	$C_{D2} = 100 \text{ nF}$
Reset reaction time	$T_{rr}$	–	–	5.0	$\mu\text{s}$	$C_{D2} = 100 \text{ nF}$

**Reset Output RO2**

Reset switching threshold	$V_{RT2}$	4.55	4.65	4.8	V	–
	$V_{RT2}/V_{Q2}$	90	93	96	%	–
Reset threshold headroom	$V_{R2\text{HEAD}}$	200	350	500	mV	$V_{Q2} - V_{RT2}$
Reset output sink current	$I_{RO2}$	1.0	–	–	mA	$V_{Q2} = 5 \text{ V}, V_{D2} = 0 \text{ V}; V_{RO2} = 0.3 \text{ V}$
Reset output low voltage	$V_{RO2L}$	–	0.15	0.3	V	$V_{Q2} \geq 1 \text{ V}; I_{RO2} = 1 \text{ mA}$
Reset high voltage	$V_{RO2H}$	4.5	–	–	V	$R_{RO2, \text{ext}} = 4.7 \text{ k}\Omega$

**Table 4 Electrical Characteristics (cont'd)**
 $V_{I1} = 13.5 \text{ V}; V_{INH1} = V_{INH2} = 5 \text{ V}; -40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C};$  unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		

**Main (Tracked) Regulator**
**Output Q1**

Output voltage	$V_{Q1}$	4.875	5.0	5.125	V	$1 \text{ mA} < I_{Q1} < 200 \text{ mA};$ $6 \text{ V} < V_1 < 28 \text{ V}$
Output voltage tracking accuracy	$\Delta V_Q = V_{Q2} - V_{Q1}$	-25	5	25	mV	$1 \text{ mA} < I_{Q1} < 200 \text{ mA};$ $6 \text{ V} < V_1 < 28 \text{ V}$
Output voltage tracking accuracy	$\Delta V_Q = V_{Q2} - V_{Q1}$	-25	5	25	mV	$1 \text{ mA} < I_{Q1} < 300 \text{ mA};$ $8 \text{ V} < V_1 < 28 \text{ V}$
Output current limitation	$I_{Q1}$	350	500	–	mA	$V_{Q1} = 4.5 \text{ V}$
Output drop voltage $V_{DRQ1} = V_1 - V_{Q1}$	$V_{DRQ1}$	–	300	600	mV	$I_{Q1} = 200 \text{ mA}^{1)}$
Load regulation	$\Delta V_{Q1,Lo}$	–	5	50	mV	$5 \text{ mA} < I_{Q1} < 300 \text{ mA}$
Line regulation	$\Delta V_{Q1,Li}$	–	5	25	mV	$I_{Q1} = 5 \text{ mA};$ $6 \text{ V} < V_1 < 28 \text{ V}$
Power Supply Ripple Rejection	$PSRR$	–	65	–	dB	$f_r = 100 \text{ Hz};$ $V_r = 1 \text{ V}_{pp}$

**Current Consumption**

Quiescent current; $I_q = I_1 - I_{Q1} - I_{Q2}$	$I_q$	–	10	20	mA	$I_{Q1} = 300 \text{ mA};$ $I_{Q2} = 500 \text{ } \mu\text{A};$ $V_{Q1}$ and $V_{Q2}$ on
Quiescent current; $I_q = I_1 - I_{Q1} - I_{Q2}$	$I_q$	–	250	500	$\mu\text{A}$	$I_{Q2} = I_{Q1} = 500 \text{ } \mu\text{A};$ $V_{Q1}$ and $V_{Q2}$ on

**Inhibit Input  $\overline{INH1}$** 

Turn-on Voltage	$V_{\overline{INH1} \text{ ON}}$	–	–	2.3	V	$V_{Q1}$ on
Turn-off Voltage	$V_{\overline{INH1} \text{ OFF}}$	0.7	–	–	V	$V_{Q1}$ off
H-input current	$I_{\overline{INH1} \text{ ON}}$	-1	3.5	5	$\mu\text{A}$	$3.0 \text{ V} < V_{INH1} < 5 \text{ V};$ (see <a href="#">Page 14</a> )
L-input current	$I_{\overline{INH1} \text{ OFF}}$	-1	0.1	1	$\mu\text{A}$	$0 \text{ V} < V_{INH1} < 0.8 \text{ V}$

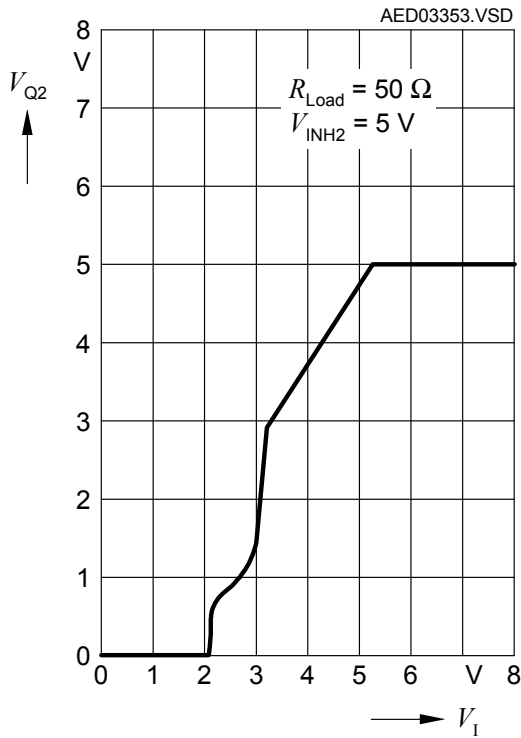
**Table 4 Electrical Characteristics (cont'd)**
 $V_{I1} = 13.5 \text{ V}; V_{INH1} = V_{INH2} = 5 \text{ V}; -40 \text{ }^\circ\text{C} < T_j < 150 \text{ }^\circ\text{C};$  unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
<b>Reset Timing D1</b>						
Charge current	$I_{DC1}$	4.0	8.0	14.0	$\mu\text{A}$	$V_{D1} = 1 \text{ V}$
Upper timing threshold	$V_{DU1}$	1.6	1.8	2.2	V	–
Lower timing threshold	$V_{DL2}$	0.3	0.4	0.6	V	–
Saturation Voltage	$V_{D1,SAT}$	–	–	100	mV	$V_{Q1} < V_{RT1}$
Reset delay time	$T_{RD1}$	14	20	30	ms	$C_{D1} = 100 \text{ nF}$
Reset reaction time	$T_{rr}$	–	–	10	$\mu\text{s}$	$C_{D1} = 100 \text{ nF}$
<b>Reset Output RO1</b>						
Reset switching threshold	$V_{RT1}$	4.5	4.65	4.8	V	–
	$V_{RT1}/V_{Q1}$	90	93	96	%	–
Reset threshold headroom	$V_{R1HEAD}$	200	350	500	mV	$V_{Q1} - V_{RT1}$
Reset output sink current	$I_{RO1}$	1.0	–	–	mA	$V_{Q1} = 5.0 \text{ V}; V_{Q2} = 5.0 \text{ V}; V_{D1} = 0 \text{ V}; V_{RO1} = 0.3 \text{ V}$
Reset output low voltage	$V_{RO1L}$	–	0.15	0.3	V	$V_{Q1} \geq 1 \text{ V}$ $I_{RO1} = 1 \text{ mA}$
Reset output high voltage	$V_{RO1H}$	4.5	–	–	V	$R_{RO1,ext} = 4.7 \text{ k}\Omega$

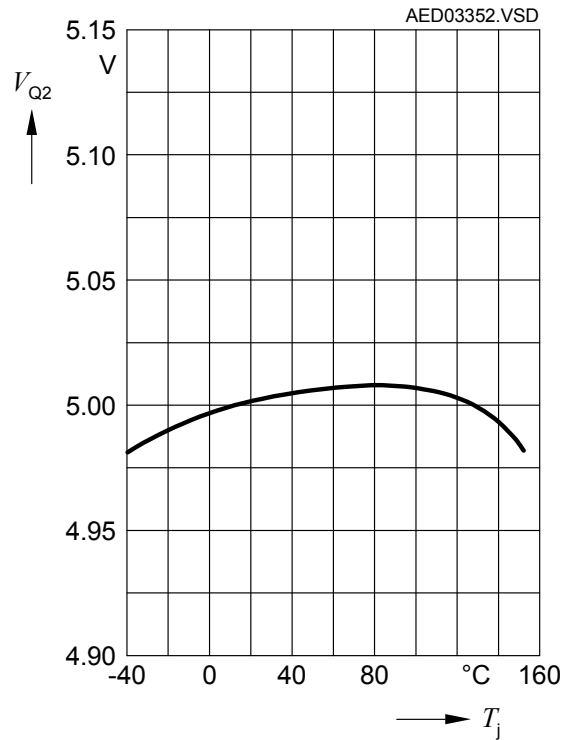
1) Drop voltage =  $V_I - V_Q$  (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

Typical Performance Characteristics

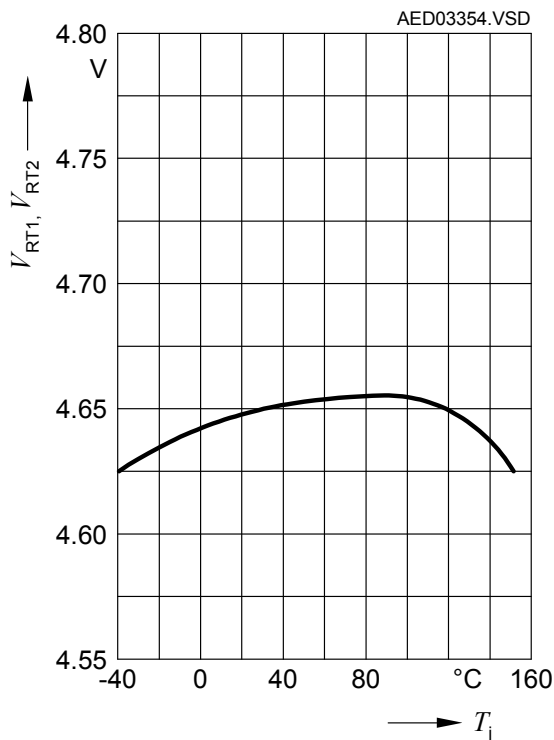
Output Voltage  $V_{Q2}$  versus Input Voltage  $V_I$



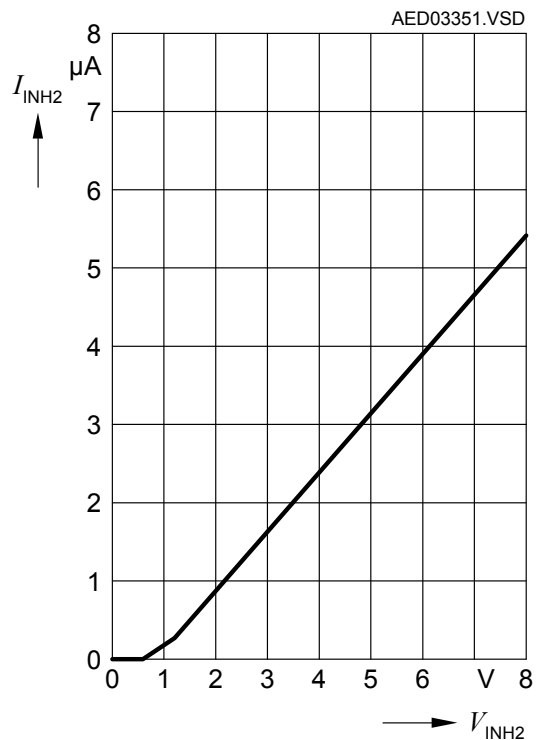
Output Voltage  $V_{Q2}$  versus Junction Temperature  $T_J$



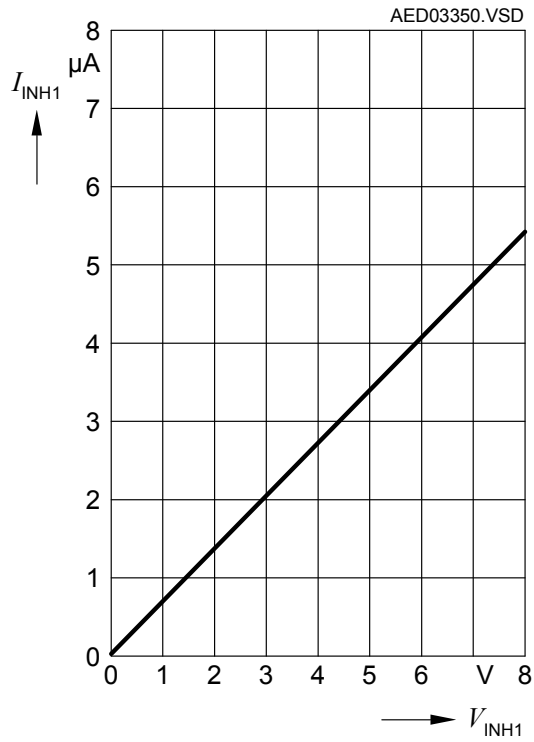
Reset Thresholds  $V_{RT1}$ ,  $V_{RT2}$  versus Junction Temperature  $T_J$



INH2 Input Current versus Inhibit Voltage



### INH1 Input Current versus Inhibit Voltage



Package Outline

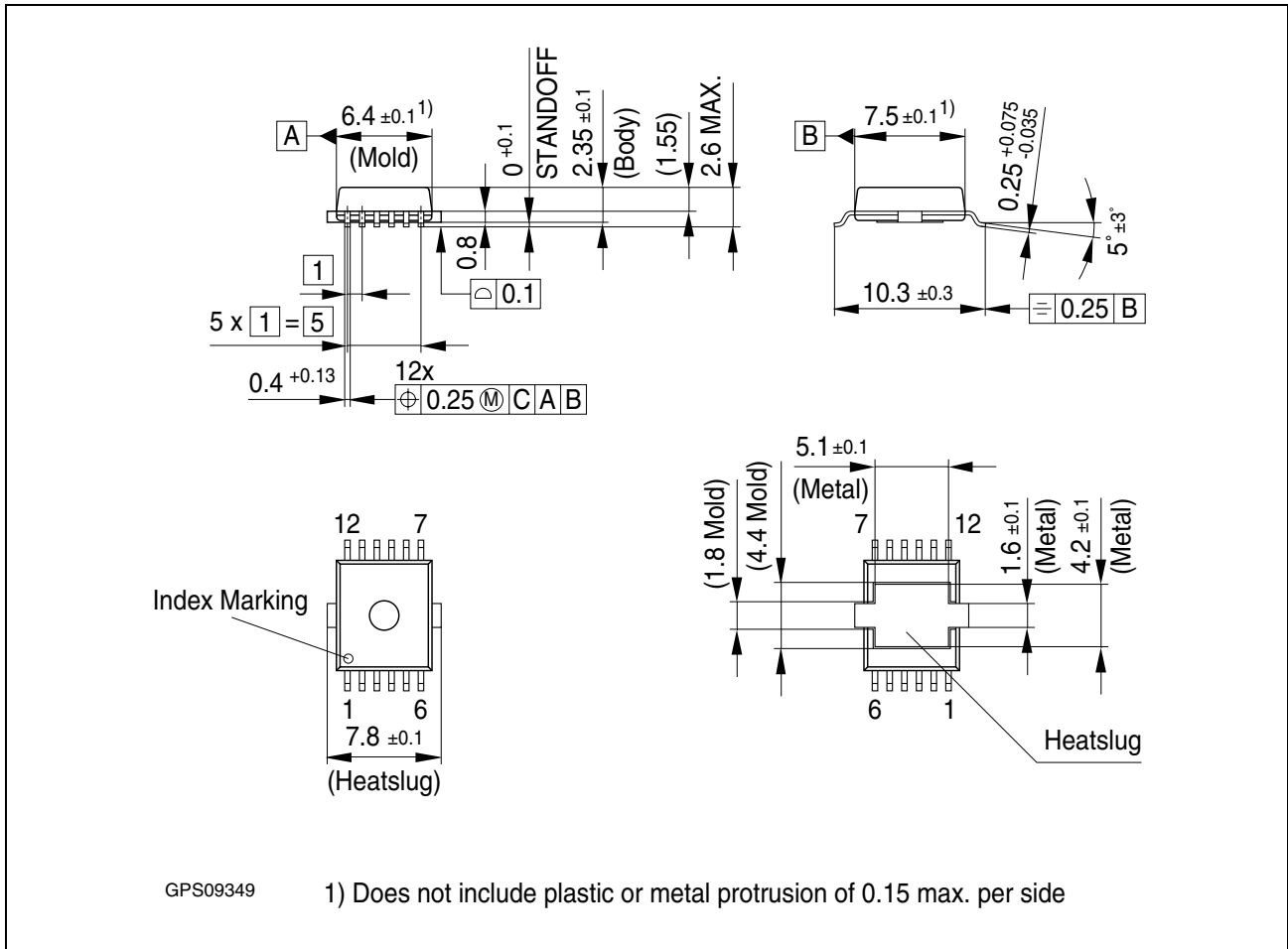


Figure 4 PG-DSO-12-11 (Plastic Dual Small Outline)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": <http://www.infineon.com/products>.

SMD = Surface Mounted Device

Dimensions in mm

## Revision History

Version	Date	Changes
Rev. 1.2	2008-10-28	<p>Modification according to PCN No. 2007-117-A:</p> <ul style="list-style-type: none"> <li>• <b>“Watchdog and Reset Timing D2” on Page 10:</b> Lower timing threshold <math>V_{DL2}</math>: Max limit change to 0.6V (was 0.5V) and typ. limit change to 0.45V (was 0.4V). The change does not impact watchdog or reset timing limits</li> </ul>
Rev. 1.1	2007-12-19	<p>Modification according to PCN No. 2007-117-A:</p> <ul style="list-style-type: none"> <li>• Page 9: Quiescent current <math>I_q</math>; inhibited (<math>V_{INH1} = V_{INH2} = 0\text{ V}</math>; <math>T_j &lt; 150\text{ °C}</math>): Max. limit changed to 20<math>\mu</math>A (was 15<math>\mu</math>A).</li> </ul>
Rev 1.0	2006-12-21	Initial version final datasheet



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#### **Information**

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

#### **Warnings**

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