



## 1 Overview

### Features

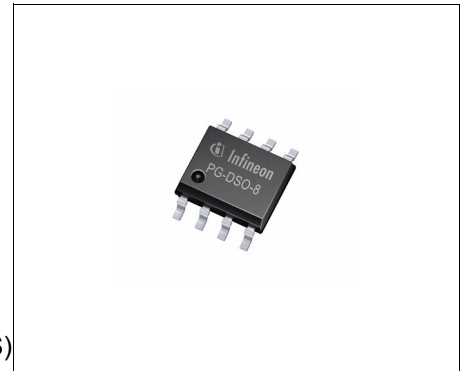
- 70 mA output current capability
- Very tight output tracking tolerance to reference
- Output voltage adjustable down to 2.0 V
- Stable operation with 1  $\mu$ F ceramic output capacitor
- Flexibility of output voltage adjust higher or lower than reference, proportional to the reference voltage (version GA / EJ A)
- Status output to indicate short circuits at the output (version GS / EJ S)
- Very low dropout voltage of typ. 0.2 V @ maximum output current
- Combined reference / enable input
- Very low current consumption in OFF mode
- Wide input voltage range  $-20 \text{ V} \leq V_I \leq +45 \text{ V}$
- Wide temperature range:  $-40 \text{ }^\circ\text{C} \leq T_J \leq 150 \text{ }^\circ\text{C}$
- Output protected against short circuit to GND and battery
- Input protected against reverse polarity
- Overtemperature protection
- Green product (RoHS compliant)
- AEC qualified

### Functional Description

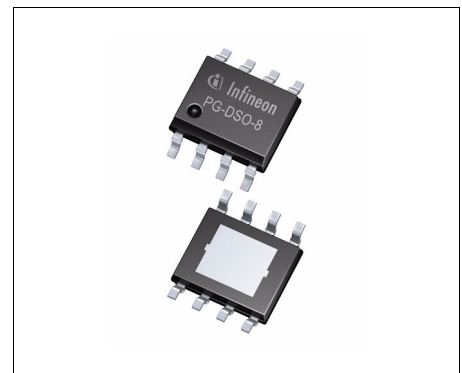
The TLE4254 is a monolithic integrated low-dropout voltage tracking regulator with high accuracy in small PG-DSO-8 packages. The IC is designed to supply off-board systems, e. g. sensors in powertrain management systems under the severe conditions of automotive applications. Therefore, the IC is equipped with additional protection functions against reverse polarity and short circuit to GND and battery.

With supply voltages up to 40 V, the output voltage follows a reference voltage applied at the adjust input with very high accuracy. The reference voltage applied directly to the adjust input or by an e. g. external resistor divider can be 2.0 V at minimum.

The output is able to drive loads up to 70 mA while the device follows with high accuracy the e. g. 5 V output of a main voltage regulator acting as reference.



**PG-DSO-8**



**PG-DSO-8 exposed pad**

Type	Package	Marking
TLE4254GA	PG-DSO-8	4254GA
TLE4254GS	PG-DSO-8	4254GS
TLE4254EJ A	PG-DSO-8 exposed pad	4254EJA
TLE4254EJ S	PG-DSO-8 exposed pad	4254EJS

The TLE4254 can be set into shutdown mode in order to reduce the current consumption to a minimum. This suits the IC for low power battery applications.

Versions "GS" and "EJ S" offer an open collector status output indicating an overvoltage and undervoltage error condition of the output voltage.

Versions "GA" and "EJ A" allow setting the output voltage to higher value than the reference voltage by connecting a voltage divider to the feedback pin "FB".

## 2 Block Diagram

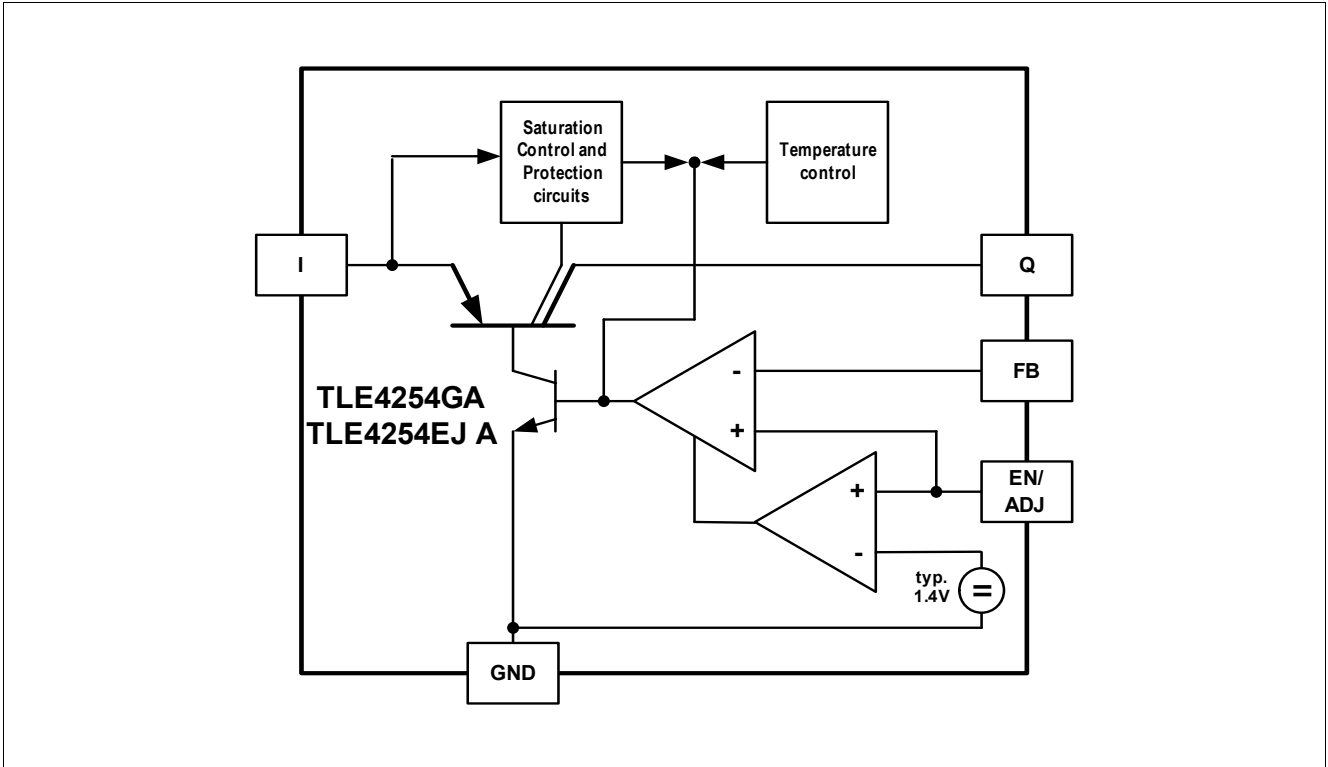


Figure 1 Block Diagram TLE4254GA and TLE4254EJ A

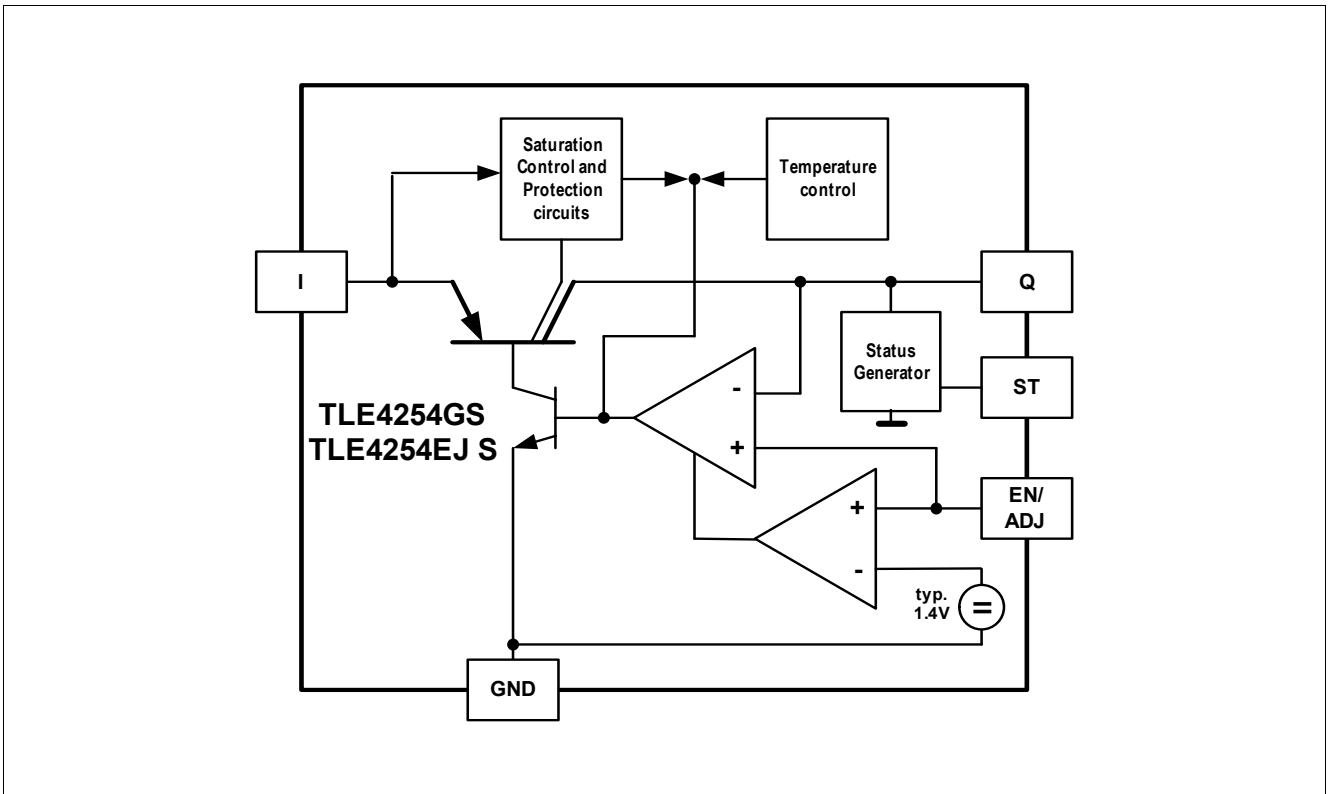


Figure 2 Block Diagram TLE4254GS and TLE4254EJ S

### 3 Pin Definitions and Functions

#### 3.1 Pin Assignment TLE4254GA and TLE4254GS

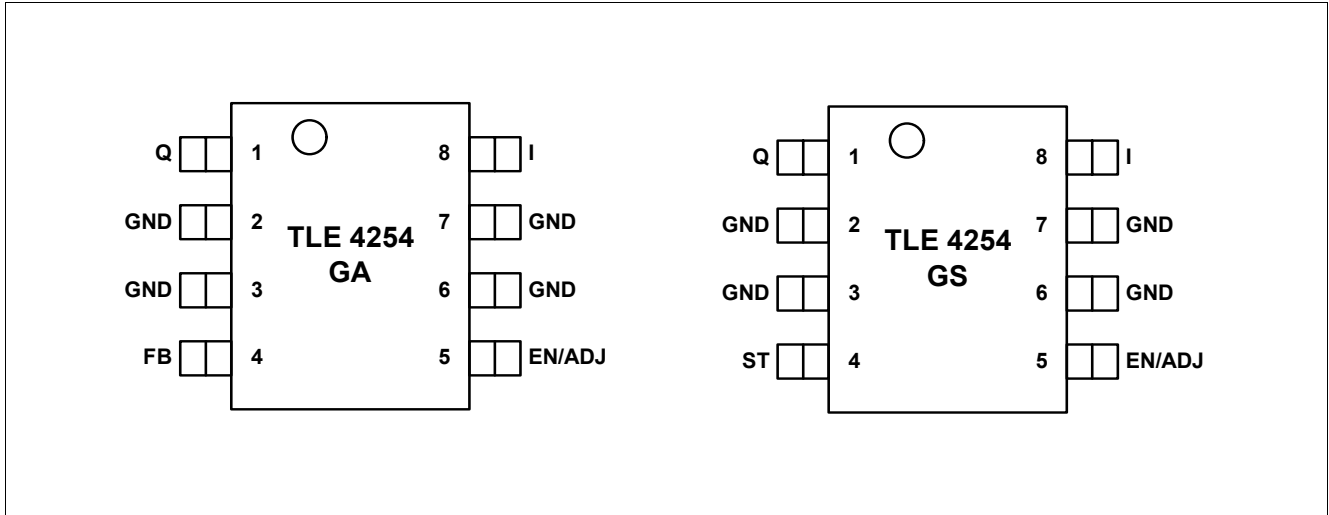


Figure 3 Pin Configurations TLE4254GA and TLE4254GS

#### 3.2 Pin Functions TLE4254GA and TLE4254GS

Pin	Symbol	Function
1	Q	<b>Tracker Output.</b> Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the table “Functional Range”.
2, 3, 6, 7	GND	<b>Ground reference.</b> Interconnect the pins on PCB. Connect to heatsink area.
4	FB (version GA)	<b>Feedback input (version GA only).</b> Non inverting input of the internal error amplifier to control the output voltage. Connect this pin directly to the output pin in order to obtain lower or equal output voltages with respect to the reference voltage. Connect a voltage divider for higher output voltages than the reference. (See also application information.)
4	ST (version GS)	<b>Tracking Regulator Status Output (version GS only).</b> Open collector output. Connect via a pull-up resistor to a positive voltage rail. A low signal indicates fault condions at the regulator’s output.
5	EN/ADJ	<b>Adjust / Enable.</b> Connect the reference to this pin. The active high signal of the reference turns on the device; a low signal disables the IC. The reference voltage can be connected directly or by a voltage divider for lower output voltages (see application information).
8	I	<b>Input.</b> IC supply. For compensating line influences, a capacitor close to the IC terminals is recommended.

### 3.3 Pin Assignment TLE4254EJ A and TLE4254EJ S

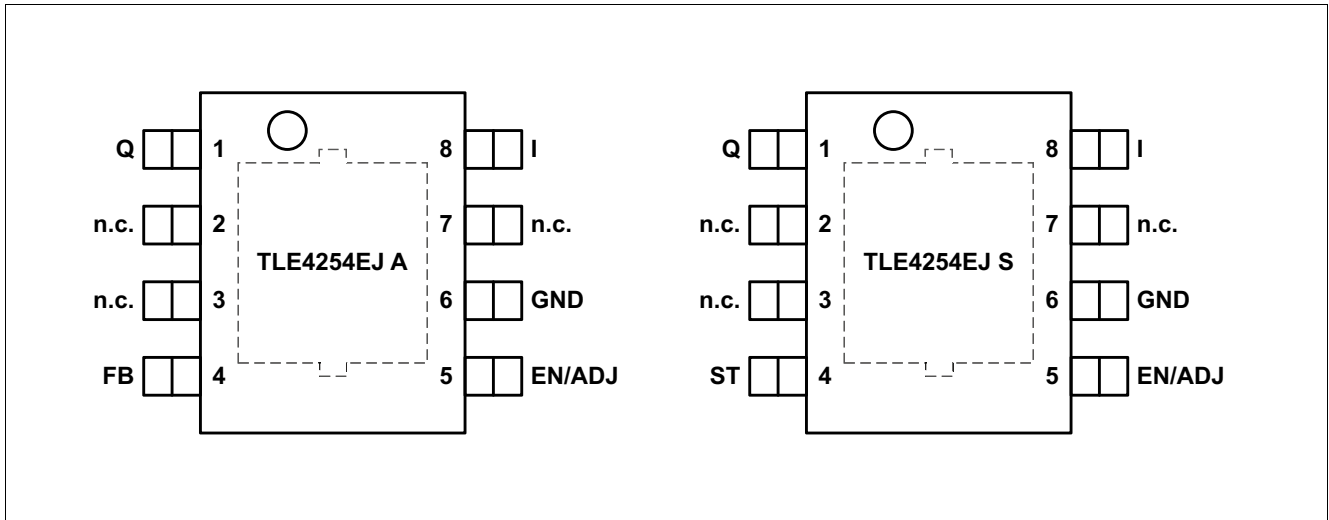


Figure 4 Pin Configurations TLE4254EJ A and TLE4254EJ S

### 3.4 Pin Functions TLE4254EJ A and TLE4254EJ S

Pin	Symbol	Function
1	Q	<b>Tracker Output.</b> Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the table “Functional Range”.
2, 3, 7	n.c.	<b>not connected</b> connect to GND
4	FB (version EJ A)	<b>Feedback input (version EJ A only).</b> Non inverting input of the internal error amplifier to control the output voltage. Connect this pin directly to the output pin in order to obtain lower or equal output voltages with respect to the reference voltage. Connect a voltage divider for higher output voltages than the reference. (See also application information.)
4	ST (version EJ S)	<b>Tracking Regulator Status Output (version GS only).</b> Open collector output. Connect via a pull-up resistor to a positive voltage rail. A low signal indicates fault condions at the regulator’s output.
5	EN/ADJ	<b>Adjust / Enable.</b> Connect the reference to this pin. The active high signal of the reference turns on the device; a low signal disables the IC. The reference voltage can be connected directly or by a voltage divider for lower output voltages (see application information).
6	GND	<b>Ground reference.</b> Interconnect the pins on PCB. Connect to heatsink area.
8	I	<b>Input.</b> IC supply. For compensating line influences, a capacitor close to the IC terminals is recommended.
Pad	–	<b>Exposed Pad</b> connect to GND

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings <sup>1)</sup>

-40 °C ≤ T<sub>j</sub> ≤ 150 °C; all voltages with respect to ground (unless otherwise specified).

Not subject to production test; specified by design.

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
<b>Voltages</b>						
4.1.1	Input voltage	V <sub>I</sub>	-20	45	V	–
4.1.2	Adjust / Enable input voltage	V <sub>ADJ/EN</sub>	-20	45	V	–
4.1.3	Output voltage	V <sub>Q</sub>	-5	45	V	–
4.1.4	Feedback input voltage (version GA / EJ A)	V <sub>FB</sub>	-20	45	V	–
4.1.5	Status output voltage (version GS / EJ S)	V <sub>ST</sub>	-0.3	7	V	–
<b>Temperatures</b>						
4.1.6	Junction Temperature	T <sub>j</sub>	-40	150	°C	–
4.1.7	Storage Temperature	T <sub>stg</sub>	-50	150	°C	–
<b>ESD Rating</b>						
4.1.8	ESD Susceptibility	V <sub>ESD,HBM</sub>	4	–	kV	HBM <sup>2)</sup>
4.1.9		V <sub>ESD,CDM</sub>	1	–	kV	CDM <sup>3)</sup>

1) Not subject to production test, specified by design.

2) ESD susceptibility Human Body Model "HBM" according to AEC-Q100-002 - JESD22-A114

3) ESD susceptibility Charged Device Model "CDM" according to ESDA STM5.3.1

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input Voltage	$V_I$	4	45	V	$V_I \geq V_Q + V_{dr}$
4.2.1	Adjust / Enable Input Voltage (Voltage Tracking Range)	$V_{ADJ/EN}$	2.0	–	V	–
4.2.2	Junction Temperature	$T_j$	-40	150	°C	–
4.2.3	Output Capacitor	$C_Q$	1	–	µF	– <sup>1)</sup>
4.2.4		$ESR_{CQ}$	–	5	Ω	– <sup>1)</sup>

1) Not subject to production test; specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

## 4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		

PG-DSO-8:

4.3.1	Junction to Ambient	$R_{thJA}$	–	155	–	K/W	Footprint only <sup>1) 2)</sup>
4.3.2			–	96	–	K/W	300 mm <sup>2</sup> PCB heatsink area <sup>1) 2)</sup>
4.3.3			–	86	–	K/W	600 mm <sup>2</sup> PCB heatsink area <sup>2) 1)</sup>

PG-DSO-8 exposed pad:

4.3.4	Junction to Case	$R_{thJC}$	–	15	–	K/W	measured to exposed pad
4.3.5	Junction to Ambient	$R_{thJA}$	–	47	–	K/W	– <sup>3)</sup>
4.3.6			–	159	–	K/W	Footprint only <sup>2) 1)</sup>
4.3.7			–	71	–	K/W	300 mm <sup>2</sup> PCB heatsink area <sup>2) 1)</sup>
4.3.8			–	60	–	K/W	600 mm <sup>2</sup> PCB heatsink area <sup>2) 1)</sup>

1) Not subject to production test; specified by design.

2) Package mounted on PCB FR4; 80 x 80 x 1.5 mm; 35 µm Cu, 5 µm Sn; horizontal position; zero airflow.

3) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

## 5 Electrical Characteristics

### 5.1 Tracking Regulator

The output voltage  $V_Q$  is controlled by comparing it to the voltage applied at pin ADJ/EN and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor  $C_Q$ , the load current, the chip temperature and the poles/zeros introduced by the integrated circuit and the load. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table "Functional Range" have to be maintained. For details see also the typical performance graph "Output Capacitor Series Resistor  $ESR_{CQ}$  vs. Output Current  $I_Q$ ". Also, the output capacitor shall be sized to buffer load transients.

An input capacitor  $C_I$  is strongly recommended to buffer line influences. Connect the capacitors close to the IC terminals.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at high input voltages.

The overtemperature protection circuit prevents the IC from immediate destruction under fault conditions (e. g. output continuously short-circuited) by reducing the output current. A thermal balance below 200 °C junction temperature is established. Please note that a junction temperature above 150 °C is outside the maximum ratings and reduces the IC lifetime.

The TLE4254 allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

**Table 1 Electrical Characteristics Tracking Regulator**

$V_I = 13.5\text{ V}$ ;  $V_{ADJ/EN} \geq 2.0\text{ V}$ ;  $V_{FB} = V_Q$  (version GA / EJ A);  $-40\text{ °C} \leq T_j \leq 150\text{ °C}$ ;  $C_Q = 1\text{ }\mu\text{F}$ ;  
all voltages with respect to ground (unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
5.1.1	Output Voltage Tracking Accuracy $\Delta V_Q = V_{EN/ADJ} - V_Q$	$\Delta V_Q$	-5	–	5	mV	$8\text{ V} \leq V_I \leq 18\text{ V}$ ; $0.1\text{ mA} \leq I_Q \leq 60\text{ mA}$ ; $V_{ADJ/EN} = 5\text{ V}$
5.1.2			-10	–	10	mV	$5.5\text{ V} \leq V_I \leq 26\text{ V}$ ; $0.1\text{ mA} \leq I_Q \leq 60\text{ mA}$ ; $V_{ADJ/EN} = 5\text{ V}$
5.1.3			-10	–	10	mV	$5.5\text{ V} \leq V_I \leq 32\text{ V}$ ; $0.1\text{ mA} \leq I_Q \leq 30\text{ mA}$ ; $V_{ADJ/EN} = 5\text{ V}$
5.1.4	Load Regulation steady-state	$ dV_{Q,load} $	–	1	10	mV	$I_Q = 0.1\text{ mA to }70\text{ mA}$ ; $V_{ADJ/EN} = 5\text{ V}$
5.1.5	Line Regulation steady-state	$ dV_{Q,line} $	–	1	10	mV	$V_I = 5.5\text{ V to }32\text{ V}$ ; $I_Q = 5\text{ mA}$ $V_{ADJ/EN} = 5\text{ V}$



**Table 1 Electrical Characteristics Tracking Regulator**

$V_I = 13.5 \text{ V}$ ;  $V_{\text{ADJ/EN}} \geq 2.0 \text{ V}$ ;  $V_{\text{FB}} = V_Q$  (version GA / EJ A);  $-40 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$ ;  $C_Q = 1 \text{ } \mu\text{F}$ ;  
all voltages with respect to ground (unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
5.1.6	Power Supply Ripple Rejection	$PSRR$	60	–	–	dB	$f_{\text{ripple}} = 100 \text{ Hz}$ ; $V_{\text{ripple}} = 1 \text{ Vpp}$ $I_Q = 5 \text{ mA}$ $C_Q = 10 \text{ } \mu\text{F}$ , ceramic type <sup>1)</sup>
5.1.7	Dropout Voltage $V_{\text{dr}} = V_I - V_Q$	$V_{\text{dr}}$	–	200	400	mV	$I_Q = 70 \text{ mA}$ <sup>2)</sup>
5.1.8	Output Current Limitation	$I_{Q,\text{max}}$	71	100	150	mA	$V_Q = (V_{\text{ADJ/EN}} - 0.1 \text{ V})$ ; $V_{\text{ADJ/EN}} = 5 \text{ V}$
5.1.9	Reverse Current	$I_Q$	-4	-2	–	mA	$V_I = 0 \text{ V}$ ; $V_Q = 32 \text{ V}$ ; $V_{\text{ADJ/EN}} = 5 \text{ V}$
5.1.10	Reverse Current at Negative Input Voltage	$I_I$	-5	-3	–	mA	$V_I = -16 \text{ V}$ ; $V_Q = 0 \text{ V}$ ; $V_{\text{ADJ/EN}} = 5 \text{ V}$

**Feedback Input FB (version GA / EJ A only):**

5.1.11	Feedback Input Biasing Current	$I_{\text{FB}}$	–	0.1	0.5	$\mu\text{A}$	$V_{\text{FB}} = 5 \text{ V}$
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**Overtemperature Protection:**

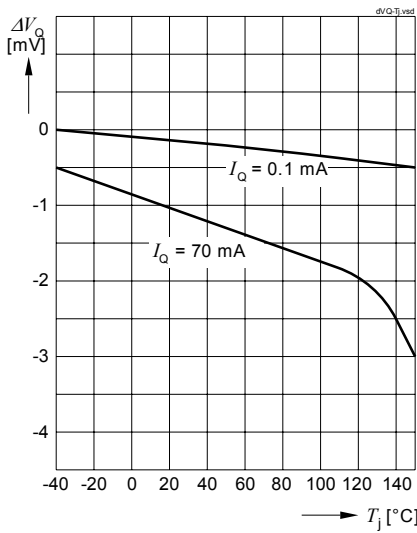
5.1.12	Junction Temperature Equilibrium	$T_{j,\text{eq}}$	151	–	200	$^\circ\text{C}$	$T_j$ increasing due to power dissipation generated by the IC <sup>1)</sup>
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1) Parameter not subject to production test; specified by design.

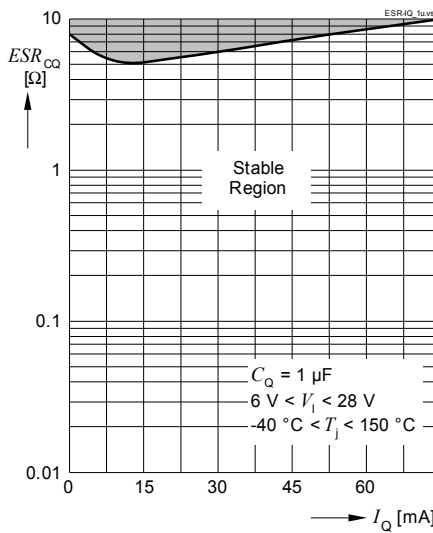
2) Measured when the output voltage  $V_Q$  has dropped 100 mV from its nominal value.

Typical Performance Characteristics Tracking Regulator

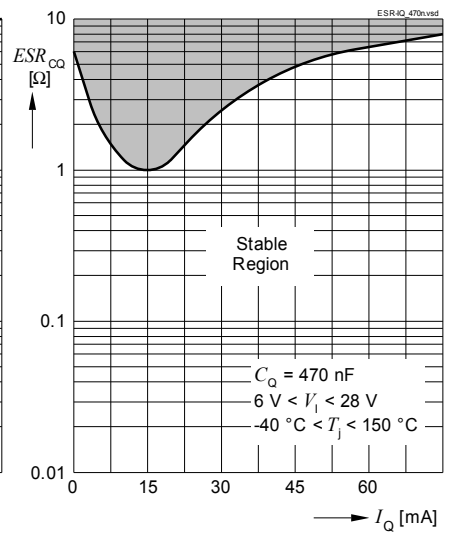
Tracking Accuracy  $\Delta V_Q$  vs. Junction Temperature  $T_j$



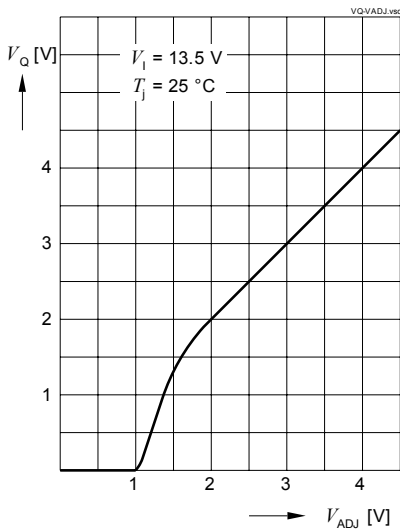
Output Capacitor Series Resistor  $ESR_{CQ}$  vs. Output Current  $I_Q$



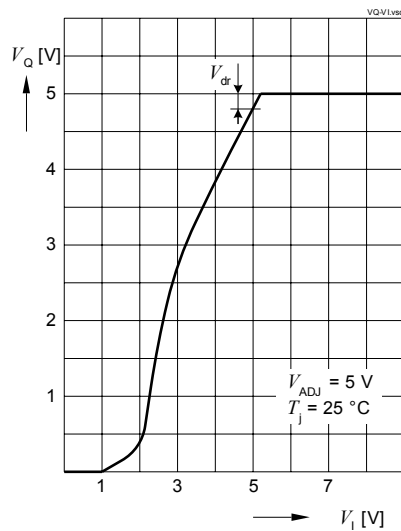
Output Capacitor Series Resistor  $ESR_{CQ}$  vs. Output Current  $I_Q$



Output Voltage  $V_Q$  vs. Adjust Voltage  $V_{ADJ,EN}$

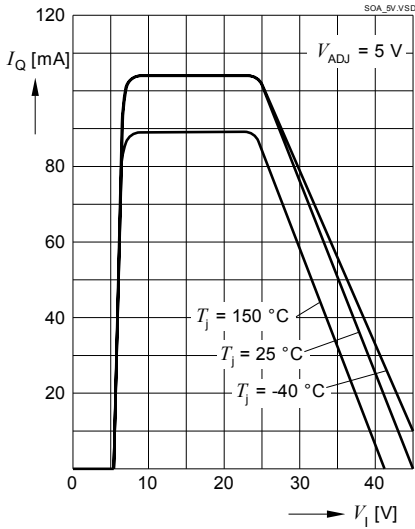


Output Voltage  $V_Q$  vs. Input Voltage  $V_I$

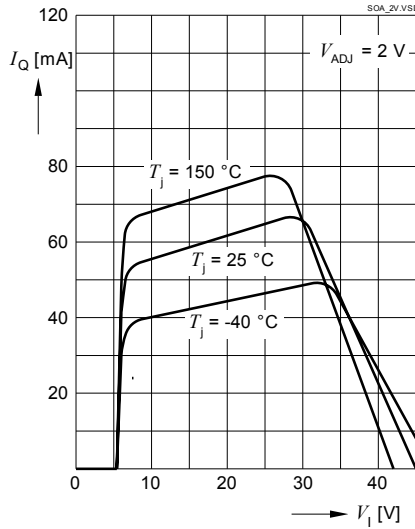


Typical Performance Characteristics Tracking Regulator

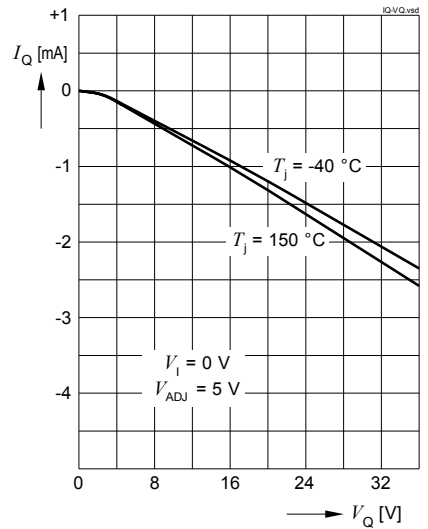
Output Current Limitation  $I_{Q,max}$  vs. Input Voltage  $V_i$ ,  $V_{ADJ,EN} = 5V$



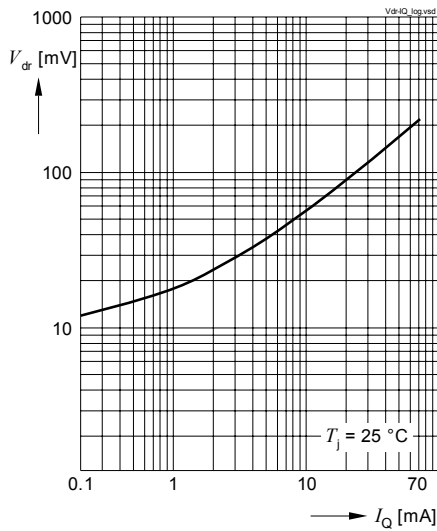
Output Current Limitation  $I_{Q,max}$  vs. Input Voltage  $V_i$ ,  $V_{ADJ,EN} = 2V$



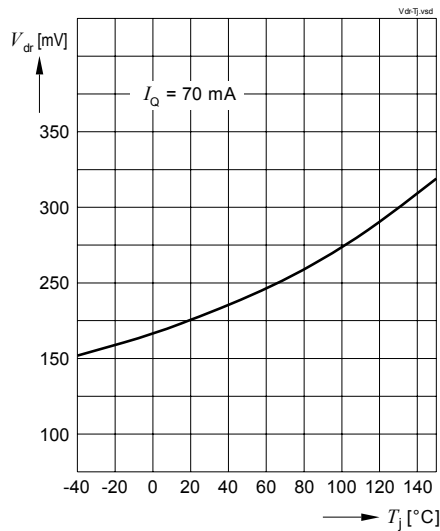
Reverse Output Current  $I_Q$  vs. Output Voltage  $V_Q$



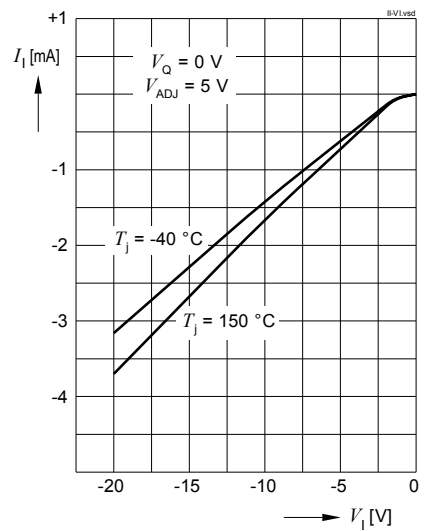
Dropout Voltage  $V_{dr}$  vs. Output Current  $I_Q$



Dropout Voltage  $V_{dr}$  vs. Junction Temperature  $T_j$



Reverse Current  $I_i$  vs. Input Voltage  $V_i$



## 5.2 Current Consumption

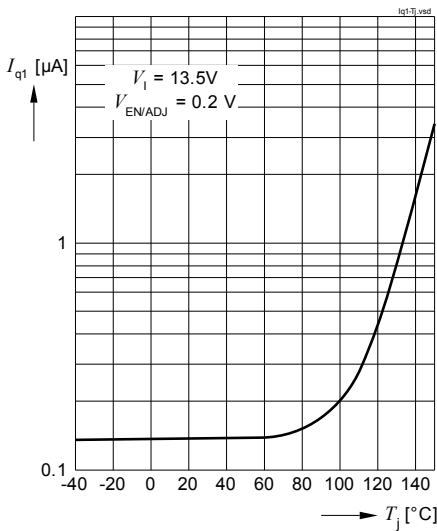
**Table 2 Electrical Characteristics Current Consumption**

$V_I = 13.5\text{ V}$ ;  $V_{\text{ADJ/EN}} \geq 2.0\text{ V}$ ;  $V_{\text{FB}} = V_Q$  (version GA / EJ A);  $-40\text{ }^\circ\text{C} \leq T_j \leq 150\text{ }^\circ\text{C}$ ;  $C_Q = 1\text{ }\mu\text{F}$   
all voltages with respect to ground (unless otherwise specified).

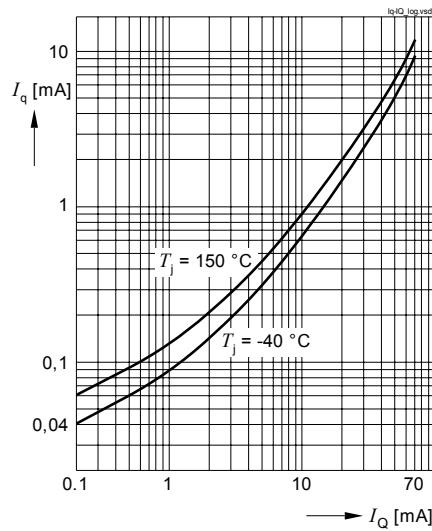
Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.13	Quiescent Current Stand-by Mode	$I_{q1}$	–	1	5	$\mu\text{A}$	$V_{\text{ADJ/EN}} \leq 0.4\text{ V}$ ; $T_j \leq 125\text{ }^\circ\text{C}$
5.2.14	Current Consumption $I_q = I_I - I_Q$	$I_{q2}$	–	50	80	$\mu\text{A}$	$I_Q \leq 100\text{ }\mu\text{A}$ ; $V_{\text{ADJ/EN}} = 5\text{ V}$
5.2.15			–	9	15	$\text{mA}$	$I_Q \leq 70\text{ mA}$ ; $V_{\text{ADJ/EN}} = 5\text{ V}$

### Typical Performance Characteristics Current Consumption

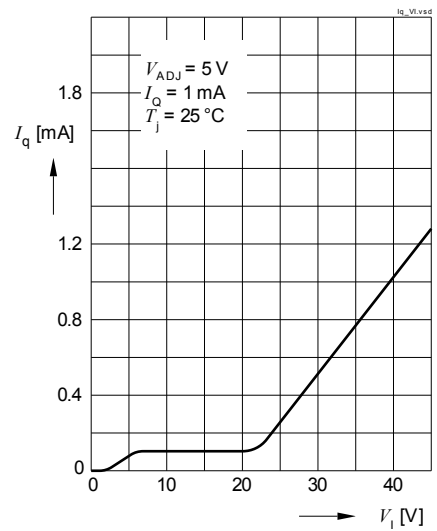
**Quiescent Current  $I_{q1}$  vs. Junction Temperature  $T_j$**



**Current Consumption  $I_{q2}$  vs. Output Current  $I_Q$**



**Current Consumption  $I_q$  vs. Input Voltage  $V_I$**



### 5.3 Adjust / Enable Input

In order to reduce the quiescent current to a minimum, the TLE4254 can be switched to stand-by mode by setting the adjust/enable input "ADJ/EN" to "low".

In case the pin "ADJ/EN" is left open, an internal pull-down resistor keeps the voltage at the pin low and therefore ensures that the regulator is switched off.

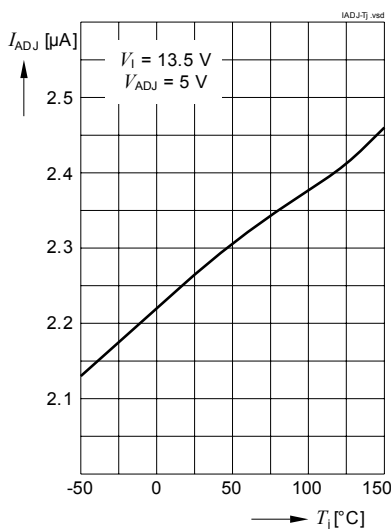
**Table 3 Electrical Characteristics Adjust / Enable**

$V_I = 13.5\text{ V}$ ;  $V_{ADJ/EN} \geq 2.0\text{ V}$ ;  $V_{FB} = V_Q$  (version GA / EJ A);  $-40\text{ °C} \leq T_j \leq 150\text{ °C}$ ;  $C_Q = 1\text{ }\mu\text{F}$   
all voltages with respect to ground (unless otherwise specified).

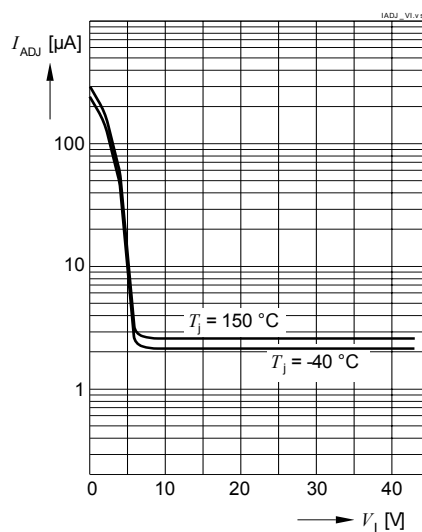
Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
5.3.16	Adjust / Enable Low Signal Valid	$V_{ADJ/EN,low}$	–	–	0.4	V	$V_Q = 0\text{ V}$ ; $I_Q \leq 5\text{ }\mu\text{A}$ @ $T_j \leq 125\text{ °C}$
5.3.17	Adjust / Enable High Signal Valid (Tracking Region)	$V_{ADJ/EN,high}$	2	–	–	V	$V_Q$ settled
5.3.18	Adjust / Enable Input Current	$I_{ADJ/EN}$	–	2	3	$\mu\text{A}$	$V_{ADJ/EN} = 5\text{ V}$
5.3.19	Adjust / Enable Input Current if Input tied to GND	$I_{ADJ/EN}$	–	0.3	0.6	mA	$V_{ADJ/EN} = 5\text{ V}$ ; $V_I = 0\text{ V}$
5.3.20	Adjust / Enable internal pull-down resistor	$R_{ADJ/EN}$	1.7	2.5	3.3	M $\Omega$	

#### Typical Performance Characteristics Adjust / Enable Input

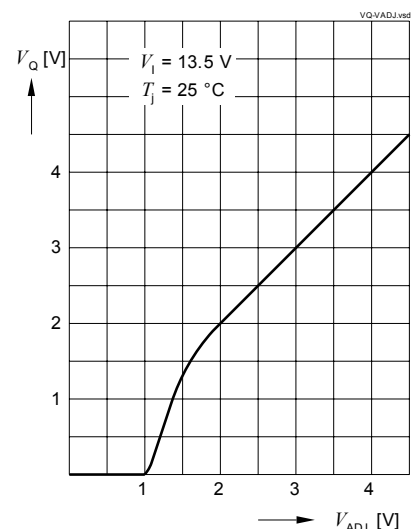
**Adjust / Enable Input Current  $I_{ADJ/EN}$  vs.  $T_j$**



**Adjust / Enable Input Current  $I_{ADJ/EN}$  vs.  $V_I$**



**Startup Sequence  $V_Q$  vs.  $V_{ADJ,EN}$**



## 5.4 Status Output (version GS / EJ S only)

The status output ST indicates an overvoltage or undervoltage situation at the regulator's output Q. Therefore, the output voltage  $V_Q$  is compared to the reference voltage  $V_{ADJ/EN}$ . Variations of the output voltage are indicated by a low signal at the status output ST. Transients shorter than the status reaction time  $t_{ST,r}$  will not trigger the status output.

The status output ST is an open collector output, requiring a pull-up resistor to a positive voltage rail.

**Table 4 Electrical Characteristics Status Output ST (Version GS / EJ S only)**

$V_I = 13.5 \text{ V}$ ;  $V_{ADJ/EN} \geq 2.0 \text{ V}$ ;  $-40 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$ ;  $C_Q = 1 \text{ } \mu\text{F}$   
all voltages with respect to ground (unless otherwise specified).

Pos.	Parameter	Symbol	Limit Values			Unit	Test Condition
			Min.	Typ.	Max.		
5.4.21	Status switching threshold, undervoltage	$V_{Q,UV}$	$V_{ADJ/EN}$ - 120	$V_{ADJ/EN}$ - 70	$V_{ADJ/EN}$ - 50	mV	$V_Q$ decreasing
5.4.22	Status switching threshold, overvoltage	$V_{Q,OV}$	$V_{ADJ/EN}$ + 50	$V_{ADJ/EN}$ + 70	$V_{ADJ/EN}$ + 120	mV	$V_Q$ increasing
5.4.23	Status reaction time	$t_{ST,r}$	10	15	30	$\mu\text{s}$	–
5.4.24	Status output low voltage	$V_{ST,low}$	–	–	0.4	V	$I_{ST} = 1 \text{ mA}$ ; $V_I \geq 4 \text{ V}$
5.4.25	Status output sink current limitation	$I_{ST,max}$	1	–	–	mA	$I_{ST} = 1 \text{ mA}$ ; $V_{ST} = 0.8 \text{ V}$
5.4.26	Status output leakage current	$I_{ST,leak}$	–	0	2	$\mu\text{A}$	$V_Q = V_{ADJ/EN}$ $V_{ST} = 5 \text{ V}$

## 6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The application circuits shown are simplified examples. The function must be verified in the real application.

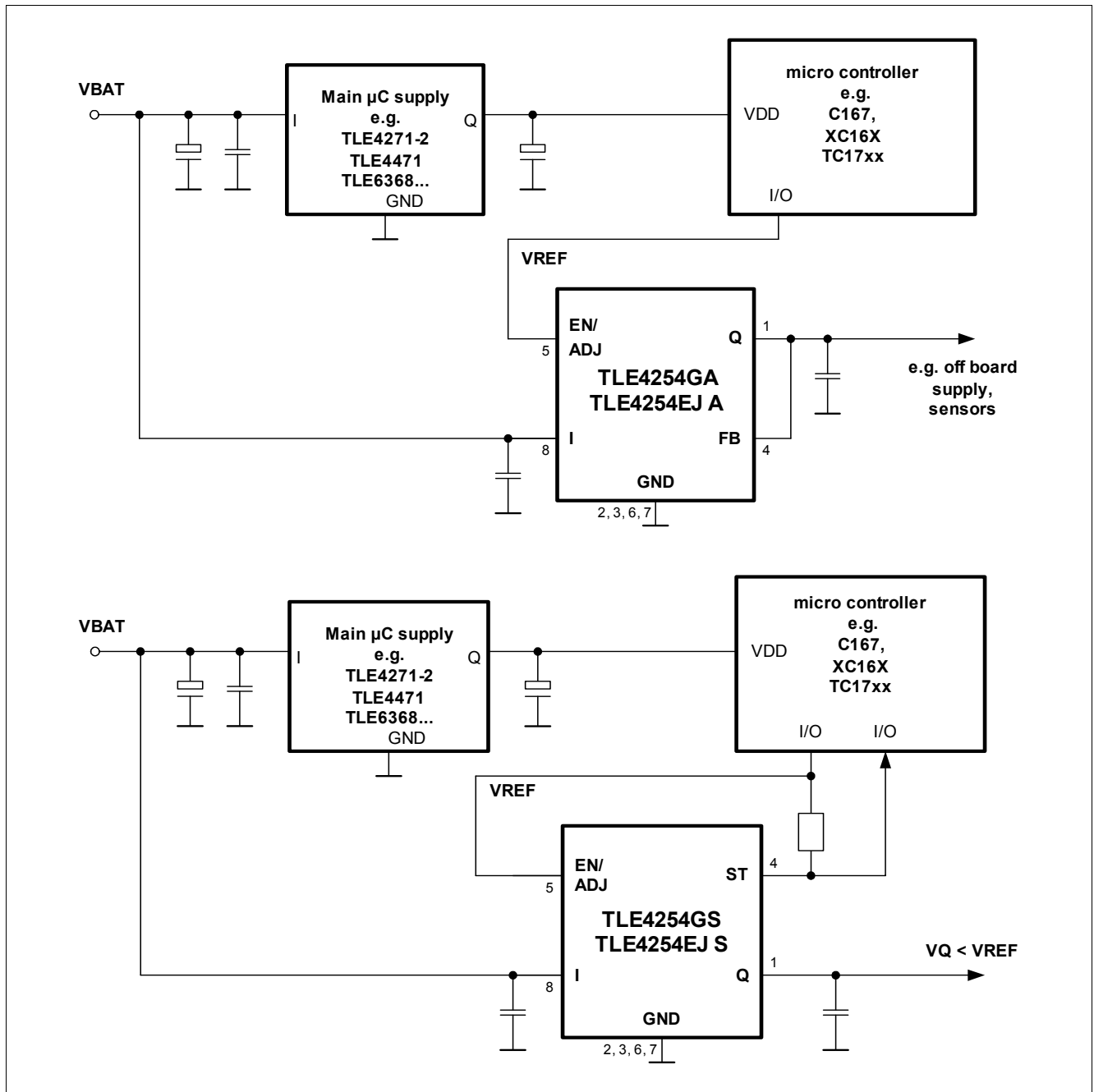
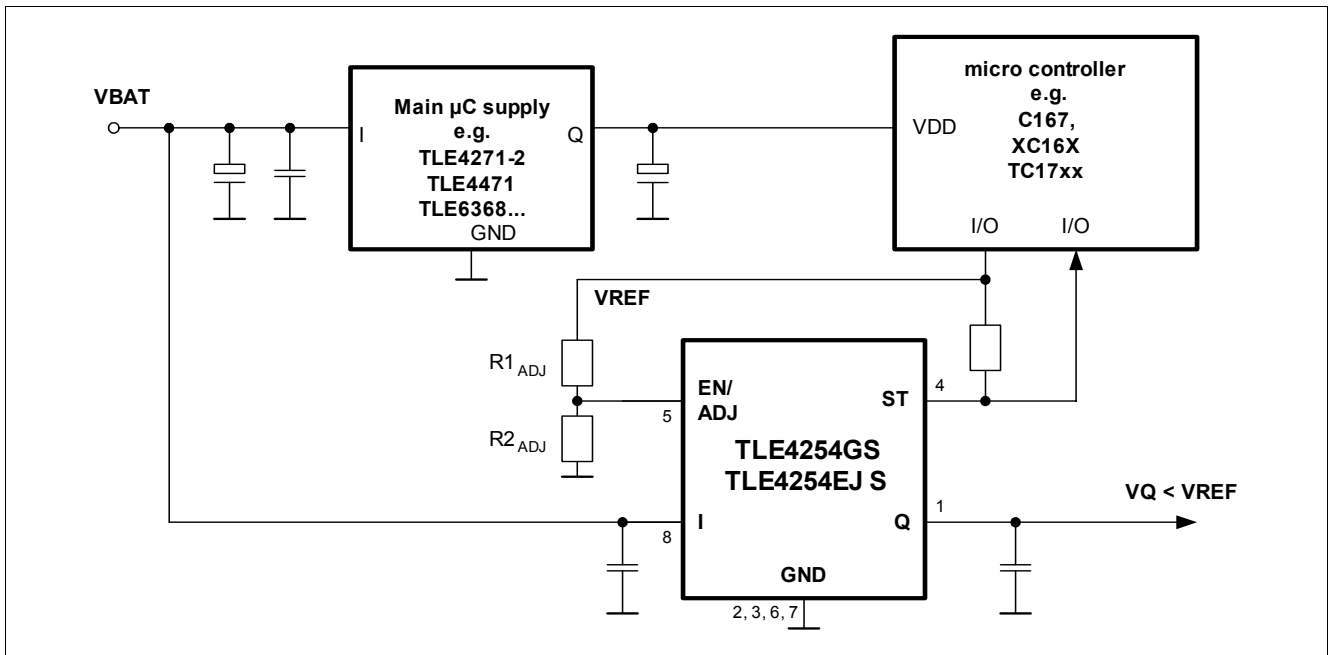


Figure 5 Application circuit: Output voltage  $V_Q$  equal to reference voltage  $V_{ADJ/EN}$

Figure 5 shows a typical schematic for applications where the tracker output voltage  $V_Q$  equals the reference voltage  $V_{REF}$  applied to the pin “EN/ADJ”. At version GA / EJ A, the pin FB is directly connected to the output “Q”. The reference voltage is directly applied to “EN/ADJ”.



**Figure 6** Application circuit: Output voltage  $V_Q$  lower than reference voltage  $V_{REF}$   
Status Output feedback to microcontroller (version GS / EJ S)

In order to obtain a lower output voltage  $V_Q$  at the tracker output than the reference voltage  $V_{REF}$ , a voltage divider according to **Application circuit: Output voltage  $V_Q$  lower than reference voltage  $V_{REF}$  Status Output feedback to microcontroller (version GS / EJ S)** has to be used. The output voltage  $V_Q$  then calculates:

$$V_Q = V_{REF} \cdot \left( \frac{R2_{ADJ}}{R1_{ADJ} + R2_{ADJ}} \right)$$

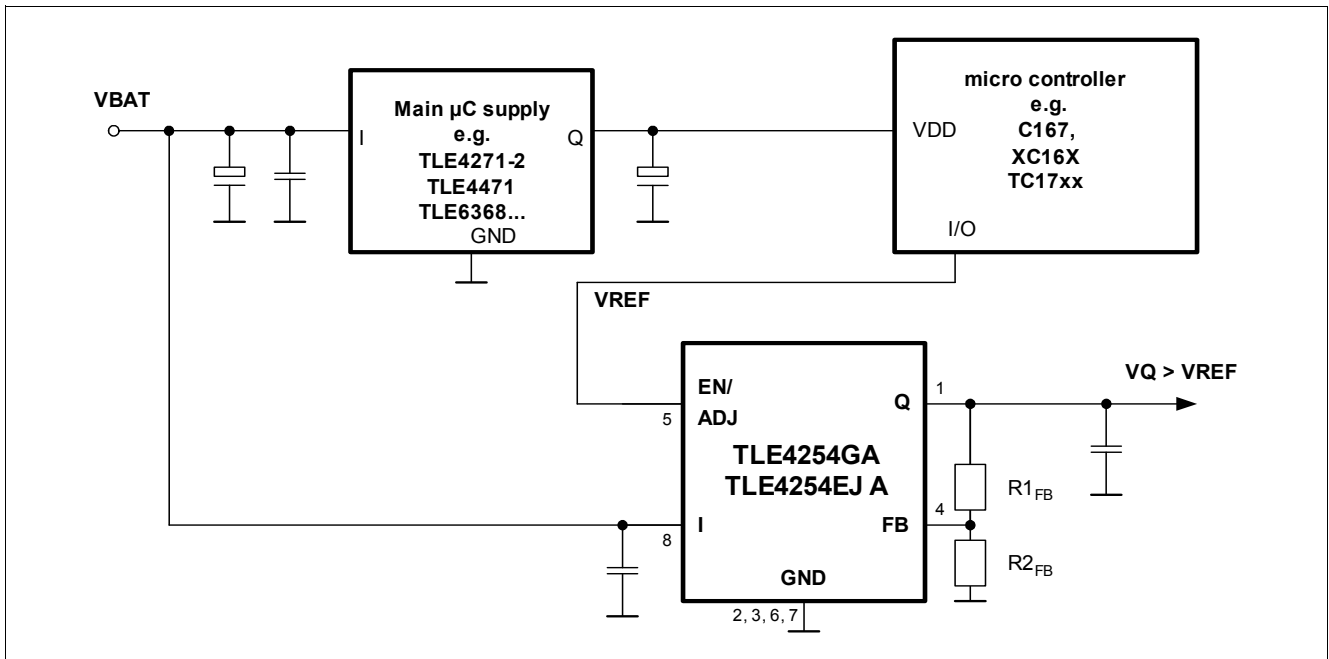
With a given reference voltage  $V_{REF}$ , the desired output voltage  $V_Q$  and the resistor value  $R1_{ADJ}$ , the resistor value for  $R2_{ADJ}$  is given by:

$$R2_{ADJ} = R1_{ADJ} \cdot \left( \frac{V_Q}{V_{REF} - V_Q} \right)$$

Taking into consideration also the effect of the internal EN/ADJ pull-down resistor, the external resistor divider's  $R2_{ADJ}$  has to be selected to:

$$R2_{ADJ,select} = \left( \frac{R2_{ADJ} \cdot R_{PullDown,min}}{R_{PullDown,min} - R2_{ADJ}} \right)$$





**Figure 7 Application circuit: Output voltage  $V_Q$  higher than reference voltage  $V_{REF}$  (version GA / EJ A only)**

For output voltages higher than the reference voltage, the voltage divider has to be applied between the feedback and the output according to **Application circuit: Output voltage  $V_Q$  higher than reference voltage  $V_{REF}$  (version GA / EJ A only)**. The equation for the output voltage with respect to the reference voltage is given by:

$$V_Q = V_{REF} \cdot \left( \frac{R1_{FB} + R2_{FB}}{R2_{FB}} \right)$$

Keep in mind that the input voltage has to be at minimum equal to the output voltage plus the dropout voltage of the regulator.

With a given reference voltage  $V_{REF}$ , the desired output voltage  $V_Q$  and the resistor value  $R1_{FB}$ , the resistor value for  $R2_{FB}$  is given by:

$$R2_{FB} = R1_{FB} \cdot \left( \frac{V_{REF}}{V_Q - V_{REF}} \right)$$

## 7 Package Outlines

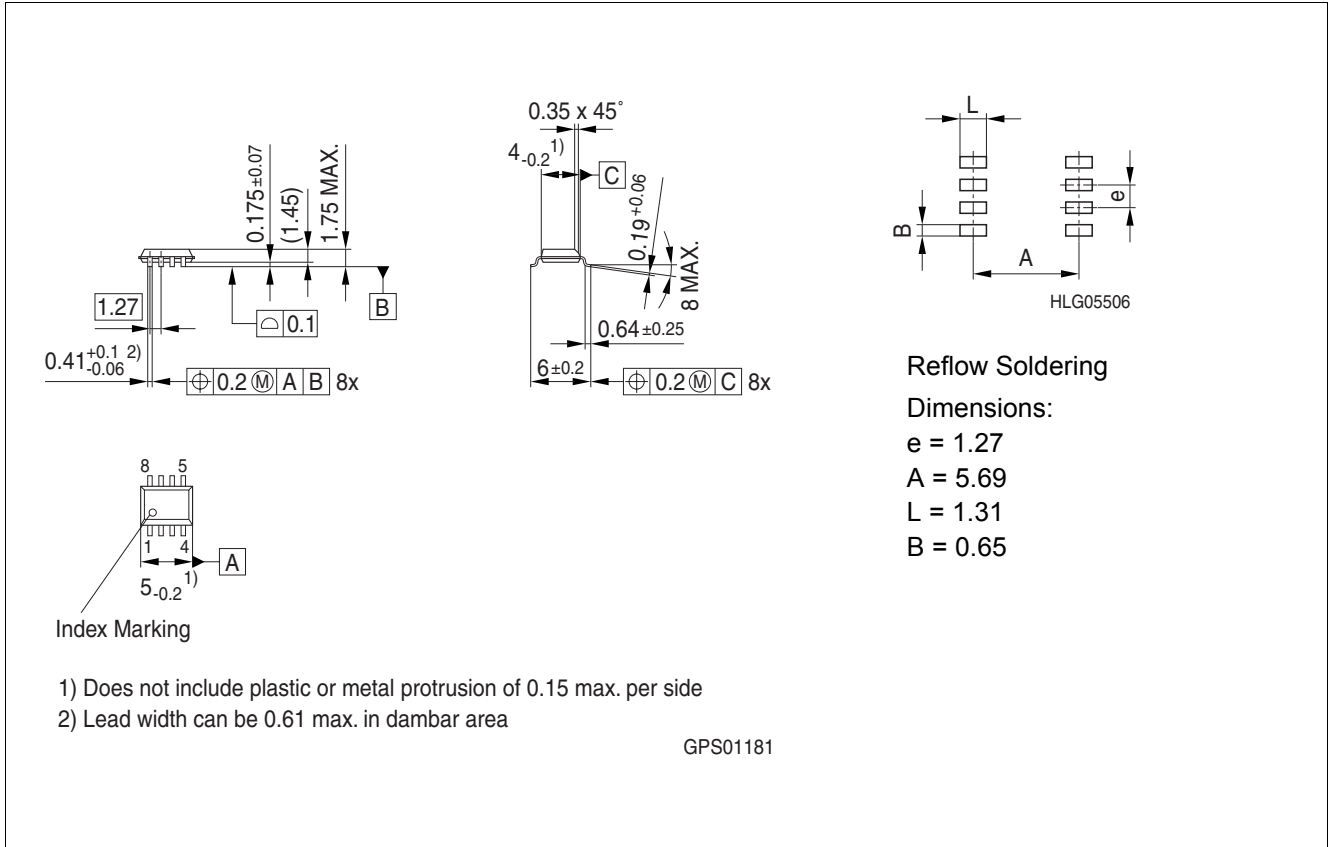
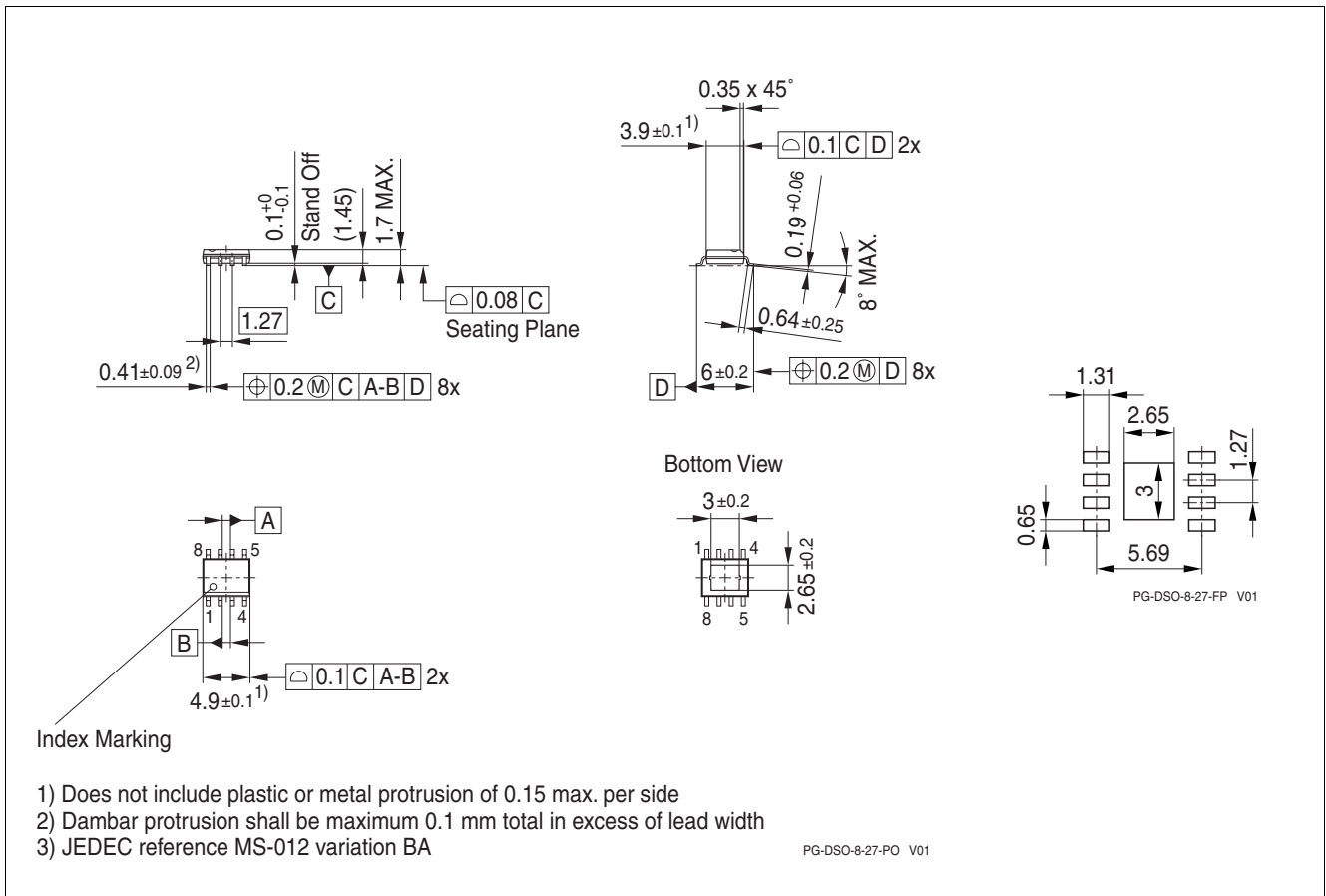


Figure 8 Outline and footprint PG-DSO-8



**Outline and footprint PG-DSO-8 exposed pad**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

## 8 Revision History

Revision History:	2009-11-18 Updated Version, product versions TLE4254EJ A and TLE4254EJ S in PG-DSO-8 exposed pad and all related description added	Rev. 1.2
Previous Version:	2008-07-16	Rev. 1.1
	typing errors corrected	
Previous Version:	2006-11-22	Rev. 1.0
	<b>“Package Outlines” on Page 18</b> Drawing Updated	

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