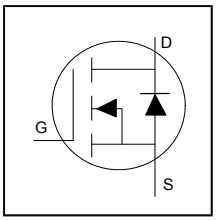
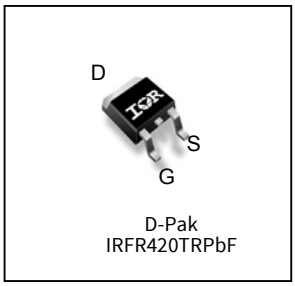
HEXFET® Power MOSFET

Benefits

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFR420)
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Pb-Free ; RoHS Compliant ; Halogen-Free



V_{DSS}	500V
$R_{DS(on)\ max}$	3.0Ω
$I_{D\ (Silicon\ Limited)}$	2.4A



D-Pak
IRFR420TRPbF

Halogen-Free RoHS

Description

Third Generation HEXFETs from Infineon Technology provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFR420PbF	D-Pak	Tape and Reel	2000	IRFR420TRPbF

Table of Contents

1 Parameters

Table1 Key performance parameters

Parameter	Values	Units
V_{DS}	500	V
$R_{DS(on)\ max}$	3.0	Ω
I_D	2.4	A

2 Maximum ratings and thermal characteristics

Table 2 Maximum ratings (at T_J=25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Values	Unit
Continuous Drain Current	I_D	T_C = 25°C, V_{GS} @ 10V	2.4	A
Continuous Drain Current	I_D	T_C = 100°C, V_{GS} @ 10V	1.5	
Pulsed Drain Current ①	I_{DM}	T_C = 25°C	8.0	
Maximum Power Dissipation	P_D	T_C = 25°C	42	W
Maximum Power Dissipation (PCB Mount)⑤	P_D	T_A = 25°C	2.5	
Linear Derating Factor		T_C = 25°C	0.33	W/°C
Linear Derating Factor (PCB Mount)⑤		T_A = 25°C	0.02	
Gate-to-Source Voltage	V_{GS}	-	± 20	V
Operating Junction and Storage Temperature Range	T_J T_{STG}	-	-55 to + 150	°C
Soldering Temperature, for 10 seconds (1.6mm from case)	-	-	260	

Table 3 Thermal characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Junction-to-Case ⑥	$R_{\theta JC}$	T_J approximately 90°C	-	-	3.0	°C/W
Junction-to-Ambient (PCB Mount) ⑤	$R_{\theta JA}$	-	-	-	50	
Junction-to-Ambient	$R_{\theta JA}$	-	-	-	110	

Table 4 Avalanche characteristics

Parameter	Symbol	Values	Unit
Single Pulse Avalanche Energy ②	$E_{AS\ (Thermally\ limited)}$	400	mJ
Avalanche Current ①	I_{AR}	2.4	A
Repetitive Avalanche Energy ①	E_{AR}	4.2	mJ

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Figure 11).

② Limited by T_{Jmax} , starting T_J = 25°C, L = 139mH, R_G = 25Ω, I_{AS} = 2.4A, V_{GS} =10V. (See Figure 10).

③ I_{SD} ≤2.4A, di/dt ≤50A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤150°C.

④ Pulse width ≤300µs; duty cycle ≤2%.

⑤ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.please refer to application note to AN-994.

⑥ R_θ is measured at T_J approximately 90°C.

3 Electrical characteristics

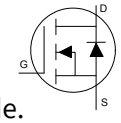
Table 5 Static characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250µA	500	-	-	V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	Reference to 25°C, I_D = 1mA	-	0.59	-	V/°C
Static Drain-to-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 1.4A	-	-	3.0	Ω
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} =500V, V_{GS} =0V	-	-	25	µA
		V_{DS} =400V,V_{GS} = 0V,T_J =125°C	-	-	250	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 20V	-	-	100	nA
Gate-to-Source Reverse Leakage	I_{GSS}	V_{GS} = -20V	-	-	-100	

Table 6 Dynamic characteristics

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Forward Trans conductance	gfs	V_{DS} = 50V, I_D = 1.4A	1.5	-	-	S
Total Gate Charge	Q_g	I_D = 2.1A V_{DS} = 400V V_{GS} = 10V See Fig.6 and 13	-	-	19	nC
Gate-to-Source Charge	Q_{gs}		-	-	3.3	
Gate-to-Drain Charge	Q_{gd}		-	-	13	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 250V I_D = 2.1A R_G = 18Ω R_D = 120Ω, See Fig.10	-	8.0	-	ns
Rise Time	t_r		-	8.6	-	
Turn-Off Delay Time	$t_{d(off)}$		-	33	-	
Fall Time	t_f		-	16	-	
Internal Drain Inductance	L_D	Between lead, 6mm (0.25in.) from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_s		-	7.5	-	
Input Capacitance	C_{iss}	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz, See Fig.5	-	360	-	pF
Output Capacitance	C_{oss}		-	92	-	
Reverse Transfer Capacitance	C_{rss}		-	37	-	

Table 7 Reverse Diode

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode. 	-	-	2.4	A
Pulsed Source Current (Body Diode) ①	I_{SM}		-	-	8.0	
Diode Forward Voltage	V_{SD}	T_J = 25°C, I_S = 2.4A,V_{GS} = 0V ④	-	-	1.6	V
Peak Diode Recovery dv/dt ③	dv/dt	T_J = 150°C, I_S = 2.1A,V_{DS} = 500V	-	-	3.5	V/ns
Reverse Recovery Time	t_{rr}	T_J = 25°C I_F = 2.1A, di/dt = 100A/µs ④	-	260	520	ns
Reverse Recovery Charge	Q_{rr}	T_J = 25°C	-	0.7	1.4	µC

4 Electrical characteristic diagrams

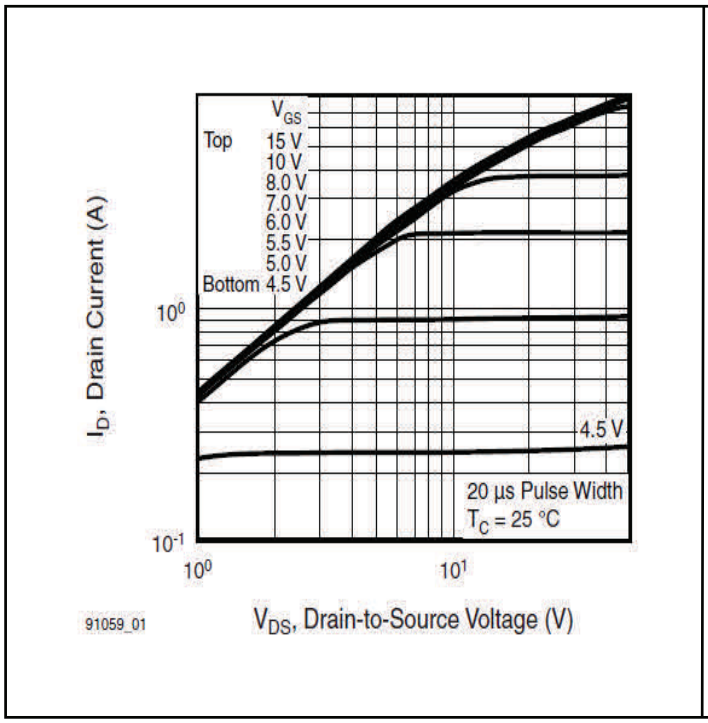


Figure 1 Typical Output Characteristics, T_C = 25°C

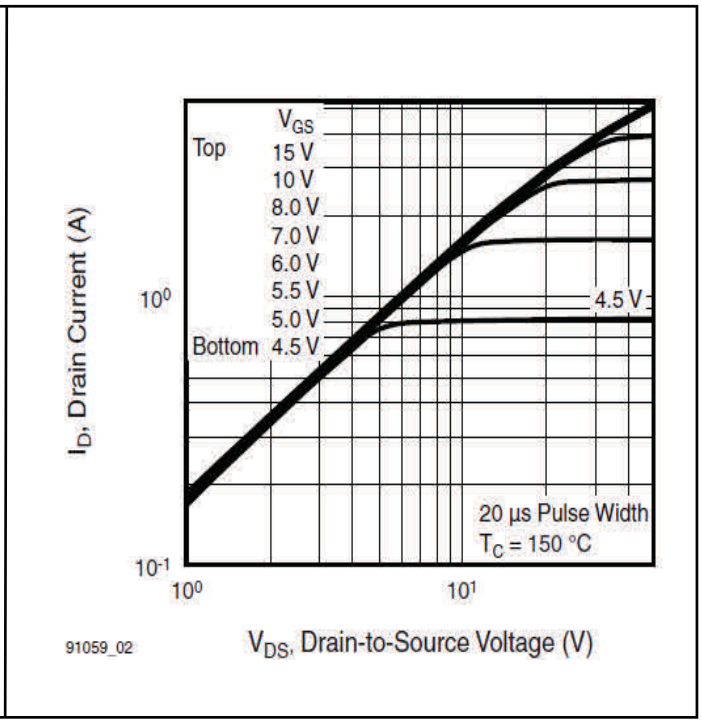


Figure 2 Typical Output Characteristics, T_C = 150°C

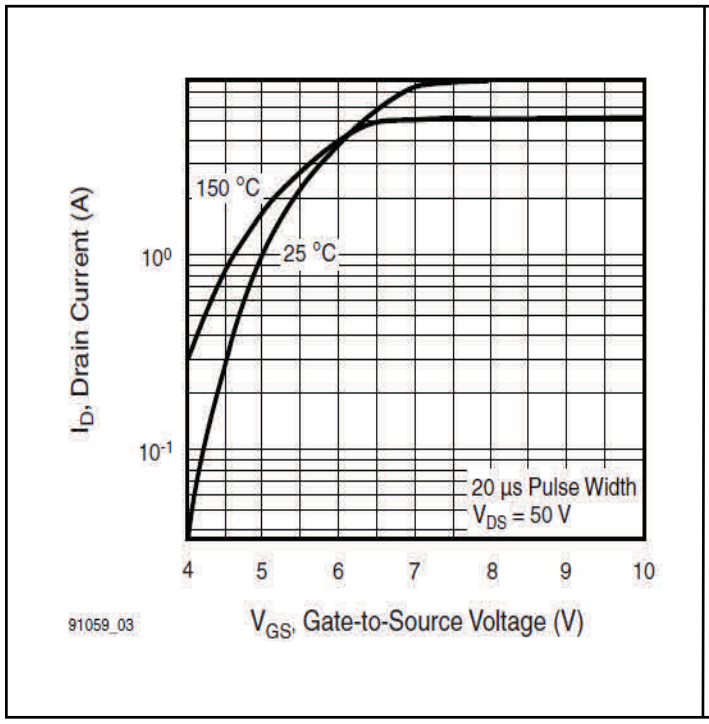


Figure 3 Typical Transfer Characteristics

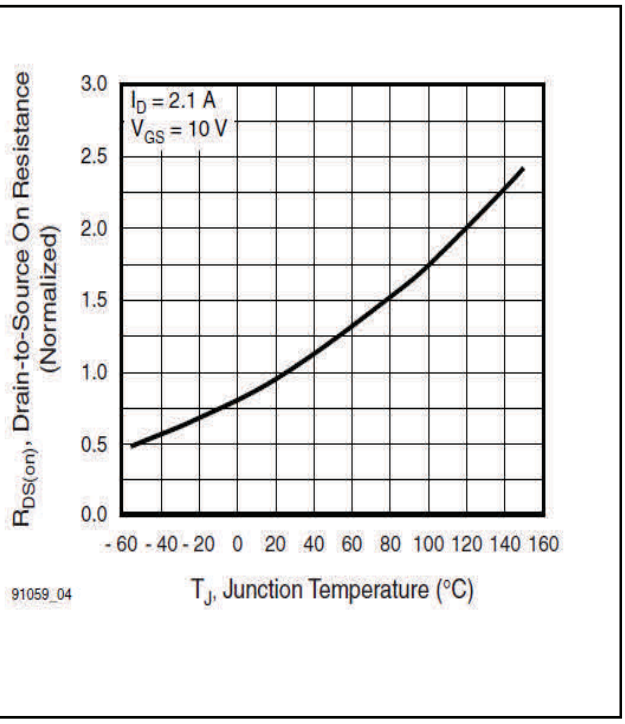


Figure 4 Normalized On-Resistance vs. Temperature

Electrical characteristic diagrams

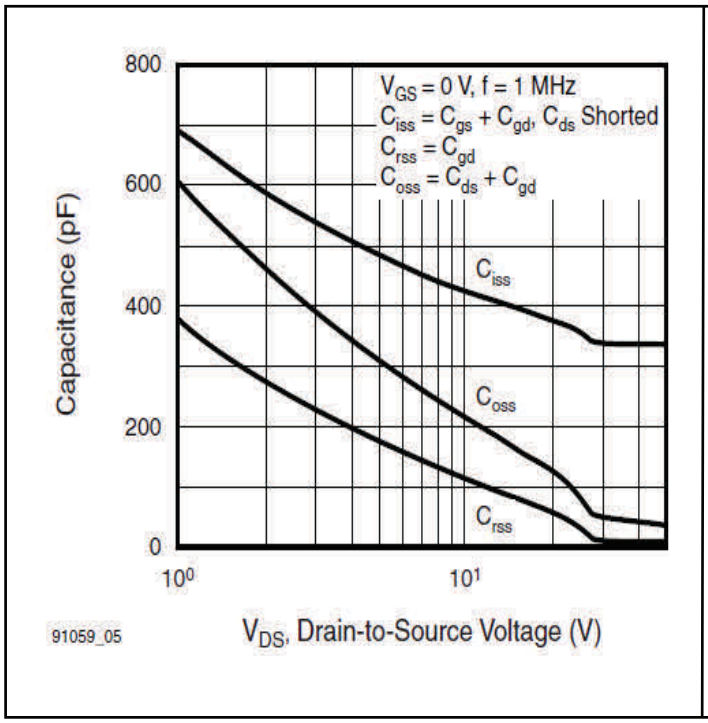


Figure 5 Typical Capacitance vs. Drain-to-Source Voltage

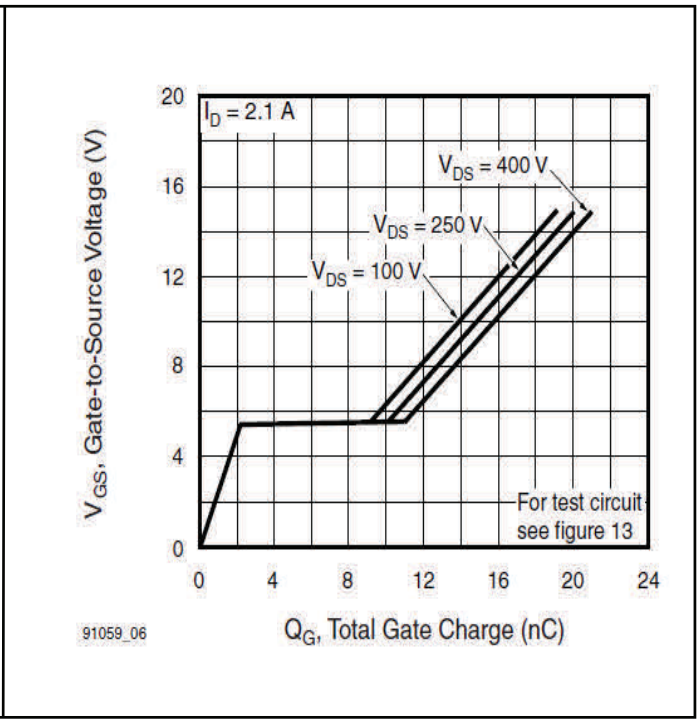


Figure 6 Typical Gate Charge vs. Gate-to-Source Voltage

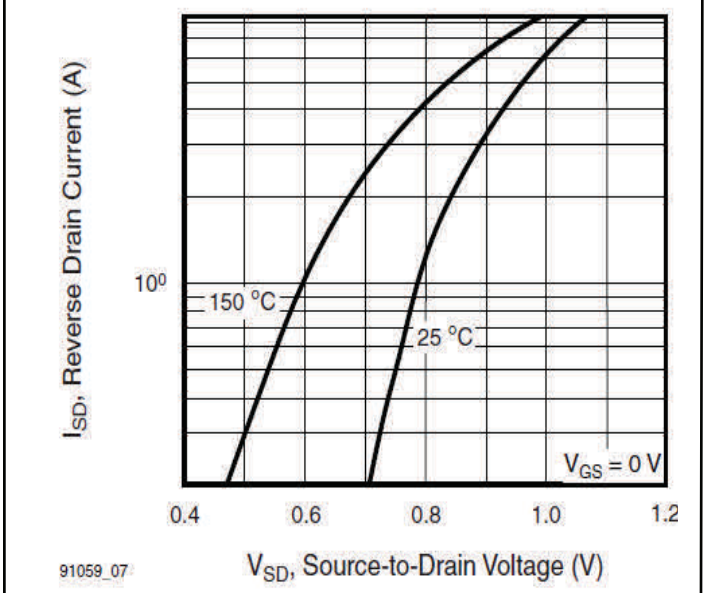


Figure 7 Typical Source-Drain Diode Forward Voltage

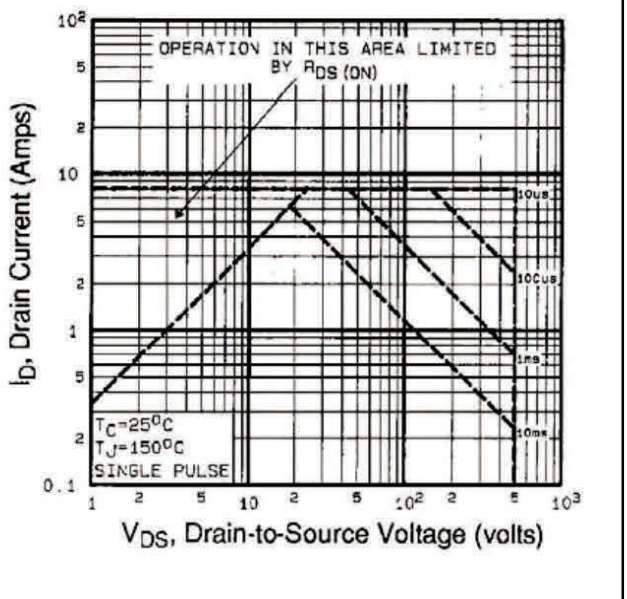


Figure 8 Maximum Safe Operating Area

Electrical characteristic diagrams

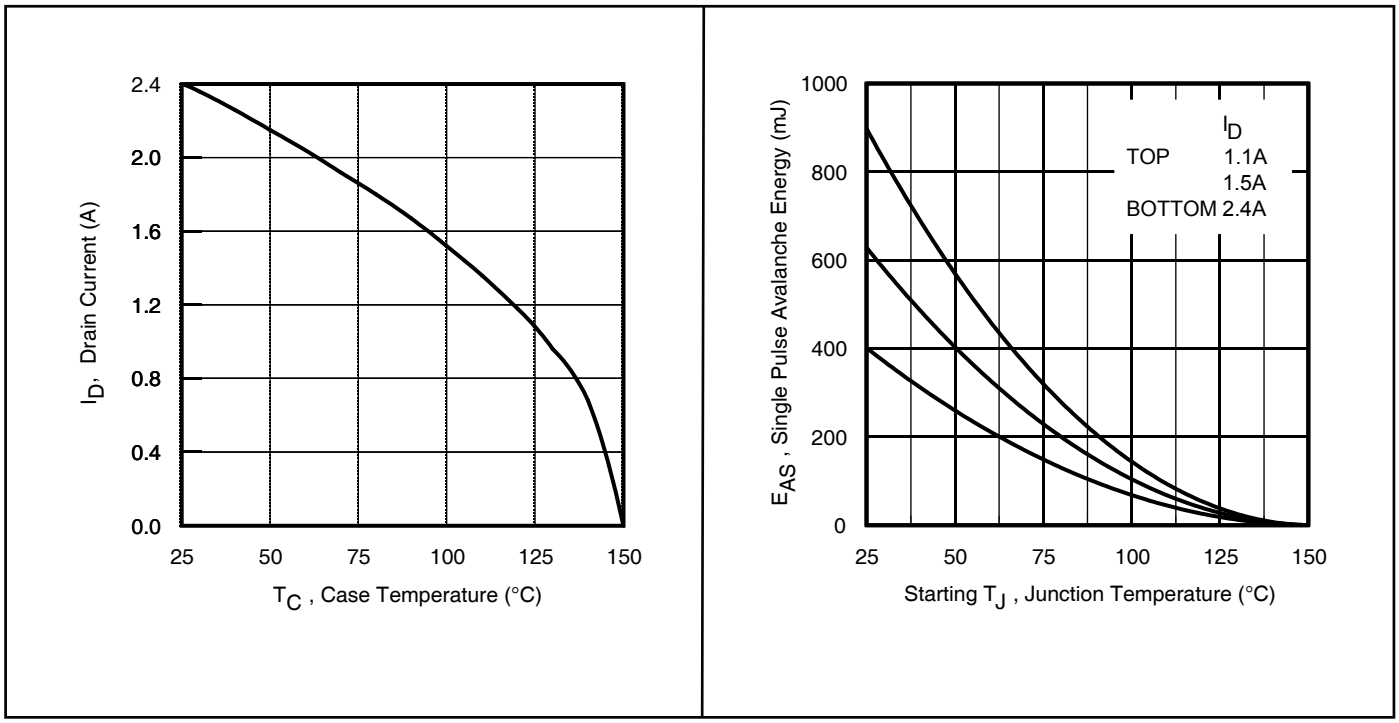


Figure 9 Maximum Drain Current vs. Case Temperature

Figure 10 Maximum Avalanche Energy vs. Temperature

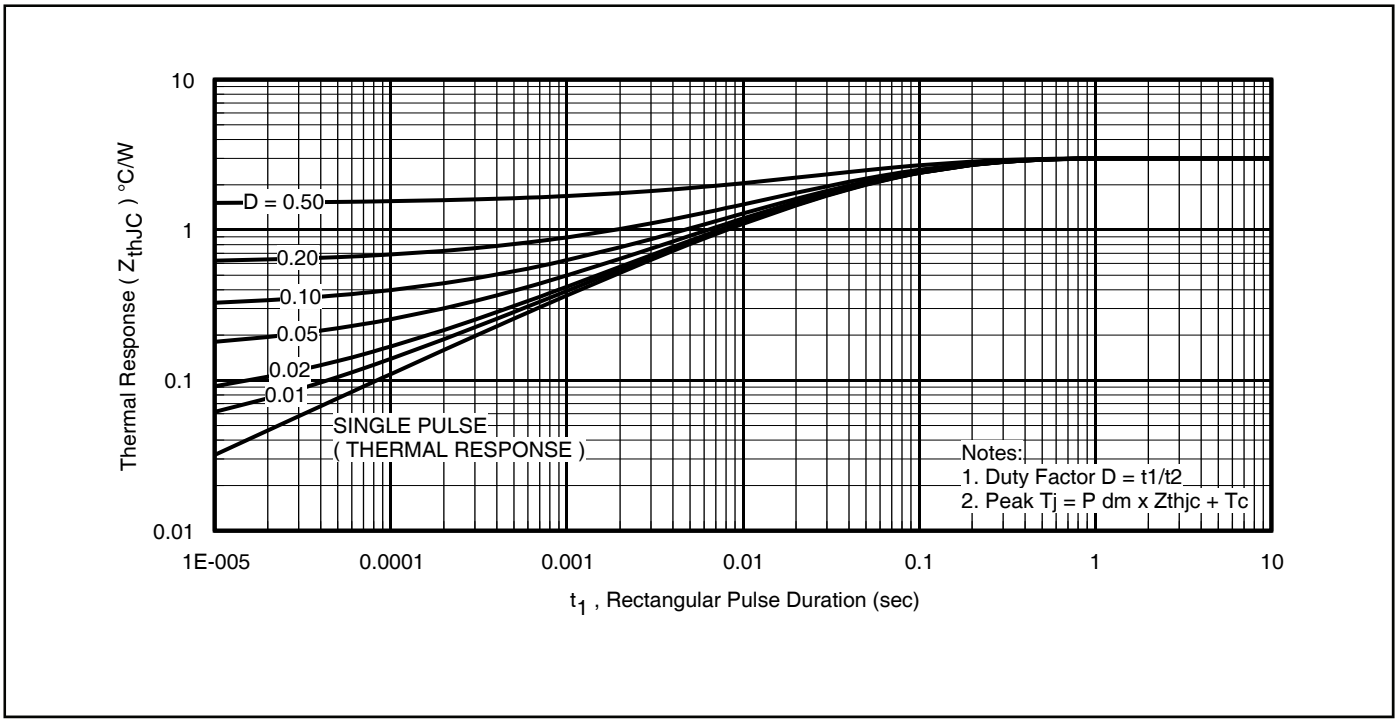


Figure 11 Maximum Effective Transient Thermal Impedance, Junction-to-Case

Electrical characteristic diagrams

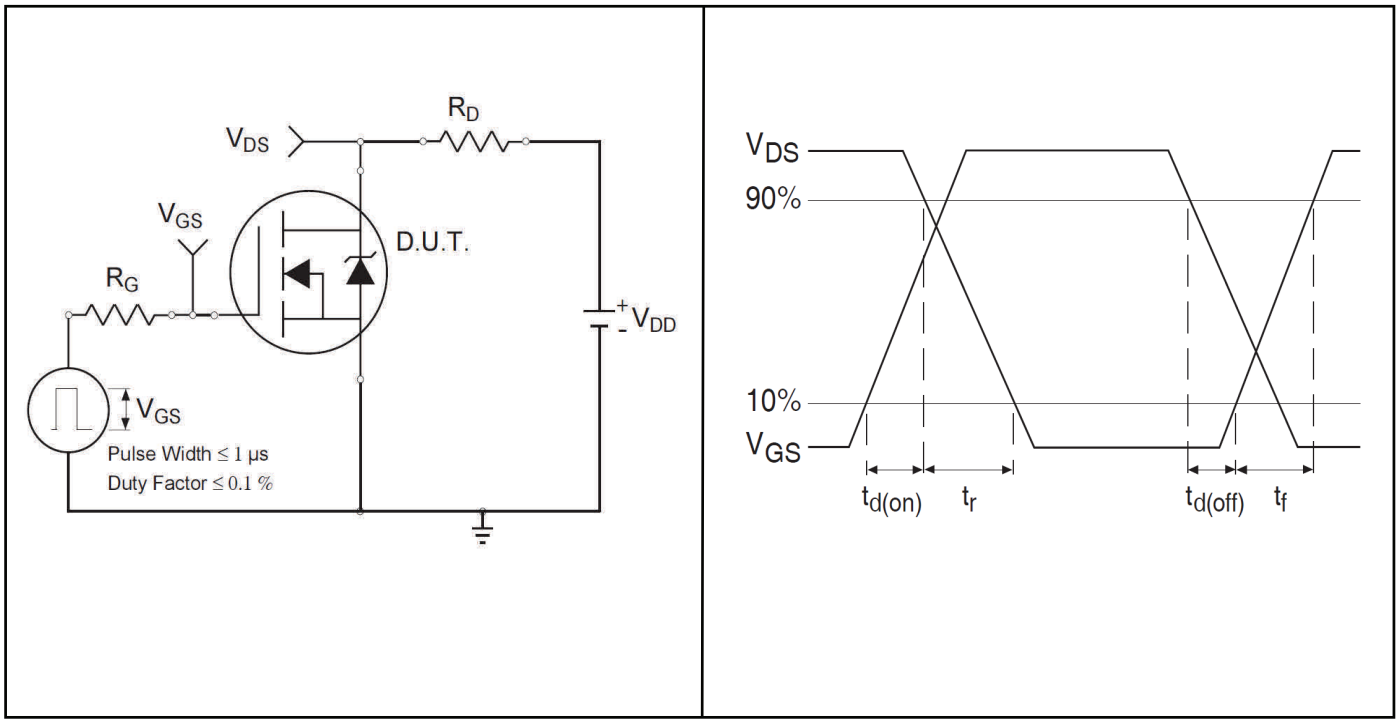


Figure 12a Switching Time Test Circuit

Figure 12b Switching Time Waveforms

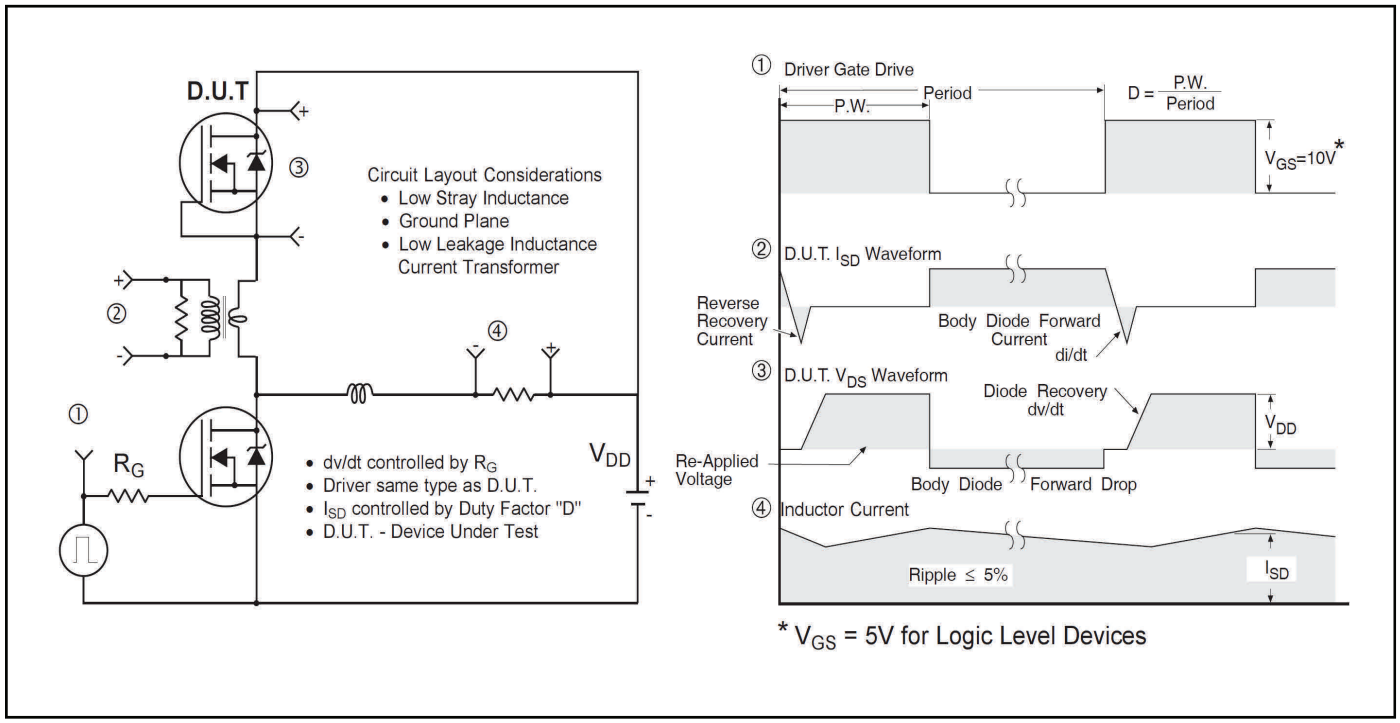


Figure 13 Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET™ Power MOSFETs

Electrical characteristic diagrams

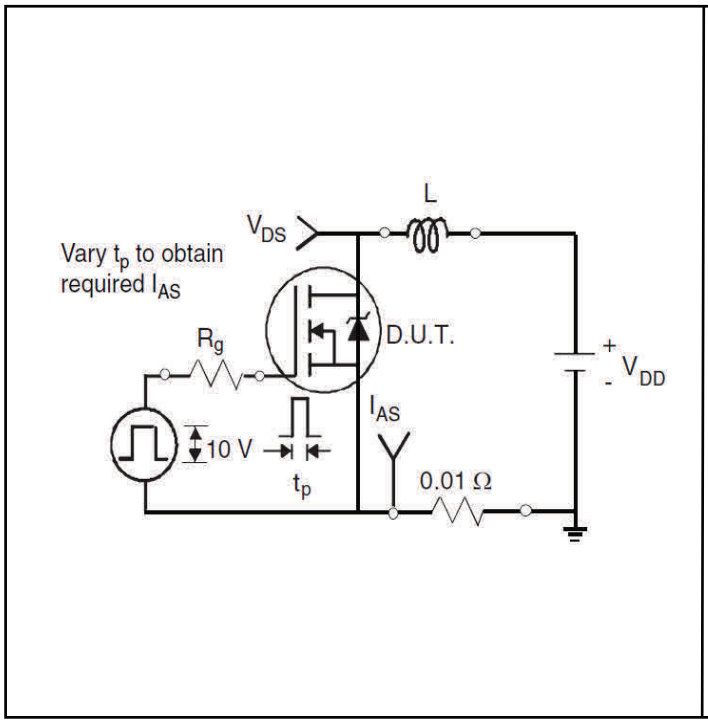


Figure 14a Unclamped Inductive Test Circuit

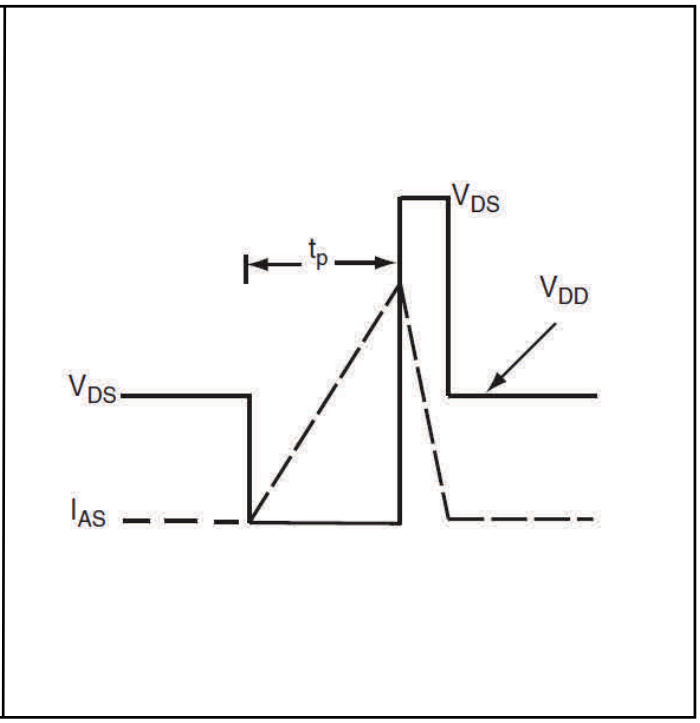


Figure 14b Unclamped Inductive Waveforms

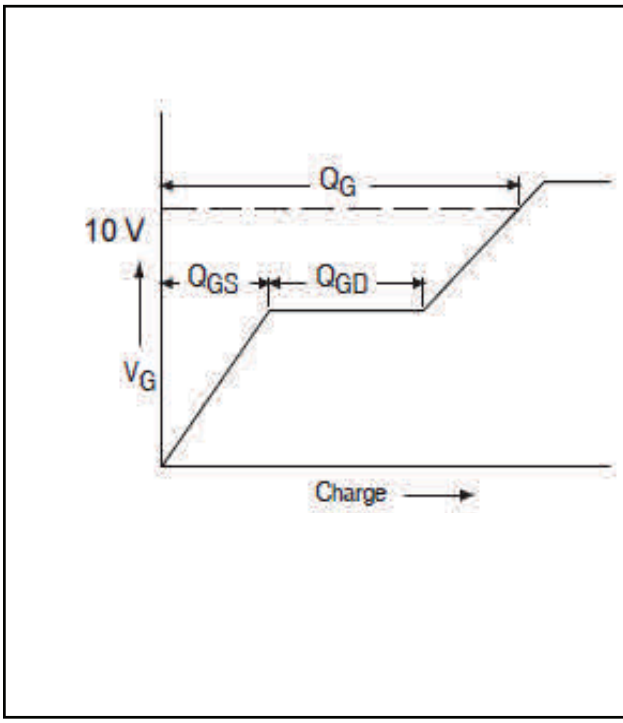


Figure 15a Gate Charge Waveform

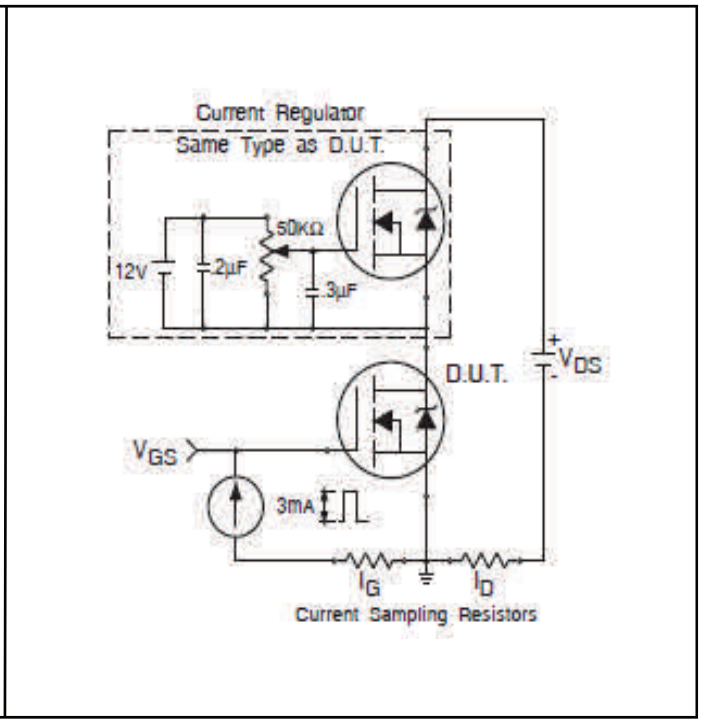
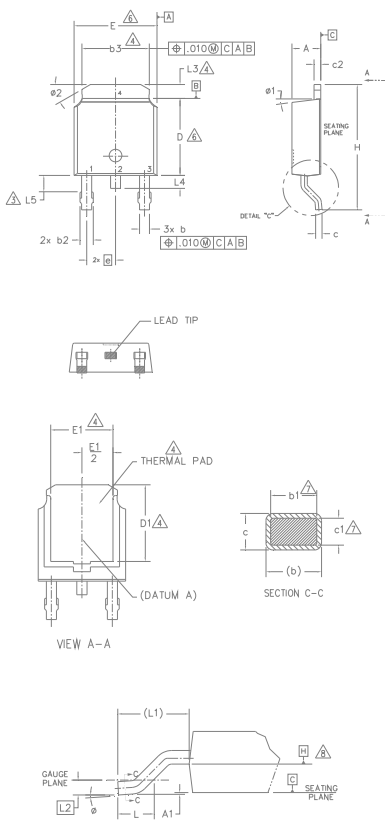


Figure 15b Gate Charge Test Circuit

5 Package Information

D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

3.– LEAD DIMENSION UNCONTROLLED IN L5.

4.– DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.

5.– SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.

6.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .006 [0.15] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

7.– DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.

8.– DATUM A & B TO BE DETERMINED AT DATUM PLANE H.

9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.64	0.89	.025	.035	
b1	0.64	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

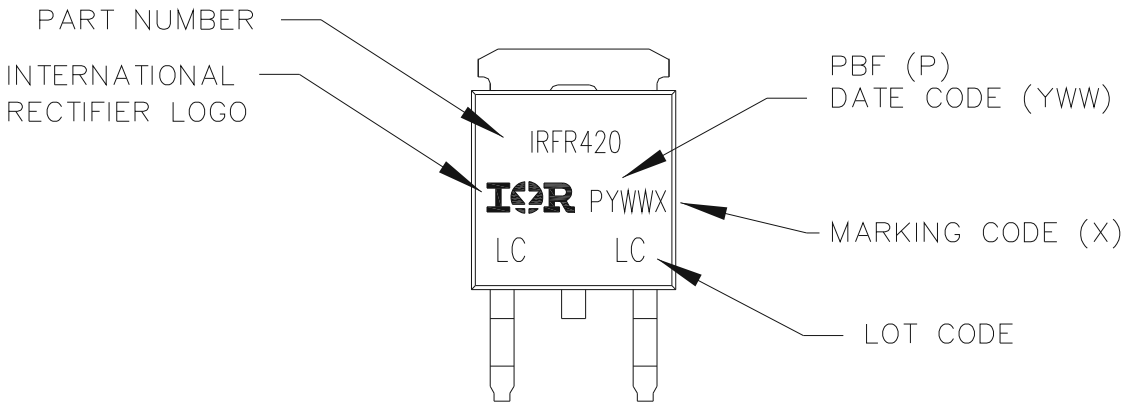
HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

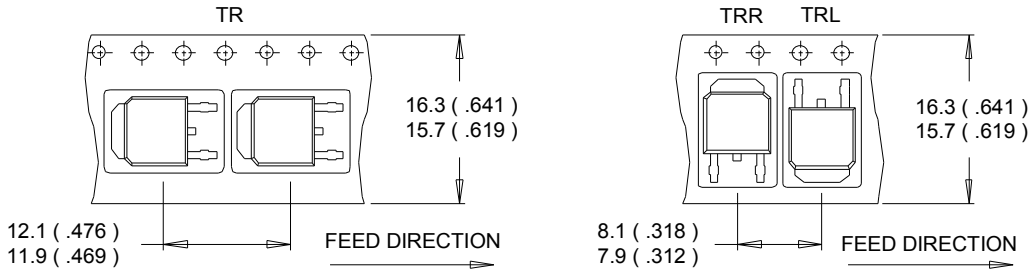
IGBT & CoPAK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

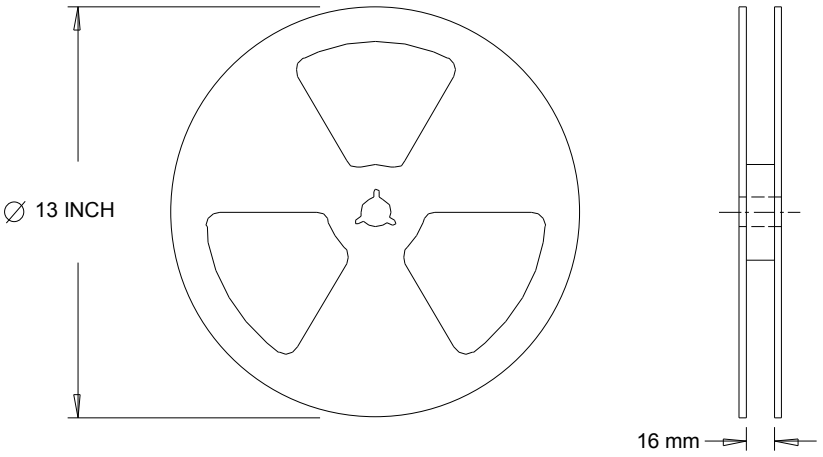
D-Pak (TO-252AA) Part Marking Information



D-Pak (TO-252AA) Tape & Reel Information Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

6 Qualification Information

Qualification Information

Qualification Level	Industrial (per JEDEC JESD47F) †	
Moisture Sensitivity Level	D-Pak	MSL1
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Revision History

Major changes since the last revision

Page or Reference	Revision	Date	Description of changes
All pages	1.0	2017-08-01	• First release data sheet.

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Email: erratum@infineon.com

Document reference

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