

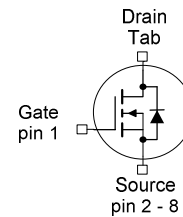
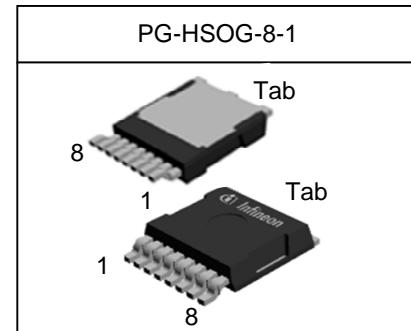
**OptiMOS™-T2 Power-Transistor**

**Features**

- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- Ultra low Rds(on)
- 100% Avalanche tested

**Product Summary**

$V_{DS}$	40	V
$R_{DS(on)}$	0.74	mΩ
$I_D$	300	A



Type	Package	Marking
IAUS300N04S4N007	PG-HSOG-8-1	A04S4N07

**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_C=25\text{ °C}$ , $V_{GS}=10\text{V}^{(1)}$	300	A
		$T_C=100\text{ °C}$ , $V_{GS}=10\text{ V}^{(2)}$	300	
Pulsed drain current <sup>(2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	1200	
Avalanche energy, single pulse <sup>(2)</sup>	$E_{AS}$	$I_D=150\text{ A}$	1100	mJ
Avalanche current, single pulse	$I_{AS}$	-	300	A
Gate source voltage	$V_{GS}$	-	±20	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	375	W
Operating and storage temperature	$T_j, T_{stg}$	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics<sup>2)</sup>**

Thermal resistance, junction - case	$R_{thJC}$	-	-	-	0.4	K/W
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>3)</sup>	-	-	40	

**Electrical characteristics, at  $T_j=25$  °C, unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0$ V, $I_D=1$ mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=275$ $\mu$ A	2.0	3.0	4.0	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=40$ V, $V_{GS}=0$ V, $T_j=25$ °C	-	0.1	10	$\mu$ A
		$V_{DS}=18$ V, $V_{GS}=0$ V, $T_j=85$ °C <sup>2)</sup>	-	1	20	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20$ V, $V_{DS}=0$ V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10$ V, $I_D=100$ A	-	0.50	0.74	m $\Omega$

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	21043	27356	pF
Output capacitance	$C_{oss}$		-	4485	5831	
Reverse transfer capacitance	$C_{rss}$		-	160	368	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V},$ $I_D=300\text{ A}, R_G=3.5\ \Omega$	-	56	-	ns
Rise time	$t_r$		-	18	-	
Turn-off delay time	$t_{d(off)}$		-	90	-	
Fall time	$t_f$		-	49	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=32\text{ V}, I_D=300\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	113	160	nC
Gate to drain charge	$Q_{gd}$		-	36	90	
Gate charge total	$Q_g$		-	263	342	
Gate plateau voltage	$V_{plateau}$		-	5.4	-	V
Output charge	$Q_{oss}$	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	48	64	

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	300	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$		-	-	1200	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=100\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.9	1.3	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=20\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	90	-	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$		-	147	-	nC

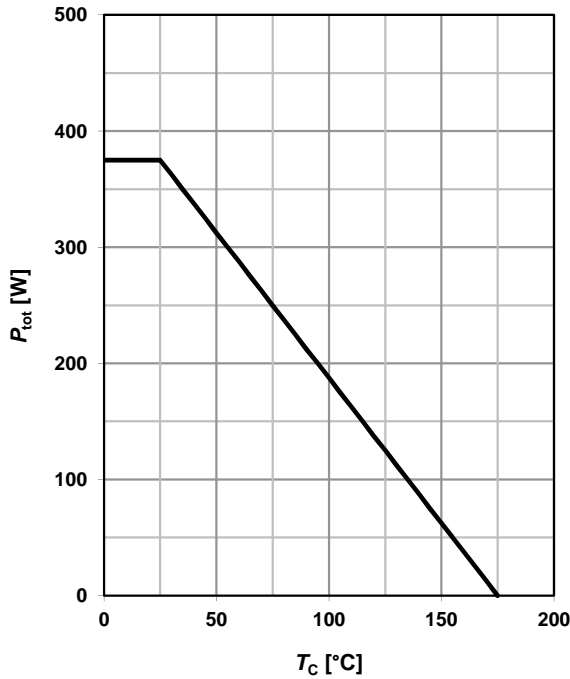
<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC} = 0.4\text{ K/W}$  the chip is able to carry 553A at 25°C.

<sup>2)</sup> Defined by design. Not subject to production test.

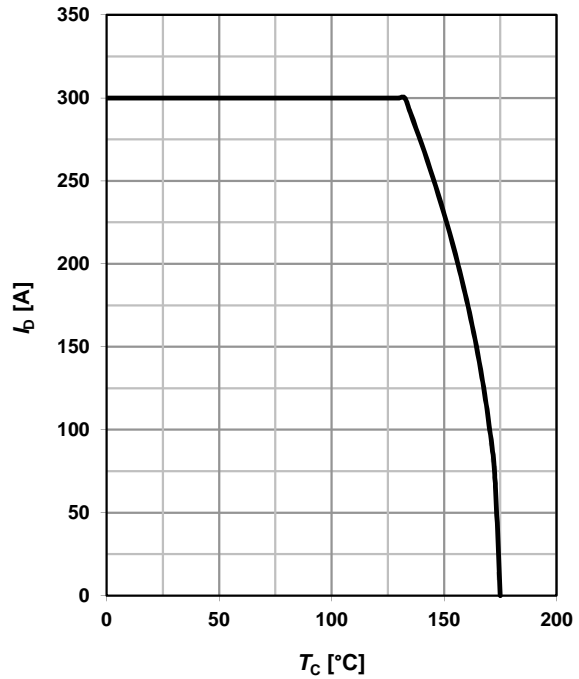
<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

**1 Power dissipation**

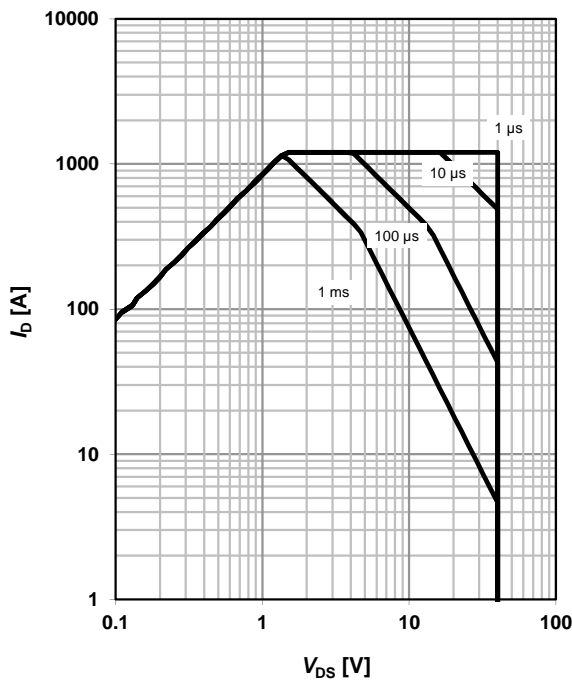
$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$


**2 Drain current**

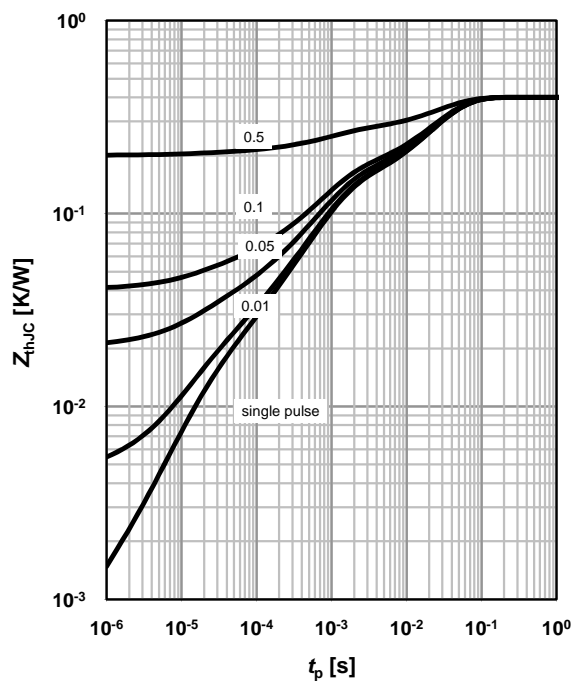
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$


**3 Safe operating area**

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

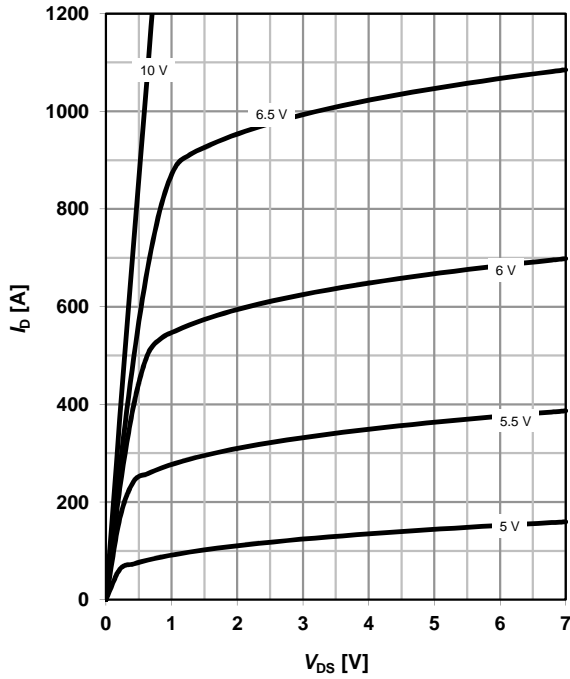
 parameter:  $t_p$ 

**4 Max. transient thermal impedance**

$$Z_{\text{thJC}} = f(t_p)$$

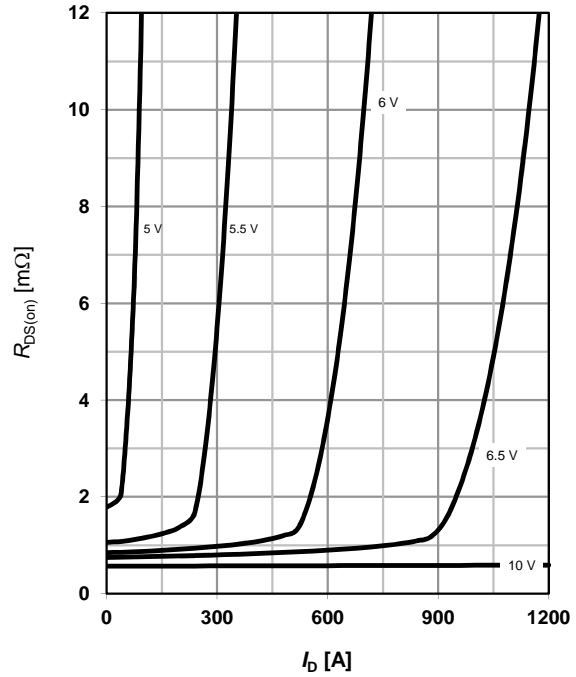
 parameter:  $D = t_p/T$ 


**5 Typ. output characteristics**

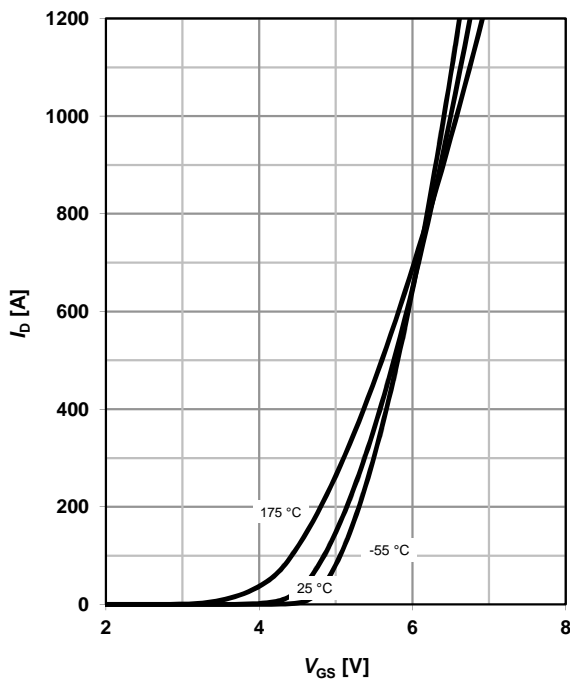
$$I_D = f(V_{DS}); T_j = 25\text{ °C}$$

 parameter:  $V_{GS}$ 

**6 Typ. drain-source on-state resistance**

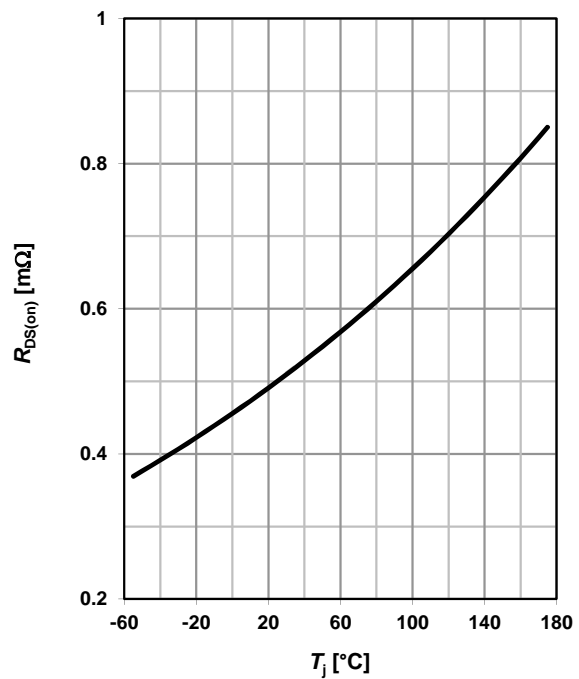
$$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$$

 parameter:  $V_{GS}$ 

**7 Typ. transfer characteristics**

$$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$$

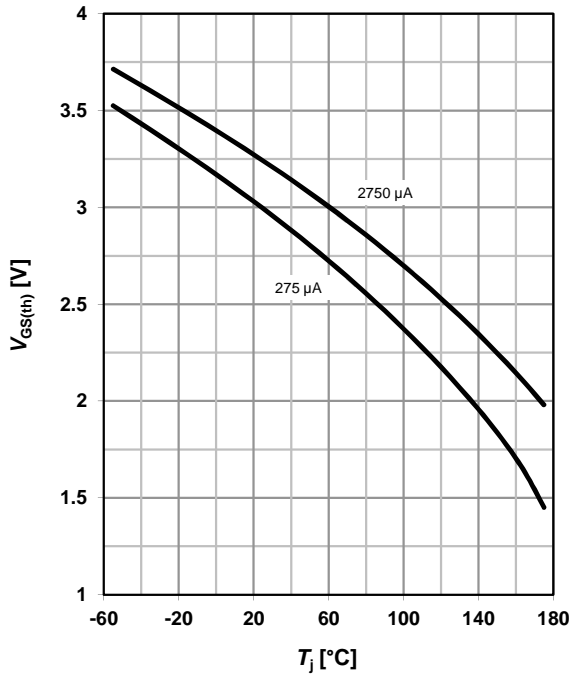
 parameter:  $T_j$ 

**8 Typ. drain-source on-state resistance**

$$R_{DS(on)} = f(T_j); I_D = 100\text{ A}; V_{GS} = 10\text{ V}$$

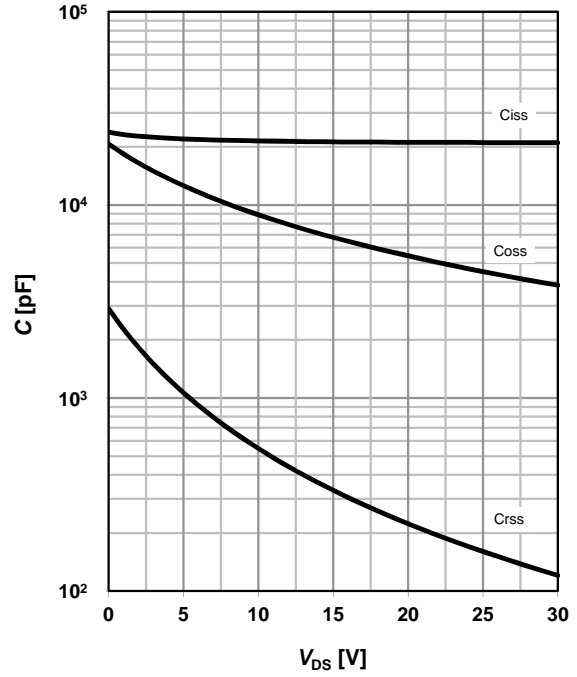


**9 Typ. gate threshold voltage**

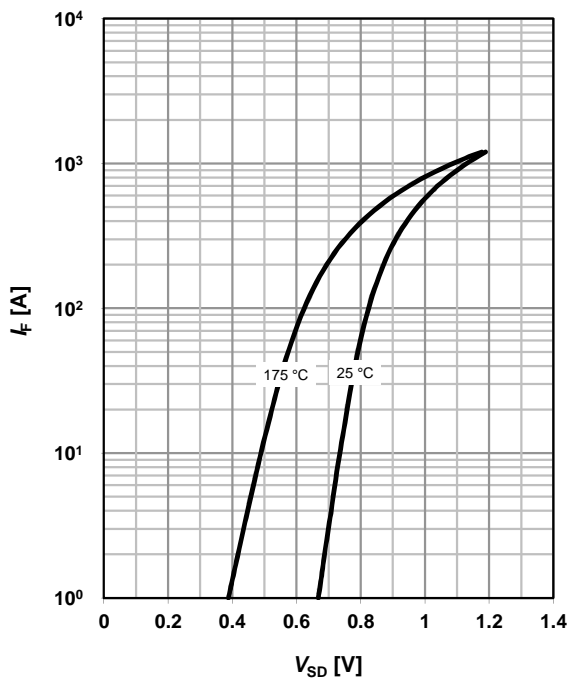
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

 parameter:  $I_D$ 

**10 Typ. capacitances**

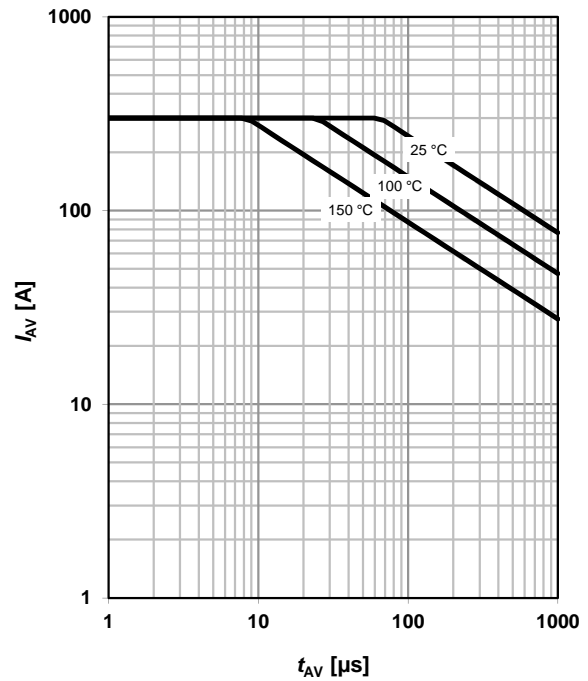
$$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$$


**11 Typical forward diode characteristics**

$$I_F = f(V_{SD})$$

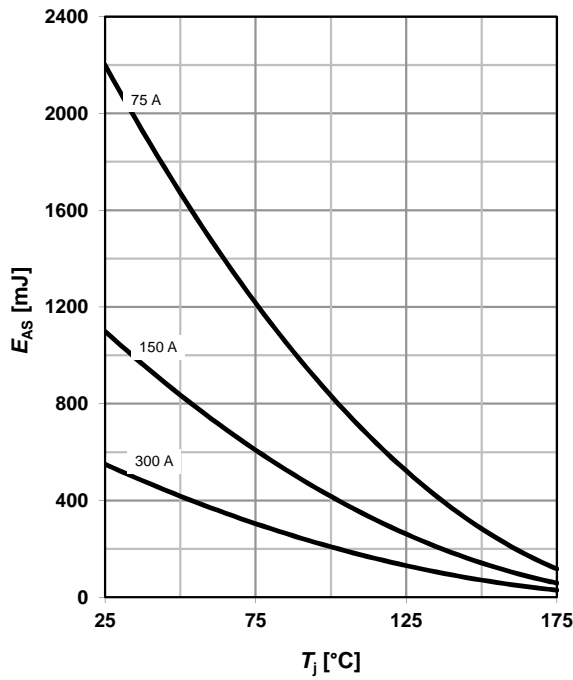
 parameter:  $T_j$ 

**12 Typ. avalanche characteristics**

$$I_{AS} = f(t_{AV})$$

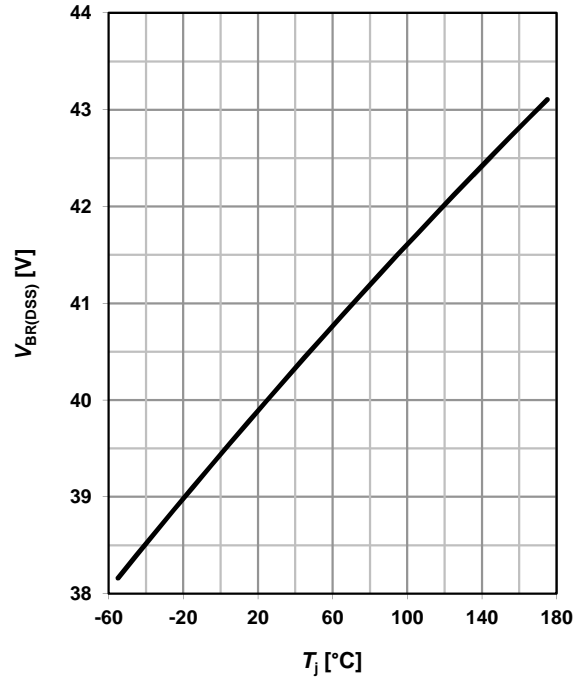
 parameter:  $T_{j(start)}$ 


**13 Typical avalanche energy**

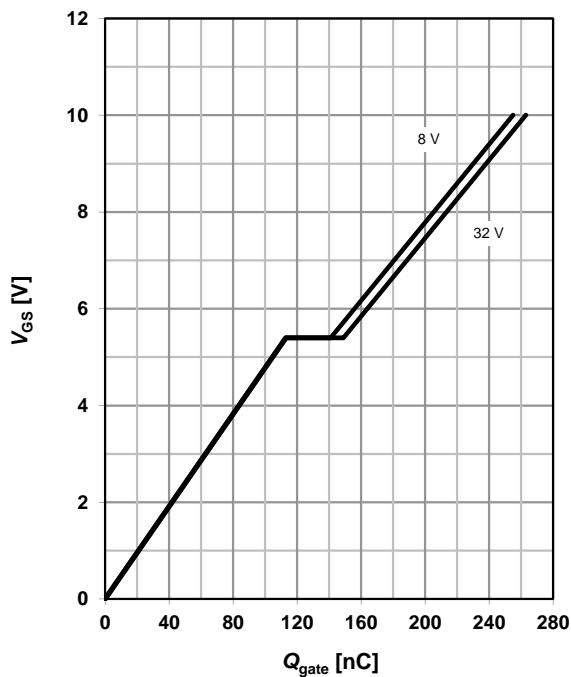
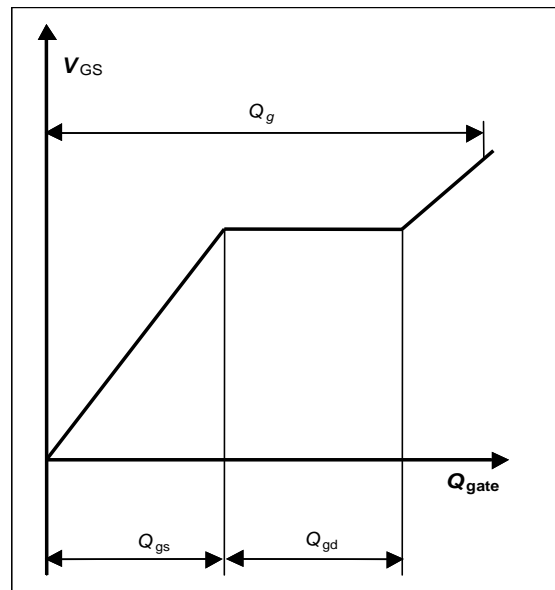
$$E_{AS} = f(T_j)$$

 parameter:  $I_D$ 

**14 Drain-source breakdown voltage**

$$V_{BR(DSS)} = f(T_j); I_{D\_typ} = 1 \text{ mA}$$


**15 Typ. gate charge**

$$V_{GS} = f(Q_{gate}); I_D = 300 \text{ A pulsed}$$

 parameter:  $V_{DD}$ 

**16 Gate charge waveforms**


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Revision History

Version	Date	Changes
Version 1.0	4/10/2017	Final Datasheet