

# HITFET - BTS3125TF

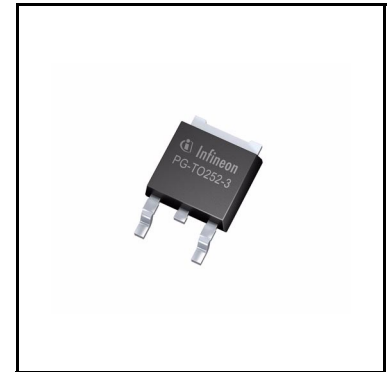
## Smart Low-Side Power Switch



### 1 Overview

#### Basic Features

- Single channel device
- Very low output leakage current in OFF state
- Electrostatic discharge protection (ESD)
- Embedded protection functions (see below)
- Green Product (RoHS compliant)
- AEC Qualified



#### Applications

- Suitable for resistive, inductive and capacitive loads
- Replaces electromechanical relays, fuses and discrete circuits

#### Description

The BTS3125TF is a 125 mΩ single channel Smart Low-Side Power Switch within a PG-TO252-3 package providing embedded protective functions. The power transistor is built by an N-channel vertical power MOSFET.

The device is monolithically integrated. The BTS3125TF is automotive qualified and is optimized for 12 V automotive applications.

| Type      | Package    | Marking |
|-----------|------------|---------|
| BTS3125TF | PG-TO252-3 | S3125TF |

**Table 1 Product Summary**

|  |                 |           |
|--|-----------------|-----------|
| Operating voltage range  | $V_{OUT}$       | 0 .. 31 V |
| Maximum load voltage   | $V_{BAT(LD)}$   | 40 V      |
| Maximum input voltage  | $V_{IN}$        | 5.5 V     |
| Maximum On-State resistance at $T_J = 150^{\circ}\text{C}$ , $V_{IN} = 5\text{ V}$ | $R_{DS(ON)}$    | 250 mΩ    |
| Nominal load current   | $I_{L(NOM)}$    | 2 A       |
| Minimum current limitation   | $I_{L(LIM)}$    | 7 A       |
| Maximum OFF state load current at $T_J \leq 85^{\circ}\text{C}$                    | $I_{L(OFF)_85}$ | 0.6 μA    |

## Overview

### Protection Functions

- Over temperature shut-down with automatic-restart
- Active clamp over voltage protection
- Current limitation

### Detailed Description

The device is able to switch all kind of resistive, inductive and capacitive loads, limited by maximum clamping energy and maximum current capabilities.

The BTS3125TF offers ESD protection on the IN pin which refers to the Source pin (Ground).

The over temperature protection prevents the device from overheating due to overload and/or bad cooling conditions. The temperature information is given by a temperature sensor in the power MOSFET.

The BTS3125TF has an auto-restart thermal shut-down function. The device will turn on again, if input is still high, after the measured temperature has dropped below the thermal hysteresis.

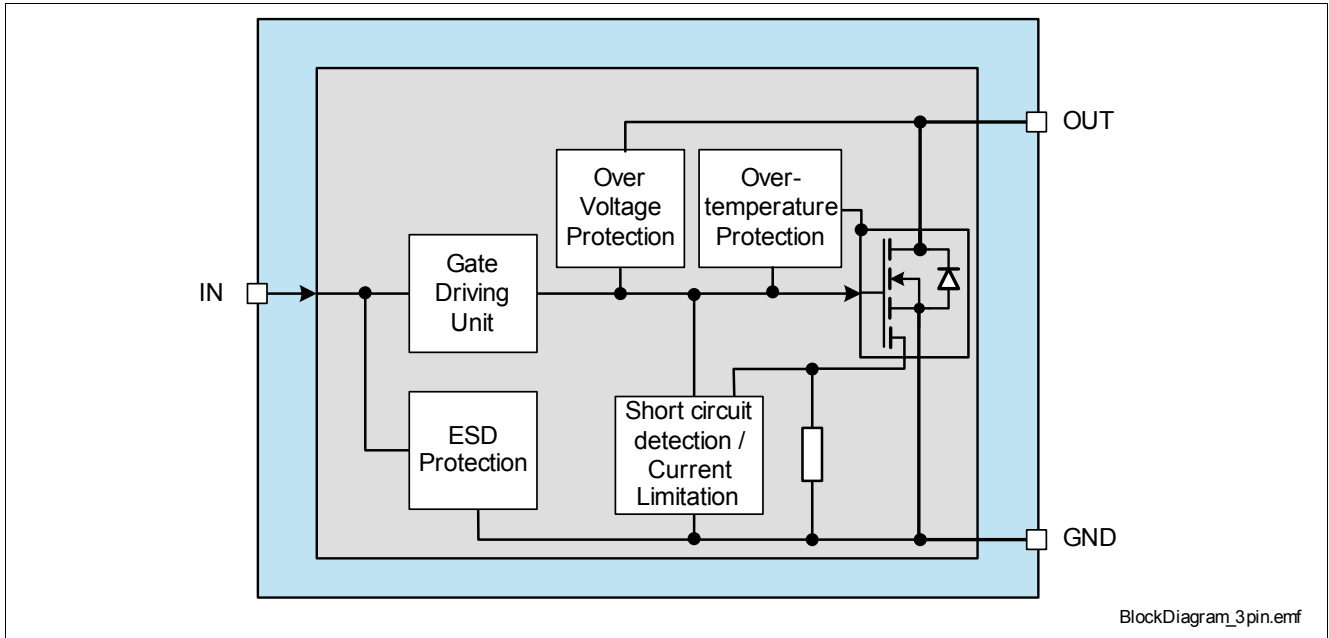
The over voltage protection can be activated during load dump or inductive turn off conditions. The power MOSFET is limiting the drain-source voltage, if it rises above the  $V_{OUT(CLAMP)}$ .

## Table of Contents

|           |   |           |
|-----------|---|-----------|
| <b>1</b>  | <b>Overview</b> .....                               | <b>1</b>  |
|           | <b>Table of Contents</b> .....                      | <b>3</b>  |
| <b>2</b>  | <b>Block Diagram</b> .....                          | <b>4</b>  |
| <b>3</b>  | <b>Pin Configuration</b> .....                      | <b>5</b>  |
| 3.1       | Pin Assignment BTS3125TF .....                      | 5         |
| 3.2       | Pin Definitions and Functions .....                 | 5         |
| 3.3       | Voltage and current definition .....                | 5         |
| <b>4</b>  | <b>General Product Characteristics</b> .....        | <b>6</b>  |
| 4.1       | Absolute Maximum Ratings .....                      | 6         |
| 4.2       | Functional Range .....                              | 7         |
| 4.3       | Thermal Resistance .....                            | 8         |
| 4.3.1     | PCB set up .....                                    | 8         |
| 4.3.2     | Transient Thermal Impedance .....                   | 9         |
| <b>5</b>  | <b>Power Stage</b> .....                            | <b>11</b> |
| 5.1       | Output On-state Resistance .....                    | 11        |
| 5.2       | Resistive Load Output Timing .....                  | 11        |
| 5.3       | Inductive Load .....                                | 12        |
| 5.3.1     | Output Clamping .....                               | 12        |
| 5.3.1.1   | Maximum Load Inductance .....                       | 13        |
| 5.4       | Reverse Current capability .....                    | 13        |
| 5.5       | Inverse Current capability .....                    | 14        |
| 5.6       | Characteristics .....                               | 14        |
| <b>6</b>  | <b>Protection Functions</b> .....                   | <b>15</b> |
| 6.1       | Over Voltage Clamping on OUTput .....               | 15        |
| 6.2       | Thermal Protection .....                            | 15        |
| 6.3       | Short Circuit Protection / Current limitation ..... | 15        |
| 6.4       | Characteristics .....                               | 16        |
| <b>7</b>  | <b>Input Stage</b> .....                            | <b>17</b> |
| 7.1       | Input Circuit .....                                 | 17        |
| 7.2       | Characteristics .....                               | 17        |
| <b>8</b>  | <b>Electrical Characteristics</b> .....             | <b>18</b> |
| 8.1       | Power Stage .....                                   | 18        |
| 8.2       | Protection .....                                    | 19        |
| 8.3       | Input Stage .....                                   | 21        |
| <b>9</b>  | <b>Characterization Results</b> .....               | <b>22</b> |
| 9.1       | Power Stage .....                                   | 22        |
| 9.2       | Protection .....                                    | 33        |
| 9.3       | Input Stage .....                                   | 34        |
| <b>10</b> | <b>Application Information</b> .....                | <b>36</b> |
| 10.1      | Application Diagram .....                           | 36        |
| <b>11</b> | <b>Package Outlines</b> .....                       | <b>37</b> |
| <b>12</b> | <b>Revision History</b> .....                       | <b>38</b> |

**Block Diagram**

**2 Block Diagram**

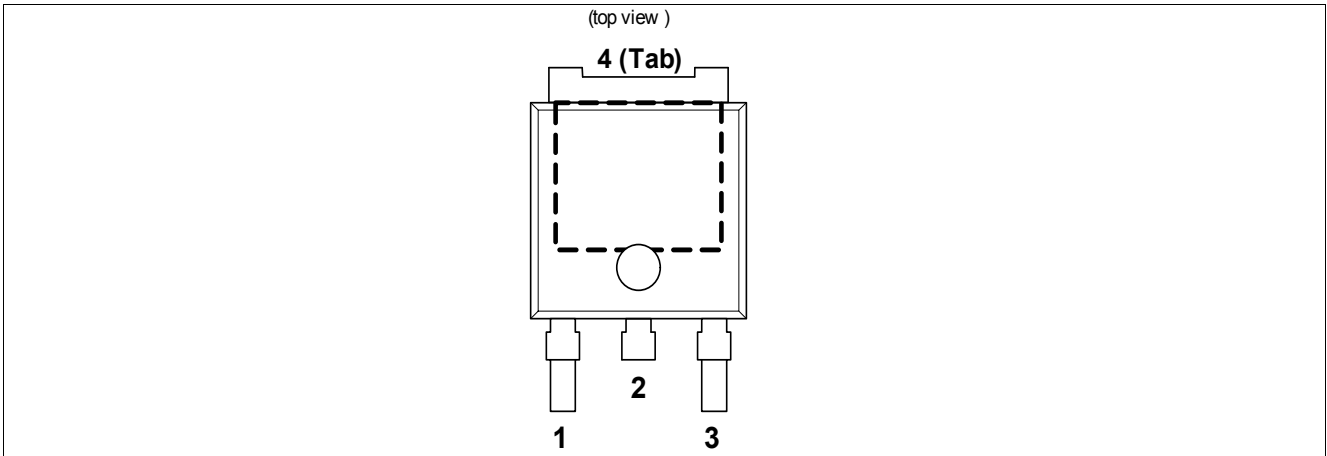


**Figure 1 Block Diagram**

**Pin Configuration**

**3 Pin Configuration**

**3.1 Pin Assignment BTS3125TF**



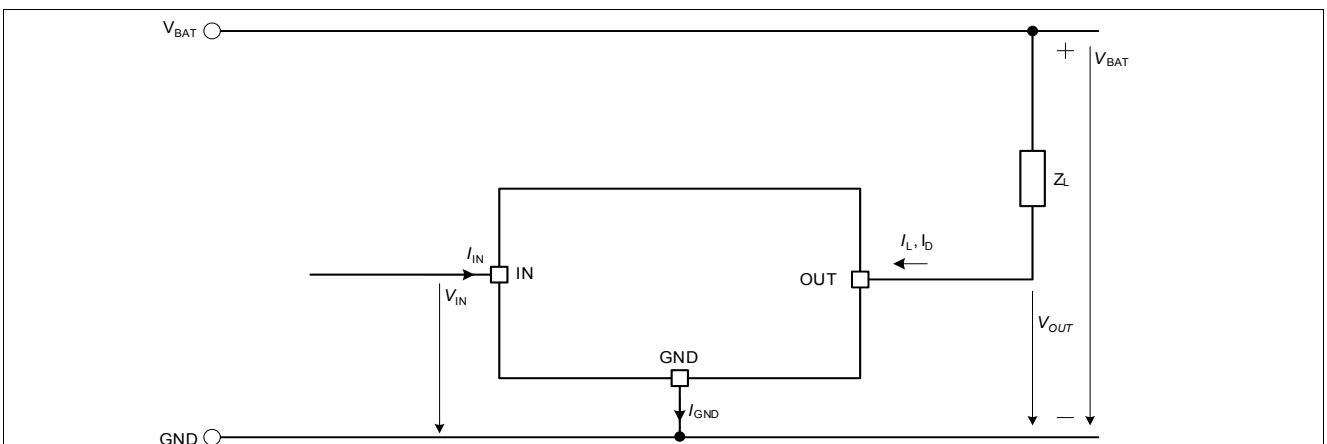
**Figure 2 Pin Configuration. PG-T0252-3**

**3.2 Pin Definitions and Functions**

| Pin | Symbol | Function                              |
|-----|--------|---------------------------------------|
| 1   | IN     | Input pin                             |
| 2,4 | OUT    | Drain, Load connection for power DMOS |
| 3   | GND    | Ground, Source of power DMOS          |

**3.3 Voltage and current definition**

**Figure 3** shows all external terms used in this data sheet, with associated convention for positive values.



**Figure 3 Naming definition of electrical parameters**

**General Product Characteristics**

**4 General Product Characteristics**

**4.1 Absolute Maximum Ratings**

**Table 2 Absolute Maximum Ratings<sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter   | Symbol                | Values |      |                     | Unit | Note or Test Condition  | Number   |
|---|-----------------------|--------|------|---------------------|------|---|----------|
|   |                       | Min.   | Typ. | Max.                |      |   |          |
| <b>Voltages</b>   |                       |        |      |                     |      |   |          |
| Output voltage  | $V_{\text{OUT}}$      | -      | -    | 40                  | V    | internally clamped  | P_4.1.1  |
| Battery voltage for short circuit protection                  | $V_{\text{BAT(SC)}}$  | -      | -    | 31                  | V    | $l = 0$ or $5$ m<br>$R_{\text{SC}} = 20 \text{ m}\Omega + R_{\text{Cable}}$<br>$R_{\text{Cable}} = l * 16 \text{ m}\Omega/\text{m}$<br>$L_{\text{SC}} = 5 \text{ }\mu\text{H} + L_{\text{Cable}}$<br>$L_{\text{Cable}} = l * 1 \text{ }\mu\text{H}/\text{m}$<br>$V_{\text{IN}} = 5 \text{ V}$ | P_4.1.2  |
| Battery voltage for load dump protection                      | $V_{\text{BAT(LD)}}$  | -      | -    | 40                  | V    | <sup>2)</sup><br>$R_1 = 2 \text{ }\Omega$<br>$R_L = 4.5 \text{ }\Omega$<br>$t_D = 400 \text{ ms}$<br>suppressed pulse   | P_4.1.4  |
| <b>Input Pin</b>  |                       |        |      |                     |      |   |          |
| Input Voltage   | $V_{\text{IN}}$       | -0.3   | -    | 5.5                 | V    | -   | P_4.1.7  |
| Input current in inverse condition on OUT to GND              | $I_{\text{IN}}$       | -      | -    | 2                   | mA   | <sup>3)</sup><br>$V_{\text{OUT}} < -0.3 \text{ V}$  | P_4.1.10 |
| <b>Power Stage</b>  |                       |        |      |                     |      |   |          |
| Load current  | $ I_L $               | -      | -    | $I_{\text{L(LIM)}}$ | A    | -   | P_4.1.11 |
| <b>Energies</b>   |                       |        |      |                     |      |   |          |
| Unclamped single inductive energy single pulse                | $E_{\text{AS}}$       | -      | -    | 24                  | mJ   | $I_{\text{L(0)}} = I_{\text{L(NOM)}}$<br>$V_{\text{BAT}} = 13.5 \text{ V}$<br>$T_{\text{J(0)}} = 150^\circ\text{C}$   | P_4.1.16 |
| Unclamped repetitive inductive energy pulse with 10 k cycles  | $E_{\text{AR(10k)}}$  | -      | -    | 24                  | mJ   | $I_{\text{L(0)}} = I_{\text{L(NOM)}}$<br>$V_{\text{BAT}} = 13.5 \text{ V}$<br>$T_{\text{J(0)}} = 105^\circ\text{C}$   | P_4.1.24 |
| Unclamped repetitive inductive energy pulse with 100 k cycles | $E_{\text{AR(100k)}}$ | -      | -    | 19                  | mJ   | $I_{\text{L(0)}} = I_{\text{L(NOM)}}$<br>$V_{\text{BAT}} = 13.5 \text{ V}$<br>$T_{\text{J(0)}} = 105^\circ\text{C}$   | P_4.1.28 |
| Unclamped repetitive inductive energy pulse with 1 M cycles   | $E_{\text{AR(1M)}}$   | -      | -    | 15                  | mJ   | $I_{\text{L(0)}} = I_{\text{L(NOM)}}$<br>$V_{\text{BAT}} = 13.5 \text{ V}$<br>$T_{\text{J(0)}} = 105^\circ\text{C}$   | P_4.1.32 |

**General Product Characteristics**

**Table 2 Absolute Maximum Ratings**<sup>1)</sup> (cont'd)

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                         | Symbol           | Values |      |      | Unit               | Note or Test Condition | Number   |
|-----------------------------------|------------------|--------|------|------|--------------------|------------------------|----------|
|                                   |                  | Min.   | Typ. | Max. |                    |                        |          |
| <b>Temperatures</b>               |                  |        |      |      |                    |                        |          |
| Operating temperature             | $T_J$            | -40    | –    | +150 | $^{\circ}\text{C}$ | –                      | P_4.1.37 |
| Storage temperature               | $T_{\text{STG}}$ | -55    | –    | +150 | $^{\circ}\text{C}$ | –                      | P_4.1.38 |
| <b>ESD Susceptibility</b>         |                  |        |      |      |                    |                        |          |
| ESD susceptibility (all pins)     | $V_{\text{ESD}}$ | -4     | –    | 4    | kV                 | HBM <sup>4)</sup>      | P_4.1.39 |
| ESD susceptibility OUT-pin to GND | $V_{\text{ESD}}$ | -10    | –    | 10   | kV                 | HBM <sup>4)</sup>      | P_4.1.40 |
| ESD susceptibility                | $V_{\text{ESD}}$ | -2     | –    | 2    | kV                 | CDM <sup>5)</sup>      | P_4.1.41 |

- 1) Not subject to production test, specified by design.
- 2)  $V_{\text{BAT(LD)}}$  is setup without the DUT connected to the generator per ISO 7637-1;  
 $R_i$  is the internal resistance of the load dump test pulse generator;  
 $t_p$  is the pulse duration time for load dump pulse (pulse 5) according ISO 7637-1, -2.
- 3) Maximum allowed value. Consider also inverse input current in inverse condition P\_8.3.7 in Chapter 8
- 4) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
- 5) ESD susceptibility, Charged Device Model “CDM” ESDA STM5.3.1 or ANSI/ESD S.5.3.1

**Notes**

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**4.2 Functional Range**

**Table 3 Functional Range**<sup>1)</sup>

Please refer to “**Electrical Characteristics**” on **Page 18** for test conditions

| Parameter                                    | Symbol                | Values |      |      | Unit               | Note or Test Condition        | Number  |
|--|-----------------------|--------|------|------|--------------------|-------------------------------|---------|
|  |                       | Min.   | Typ. | Max. |                    |                               |         |
| Battery Voltage Range for Nominal Operation  | $V_{\text{BAT(NOR)}}$ | 6.0    | –    | 18.0 | V                  | –                             | P_4.2.1 |
| Extended Battery Voltage Range for Operation | $V_{\text{BAT(EXT)}}$ | 0      | –    | 31   | V                  | parameter deviations possible | P_4.2.2 |
| Input Voltage Range for Nominal Operation    | $V_{\text{IN(NOR)}}$  | 3.0    | –    | 5.5  | V                  | –                             | P_4.2.3 |
| Junction Temperature                         | $T_J$                 | -40    | –    | 150  | $^{\circ}\text{C}$ | –                             | P_4.2.5 |

**General Product Characteristics**

1) Not subject to production test, specified by design

*Note:* Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

**4.3 Thermal Resistance**

*Note:* This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

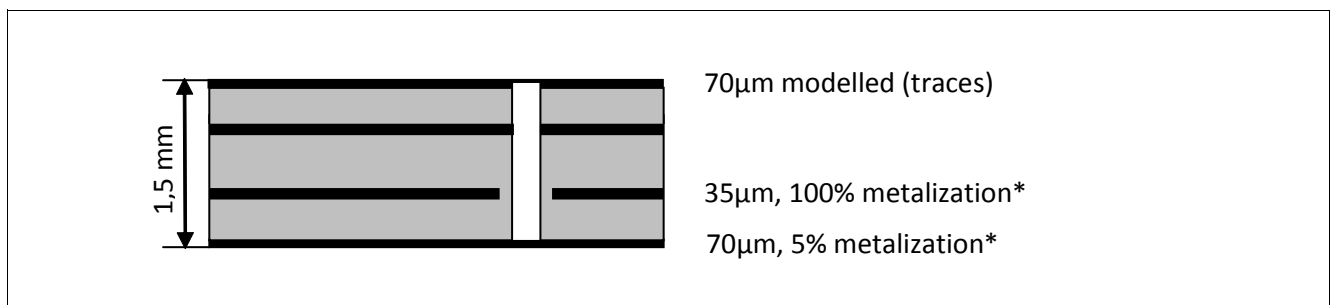
**Table 4 Thermal Resistance PG-TO252-3**

| Parameter   | Symbol           | Values |      |      | Unit | Note or Test Condition | Number   |
|---|------------------|--------|------|------|------|------------------------|----------|
|   |                  | Min.   | Typ. | Max. |      |                        |          |
| Junction to Soldering Point                       | $R_{thJSP}$      | –      | 5.1  | –    | K/W  | <sup>1) 2)</sup>       | P_4.3.4  |
| Junction to Ambient (2s2p)                        | $R_{thJA(2s2p)}$ | –      | 28   | –    | K/W  | <sup>1) 3)</sup>       | P_4.3.8  |
| Junction to Ambient (1s0p+600 mm <sup>2</sup> Cu) | $R_{thJA(1s0p)}$ | –      | 42   | –    | K/W  | <sup>1) 4)</sup>       | P_4.3.12 |

- 1) Not subject to production test, specified by design
- 2) Specified  $R_{thJSP}$  value is simulated at natural convection on a cold plate setup (all pins are fixed to ambient temperature).  
 $T_A = 85^\circ\text{C}$ . Device is loaded with 1 W power.
- 3) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70  $\mu\text{m}$  Cu, 2 x 35  $\mu\text{m}$  Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.  
 $T_A = 85^\circ\text{C}$ , Device is loaded with 1 W power.
- 4) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 1s0p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional heatspreading copper area of 600 mm<sup>2</sup> and 70  $\mu\text{m}$  thickness.  $T_A = 85^\circ\text{C}$ , Device is loaded with 1 W power.

**4.3.1 PCB set up**

The following PCB set up was implemented to determine the transient thermal impedance<sup>1)</sup>

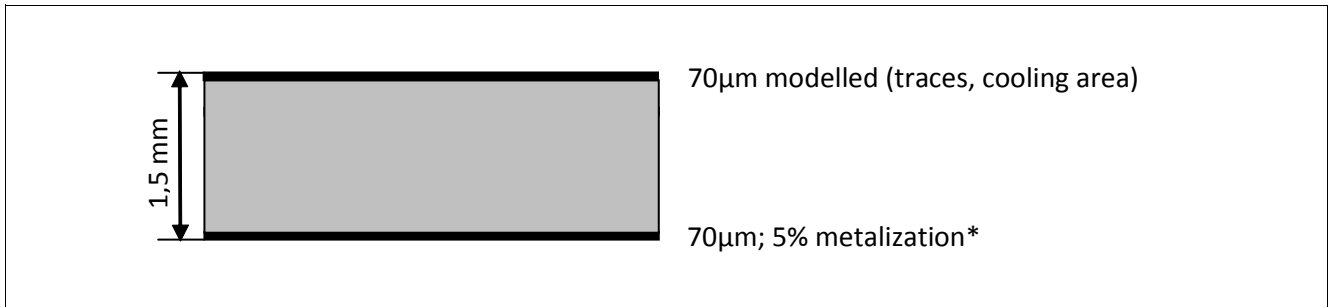


**Figure 4 Cross section JEDEC2s2p**

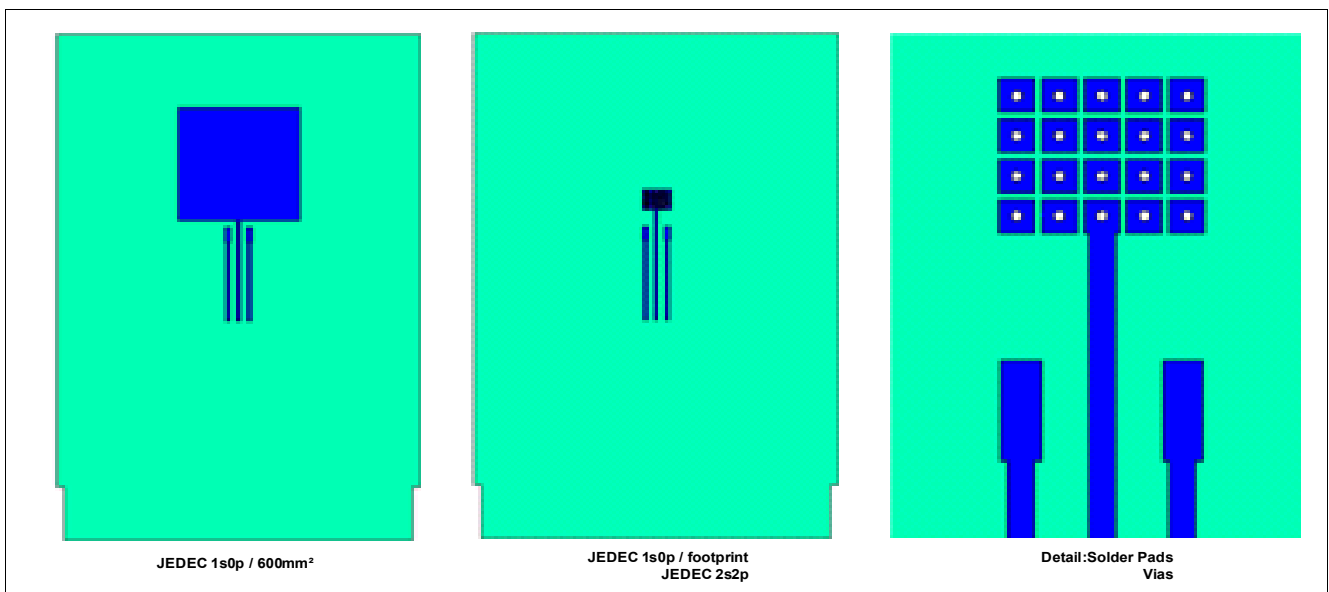
1) (\*) means percentual Cu metalization on each layer



**General Product Characteristics**



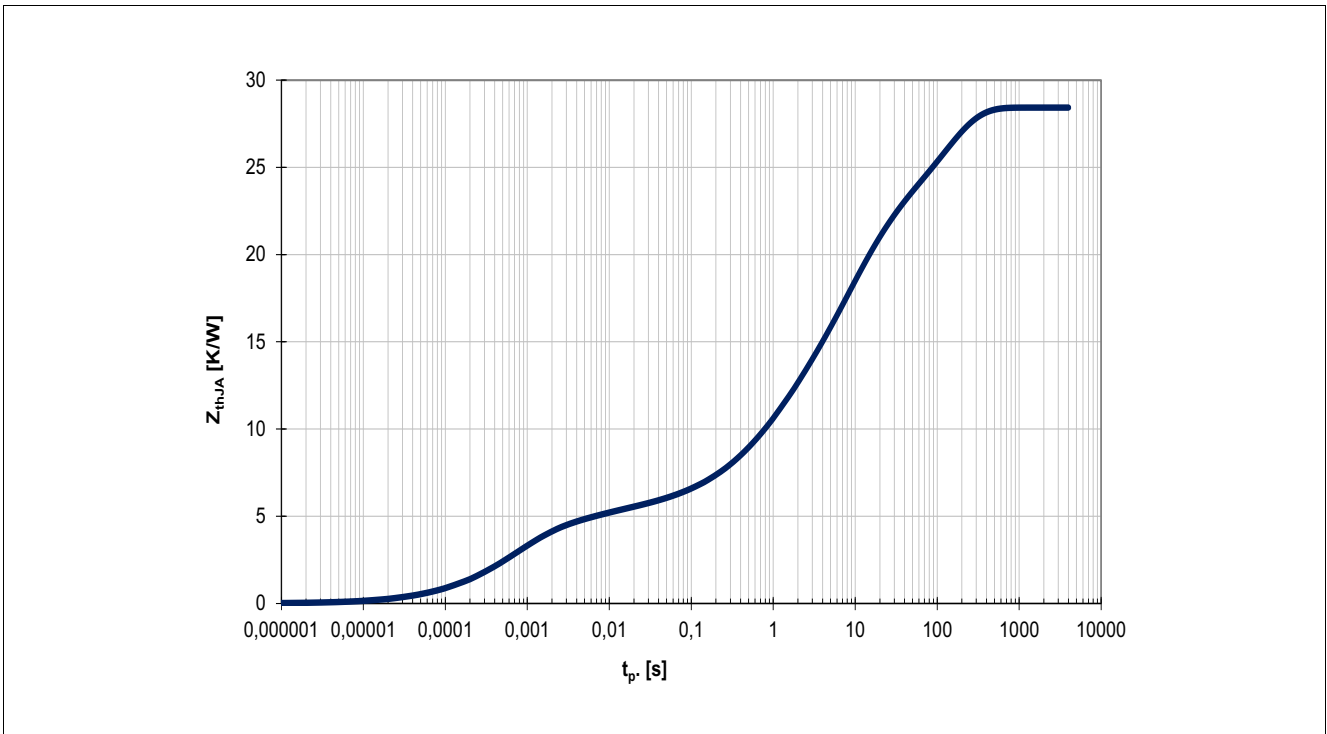
**Figure 5** Cross section JEDEC1s0p



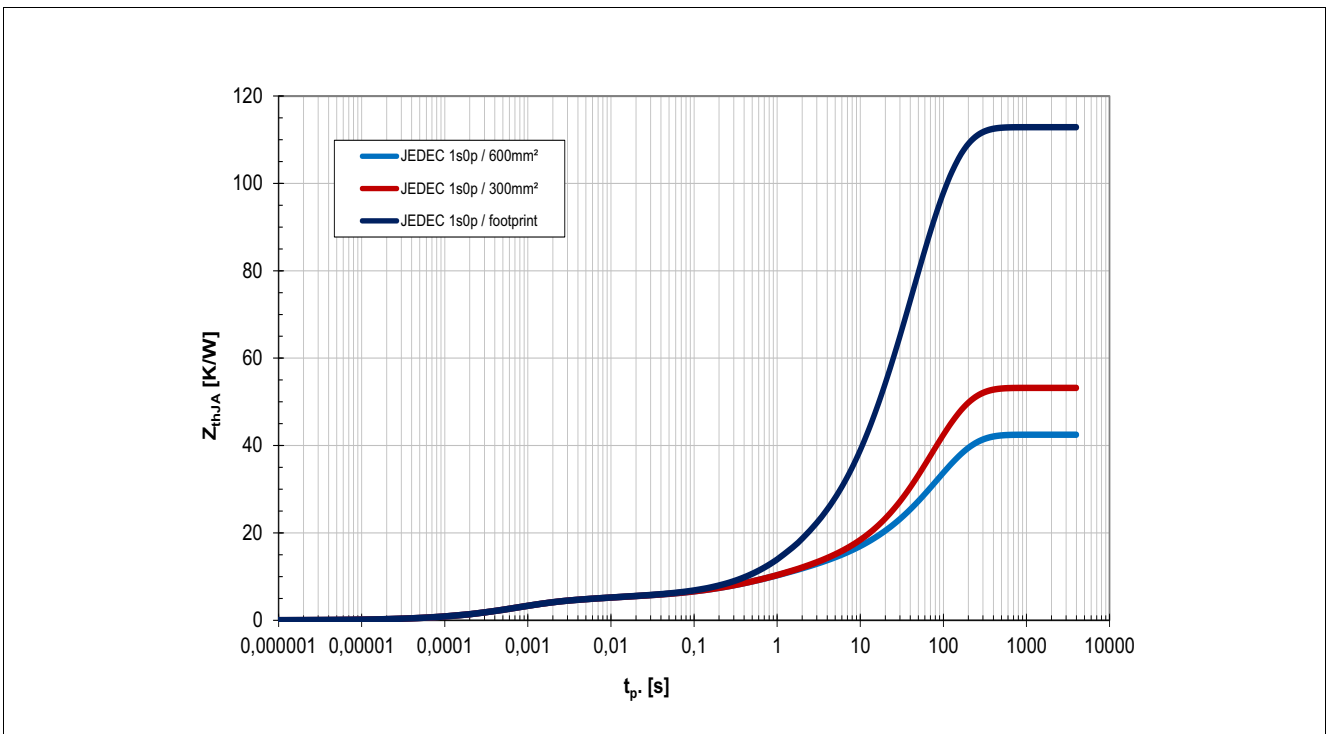
**Figure 6** PCB layout

### 4.3.2 Transient Thermal Impedance

**General Product Characteristics**



**Figure 7** Typical transient thermal impedance  $Z_{thJA} = f(t_p)$ ,  $T_A = 85^\circ\text{C}$   
 Value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 x 70 μm Cu, 2 x 35 μm Cu). Device is dissipating 1 W power.



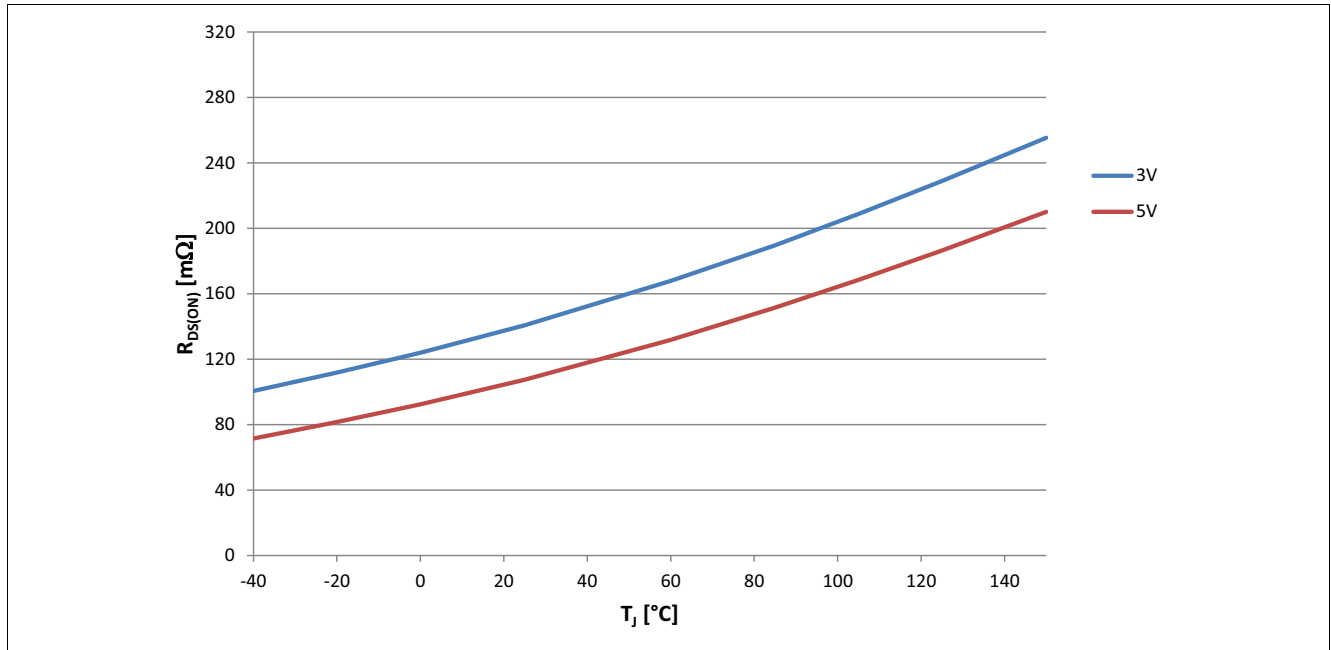
**Figure 8** Typical transient thermal impedance  $Z_{thJA} = f(t_p)$ ,  $T_a = 85^\circ\text{C}$   
 Value is according to Jedec JESD51-3 at natural convection on FR4 1s0p board. Device is dissipating 1 W power.

Power Stage

## 5 Power Stage

### 5.1 Output On-state Resistance

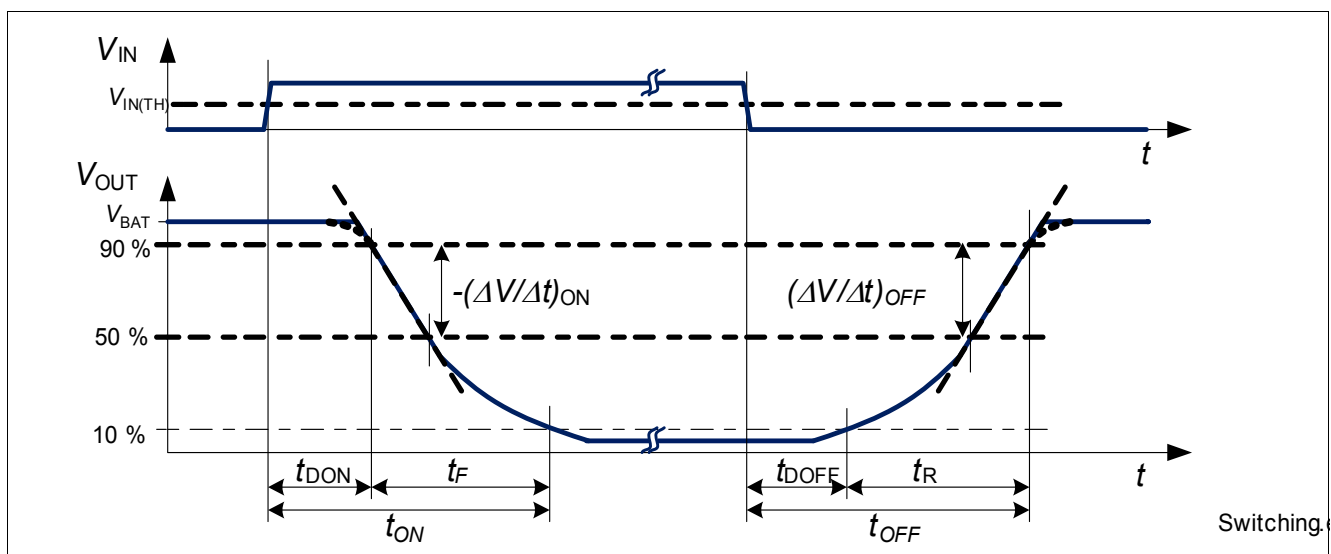
The on-state resistance depends on the junction temperature  $T_J$  and on the applied input voltage. **Figure 9** show this dependencies in terms of temperature and voltage for the typical on-state resistance  $R_{DS(ON)}$ . The behavior in reverse polarity is described in **“Reverse Current capability” on Page 13**



**Figure 9** Typical On-State Resistance,  
 $R_{DS(ON)} = f(T_J), V_{IN} = 3V; V_{IN} = 5V$

### 5.2 Resistive Load Output Timing

**Figure 10** shows the typical timing when switching a resistive load.



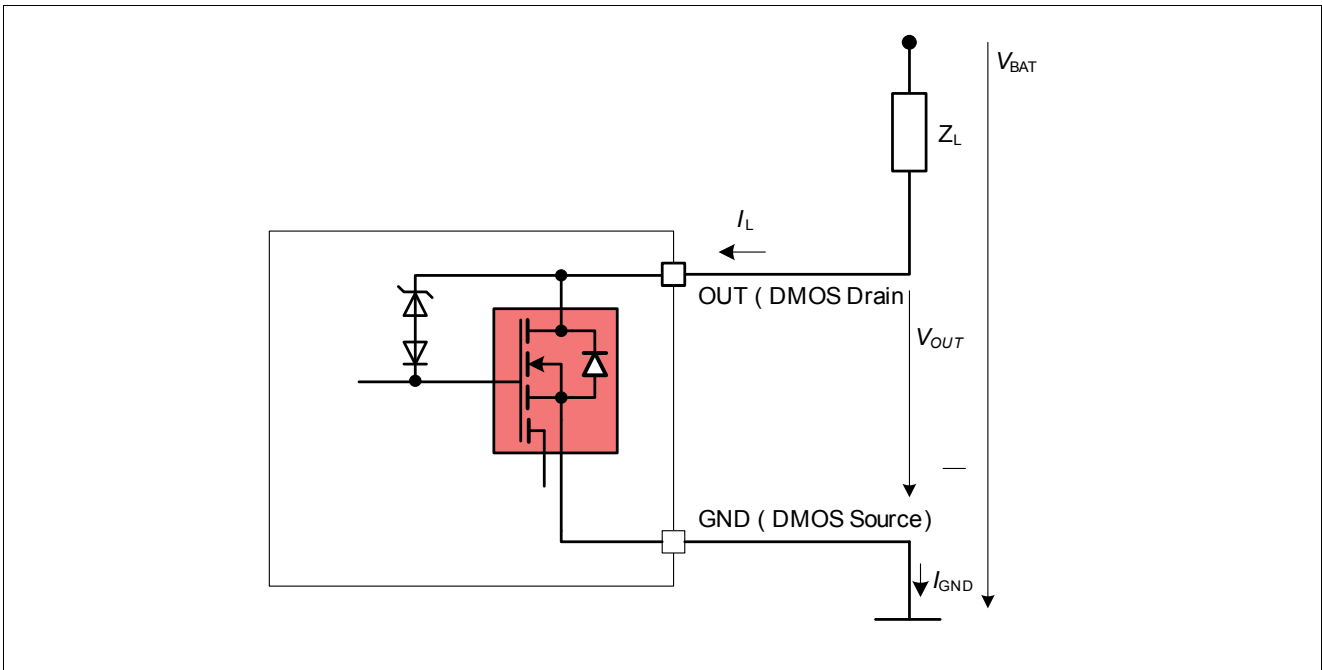
**Figure 10** Definition of Power Output Timing for Resistive Load

**Power Stage**

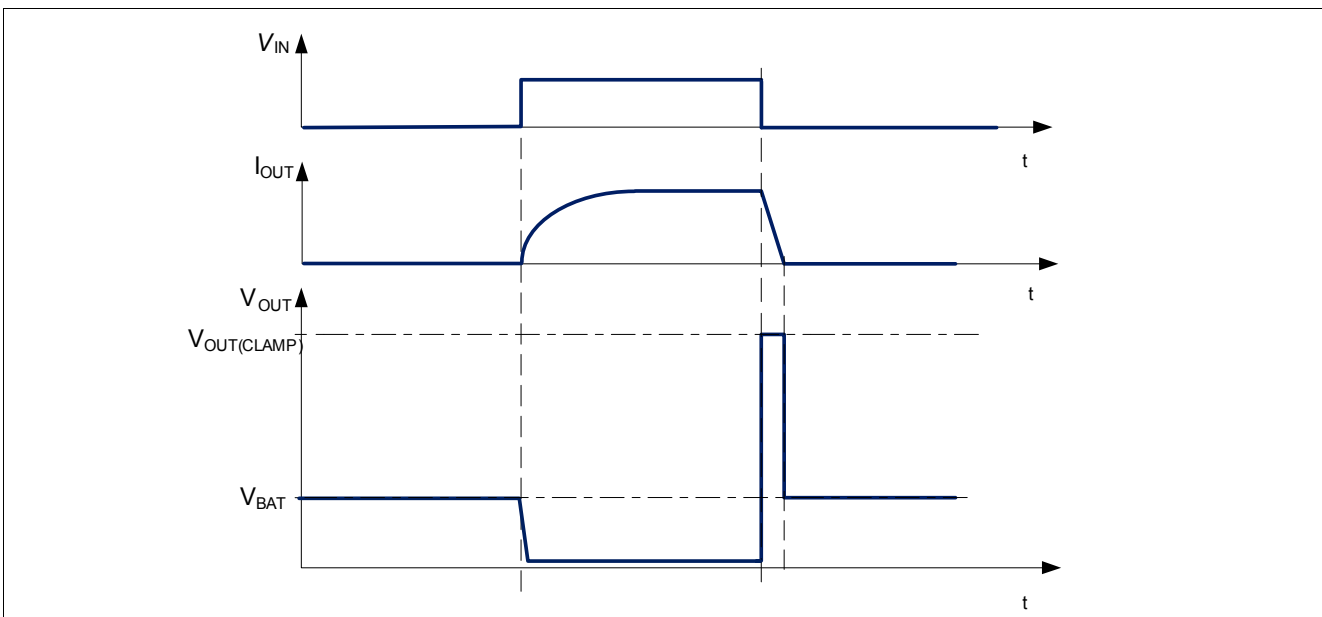
**5.3 Inductive Load**

**5.3.1 Output Clamping**

When switching off inductive loads with low side switches, the Drain-Source voltage  $V_{OUT}$  rises above battery potential, because the inductance intends to continue driving the current. To prevent unwanted high voltages the device has a voltage clamping mechanism to keep the voltage at  $V_{OUT(CLAMP)}$ . During this clamping operation mode the device heats up as it dissipates the energy from the inductance. Therefore the maximum allowed load inductance is limited. See [Figure 11](#) and [Figure 12](#) for more details.



**Figure 11 Output Clamp Circuitry**



**Figure 12 Switching an Inductive Load**

**Power Stage**

**5.3.1.1 Maximum Load Inductance**

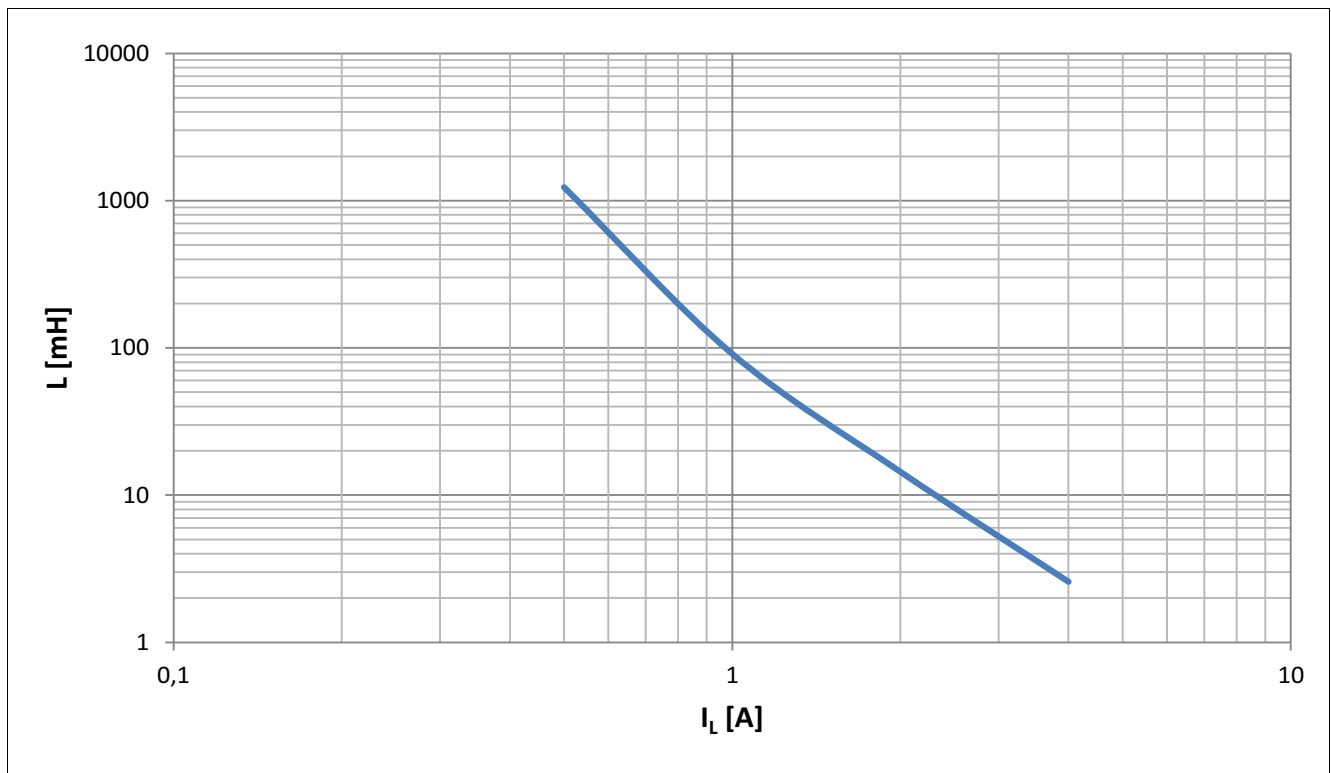
While demagnetization of inductive loads, energy has to be dissipated by the BTS3125TF. This energy can be calculated by the following equation:

$$E = V_{OUT(CLAMP)} \times \left[ \frac{V_{BAT} - V_{OUT(CLAMP)}}{R_L} \times \ln \left( 1 - \frac{R_L \times I_L}{V_{BAT} - V_{OUT(CLAMP)}} \right) + I_L \right] \times \frac{L}{R_L} \quad (5.1)$$

Following equation simplifies under the assumption of  $R_L = 0$

$$E = \frac{1}{2} L I_L^2 \times \left( 1 - \frac{V_{BAT}}{V_{BAT} - V_{OUT(CLAMP)}} \right) \quad (5.2)$$

For maximum single avalanche energy please also refer to EAS value in **“Energies” on Page 6**.



**Figure 13 Maximum load inductance for single pulse**  
 $L = f(I_L), T_{J(0)} = T_{J,start} = 150^\circ\text{C}, V_{BAT} = 13.5\text{ V}$

**5.4 Reverse Current capability**

A reverse battery situation means the OUT pin is pulled below GND potentials to  $-V_{BAT}$  via the load  $Z_L$ . In this situation the load is driven by a current through the intrinsic body diode of the BTS3125TF. During Reverse Battery all protection functions like current limitation, over temperature shut down and over voltage clamping are not available.

## Power Stage

The device is dissipating a power loss which is defined by the driven current and the voltage drop on the DMOS reverse body diode “ $-V_{OUT}$ ”.

### 5.5 Inverse Current capability

An inverse current situation means the OUT pin is pulled below GND potential by current flowing from GND to OUT (for example in half-bridge configuration and inductive load using freewheeling via the low side path).

In this situation the load is driven by a current through the intrinsic body diode (device off) of the BTS3125TF. During Inverse operation all protection functions like current limitation, over temperature shut-down and over voltage clamping are not available.

The device is dissipating a power loss which is defined by the driven current and the voltage drop on the DMOS reverse body diode “ $-V_{OUT}$ ”.

#### Input current behavior during inverse condition on Output

Please note that during inverse current on drain an increased input current can flow. To limit this current it is needed to place a resistor ( $R_{IN}$ ) in line with the input, also to prevent the microcontroller I/O pins from latching up in this case. The value of this resistor is a compromise of input voltage level in normal operation and maximum allowed device input current  $I_{IN}$  or I/O current (for example of microcontroller).

$$R_{IN(\min)} = \frac{V_{OH\mu C(\max)}}{I_{IN(\max)}} \quad (5.3)$$

with  $I_{IN(\max)} = 2 \text{ mA}$  (see also **“Absolute Maximum Ratings” on Page 6**) allow for the device;

$V_{OH\mu C(\max)}$  maximum high level voltage of the control signal (microcontroller I/O)

### 5.6 Characteristics

Please see **“Power Stage” on Page 11** for electrical characteristic table.

**Protection Functions**

**6 Protection Functions**

The device provides embedded protection functions. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as “outside” normal operation. Protection functions are not designed for continuous repetitive operation.

**6.1 Over Voltage Clamping on OUTPUT**

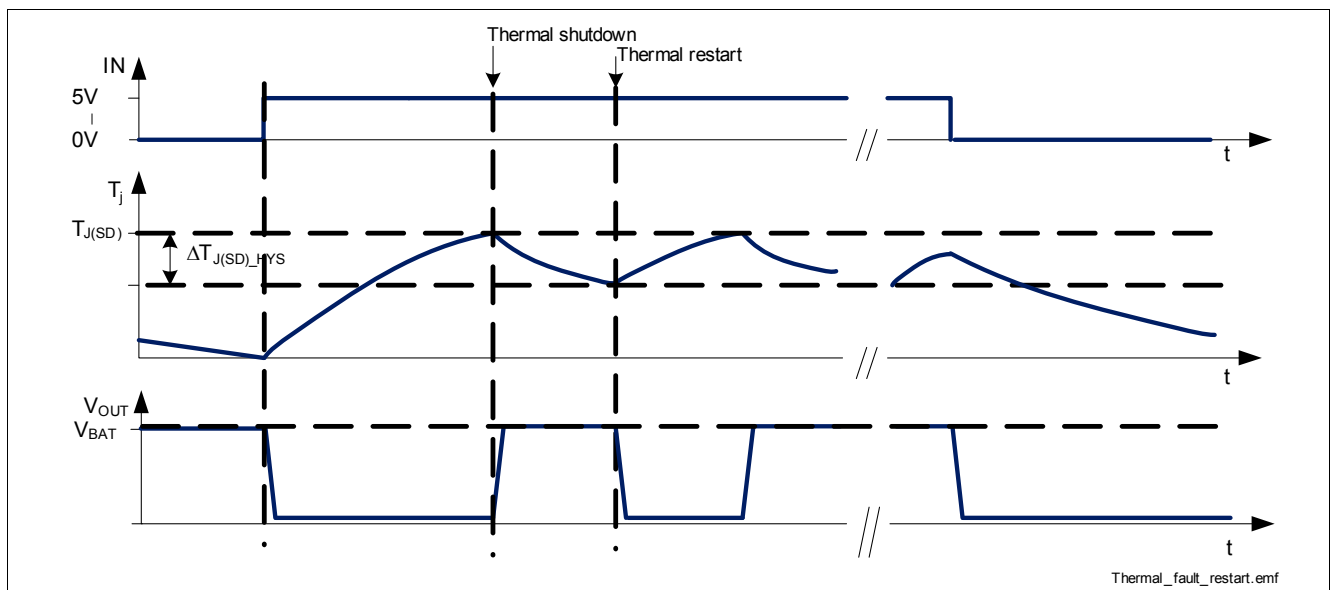
The BTS3125TF is equipped with a voltage clamp circuitry that keeps the drain-source (OUT to GND) voltage  $V_{DS}$  at a certain level  $V_{OUT(CLAMP)}$ . The over voltage clamping is overruling the other protection functions. Power dissipation has to be limited to not exceed the maximum allowed junction temperature.

This function is also used in terms of inductive clamping. Please see also [Chapter 5.3.1](#) for more details.

**6.2 Thermal Protection**

The device is protected against over temperature due to overload and / or bad cooling conditions. To ensure this a temperature sensor is located in the power MOSFET.

The BTS3125TF has a thermal protection function with automatic restart. After the device has switched off due to over temperature the device will stay off until the junction temperature has dropped down below the thermal hysteresis **“Thermal Protection” on Page 15.**



**Figure 14 Thermal protective switch OFF scenario with thermal restart**

**6.3 Short Circuit Protection / Current limitation**

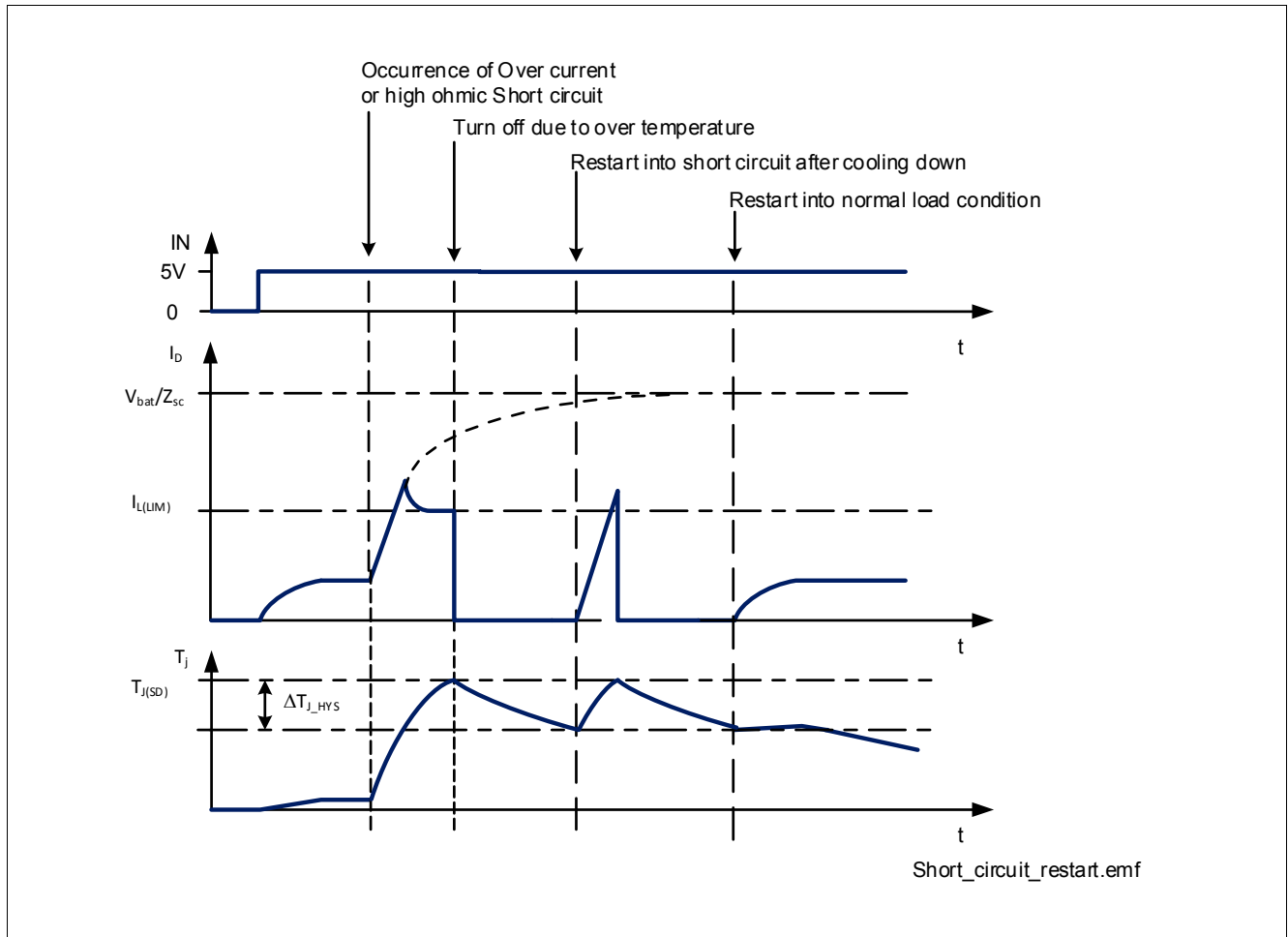
The condition short circuit is an overload condition to the device. If the load current reaches the limitation value of  $I_{L(LIM)}$  the device limits the current and starts heating up. When the thermal shutdown temperature is reached, the device turns off.

The time from the beginning of current limitation until the over temperature switch off depends strongly on the cooling conditions.

If input is still high, the device will turn on again after the measured temperature has dropped below the thermal hysteresis.

[Figure 15](#) shows this simplified behavior.

**Protection Functions**



**Figure 15 Short circuit protection via current limitation and over temperature switch off with auto-restart**

**6.4 Characteristics**

Please see **“Protection Functions” on Page 15** for electrical characteristic table.

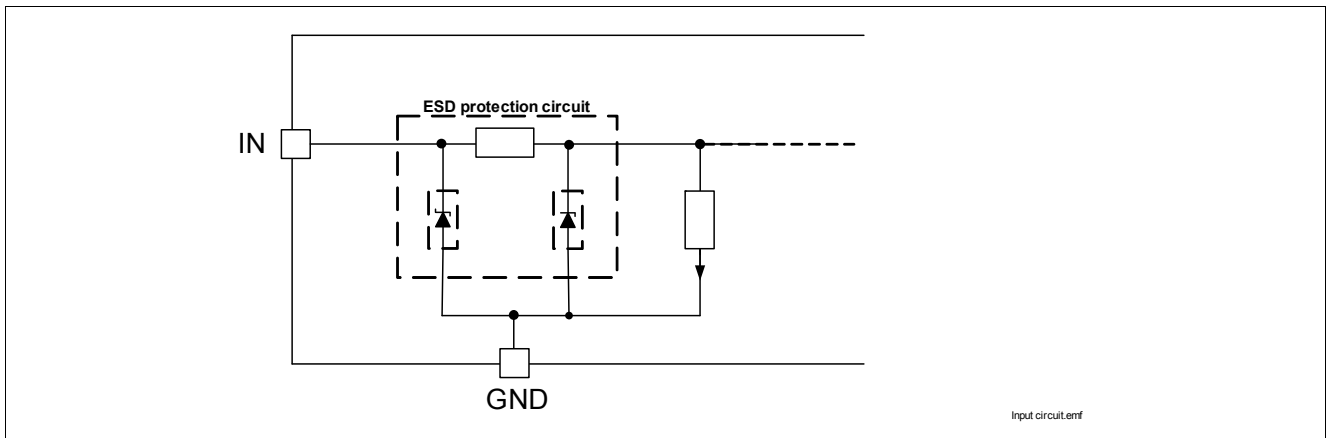


Input Stage

## 7 Input Stage

### 7.1 Input Circuit

**Figure 16** shows the input circuit of the BTS3125TF. In case of open or floating input pin, the device will automatically switch off and remain off. An ESD Zener structure protects the input circuit against ESD pulses.



**Figure 16** Simplified Input circuitry

### 7.2 Characteristics

Please see **“Input Stage” on Page 21** for electrical characteristic table.

**Electrical Characteristics**

**8 Electrical Characteristics**

**8.1 Power Stage**

Please see Chapter **“Power Stage” on Page 11** for parameter description and further details.

**Table 5 Electrical Characteristics: Power Stage**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{\text{BAT}} = 6\text{ V}$  to  $18\text{ V}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter   | Symbol                  | Values |      |      | Unit | Note or Test Condition   | Number   |
|---|-------------------------|--------|------|------|------|--|----------|
|   |                         | Min.   | Typ. | Max. |      |  |          |
| <b>Power Stage</b>                                |                         |        |      |      |      |  |          |
| On-State resistance at hot temperature (150°C)    | $R_{\text{DS(ON)}_150}$ | –      | 208  | 250  | mΩ   | $T_j = 150^\circ\text{C}$ ;<br>$V_{\text{IN}} = 5\text{ V}$ ;<br>$I_L = I_{\text{L(NOM)}}$                           | P_8.1.4  |
| On-State resistance at ambient temperature (25°C) | $R_{\text{DS(ON)}_25}$  | –      | 108  | –    | mΩ   | $T_j = 25^\circ\text{C}$ ;<br>$V_{\text{IN}} = 5\text{ V}$ ;<br>$I_L = I_{\text{L(NOM)}}$                            | P_8.1.8  |
| Nominal load current                              | $I_{\text{L(NOM)}}$     | –      | 2    | –    | A    | <sup>1)</sup><br>$T_j < 150^\circ\text{C}$ ;<br>$T_A = 85^\circ\text{C}$<br>$V_{\text{IN}} = 5\text{ V}$             | P_8.1.28 |
| OFF state load current, Output leakage current    | $I_{\text{L(OFF)}_85}$  | –      | –    | 0.6  | μA   | <sup>2)</sup><br>$V_{\text{BAT}} = 13.5\text{ V}$ ;<br>$V_{\text{IN}} = 0\text{ V}$ ;<br>$T_j \leq 85^\circ\text{C}$ | P_8.1.32 |
| OFF state load current, Output leakage current    | $I_{\text{L(OFF)}_150}$ | –      | 0.5  | 1.1  | μA   | $V_{\text{BAT}} = 18\text{ V}$ ;<br>$V_{\text{IN}} = 0\text{ V}$ ;<br>$T_j = 150^\circ\text{C}$                      | P_8.1.36 |
| Reverse body diode forward voltage                | $-V_{\text{OUT}}$       | –      | 0.8  | 1.1  | V    | $I_L = -I_{\text{L(NOM)}}$ ;<br>$V_{\text{IN}} = 0\text{ V}$   | P_8.1.45 |

**Electrical Characteristics**

**Table 5 Electrical Characteristics: Power Stage (cont'd)**

$T_j = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{\text{BAT}} = 6\text{ V}$  to  $18\text{ V}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter  | Symbol                             | Values |      |      | Unit                   | Note or Test Condition  | Number   |
|--|------------------------------------|--------|------|------|------------------------|---|----------|
|  |                                    | Min.   | Typ. | Max. |                        |   |          |
| <b>Dynamic characteristics - switching times single pulse <math>V_{\text{BAT}} = 13.5\text{ V}</math>, <math>R_L = 10\Omega</math>;</b><br><b>for definition details see <a href="#">Figure 10 “Definition of Power Output Timing for Resistive Load”</a> on <a href="#">Page 11</a></b> |                                    |        |      |      |                        |   |          |
| Turn-on time   | $t_{\text{ON}}$                    | 35     | 75   | 115  | $\mu\text{s}$          | <sup>3)</sup><br>$V_{\text{IN}} = 0\text{ V}$ to $5\text{ V}$ ;<br>$V_{\text{OUT}} = 10\% V_{\text{BAT}}$                             | P_8.1.46 |
| Turn-off time  | $t_{\text{OFF}}$                   | 70     | 135  | 210  | $\mu\text{s}$          | <sup>4)</sup><br>$V_{\text{IN}} = 5\text{ V}$ to $0\text{ V}$ ;<br>$V_{\text{OUT}} = 90\% V_{\text{BAT}}$                             | P_8.1.47 |
| Turn-on delay time   | $t_{\text{DON}}$                   | 5      | 15   | 25   | $\mu\text{s}$          | $V_{\text{IN}} = 0\text{ V}$ to $5\text{ V}$ ;<br>$V_{\text{OUT}} = 90\% V_{\text{BAT}}$  | P_8.1.48 |
| Turn-off delay time  | $t_{\text{DOFF}}$                  | 40     | 75   | 120  | $\mu\text{s}$          | $V_{\text{IN}} = 5\text{ V}$ to $0\text{ V}$ ;<br>$V_{\text{OUT}} = 10\% V_{\text{BAT}}$  | P_8.1.49 |
| Fall time, Falling output voltage (turn-on)  | $t_{\text{F}}$                     | 30     | 60   | 90   | $\mu\text{s}$          | $V_{\text{IN}} = 0\text{ V}$ to $5\text{ V}$ ;<br>$V_{\text{OUT}} = 90\% V_{\text{BAT}}$ to<br>$V_{\text{OUT}} = 10\% V_{\text{BAT}}$ | P_8.1.50 |
| Rise time, Rising output voltage   | $t_{\text{R}}$                     | 30     | 60   | 90   | $\mu\text{s}$          | $V_{\text{IN}} = 5\text{ V}$ to $0\text{ V}$ ;<br>$V_{\text{OUT}} = 10\% V_{\text{BAT}}$ to<br>$V_{\text{OUT}} = 90\% V_{\text{BAT}}$ | P_8.1.51 |
| Turn-on Slew rate  | $-(\Delta V/\Delta t)_{\text{ON}}$ | 0.22   | 0.45 | 0.65 | $\text{V}/\mu\text{s}$ | <sup>5)</sup><br>$V_{\text{OUT}} = 90\% V_{\text{BAT}}$ to<br>$V_{\text{OUT}} = 50\% V_{\text{BAT}}$                                  | P_8.1.52 |
| Turn-off Slew rate   | $(\Delta V/\Delta t)_{\text{OFF}}$ | 0.22   | 0.45 | 0.65 | $\text{V}/\mu\text{s}$ | <sup>6)</sup><br>$V_{\text{OUT}} = 50\% V_{\text{BAT}}$ to<br>$V_{\text{OUT}} = 90\% V_{\text{BAT}}$                                  | P_8.1.53 |

1) Not subject to production test, calculated by  $R_{\text{thJA}}$  (JEDEC 2s2p, PCB) and  $R_{\text{DS(ON)}}$

2) Not subject to production test, specified by design;

3) Not subject to production test, calculated with delay time ON and fall time

4) Not subject to production test, calculated with delay time OFF and rise time

5) Not subject to production test, calculated slew rate between 90% and 50%  $V_{\text{OUT}}$ ;

6) Not subject to production test, calculated slew rate between 50% and 90%  $V_{\text{OUT}}$ ;

**8.2 Protection**

Please see Chapter **“Protection Functions”** on [Page 15](#) for parameter description and further details.

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation*

**Electrical Characteristics**

**Table 6 Electrical Characteristics: Protection**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{\text{BAT}} = 6\text{ V}$  to  $18\text{ V}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter  | Symbol                     | Values |      |      | Unit             | Note or Test Condition  | Number   |
|--|----------------------------|--------|------|------|------------------|---|----------|
|  |                            | Min.   | Typ. | Max. |                  |   |          |
| <b>Thermal Protection</b>                                      |                            |        |      |      |                  |   |          |
| Thermal shut down junction temperature                         | $T_{\text{J(SD)}}$         | 150    | 175  | –    | $^\circ\text{C}$ | <sup>1)</sup><br>$3\text{ V} < V_{\text{IN}} < 5.5\text{ V}$  | P_8.2.1  |
| Thermal hysteresis   | $\Delta T_{\text{J\_HYS}}$ | –      | 15   | –    | K                | <sup>1)</sup>   | P_8.2.3  |
| <b>Overvoltage Protection</b>                                  |                            |        |      |      |                  |   |          |
| Drain clamp voltage  | $V_{\text{OUT(CLAMP)}}$    | 40     | 45   | –    | V                | $V_{\text{IN}} = 0\text{ V};$<br>$I_{\text{D}} = 4\text{ mA}$ | P_8.2.12 |
| <b>Current limitation (see also <a href="#">Figure 15</a>)</b> |                            |        |      |      |                  |   |          |
| Current limitation   | $I_{\text{L(LIM)}}$        | 7      | 10.5 | 14   | A                | $V_{\text{IN}} = 5\text{ V};$                                 | P_8.2.16 |

1) Not subject to production test, specified by design.

**Electrical Characteristics**

**8.3 Input Stage**

Please see Chapter “**Input Stage**” on **Page 17** for description and further details.

**Table 7 Electrical Characteristics: Input**

$T_j = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{\text{BAT}} = 6\text{ V}$  to  $18\text{ V}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                                      | Symbol                 | Values |      |      | Unit          | Note or Test Condition   | Number  |
|--|------------------------|--------|------|------|---------------|--|---------|
|  |                        | Min.   | Typ. | Max. |               |  |         |
| <b>Input</b>                                   |                        |        |      |      |               |  |         |
| Input Current, normal ON state                 | $I_{\text{IN(ON)}}$    | –      | 82   | 110  | $\mu\text{A}$ | $V_{\text{IN}} = 5.0\text{ V}$   | P_8.3.1 |
| Input Current, protection mode                 | $I_{\text{IN(PROT)}}$  | –      | 124  | 180  | $\mu\text{A}$ | $V_{\text{IN}} = 5.0\text{ V}$ ;   | P_8.3.6 |
| Input current, inverse condition on OUT to GND | $I_{\text{IN(-VOUT)}}$ | –      | 15   | –    | $\text{mA}$   | 1) 2)<br>$V_{\text{OUT}} < -0.3\text{ V}$ ;<br>$-0.3\text{ V} \leq V_{\text{IN}} < 5.5\text{ V}$ | P_8.3.7 |
| Input pull down current                        | $I_{\text{IN-GND}}$    | 10     | –    | –    | $\mu\text{A}$ | 3)<br>$V_{\text{IN}} = V_{\text{IN(TH)}}$  | P_8.3.8 |
| Input Voltage on-threshold                     | $V_{\text{IN(TH)}}$    | 0.8    | 2.3  | 3    | $\text{V}$    | $I_{\text{L}} = 0.4\text{ mA}$ ;<br>Power DMOS active  | P_8.3.9 |

- 1) Not subject to production test, specified by design.
- 2) Input current must not exceed the maximum ratings in Chapter 4, P\_4.1.10
- 3) Not subject to production test, specified by design.

Characterization Results

## 9 Characterization Results

Typical performance characteristics.

### 9.1 Power Stage

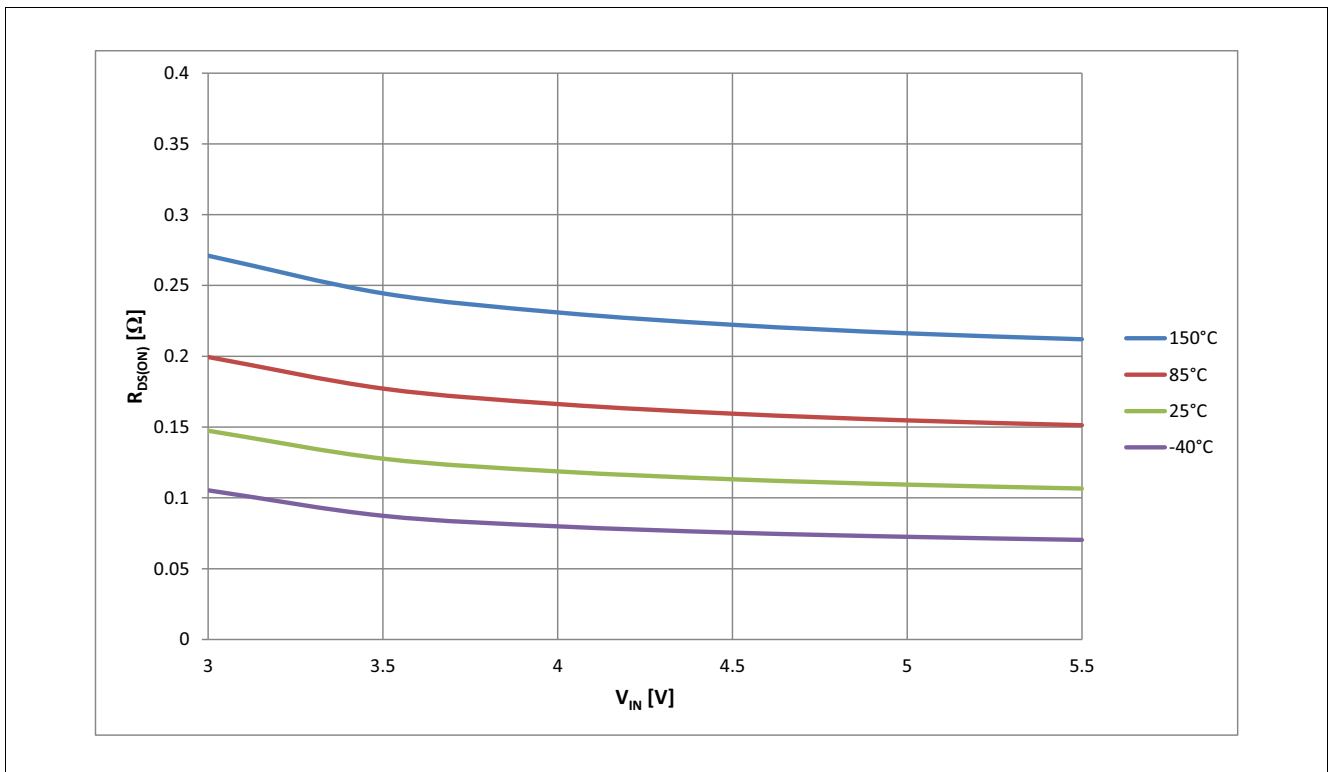
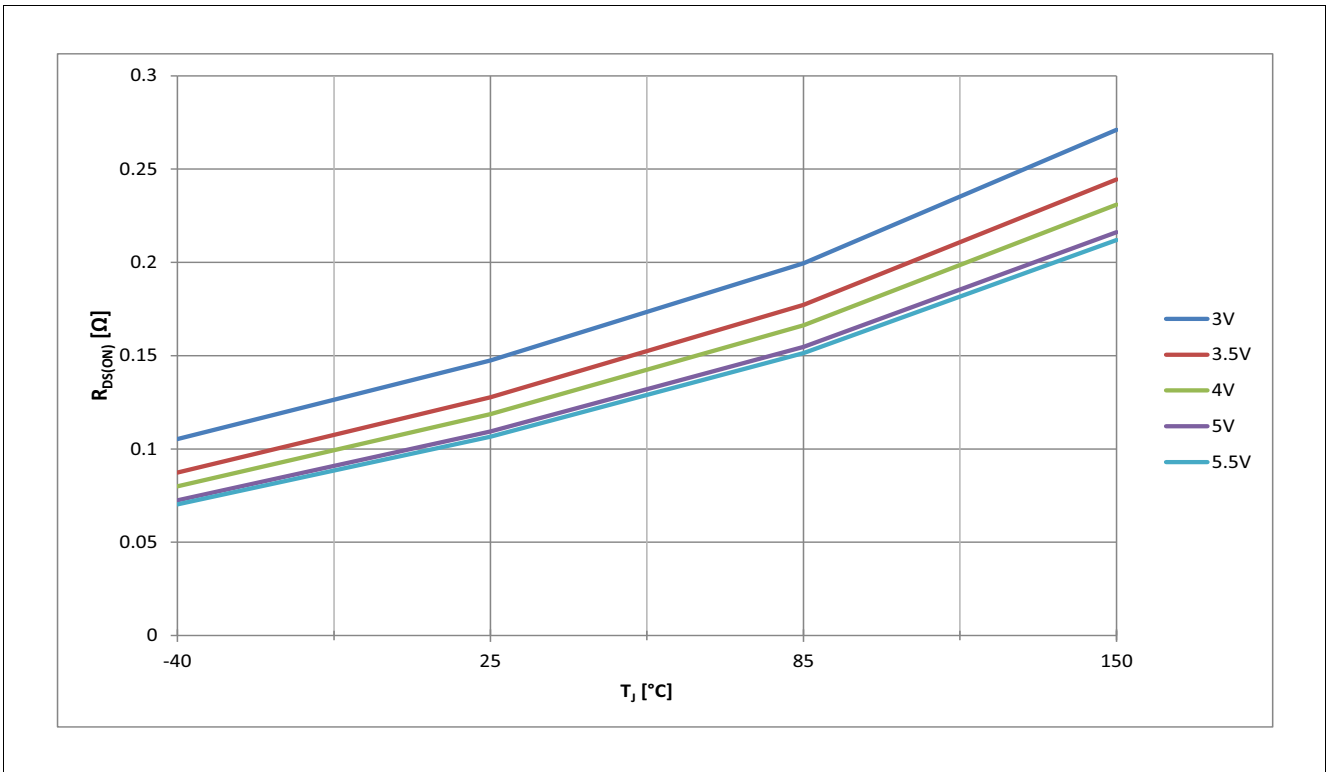
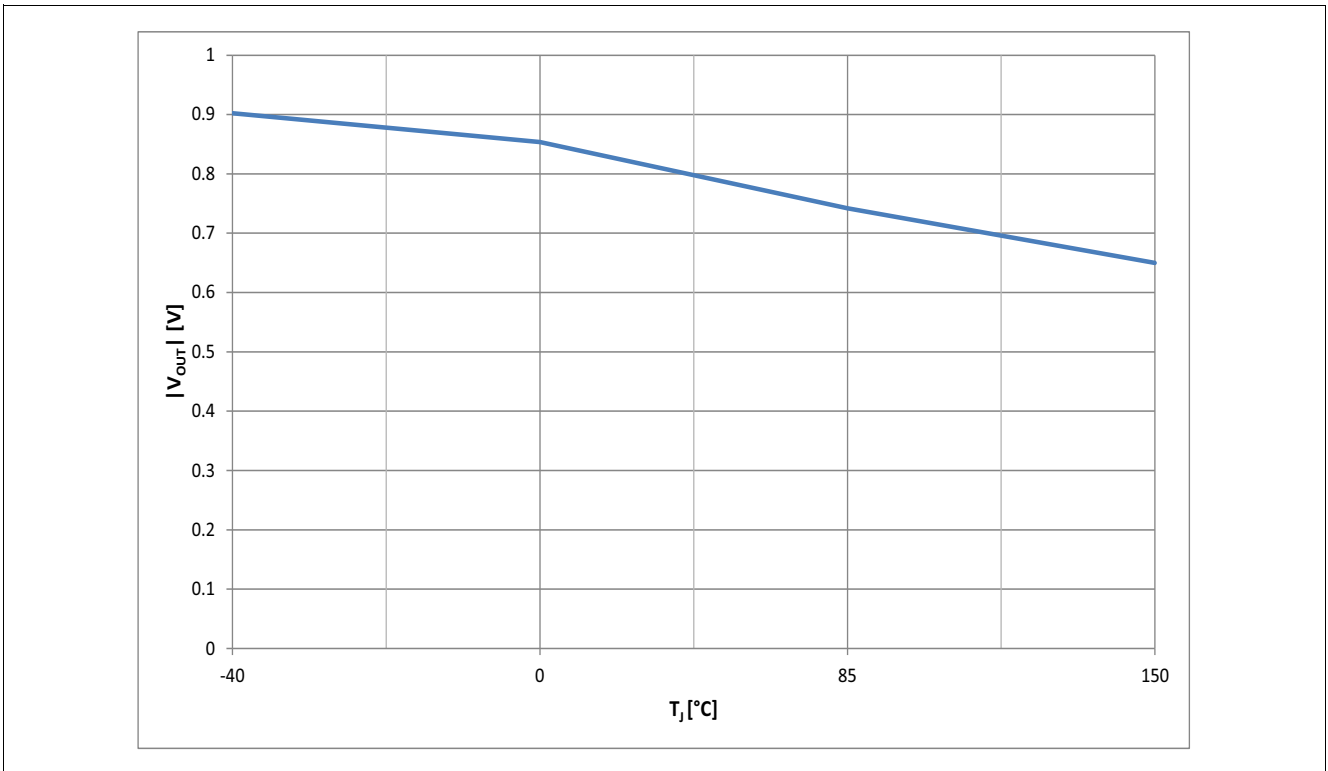


Figure 17 Typical  $R_{DS(ON)}$  vs.  $V_{IN}$  @  $T_j = -40 \dots 150^\circ\text{C}$ ,  $I_L = I_{L(NOM)}$

**Characterization Results**

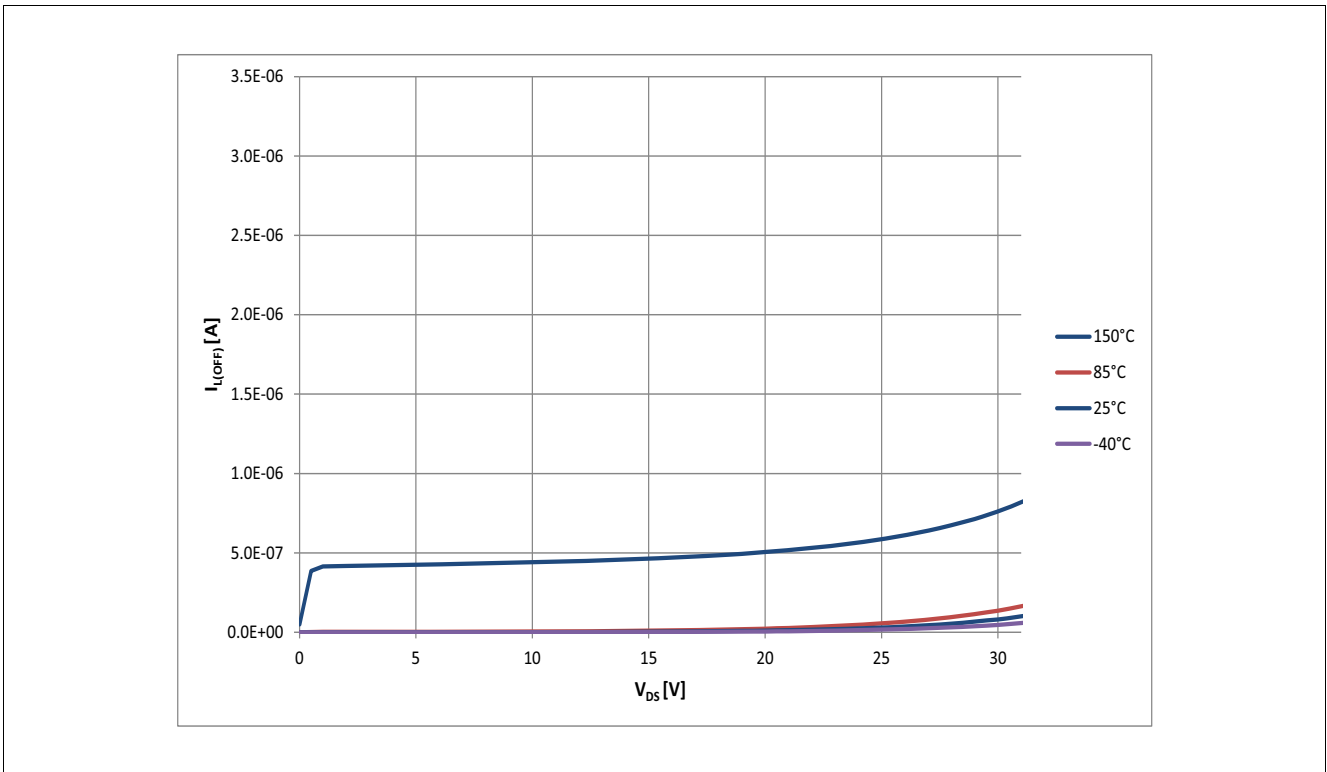


**Figure 18** Typical  $R_{DS(ON)}$  vs.  $T_J$  @  $V_{IN} = 3 \dots 5.5V, I_L = I_{L(NOM)}$

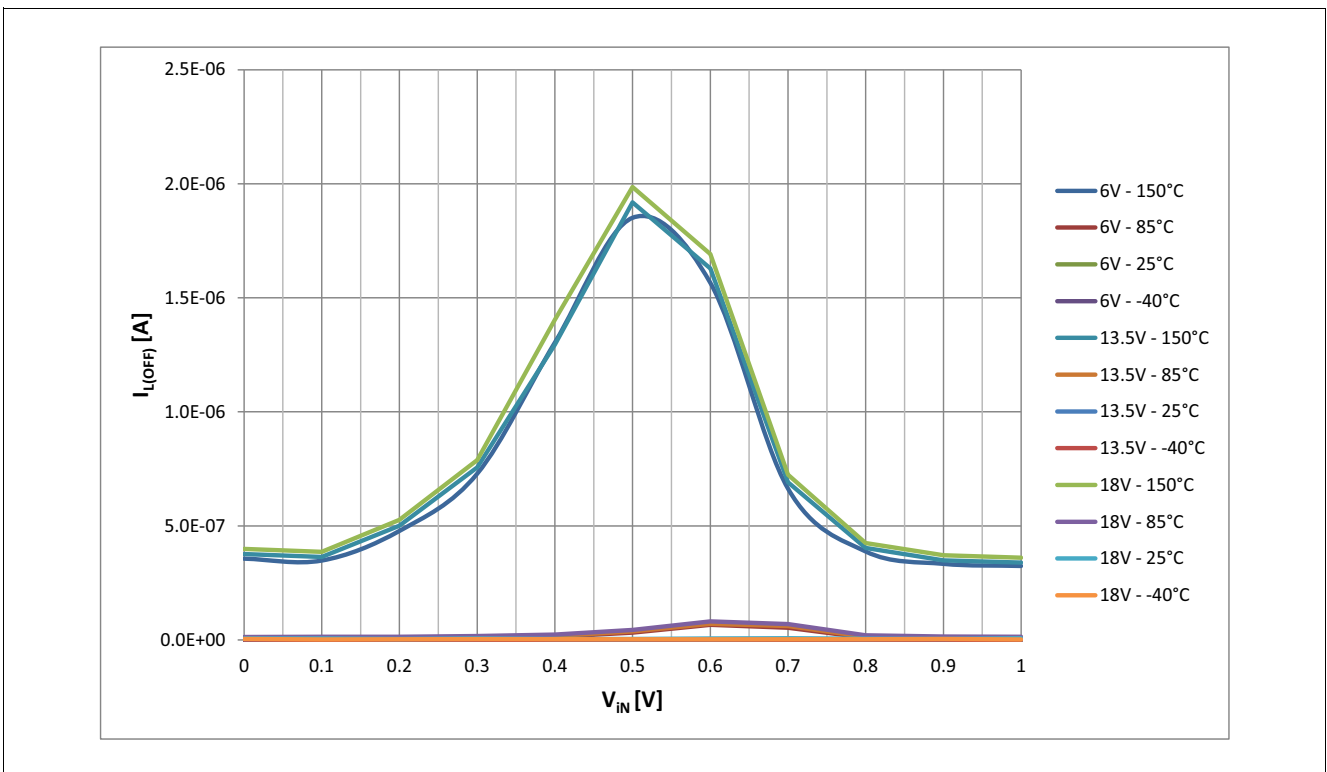


**Figure 19** Typical Reverse Diode  $|V_{OUT}|$  vs.  $T_J$  @  $I_L = I_{L(NOM)}$

**Characterization Results**



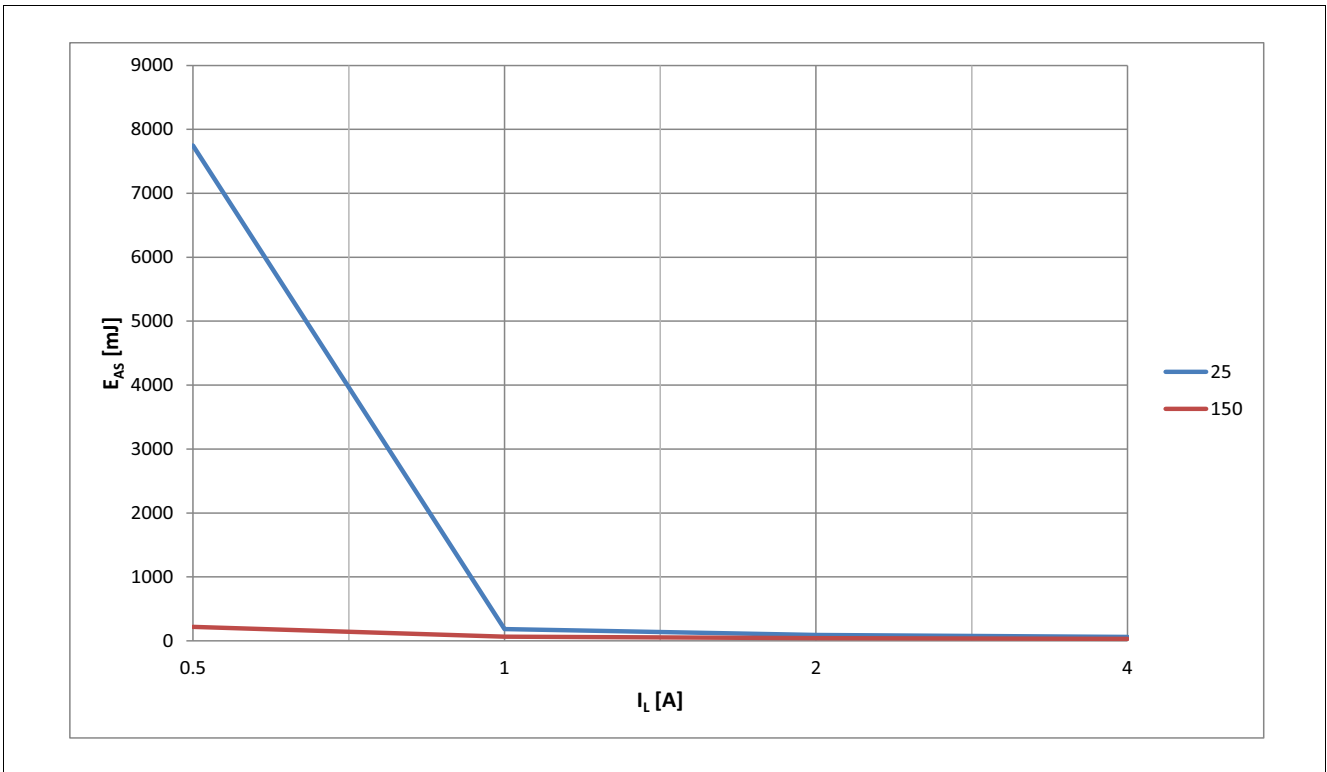
**Figure 20** Typical  $I_{L(OFF)}$  vs.  $V_{DS}$  @  $T_J = -40 \dots 150^\circ\text{C}$ ,  $V_{IN} = 0 \text{ V}$



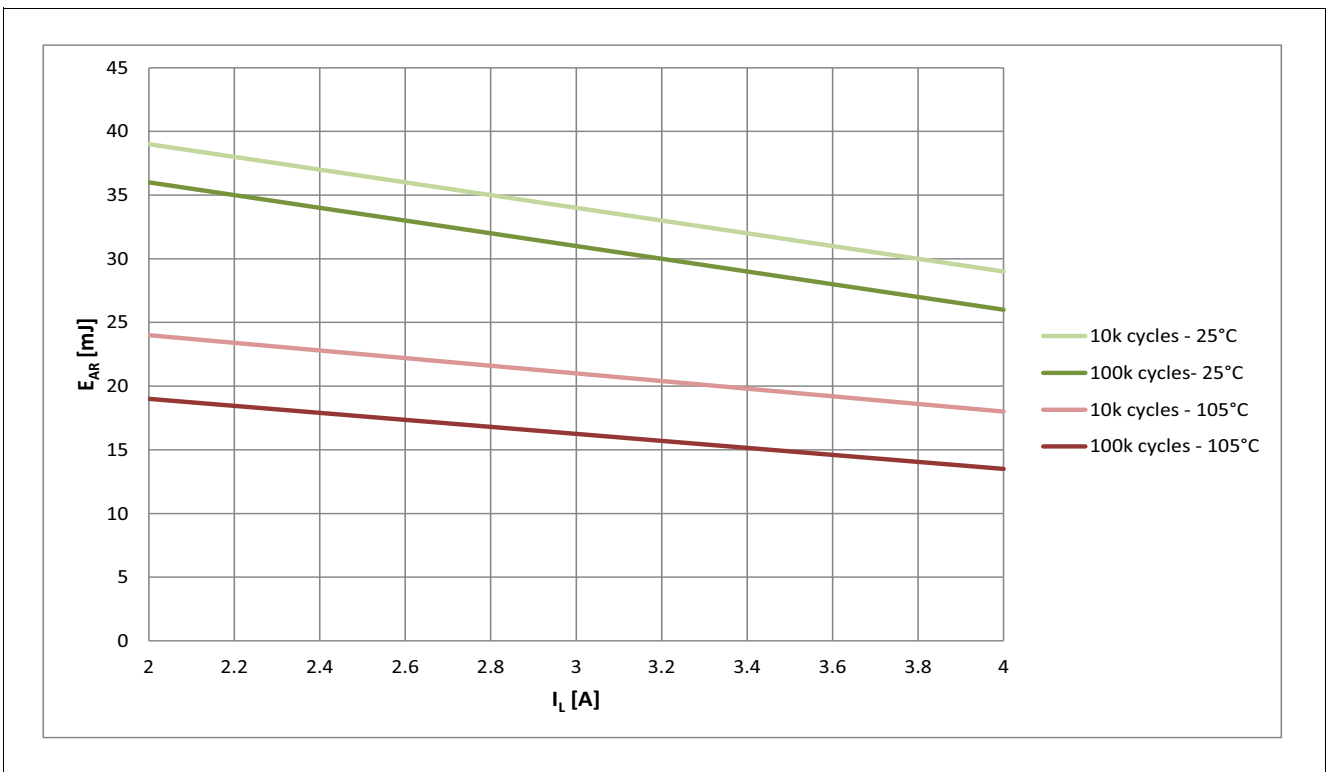
**Figure 21** Typical  $I_{L(OFF)}$  vs.  $V_{IN}$  @  $T_J = -40 \dots 150^\circ\text{C}$ ,  $V_{BAT} = 6 \dots 18 \text{ V}$



**Characterization Results**

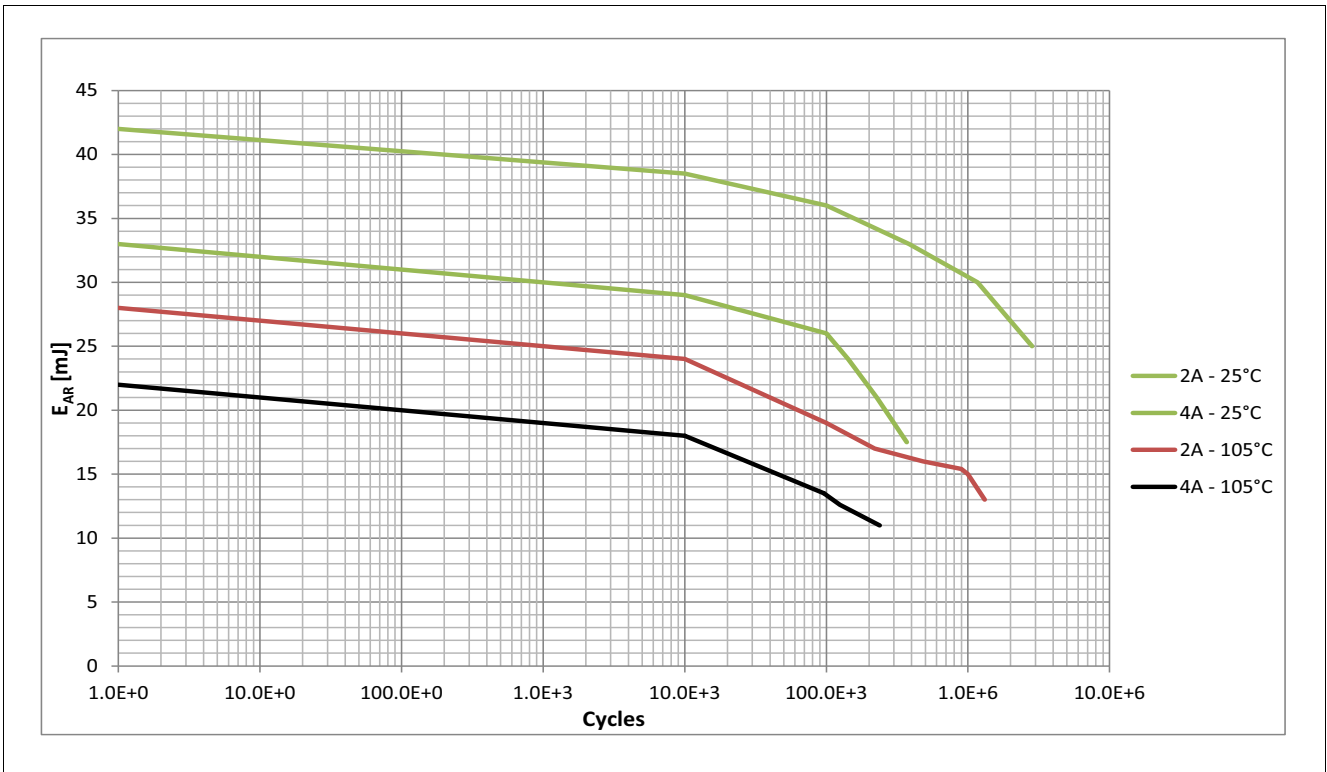


**Figure 22** Typical destruction point.  $E_{AS}$  vs.  $I_L$  @  $T_J = 25$  and  $150^\circ\text{C}$ ,  $V_{BAT} = 13.5\text{V}$



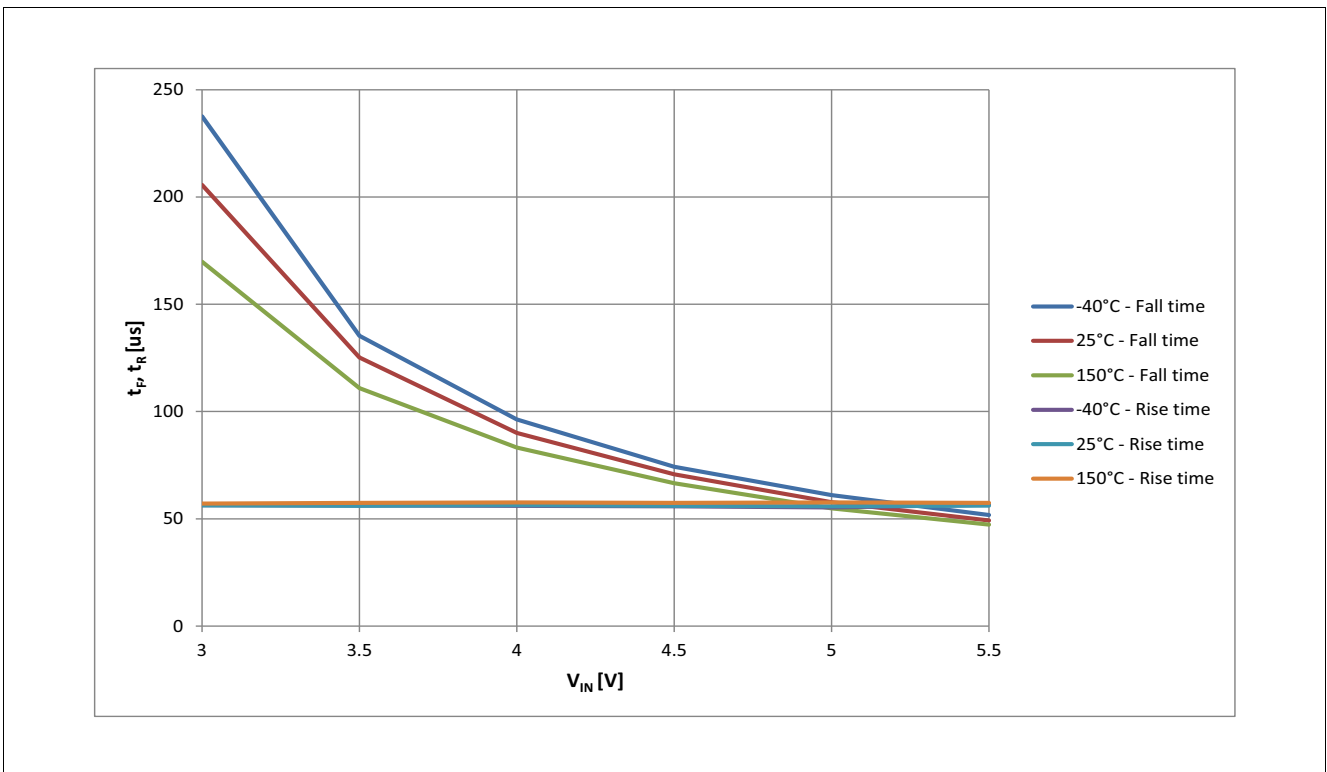
**Figure 23** Typical  $E_{AR}$  vs.  $I_L$  @  $T_J = 25$  and  $105^\circ\text{C}$ ,  $V_{BAT} = 13.5\text{V}$

**Characterization Results**



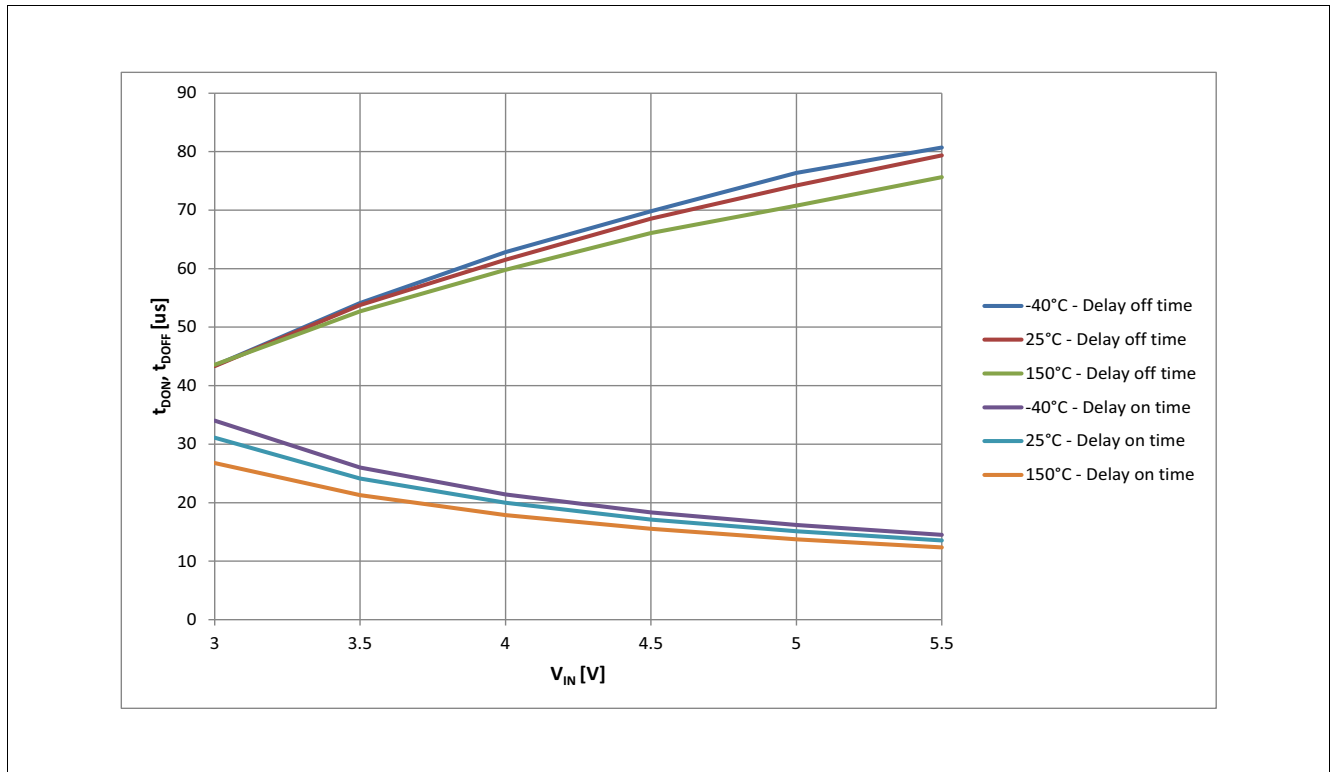
**Figure 24** Typical  $E_{AR}$  vs. Cycles @  $T_J = 25$  and  $105^\circ\text{C}$ ,  $V_{BAT} = 13.5\text{V}$

**Dynamic characteristics (switching times):**

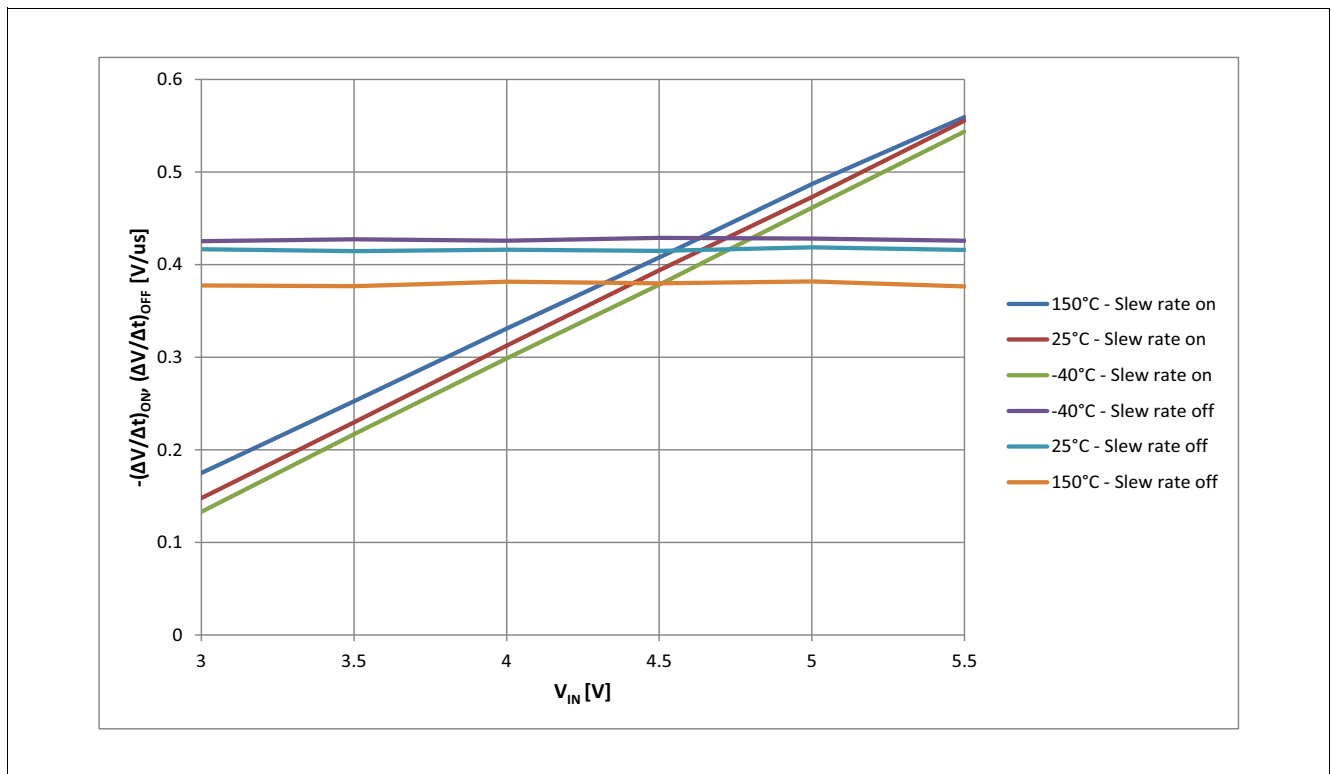


**Figure 25** Typical  $t_F$ ,  $t_R$  vs.  $V_{IN}$  @  $T_J = -40 \dots 150^\circ\text{C}$

**Characterization Results**

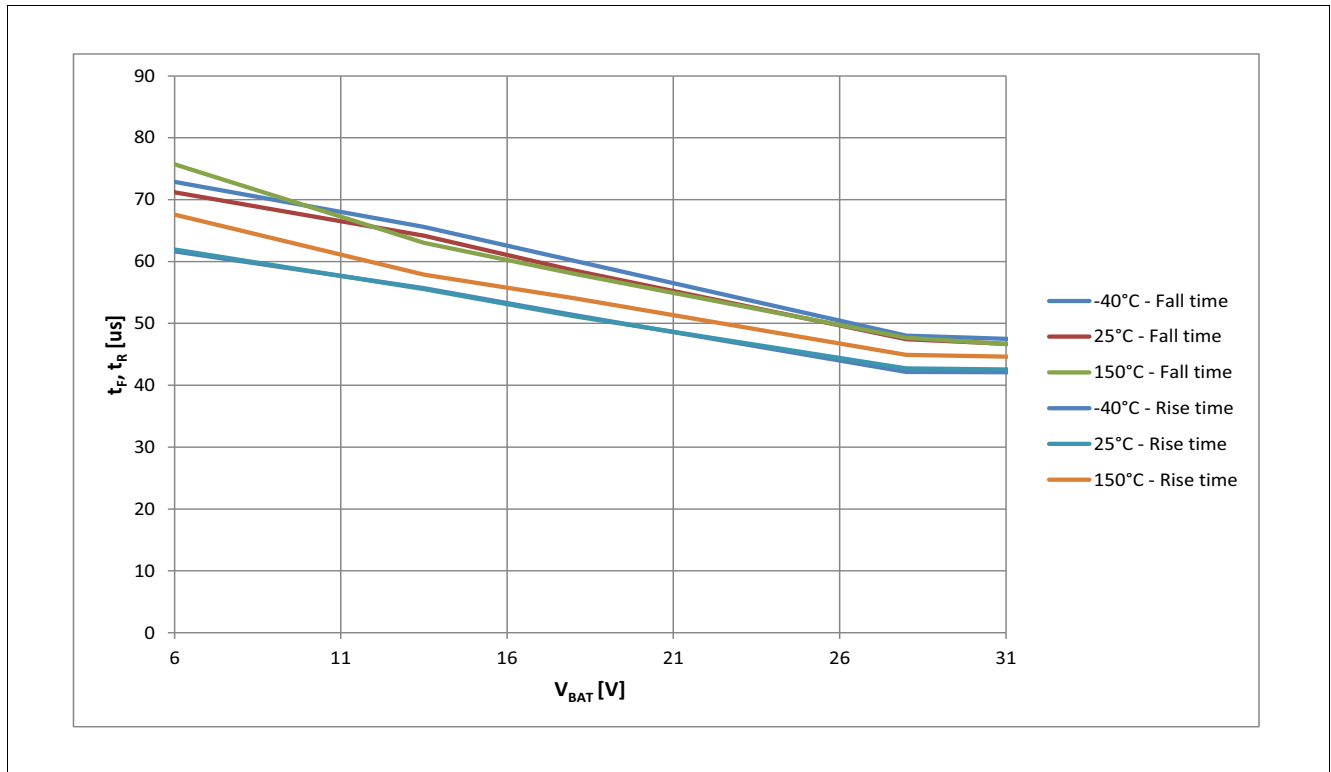


**Figure 26** Typical  $t_{DON}$ ,  $t_{DOFF}$  vs.  $V_{IN}$  @  $T_J = -40 \dots 150^\circ\text{C}$

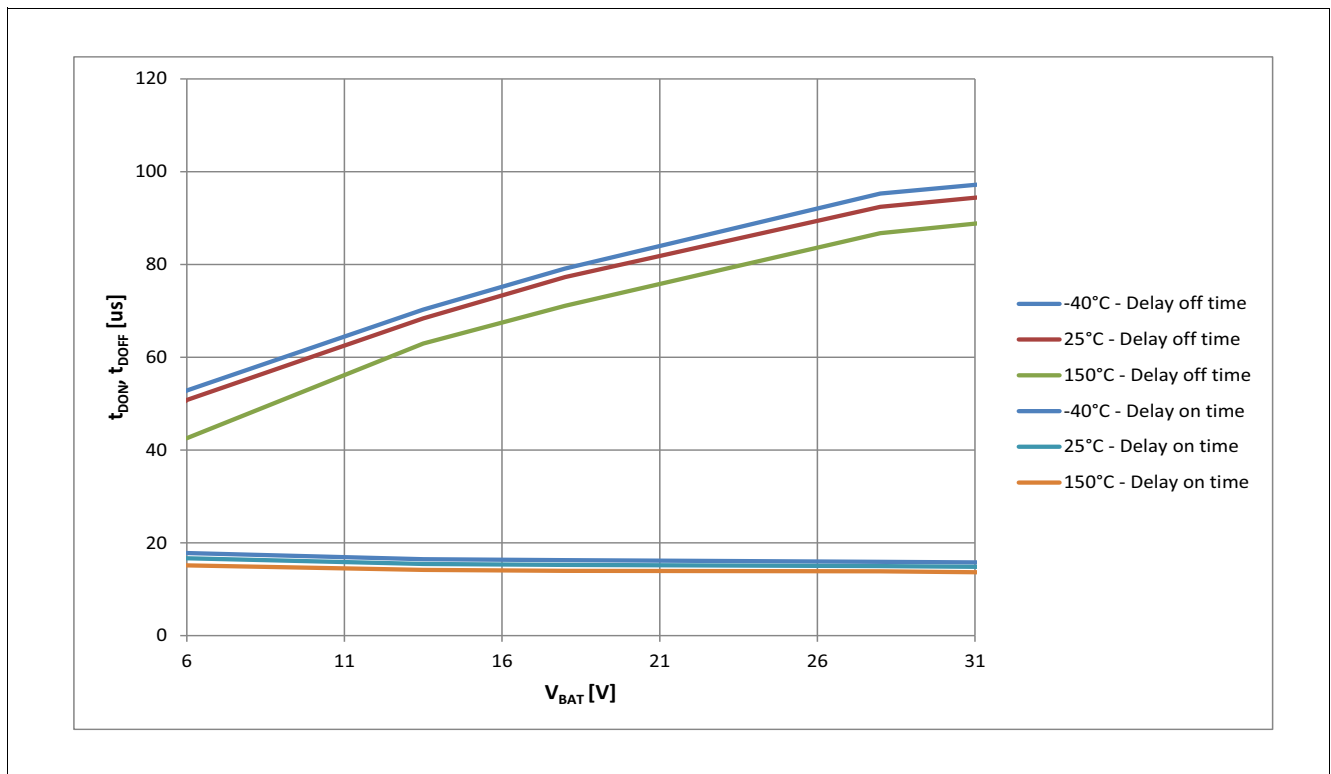


**Figure 27** Typical  $-(\Delta V/\Delta t)_{ON}$ ,  $(\Delta V/\Delta t)_{OFF}$  vs.  $V_{IN}$  @  $T_J = -40 \dots 150^\circ\text{C}$

**Characterization Results**

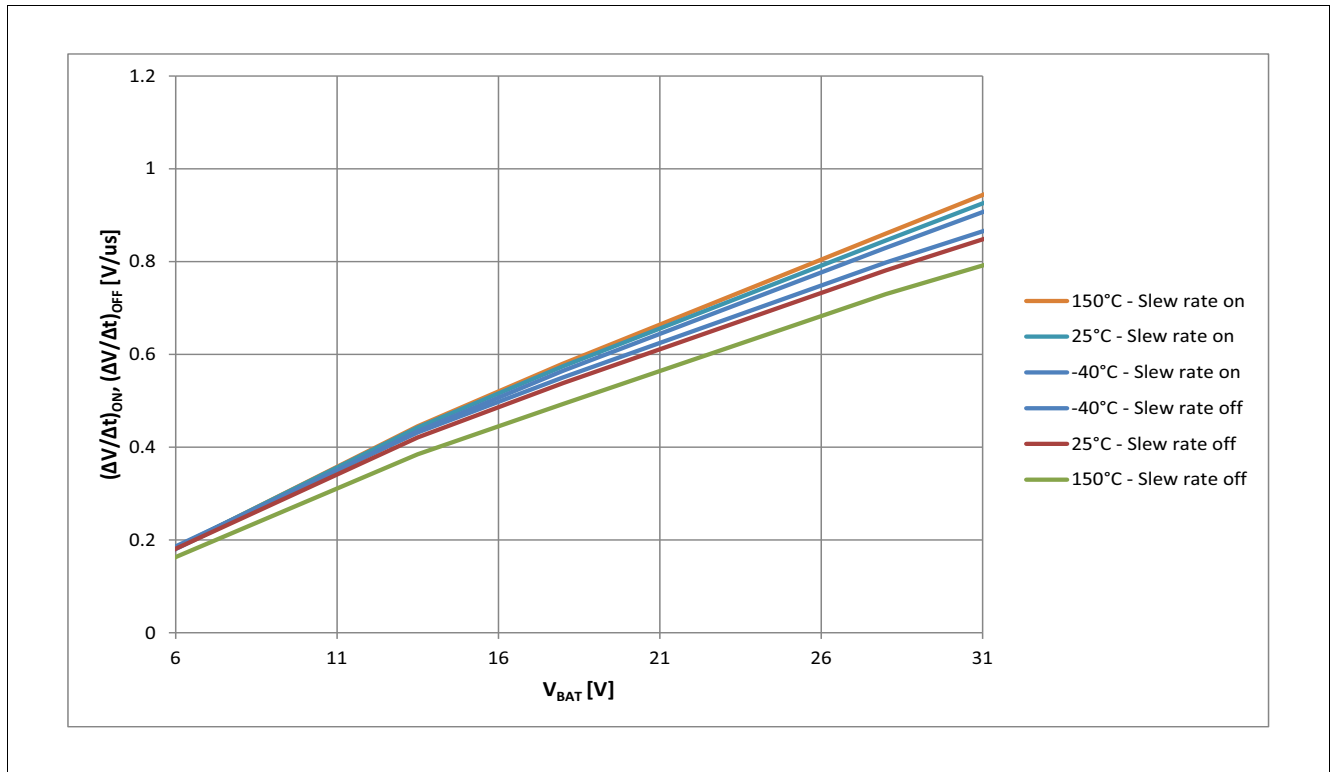


**Figure 28** Typical  $t_F$ ,  $t_R$  vs.  $V_{BAT}$  @  $V_{IN} = 5V$ ;  $T_J = -40 \dots 150^\circ C$

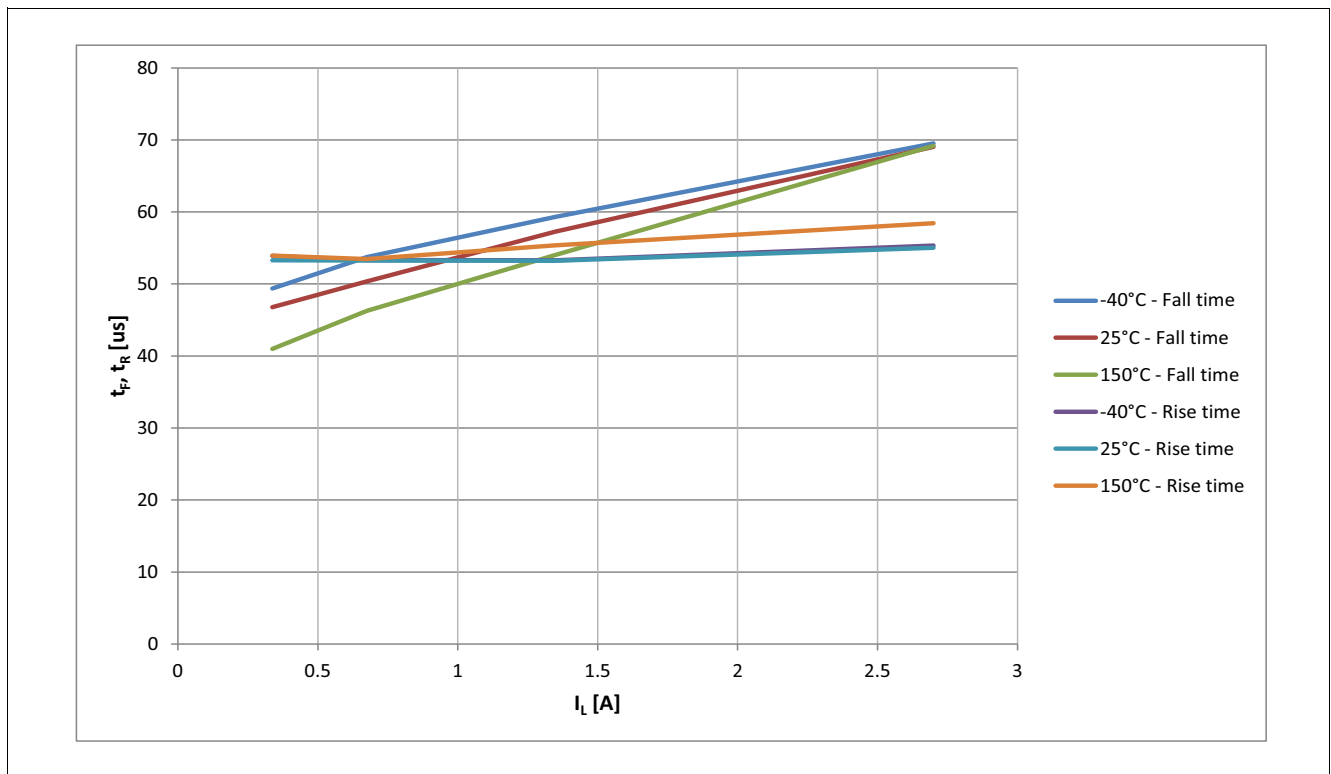


**Figure 29** Typical  $t_{DON}$ ,  $t_{DOFF}$  vs.  $V_{BAT}$  @  $V_{IN} = 5V$ ;  $T_J = -40 \dots 150^\circ C$

**Characterization Results**

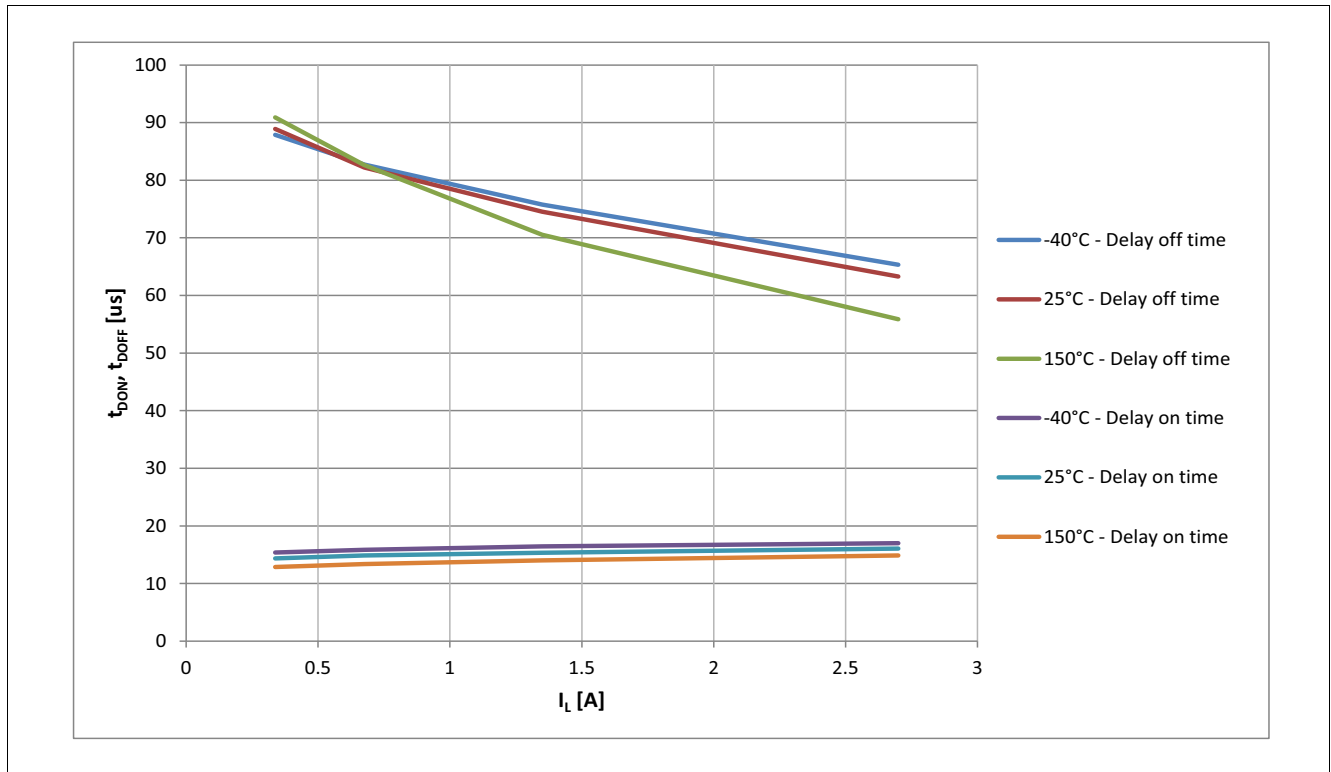


**Figure 30** Typical  $-(\Delta V/\Delta t)_{ON}$ ,  $(\Delta V/\Delta t)_{OFF}$  vs.  $V_{BAT}$  @  $V_{IN} = 5V$ ;  $T_J = -40 \dots 150^\circ C$

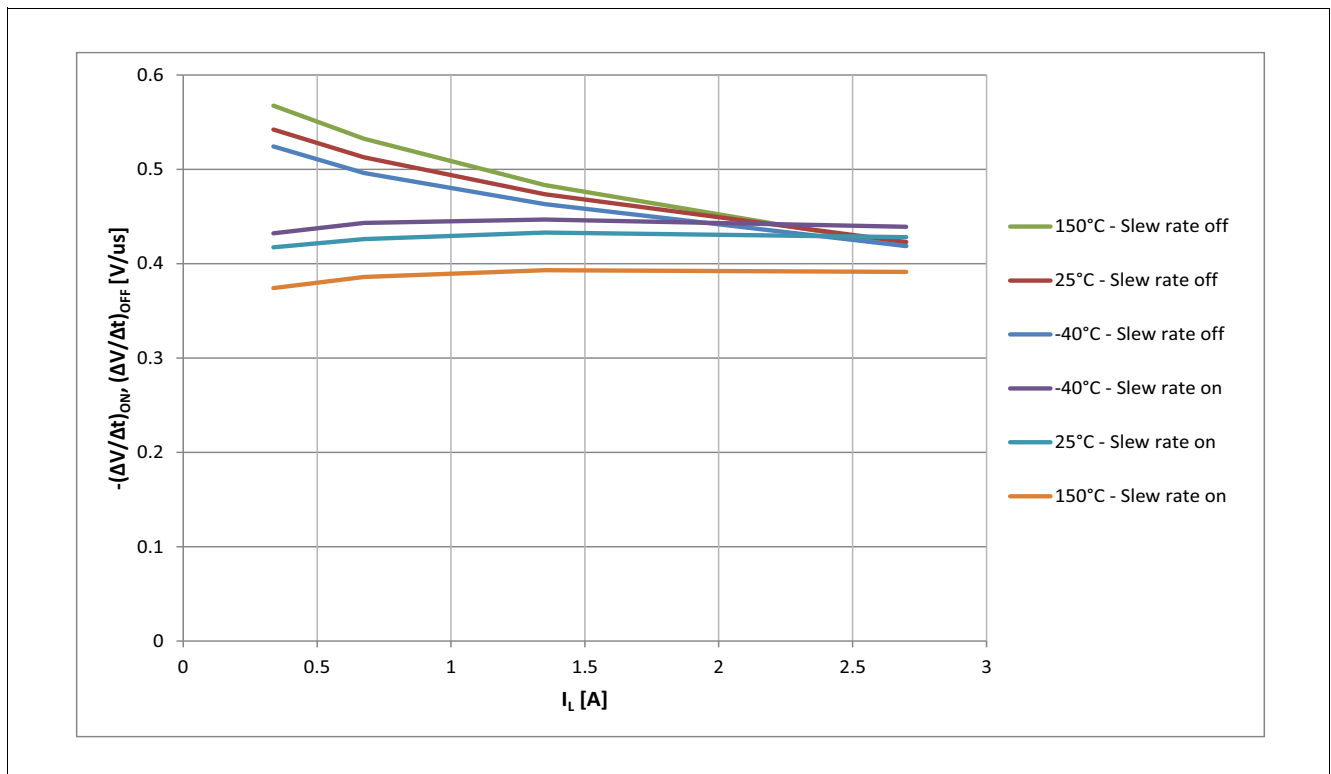


**Figure 31** Typical  $t_F$ ,  $t_R$  vs.  $I_L$  @  $V_{IN} = 5V$ ;  $T_J = -40 \dots 150^\circ C$

**Characterization Results**

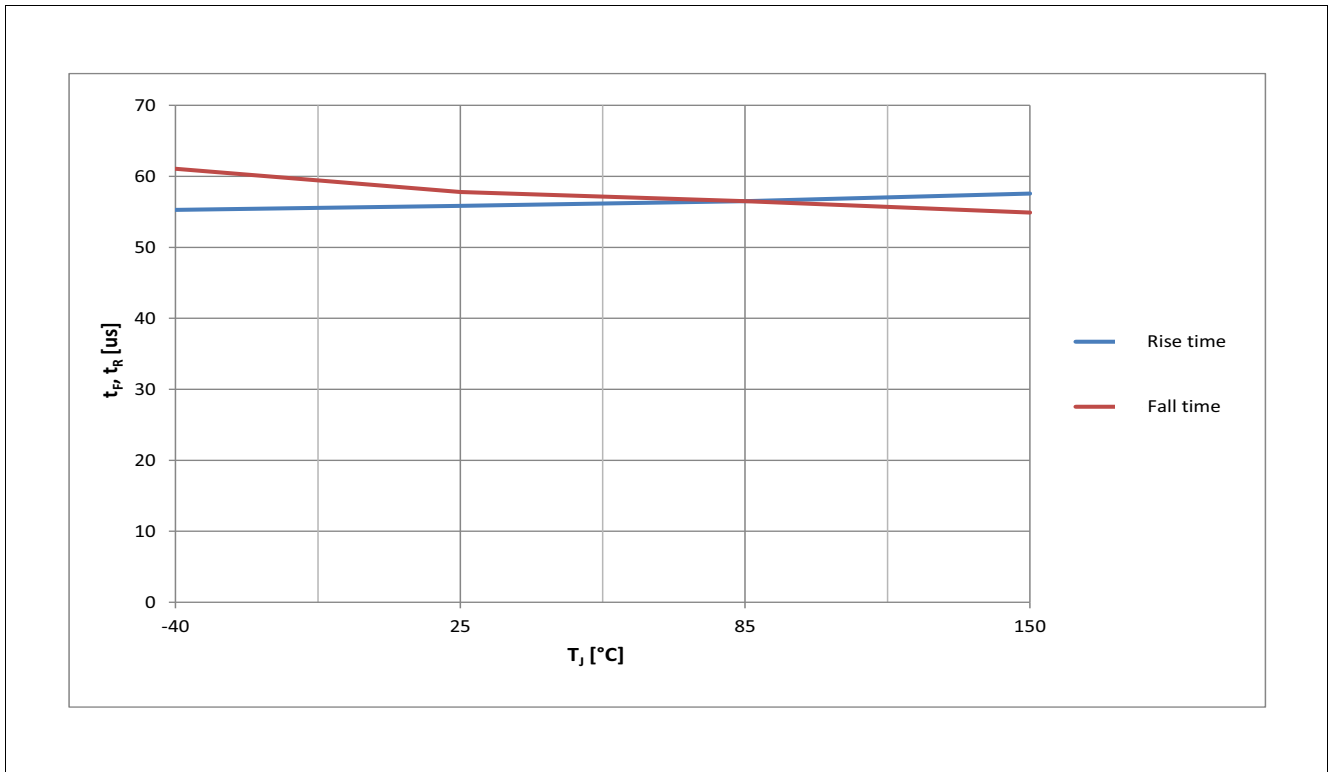


**Figure 32** Typical  $t_{DON}$ ,  $t_{DOFF}$  vs.  $I_L$  @  $V_{IN} = 5V$ ;  $T_J = -40 \dots 150^\circ C$

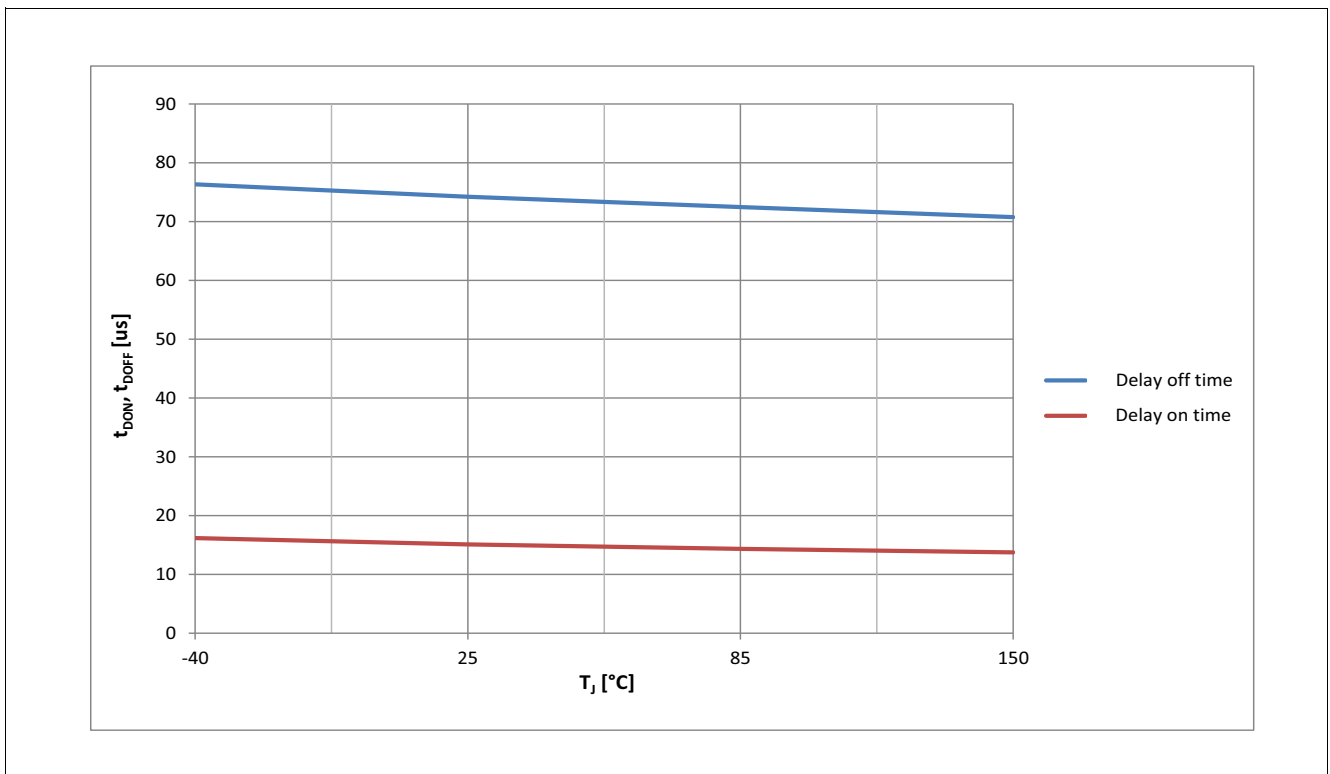


**Figure 33** Typical  $-(\Delta V/\Delta t)_{ON}$ ,  $(\Delta V/\Delta t)_{OFF}$  vs.  $I_L$  @  $V_{IN} = 5V$ ;  $T_J = -40 \dots 150^\circ C$

**Characterization Results**



**Figure 34** Typical  $t_F$ ,  $t_R$  vs.  $T_J$  @  $V_{IN} = 5\text{ V}$



**Figure 35** Typical  $t_{DON}$ ,  $t_{DOFF}$  vs.  $T_J$  @  $V_{IN} = 5\text{ V}$

Characterization Results

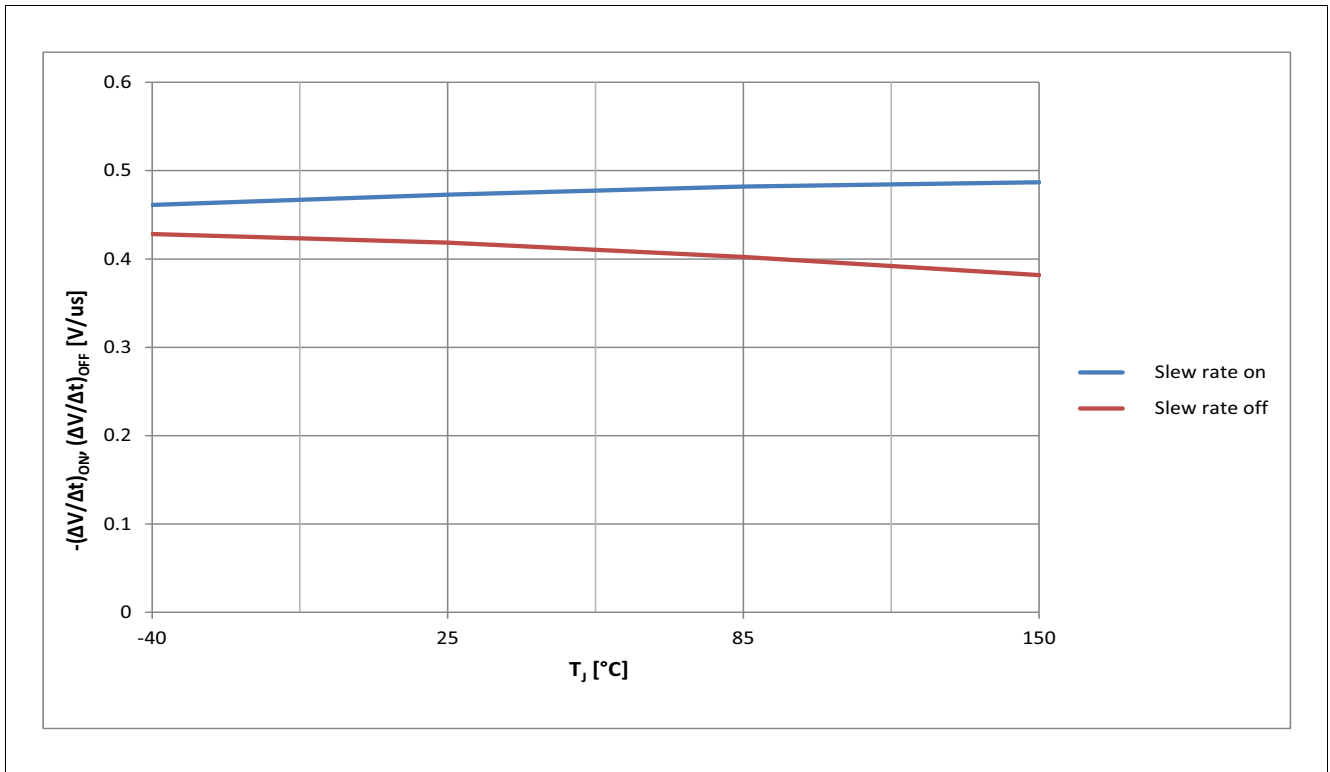


Figure 36 Typical  $-(\Delta V/\Delta t)_{ON}$ ,  $(\Delta V/\Delta t)_{OFF}$  vs.  $T_J$  @  $V_{IN} = 5 V$



Characterization Results

9.2 Protection

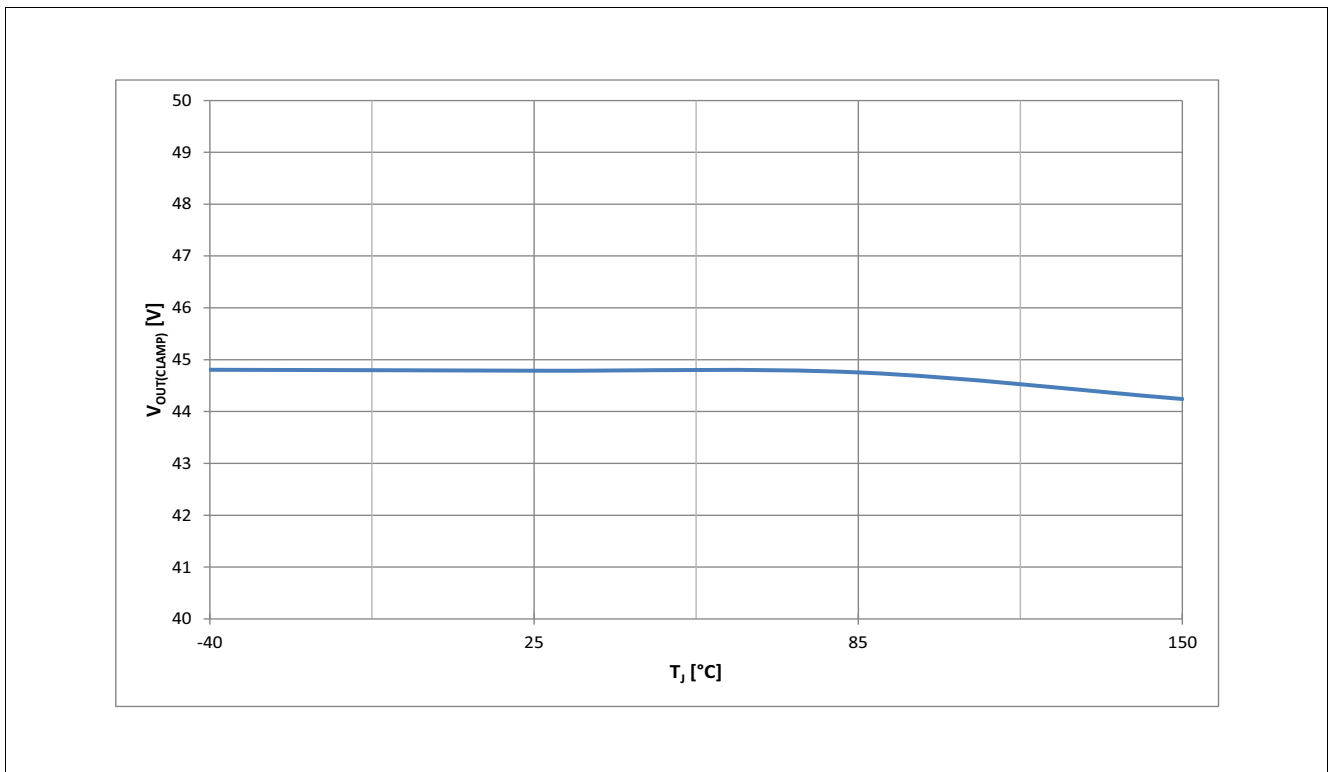


Figure 37 Typical  $V_{OUT(CLAMP)}$  vs.  $T_J$  @  $I_L = 4$  mA

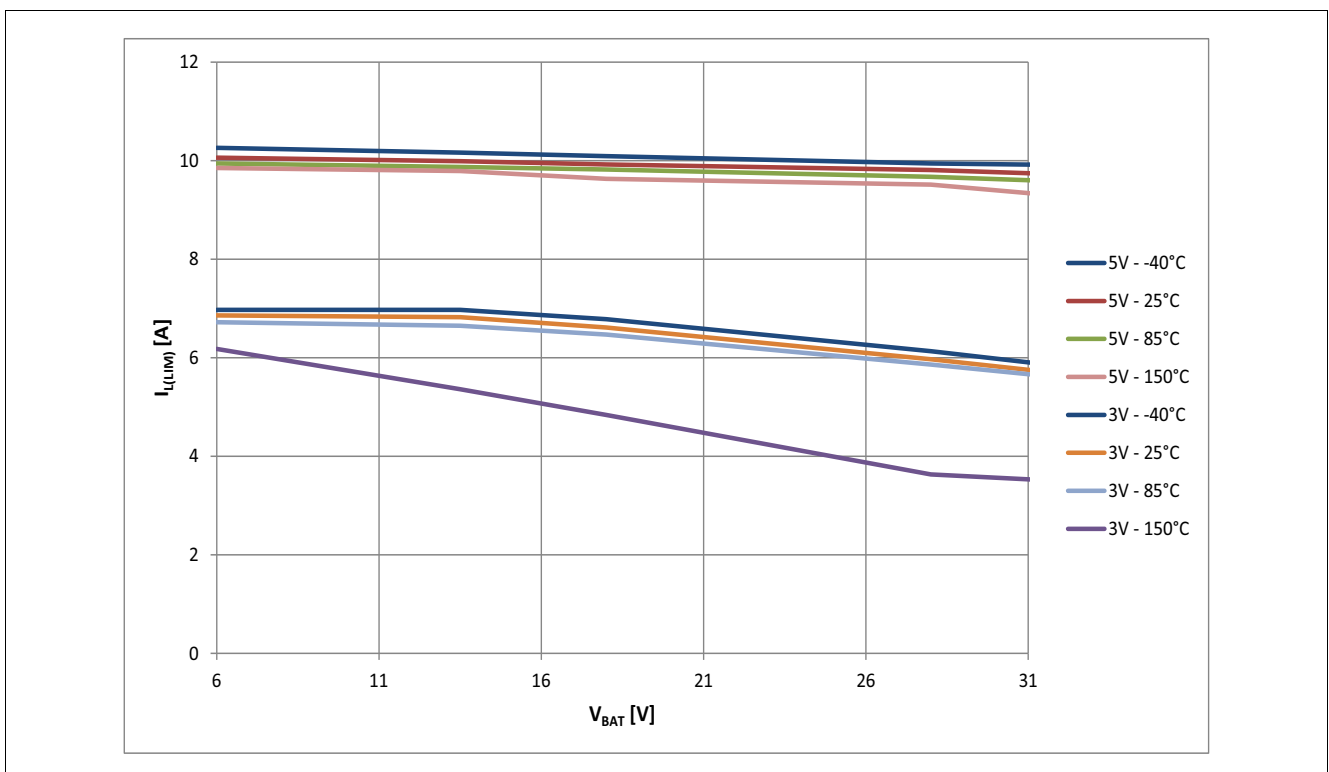
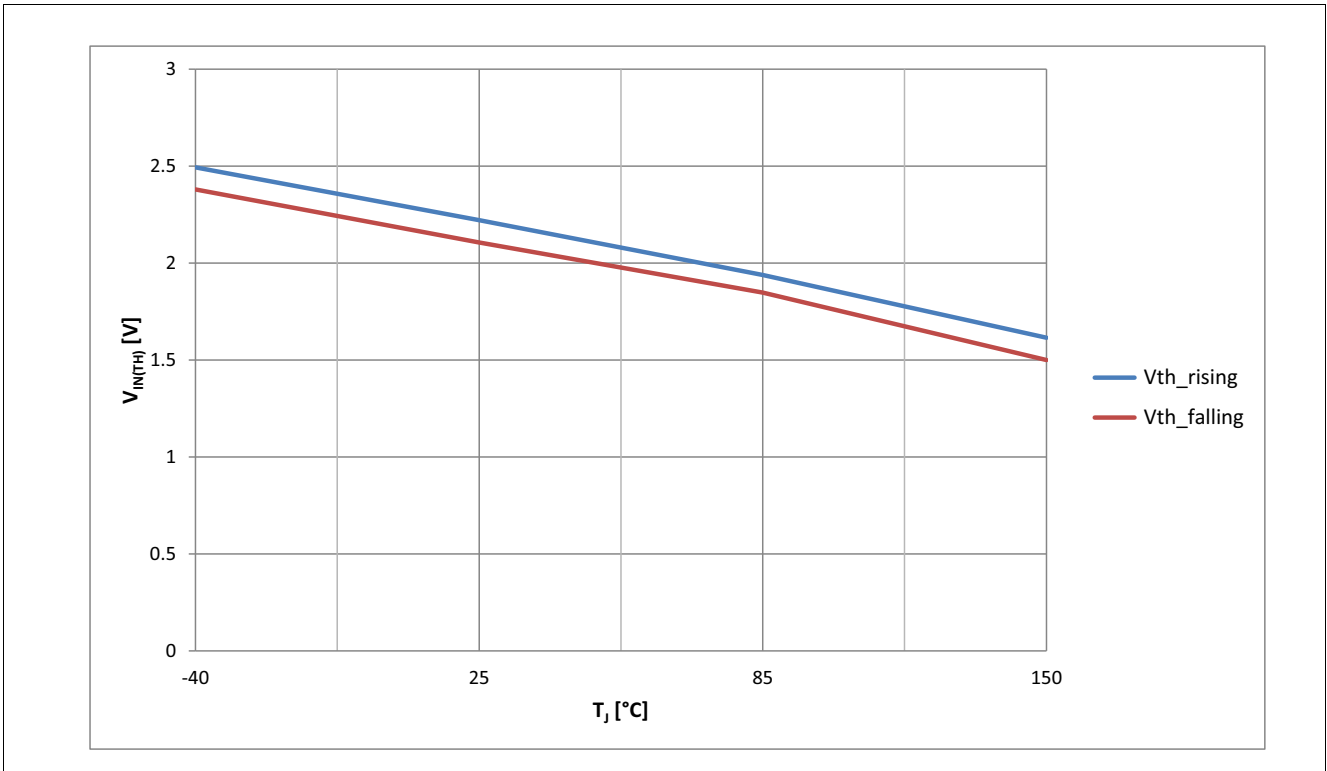


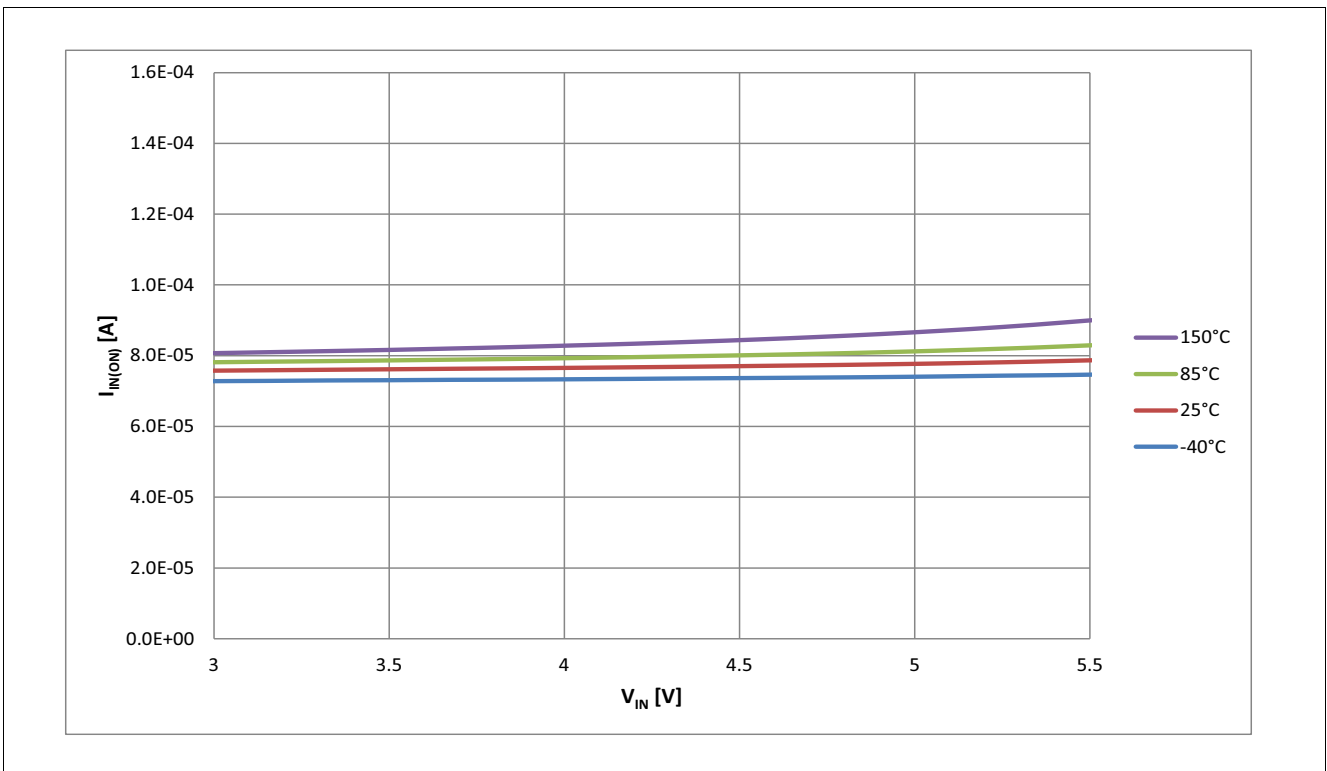
Figure 38 Typical  $I_{L(LIM)}$  vs.  $V_{BAT}$  @  $T_J = -40 \dots 150^\circ\text{C}$ ,  $V_{IN} = 3$  V and 5 V

**Characterization Results**

**9.3 Input Stage**



**Figure 39** Typical  $V_{IN(TH)}$  vs.  $T_J$  @  $I_L = 0.4$  mA



**Figure 40** Typical  $I_{IN(ON)}$  vs.  $V_{IN}$  @  $T_J = -40 \dots 150^\circ\text{C}$ ,  $I_L = I_{L(NOM)}$

Characterization Results

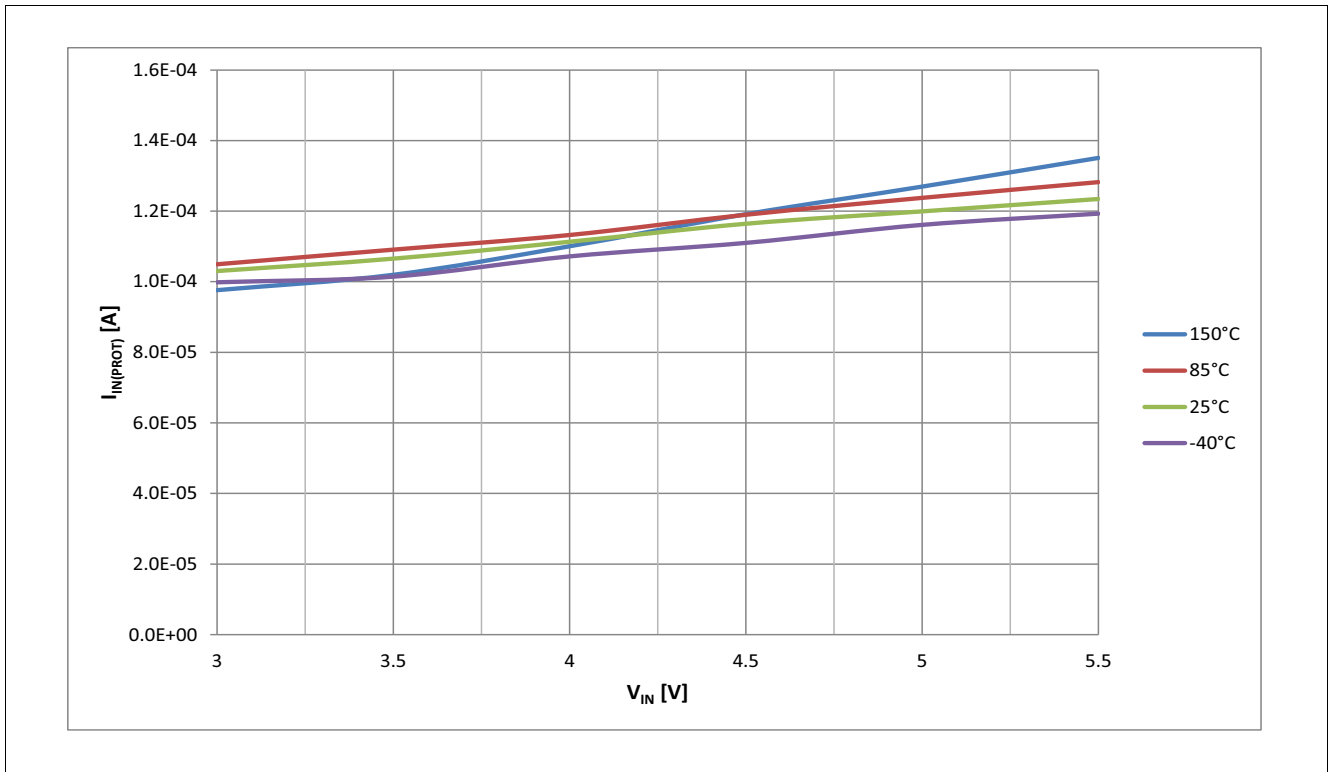


Figure 41 Typical  $I_{IN(PROT)}$  vs.  $V_{IN}$  @  $T_J = -40 \dots 150^\circ\text{C}$ ,  $I_L = I_{L(NOM)}$

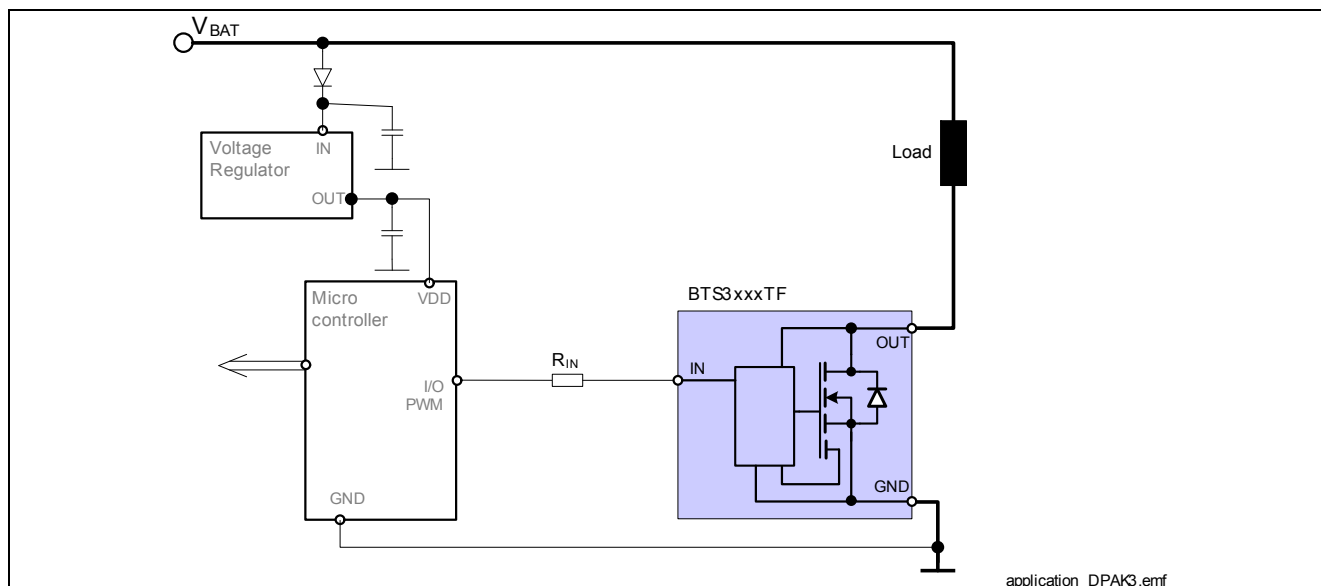
**Application Information**

**10 Application Information**

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

**10.1 Application Diagram**

An application example with the BTS3125TF is shown below.



**Figure 42 Application example circuitry**

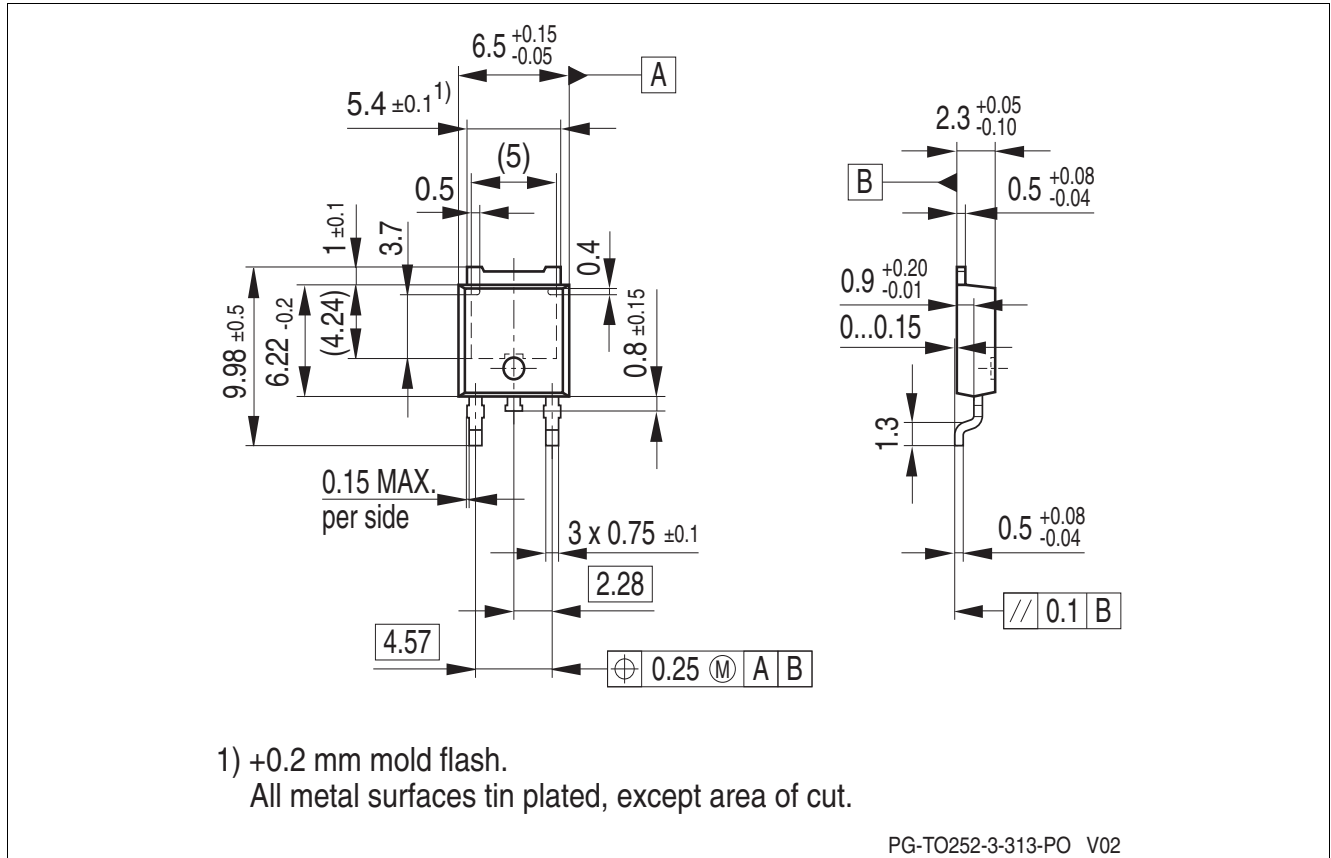
Recommended values:

$R_{IN} = 3.3 \text{ k}\Omega$  ( $V_{IN} = 5 \text{ V}$ )

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*

**Package Outlines**

**11 Package Outlines**



**Figure 43 PG-T0252-3-313 (Outline Package)**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Revision History**

## **12 Revision History**

| <b>Revision</b> | <b>Date</b> | <b>Changes</b>     |
|-----------------|-------------|--------------------|
| Rev. 1.0        | 2016-06-01  | Datasheet released |

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