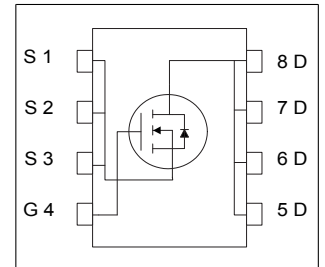
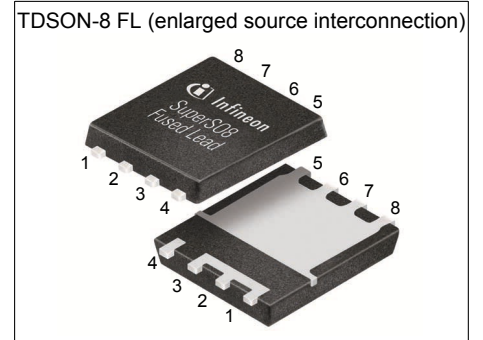


# MOSFET

## OptiMOS™ Power-MOSFET, 60 V

### Features

- Optimized for synchronous rectification
- 175 °C rated
- 100% avalanche tested
- Superior thermal resistance
- N-channel
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Higher solder joint reliability due to enlarged source interconnection



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	60	V
$R_{DS(on),max}$	1.6	mΩ
$I_D$	100	A
$Q_{oss}$	81	nC
$Q_G(0V..10V)$	71	nC

Type / Ordering Code	Package	Marking	Related Links
BSC016N06NST	TDSON-8 FL	016N06NT	-

<sup>1)</sup> J-STD20 and JESD22

## Table of Contents

Description .....	1
Maximum ratings .....	3
Thermal characteristics .....	3
Electrical characteristics .....	4
Electrical characteristics diagrams .....	6
Package Outlines .....	10
Revision History .....	13
Trademarks .....	13
Disclaimer .....	13

## 1 Maximum ratings

at  $T_j=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	100	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}^{(1)}$
Pulsed drain current <sup>(2)</sup>	$I_{D,pulse}$	-	-	400	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>(3)</sup>	$E_{AS}$	-	-	380	mJ	$I_D=50\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	167 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$ , $R_{thJA}=50\text{ K/W}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	175	°C	-

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	$R_{thJC}$	-	0.5	0.9	K/W	-
Thermal resistance, junction - case, top	$R_{thJC}$	-	-	20	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>(1)</sup>	$R_{thJA}$	-	-	50	K/W	-

<sup>1)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>2)</sup> See Diagram 3 for more detailed information

<sup>3)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	$V_{DS}=V_{GS}$ , $I_D=95\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.5 10	1 100	$\mu\text{A}$	$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	1.4 1.9	1.6 2.4	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=50\text{ A}$ $V_{GS}=6\text{ V}$ , $I_D=12.5\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	1.9	2.9	$\Omega$	-
Transconductance	$g_{fs}$	70	140	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=50\text{ A}$

**Table 5 Dynamic characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	3900	5200	6500	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	900	1200	1500	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	14	48	96	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	19	38	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	9	18	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	35	70	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	9	18	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge <sup>1)</sup>	$Q_{gs}$	16	22	30	nC	$V_{DD}=30\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold <sup>1)</sup>	$Q_{g(th)}$	10	14	19	nC	$V_{DD}=30\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	8.8	13	20	nC	$V_{DD}=30\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Switching charge <sup>1)</sup>	$Q_{sw}$	14	21	30	nC	$V_{DD}=30\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	58	71	95	nC	$V_{DD}=30\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage <sup>1)</sup>	$V_{plateau}$	3.7	4.3	4.9	V	$V_{DD}=30\text{ V}$ , $I_D=50\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET <sup>1)</sup>	$Q_{g(sync)}$	49	62	86	nC	$V_{DS}=0.1\text{ V}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	60	81	102	nC	$V_{DD}=30\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	100	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	400	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.9	1.2	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	24	61	98	ns	$V_R=30\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	39	78	156	nC	$V_R=30\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test

### 4 Electrical characteristics diagrams

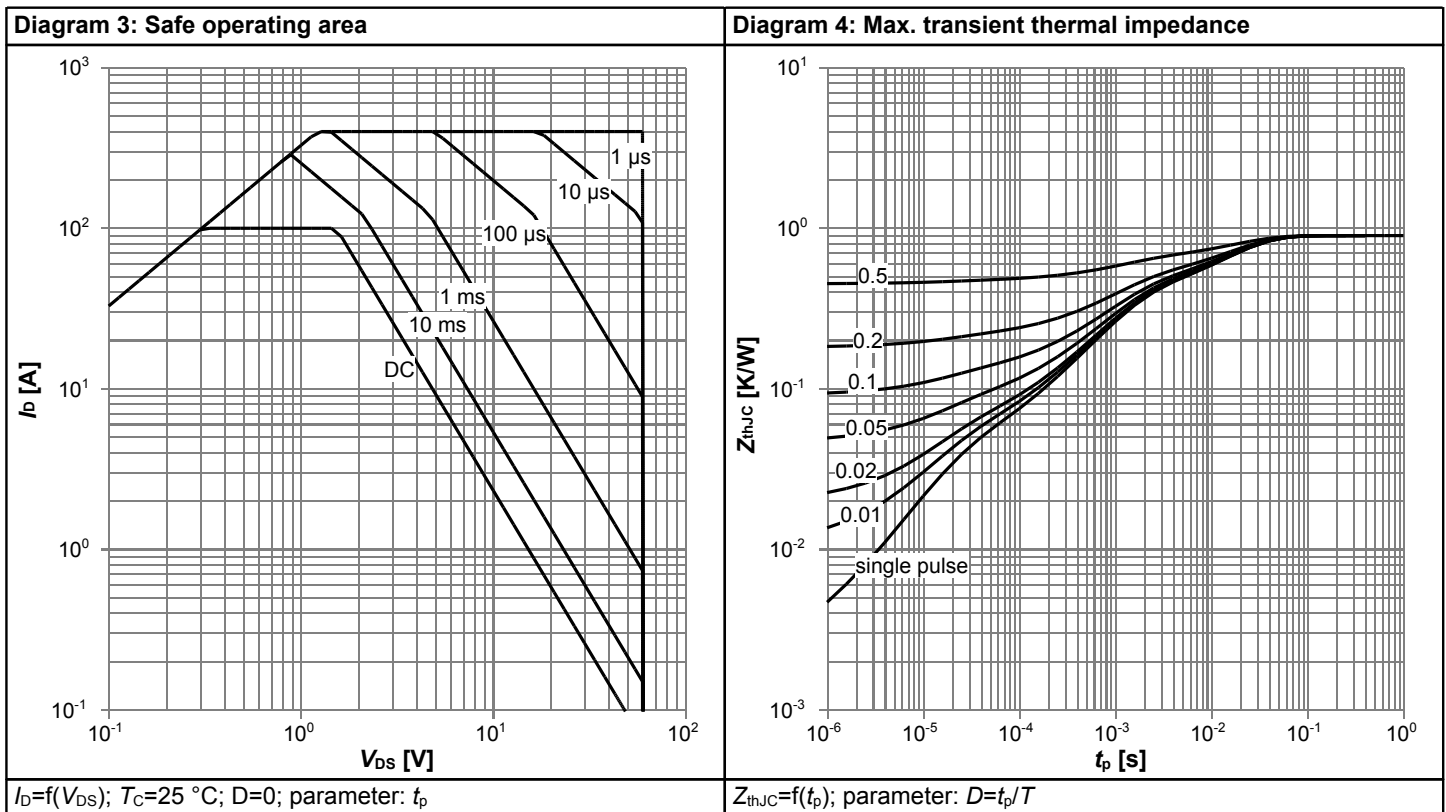
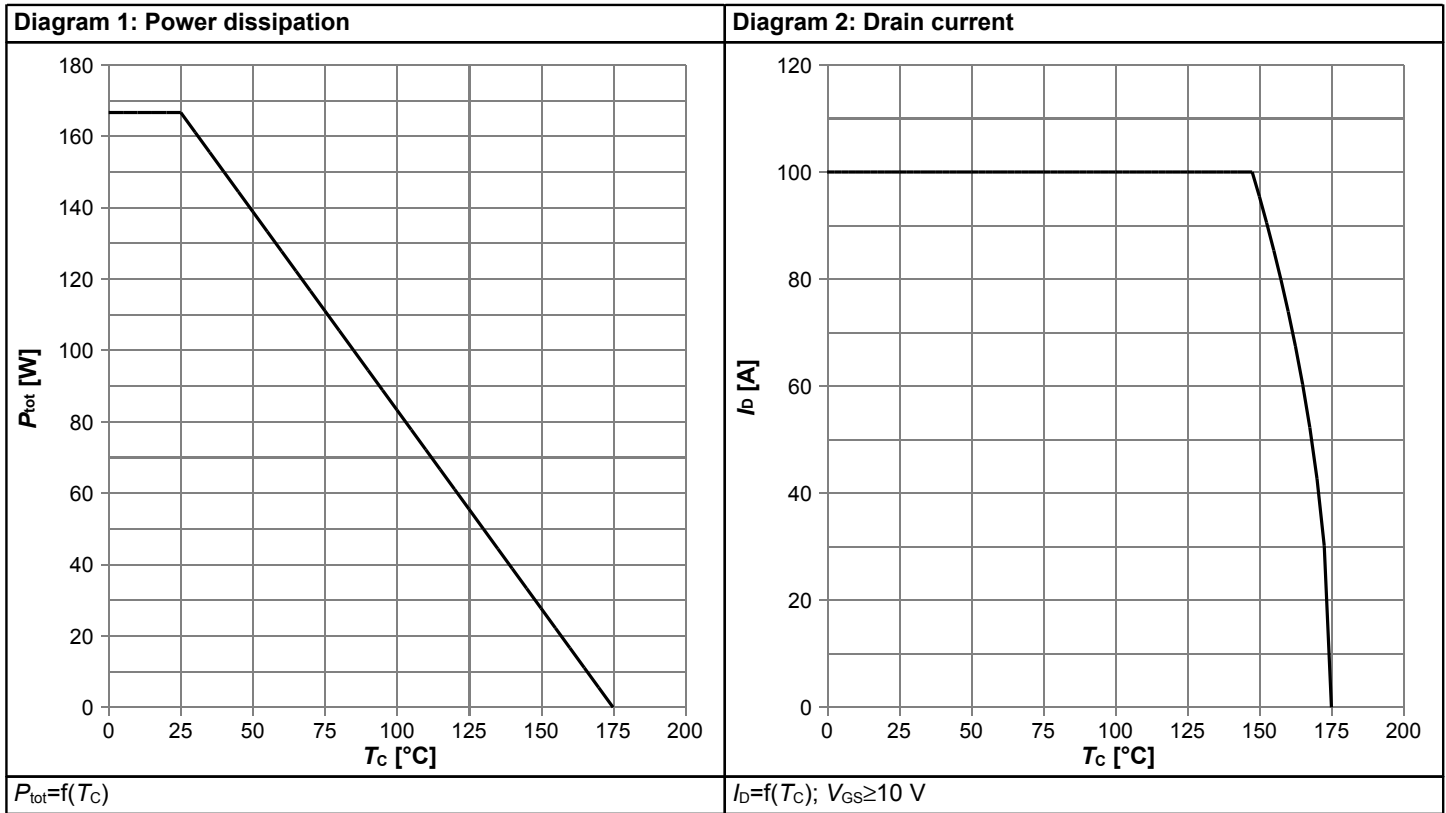
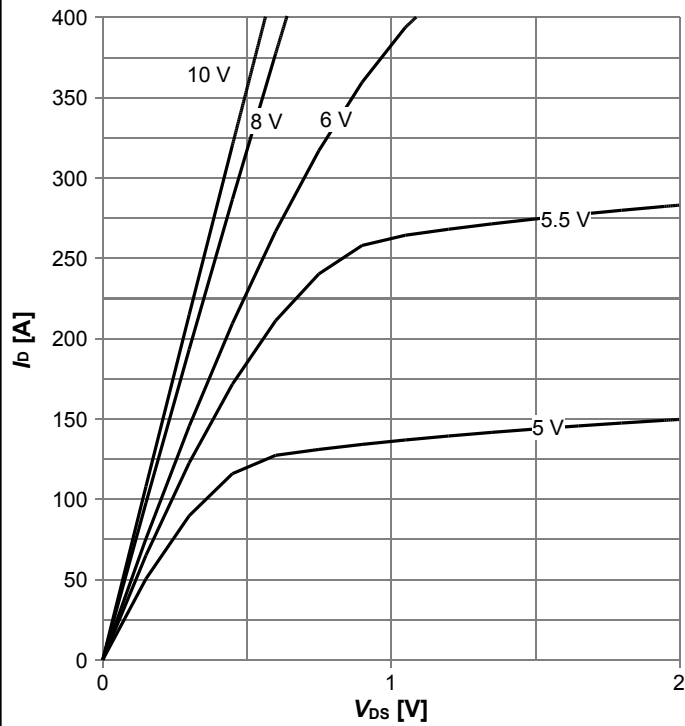
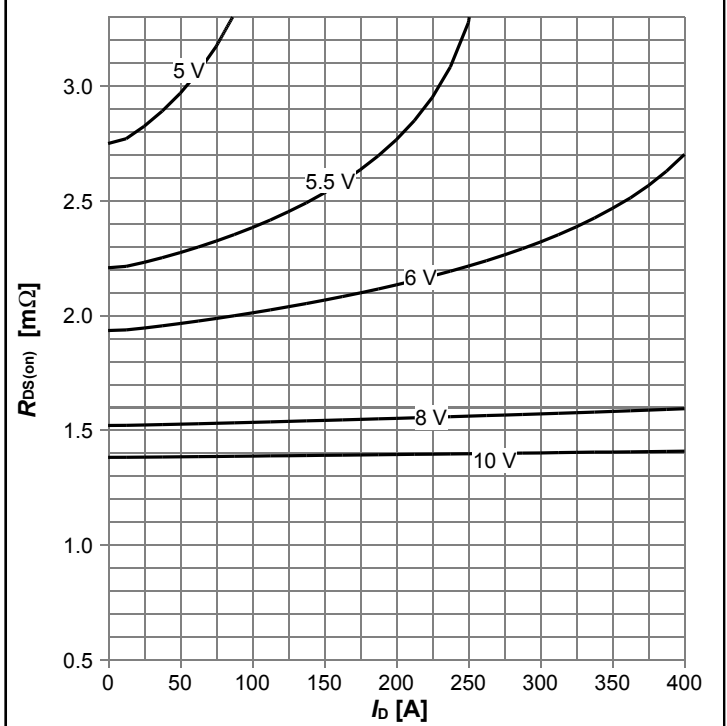


Diagram 5: Typ. output characteristics



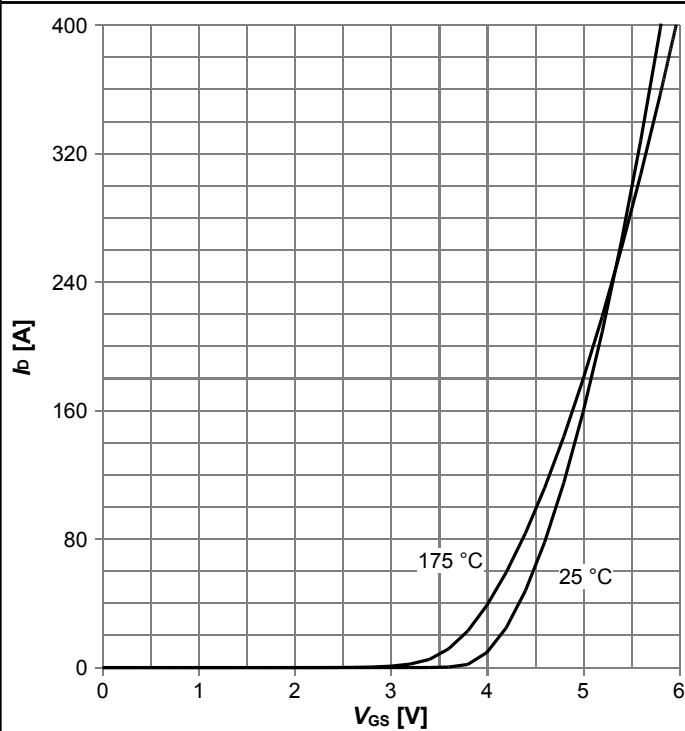
$I_D=f(V_{DS}); T_j=25\text{ °C};$  parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



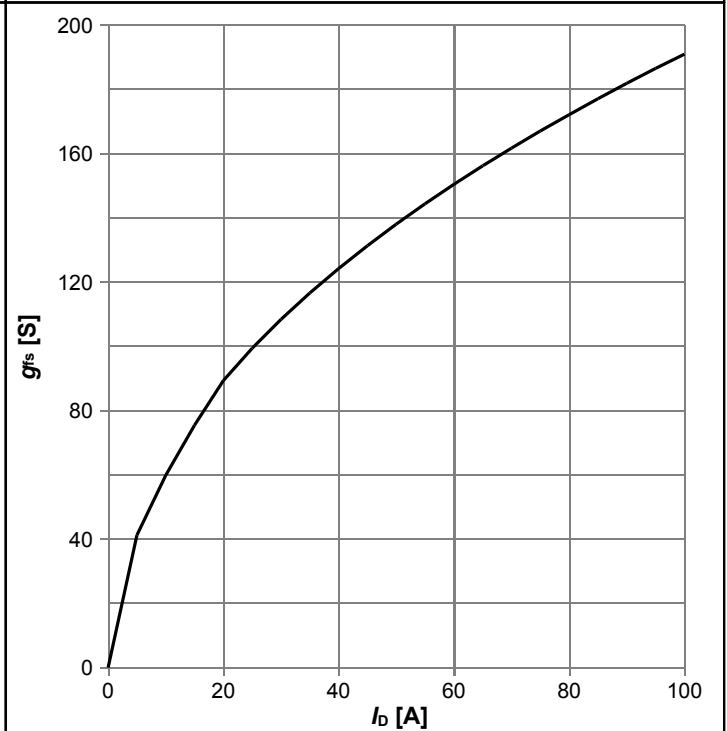
$R_{DS(on)}=f(I_D); T_j=25\text{ °C};$  parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



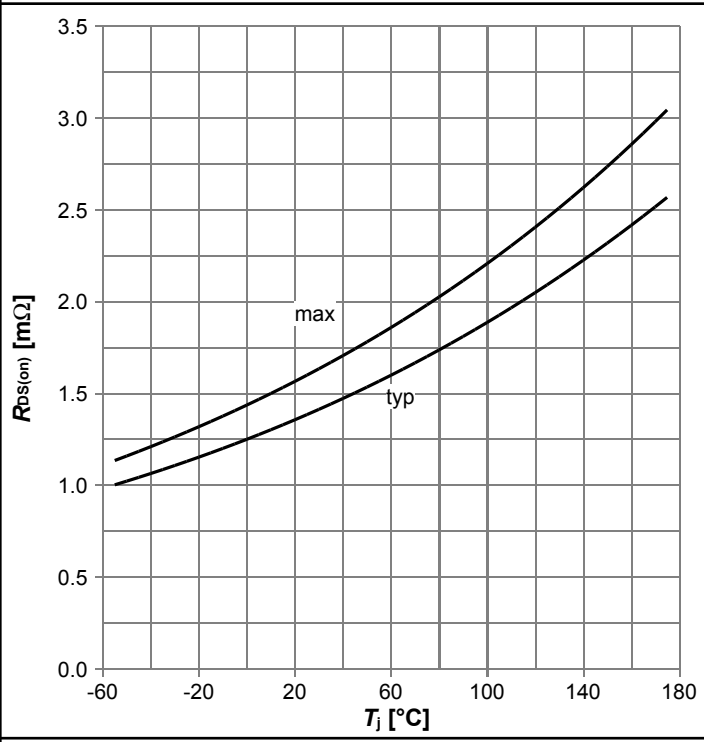
$I_D=f(V_{GS}); |V_{DS}|>2|I_D|R_{DS(on)max};$  parameter:  $T_j$

Diagram 8: Typ. forward transconductance



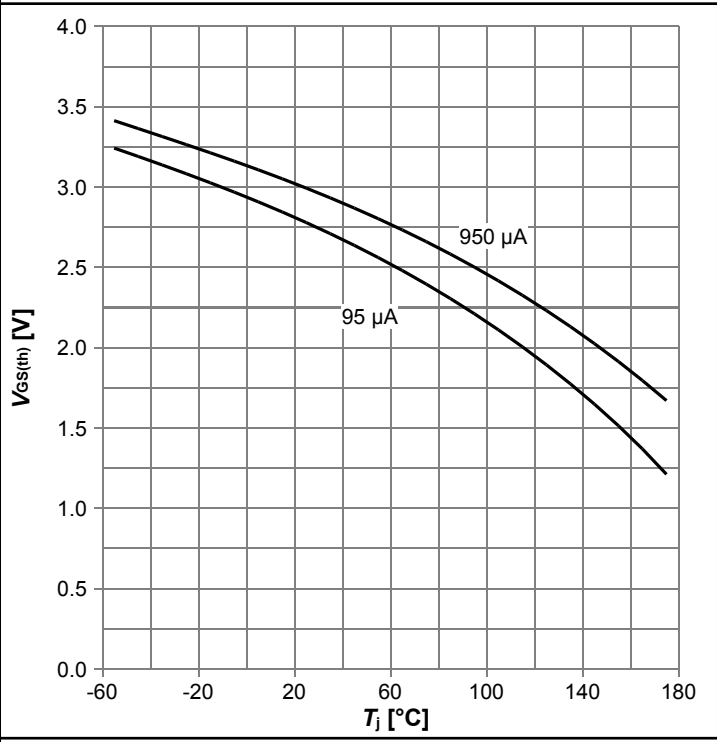
$g_{fs}=f(I_D); T_j=25\text{ °C}$

Diagram 9: Drain-source on-state resistance



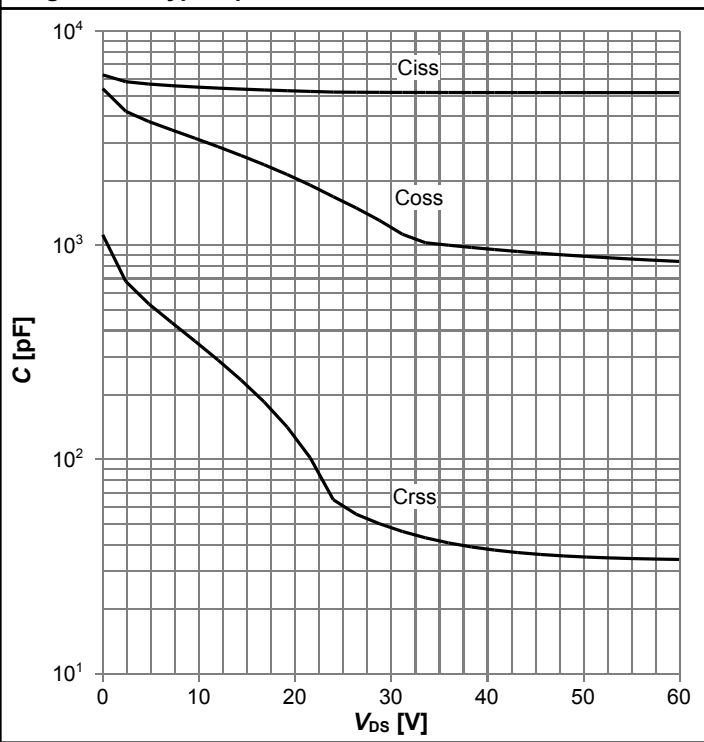
$R_{DS(on)}=f(T_j)$ ;  $I_D=50\text{ A}$ ;  $V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



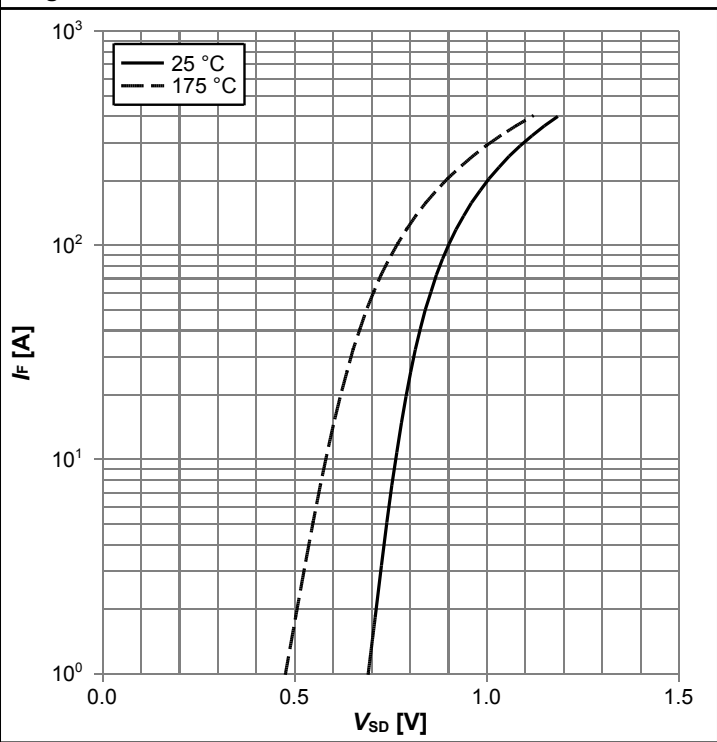
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0\text{ V}$ ;  $f=1\text{ MHz}$

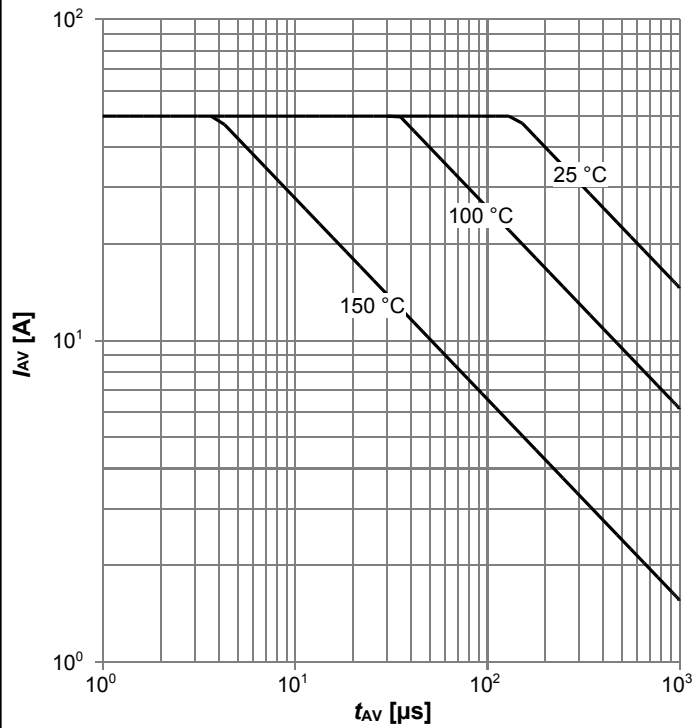
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

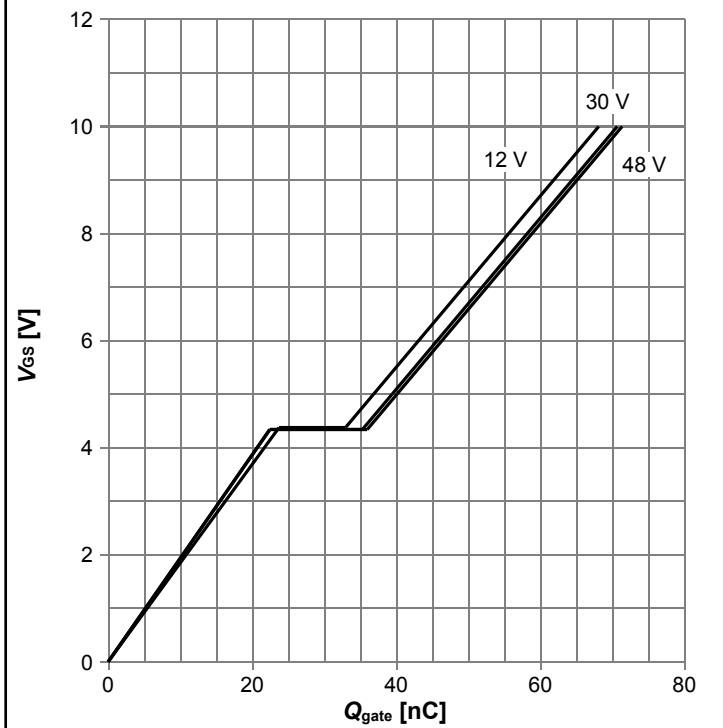


Diagram 13: Avalanche characteristics



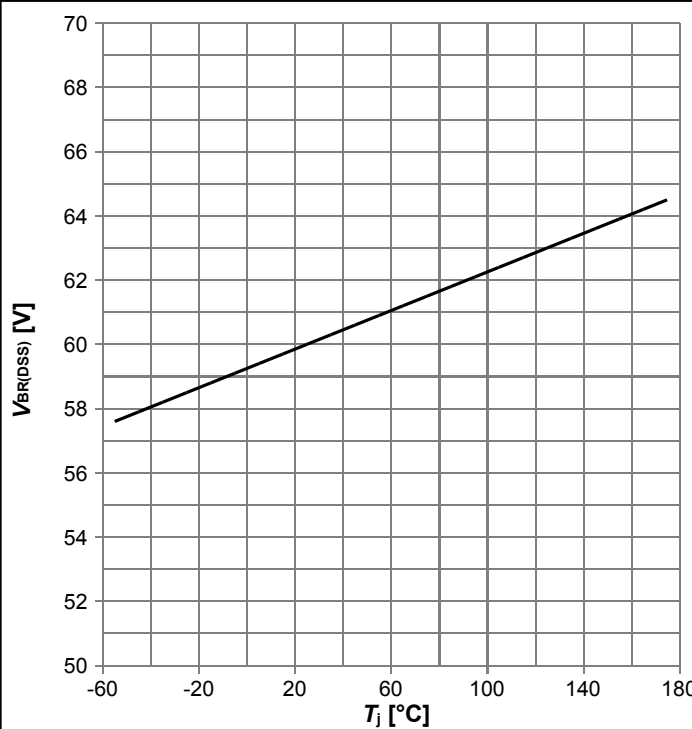
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j(start)}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate}); I_D=50$  A pulsed; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage

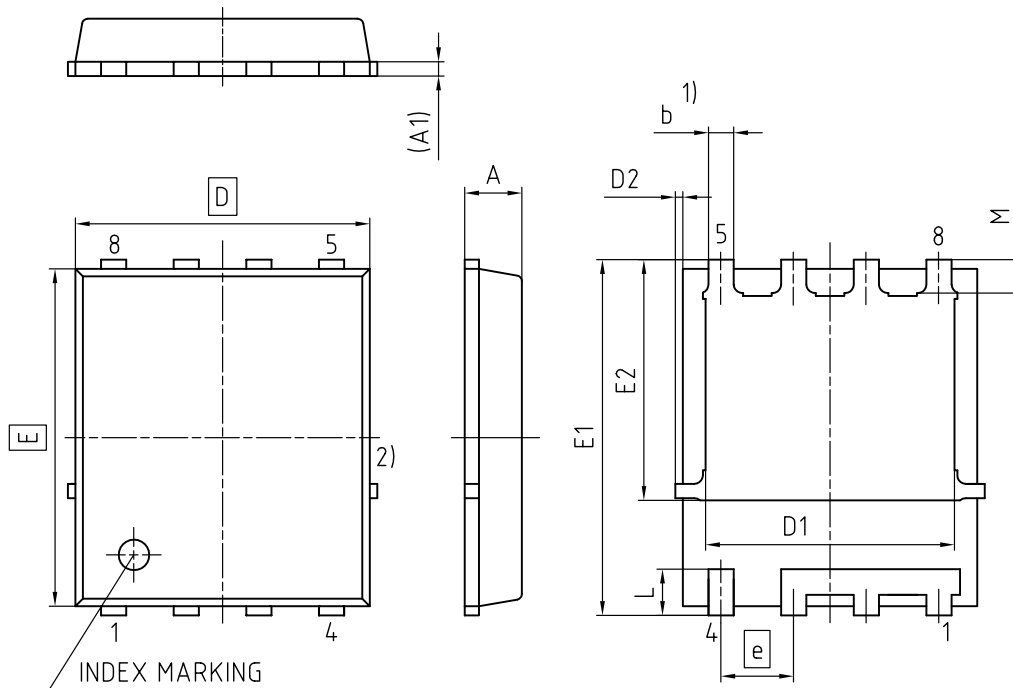


$V_{BR(DSS)}=f(T_j); I_D=1$  mA

Diagram Gate charge waveforms



## 5 Package Outlines



1) EXCLUDING MOLD FLASH  
 2) REMOVAL ON MOLD GATE  
 INTRUSION 0.1 MM  
 PROTRUSION 0.1 MM  
 LEAD LENGTH UP TO ANTI FLASH LINE  
 ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

DIMENSION	MILLIMETERS	
	MIN.	MAX.
A	0.90	1.20
A1	0.15	0.35
b	0.26	0.54
D	4.80	5.35
D1	3.70	4.40
D2	0.02	0.23
E	5.70	6.10
E1	5.90	6.42
E2	3.88	4.42
e	1.27	
L	0.69	0.90
M	0.45	0.69

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Figure 1 Outline TDSON-8 FL, dimensions in mm

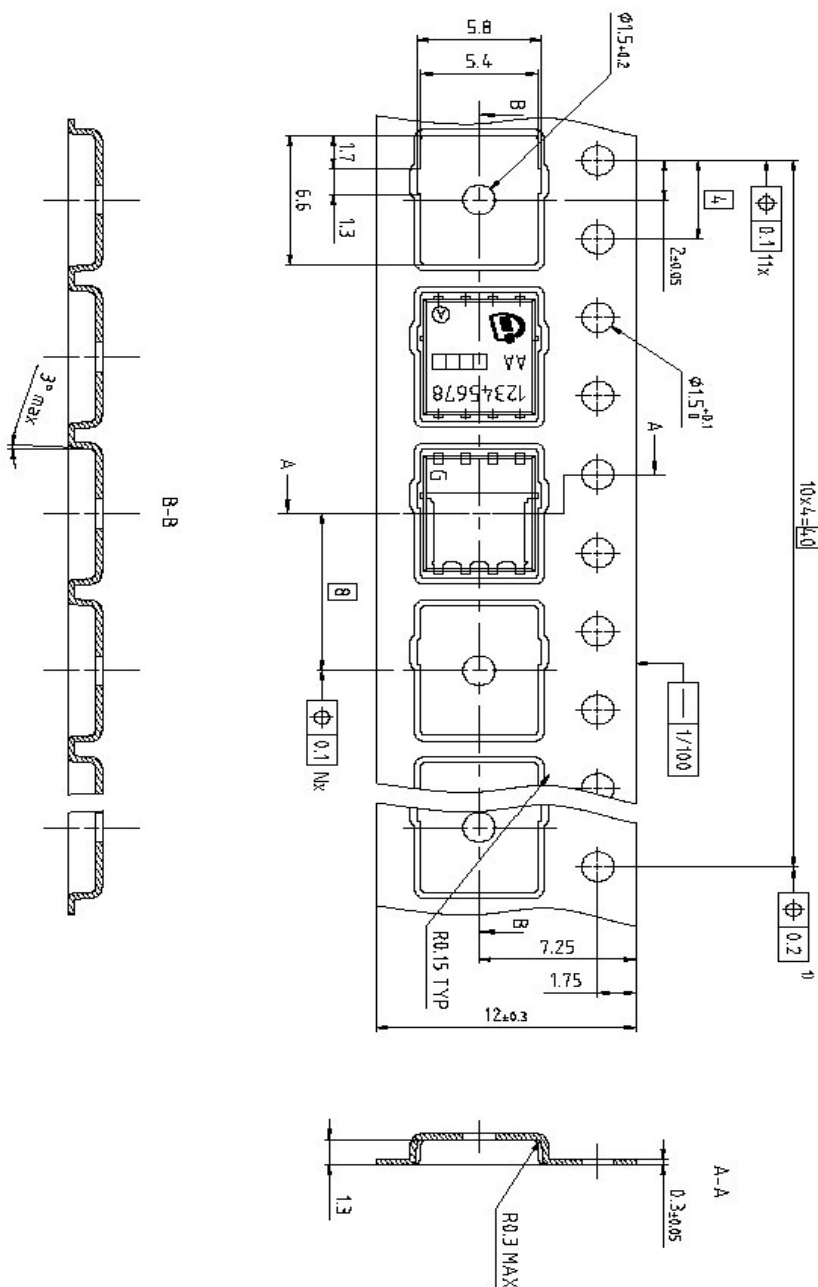


Figure 2 Outline Tape (TDSON-8 FL)

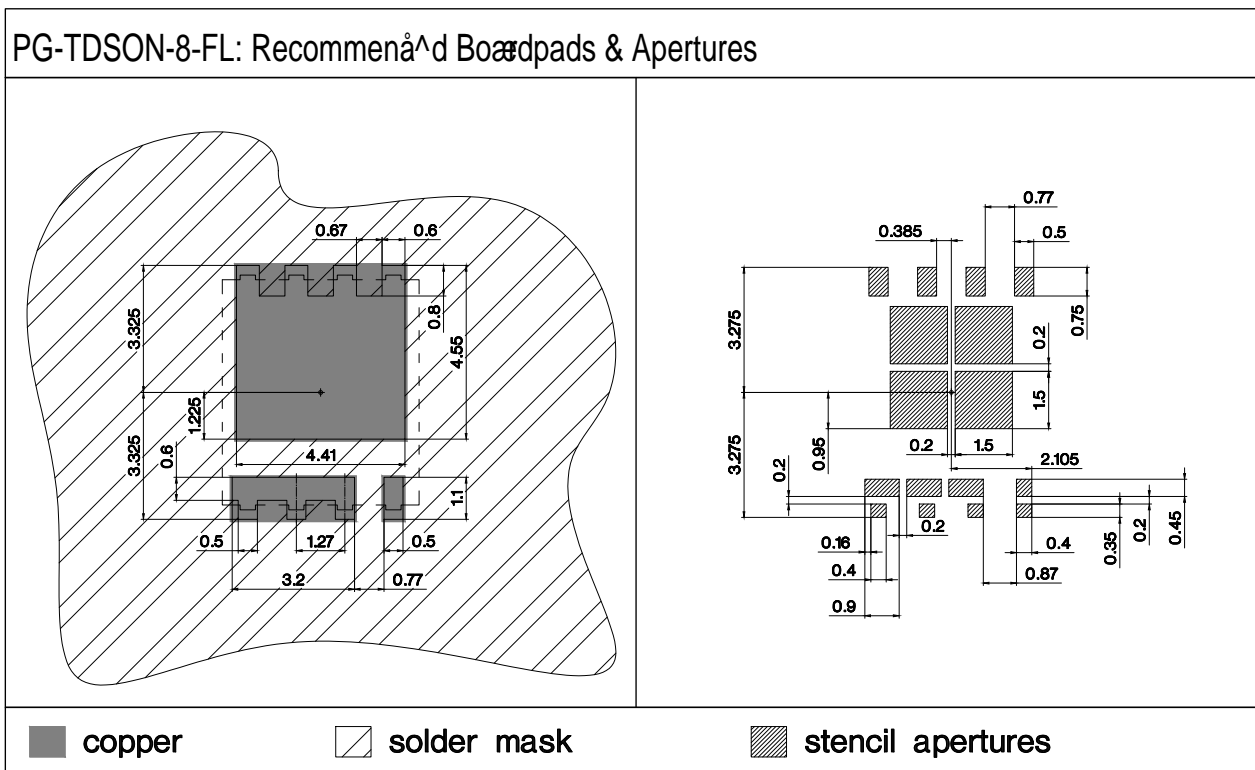


Figure 3 Outline Boardpads (TDSON-8 FL)

## Revision History

BSC016N06NST

Revision: 2019-10-22, Rev. 2.1

### Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-03-01	Release of final version
2.1	2019-10-22	Update package drawings

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