BGSA11GN10

Low R_{ON} Dual Single Pole Single Throw Antenna Tuning Switch

Data Sheet

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Power Management & Multimarket

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Revision History

Document No.: BGSA11GN10.pdf	
Revision History: 0.3	
Previous Version: 0.2	
Page	**Subjects (major changes since last revision)**
7	updated min frequency

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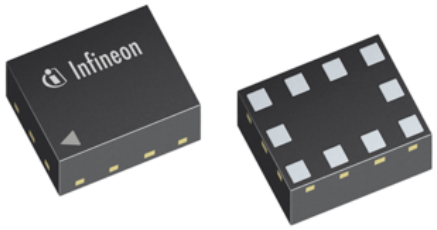
BGSA11GN10 Low R_{ON} Dual Single Pole Single Throw Antenna Tuning Switch

1 Features



- high-linearity Dual SPST for antenna aperture switching applications
- Ultra-Low R_{ON} of 0.79 Ω in ON state for each SPST, 0.38 Ω using both SPST in parallel
- Ultra-Low C_{OFF} of 250 *fF* in OFF state
- High max RF voltage OFF state handling: 36 V peak (72 V_{p-p})
- Low harmonic generation
- No power supply blocking required
- Supply voltage: 1.8 to 3.6 V
- Control voltage: 1.35 to 3.3 V (control high)
- Suitable for EDGE / C2K / LTE / WCDMA Applications
- 0.1 to 5.0 GHz coverage
- Small form factor 1.1 mm x 1.5 mm
- 400 μm pad pitch
- RoHS and WEEE compliant package

RoHS

2 Product Description

The BGSA11GN10 is a Dual Single Pole Single Throw (SPST) RF antenna aperture switch optimized for low R_{on} enabling applications up to 5.0 GHz. This single supply chip integrates on-chip CMOS logic driven by a simple, single-pin CMOS or TTL compatible control input signal. The 0.1 dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels. Unlike GaAs technology, the 0.1 dB compression point exceeds the switch maximum input power level, resulting in linear performance at all signal levels and external DC blocking capacitors at the RF ports are only required if DC voltage is applied externally. Due to its very high RF voltage ruggedness it is suited for switching any reactive devices such as inductors and capacitors in RF matching circuits without significant losses in quality factors.

Table 1: Ordering Information

Type	Package	Marking	Chip
BGSA11GN10	TSNP10-1	11	BGSA11GN10

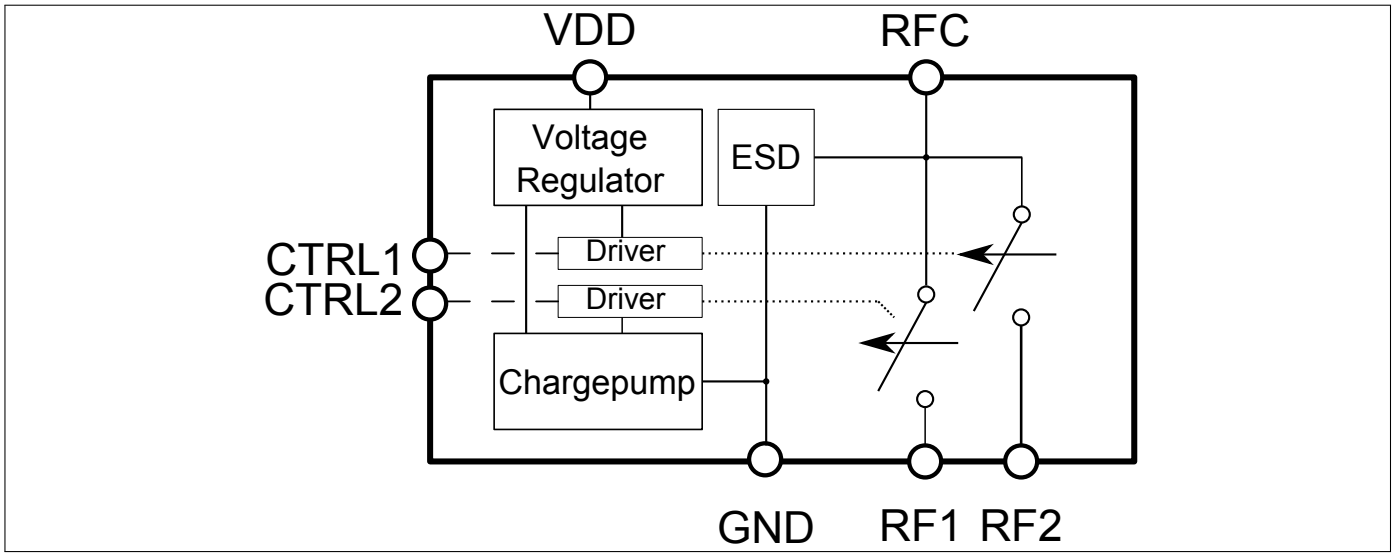


Figure 1: BGSA11GN10 block diagram

3 Maximum Ratings

Table 2: Maximum Ratings, Table I at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency Range	f	0.1	–	–	GHz	[1]
Supply voltage [2]	V_{DD}	-0.5	–	3.6	V	–
Storage temperature range	T_{STG}	-55	–	150	°C	–
RF input power	P_{RF_TRx}	–	–	39	dBm	25 % Duty Cycle
ESD capability, CDM [2]	$V_{ESD_{CDM}}$	-1.5	–	+1.5	*kV*	
ESD capability, HBM [4]	$V_{ESD_{HBM}}$	-1	–	+1	*kV*	
ESD capability, system level (RFC port) [5]	$V_{ESD_{ANT}}$	-8	–	+8	*kV*	RFC vs system GND, with 27 nH shunt inductor
Junction temperature	T_j	–	–	125	°C	–

[1] Switch has a low pass response. The DC voltage at RF ports V_{RFDC} has to be 0V.
[2] Note: Consider any ripple voltages on top of V_{DD}. A high RF ripple at the V_{DD} can exceed the maximum ratings by $V_{DD} = V_{DC} + V_{Ripple}$.
[3] Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.
[4] Human Body Model ANSI/ESDA/JEDEC JS-001-2012 (R = 1.5 kΩ, C = 100 pF).
[5] IEC 61000-4-2 (R = 330 Ω, C = 150 pF), contact discharge.

Table 3: Maximum Ratings, Table II at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum DC-voltage on RF-Ports and RF-Ground	V_{RFDC}	0	–	0	V	No DC voltages allowed on RF-Ports
Control Voltage Levels	V_{CTRL}	-0.7	–	3.3	V	–

4 Operation Ranges

Table 4: Operation Ranges

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.8	2.85	3.6	V	–
Supply current[1)]	I_{DD}	–	80	150	μA	–
Control voltage low	$V_{Ctrl,low}$	0		0.45	V	–
Control voltage high	$V_{Ctrl,high}$	1.2	1.8	2.85	V	$V_{Ctrl,high} \ll V_{DD}$
Control current low	$I_{Ctrl,low}$	-1	0	1	μA	–
Control current high	$I_{Ctrl,high}$	-1	0	1	μA	$V_{Ctrl,high} \ll V_{DD}$
Ambient temperature	T_A	-30	25	85	°C	–
RF switching time	t_{sw}	2	5	7	μs	–
Startup time	t_{sw}		20	30	μs	–

[1)] T_A = -30 °C – +85 °C, V_{VDD} = 1.8 – 3.6 V

5 Logic Table

Table 5: Logic Table

CTRL 1	CTRL 2	Mode RF1 to RFc	Mode RF2 to RFc
0	0	OFF	OFF
0	1	OFF	ON
1	0	ON	OFF
1	1	ON	ON

[1)], CTRL1 and CTRL 2 can be connected together to control both switches at once. This enables the use of both SPSTs to reduce Ron by parallel switching.

6 RF small signal parameter

Table 6: RF small signal specifications

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency range	f	0.1	–	5.0	GHz	–
Switch ON resistance	R_{ON}	0.7	0.79	0.89	Ω	RFx to RFC
Switch OFF capacitance	C_{OFF}	–	250	–	fF	RFx to RFC
Parasitic RF shunt capacitance	$C_{SH,PAR}$	–	42	–	fF	RFx to GND, extracted value for 2 GHz
Switch series inductance	L_{SER}	–	0.1	–	nH	–
Insertion Loss (1,2,3)						
824 - 960 MHz	*IL*	0.10	0.19	0.28	dB	V_{DD} = 1.8 – 3.6 *V*, T_A = -30 ... +85 °C, Z_0 = 50 Ω, RF1 or RF2 switched to RFC
1710 - 1980 MHz		0.18	0.29	0.40	dB	
1981 - 2169 MHz		0.25	0.33	0.40	dB	
2170 - 2690 MHz		0.25	0.35	0.45	dB	
Return Loss(1,2,3)						
All Ports @ 824 - 915 MHz	*RL*	25	28	36	dB	V_{DD} = 1.8 – 3.6 *V*, T_A = -30 ... +85 °C, Z_0 = 50 Ω
All Ports @ 1710 - 2169 MHz		19	25	30	dB	
All Ports @ 2170 - 2690 MHz		17	23	25	dB	
Isolation RFx to RFC(1,2,3)						
824 - 915 MHz	*ISO*	21	23	30	dB	V_{DD} = 1.8 – 3.6 *V*, T_A = -30 ... +85 °C, Z_0 = 50 Ω
1710 - 1980 MHz		15	17	20	dB	
1981 - 2169 MHz		14	16	20	dB	
2170 - 2690 MHz		12	14	18	dB	
Isolation RFx to RFx(1,2,3)						
824 - 915 MHz	*ISO*	22	24	31	dB	V_{DD} = 1.8 – 3.6 *V*, T_A = -30 ... +85 °C, Z_0 = 50 Ω
1710 - 1980 MHz		26	18	21	dB	
1981 - 2169 MHz		15	17	20	dB	
2170 - 2690 MHz		13	14	19	dB	

[1] Valid for all RF power levels, no compression behavior
[2] Network analyser input power: P_{IN} = –20 *dBm*
[3] On application board without any matching components

7 RF large signal parameter

Table 7: RF large signal specifications

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RF operating voltage	V_{RF_peak}	–	–	36	V	
Harmonic Generation up to 12.75 GHz[1,2,3]						
All RF Ports - Second Order Harmonics	P_{H2}	–	105	–	dBc	25 dBm, 50Ω, f_0 = 786 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	115	–	dBc	25 dBm, 50Ω, f_0 = 786 MHz
All RF Ports - Second Order Harmonics	P_{H2}	–	98	–	dBc	33 dBm, 50Ω, f_0 = 824 MHz
All RF Ports - Third Order Harmonics	P_{H3}	–	110	–	dBc	33 dBm, 50Ω, f_0 = 824 MHz
All RF Ports	P_{Hx}	105	–	–	dBc	25 dBm, 50Ω, CW mode
Intermodulation Distortion IMD2 [1,2,3]						
IIP2, low	IIP2,l	–	110	–	dBm	IIP2 conditions table 8
IIP2, high	IIP2,h	–	120	–	dBm	
Intermodulation Distortion IMD3 [1,2,3]						
IIP3	IIP3	–	75	–	dBm	IIP3 conditions table 9
SV LTE Intermodulation [1,2,3]						
IIP3,SVLTE	IIP3,SV	–	75	–	dBm	SV-LTE conditions table 10

[1)]Terminating Port Impedance: Z_0 = 50 Ω [2)]Supply Voltage: V_{DD} = 1.8 – 3.6 V [3)]On application board without any matching components

Table 8: IIP2 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1 Low	2140	1950	20	190	-15
Band 1 High	2140	1950	20	4090	-15
Band 5 Low	881.5	836.5	20	45	-15
Band 5 High	881.5	836.5	20	1718	-15

Table 9: IIP3 conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 1	2140	1950	20	1760	-15
Band 5	881.5	836.5	20	791.5	-15

Table 10: SV-LTE conditions table

Band	In-Band Frequency [MHz]	Blocker Frequency 1 [MHz]	Blocker Power 1 [dBm]	Blocker Frequency 2 [MHz]	Blocker Power 2 [dBm]
Band 5	872	827	23	872	14
Band 13	747	786	23	747	14
Band 20	878	833	23	2544	14

8 Package Outline and Pin Configuration

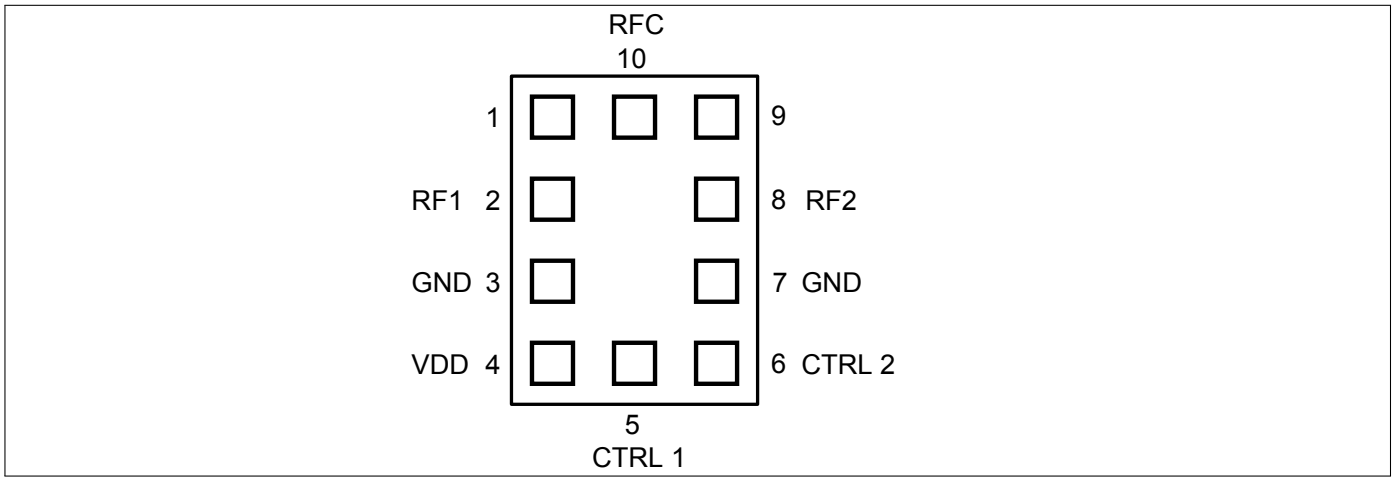


Figure 2: Pinout (top view)

Table 11: Pin Description

Pin No.	Name	Pin Type	Buffer Type	Function
1	N.C.	N.C.		Not connected
2	RF1	I/O		RF1
3	GND	GND		Ground
4	VDD	PWR		Supply voltage
5	CTRL 1	I		Control Pin
6	CTRL 2	I		Control Pin
7	GND	GND		Ground
8	RF2	I/O		RF2
9	N.C.	N.C.		Not connected
10	RFC	I/O		Common RF

Table 12: Mechanical Data

Parameter	Symbol	Value	Unit
X-Dimension	*X*	1.1 $\pm$ 0.05	*mm*
Y-Dimension	*Y*	1.5 $\pm$ 0.05	*mm*
Size	*Size*	1.65	mm^2
Height	*H*	0.375	*mm*

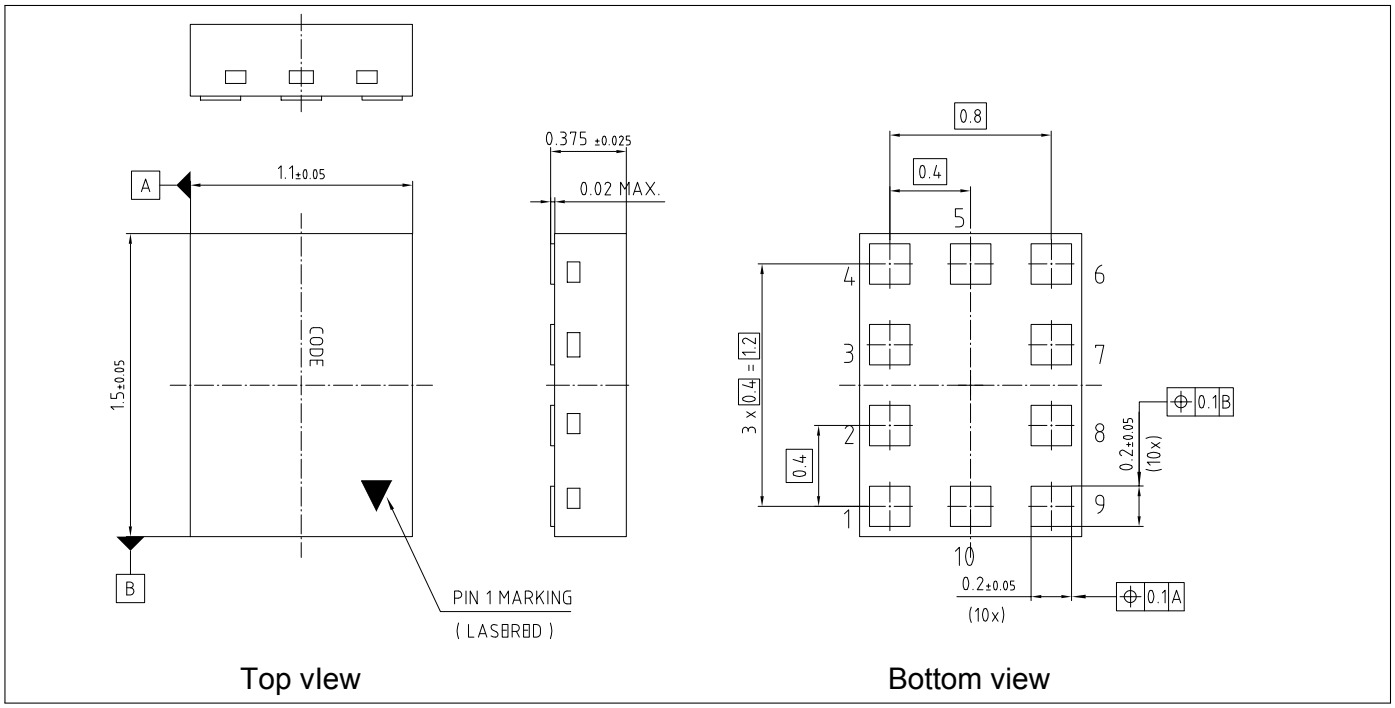


Figure 3: Package Dimensions Drawing

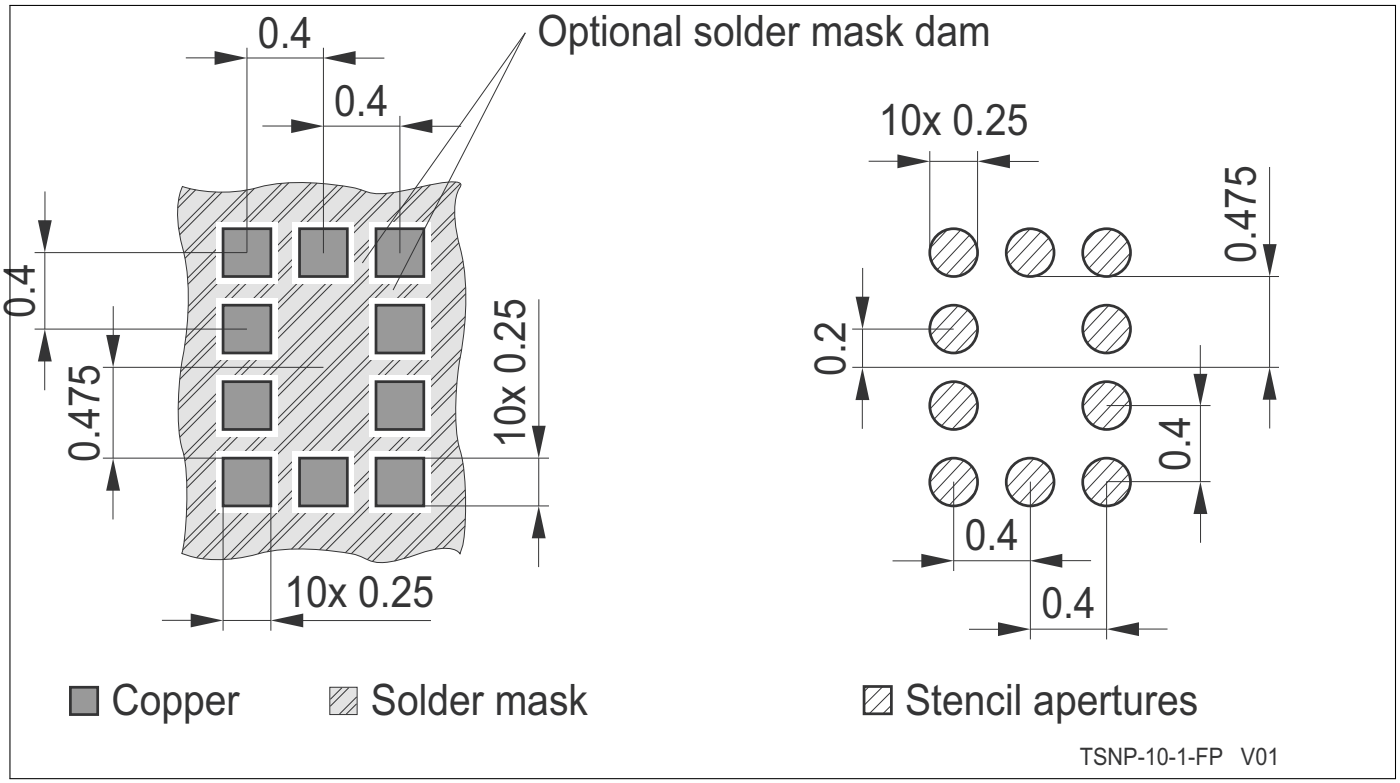


Figure 4: Land pattern and stencil mask

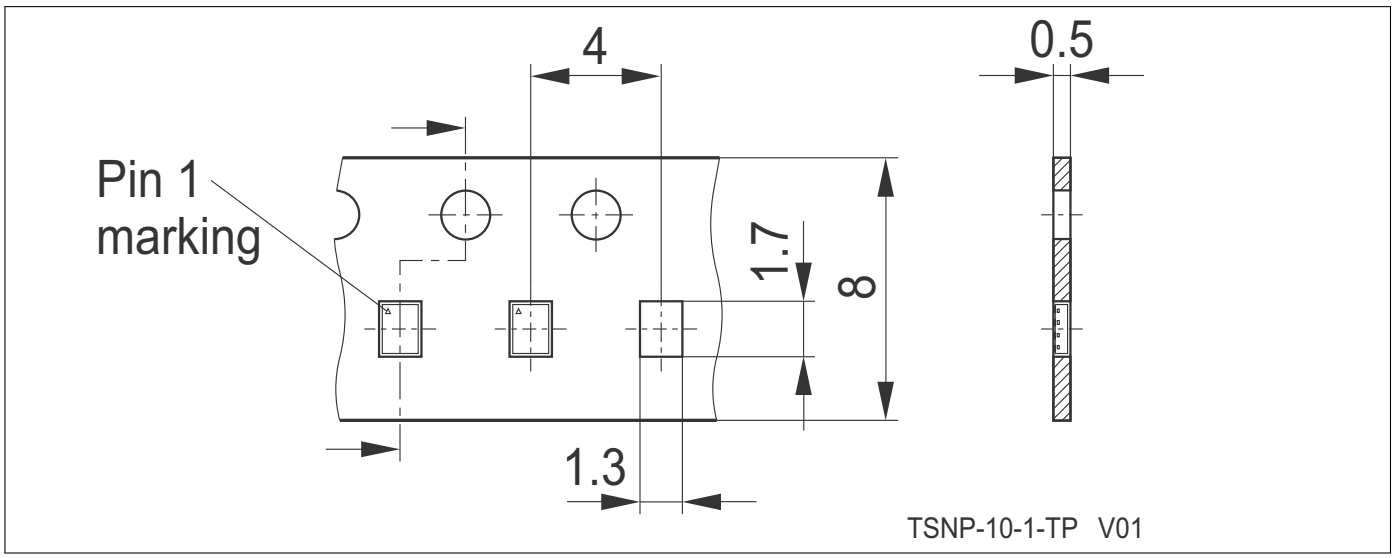


Figure 5: Tape drawing

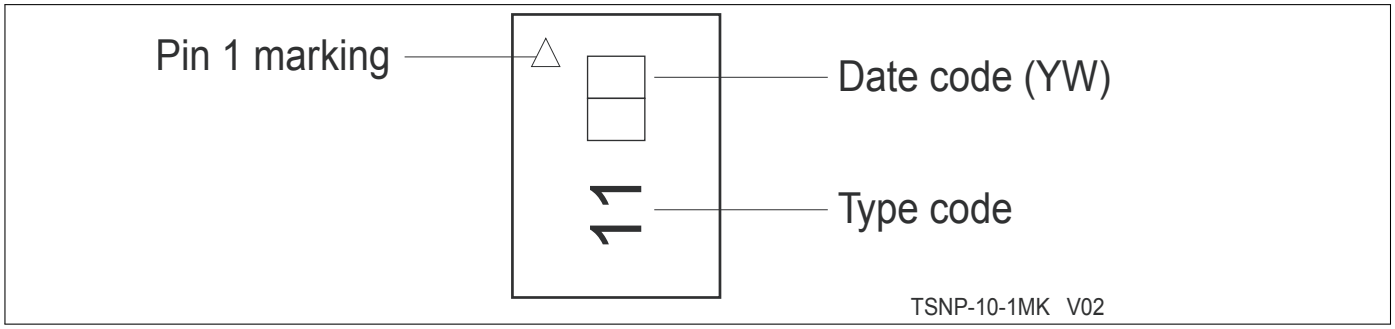


Figure 6: Package marking: Date code digits Y and W are found in Table 13/14

Table 13: Year date code marking - digit "Y"

Year	"Y"	Year	"Y"	Year	"Y"
2000	0	2010	0	2020	0
2001	1	2011	1	2021	1
2002	2	2012	2	2022	2
2003	3	2013	3	2023	3
2004	4	2014	4	2024	4
2005	5	2015	5	2025	5
2006	6	2016	6	2026	6
2007	7	2017	7	2027	7
2008	8	2018	8	2028	8
2009	9	2019	9	2029	9

Table 14: Week date code marking - digit "W"

Week	"W"	Week	"W"	Week	"W"	Week	"W"	Week	"W"
1	A	12	N	23	4	34	h	45	v
2	B	13	P	24	5	35	j	46	x
3	C	14	Q	25	6	36	k	47	y
4	D	15	R	26	7	37	l	48	z
5	E	16	S	27	a	38	n	49	8
6	F	17	T	28	b	39	p	50	9
7	G	18	U	29	c	40	q	51	2
8	H	19	V	30	d	41	r	52	3
9	J	20	W	31	e	42	s		
10	K	21	Y	32	f	43	t		
11	L	22	Z	33	g	44	u		

9 Application Examples

The BGSA11GN10 is a dual single pole single throw (SPST) RF switch in a 1.05 mm x 1.55 mm TSNP-10-1 package. Both SPST can be controlled individually by the control placed next to each other. This solution allows the use of the device for several applications shown in Fig. 7:

- Low R_{ON} = 0.79Ω SPST (a) or ultra low R_{ON} = 0.38Ω SPST (b)
- Tuning with 2 reactive devices such as capacitors or inductors. (c)
- Combinations of above.

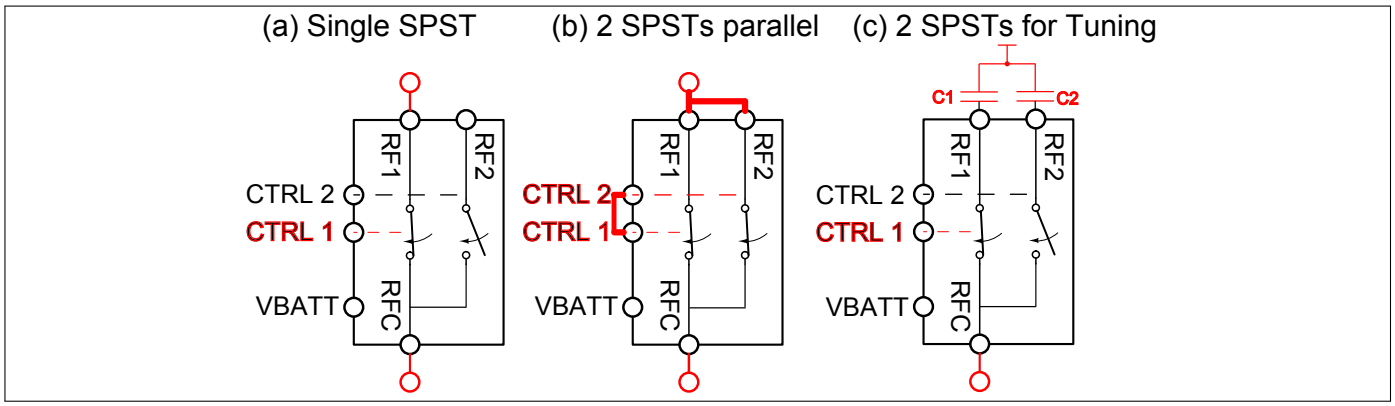


Figure 7: BGSA11GN10 realizable circuit configurations

9.1 Single SPST shunt operation

The configuration (a) is used to obtain an R_{ON} = 0.79Ω and C_{OFF} = 250fF. It can be used for series and shunt configurations. Note, that for single SPST shunt configuration, is is better to connect RFC to GND to avoid additional capacitance contribution of the unused part RF2 to GND as shown in Fig. 8. For simplicity, connecting the unused RF and Control Pin can be connected to ground.

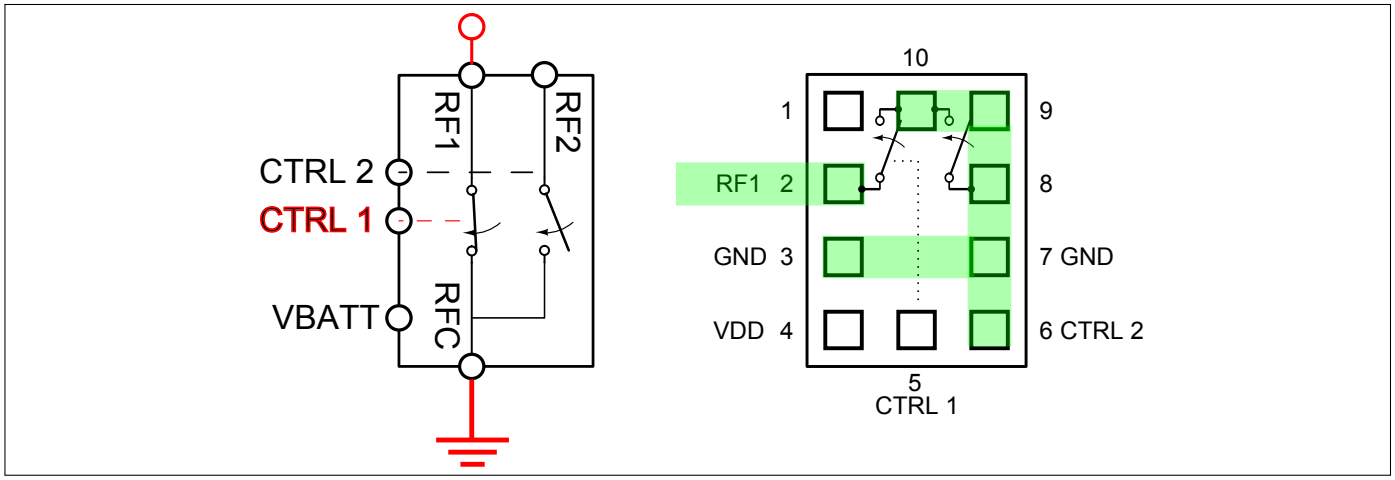


Figure 8: BGSA11GN10 single SPST shunt configuration

9.2 Low R_{ON} SPST shunt operation

For lowest possible R_{ON} = 0.38Ω operation, it is required to connect the logic inputs CTRL 1 with CTRL 2 together and same for RF1 and RF2 as shown in Fig. 9

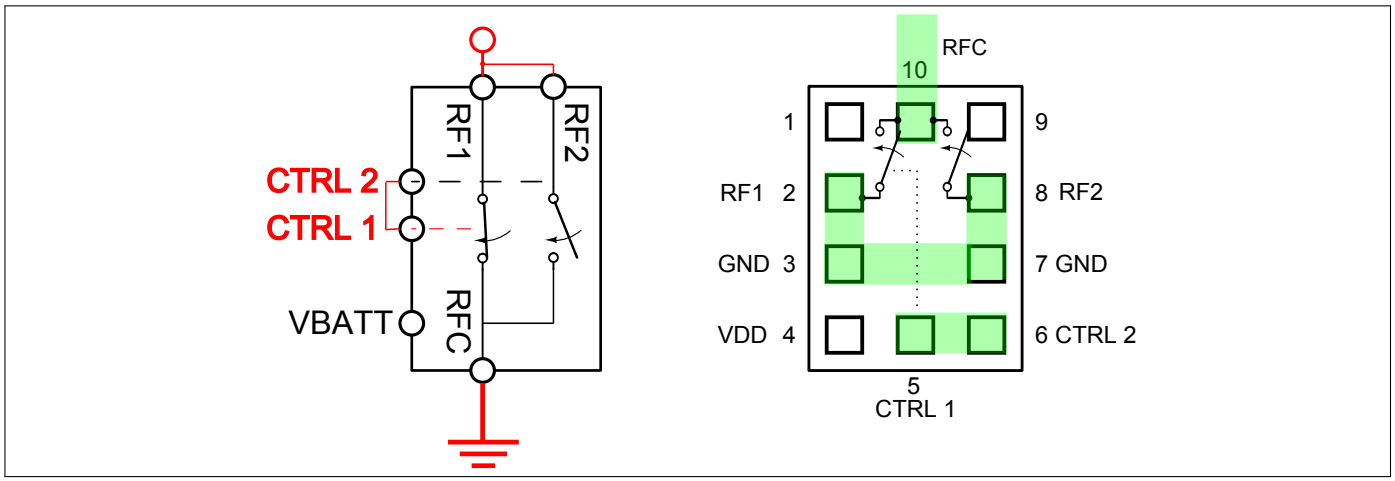


Figure 9: BGSA11GN10 low R_{ON} SPST shunt configuration

9.3 Dual SPST for RF tuning

The dual SPST can also be used for tuning applications, for example to tune capacitance or inductance. Fig. 10 shows as example a tunable capacitance with 4 steps by using 2 external MLCC capacitors. Note that the RF voltage should not exceed the specified 36 V over the switch device and also not for the used capacitor.

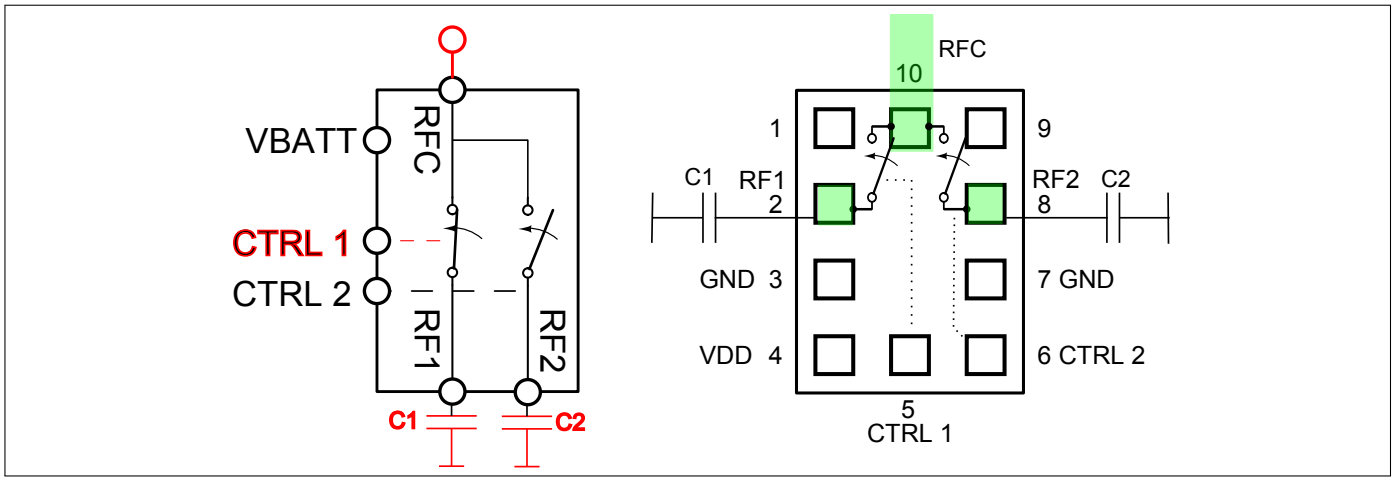


Figure 10: BGSA11GN10 as shunt capacitance tuning device

For example, resulting capacitances using C1 and C2 can be controlled as shown in table 15. Resulting Q factors can be calculated using the R_{ON} values using the equation $Q = \frac{\frac{1}{\omega C}}{R_{ON}}$ with $\omega = 2\pi f$. Same function can be realized also with inductors (Fig. 11) with $Q = \frac{\omega L}{R_{ON}}$ in table 16.

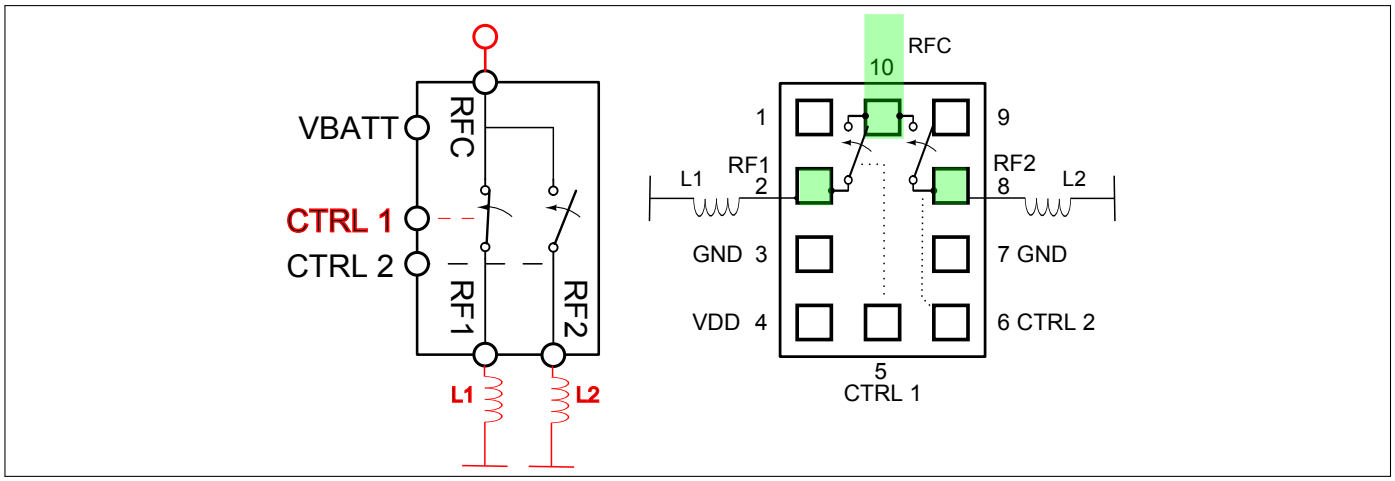


Figure 11: BGSA11GN10 as shunt inductance tuning device

Table 15: Logic Table

CTRL 1	CTRL 2	Mode RF1 to RFc	Mode RF2 to RFc	Capacitance	R_{ON}
0	0	OFF	OFF	500 fF	500 $k\Omega$
0	1	OFF	ON	250 fF + C2	0.79 Ω
1	0	ON	OFF	250 fF + C1	0.79 Ω
1	1	ON	ON	C1 + C2	0.38 Ω

Table 16: Logic Table

CTRL 1	CTRL 2	Mode RF1 to RFc	Mode RF2 to RFc	Inductance	R_{ON}
0	0	OFF	OFF	-	500 $k\Omega$
0	1	OFF	ON	L2	0.79 Ω
1	0	ON	OFF	L1	0.79 Ω
1	1	ON	ON	L1 || L2	0.38 Ω

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