

# 具有 Eco-mode 的 TPS53355 1.5V 至 15V 输入 (4.5V 至 25V 偏置)、 30A 同步降压 SWIFT™ 转换器™

## 1 特性

- 最高效率达 96%
- 转换输入电压范围: 1.5V 至 15V
- VDD 输入电压范围: 4.5V 至 25V
- 输出电压范围: 0.6V 至 5.5V
- 5V LDO 输出
- 支持单轨输入
- 具有 30A 连续输出电流的集成功率 MOSFET
- 自动跳跃 Eco-mode™ 可实现轻负载效率
- 关断电流 < 10 $\mu$ A
- 具有快速瞬态响应的 D-CAP™ 模式
- 具有外部电阻器的可选开关频率, 范围从 250kHz 至 1MHz
- 可选自动跳跃或仅 PWM 工作模式
- 内置 1% 0.6V 基准电压
- 0.7ms、1.4ms、2.8ms 和 5.6ms 可选内部电压伺服器软启动
- 集成升压开关
- 预充电启动能力
- 具有热补偿的可调过流限制
- 过压、欠压、UVLO 和过热保护
- 支持全陶瓷输出电容器
- 漏极开路电源正常指示
- 包含 NexFET™ 电源块技术
- 带 PowerPAD 的 22 引脚 QFN 封装™
- 如需 SWIFT™ 电源产品文档, 请访问 <http://www.ti.com/swift>
- 可选“绿色环保”(符合 RoHS 标准)

- 使用 TPS53355 并借助 WEBENCH® 电源设计器创建定制设计

## 2 应用

- 服务器和存储
- 工作站和台式机
- 电信基础设施

## 3 说明

TPS53355 是一款集成有金属氧化物半导体场效应晶体管 (MOSFET) 的 D-CAP™ 模式、30A 同步开关。它的设计目标是简单易用、减少外部组件, 以及适用于空间受限的电源系统。

该器件具有 5m $\Omega$ /2m $\Omega$  集成 MOSFET、1% 的精度、0.6V 的基准电压, 以及集成升压开关。富有竞争力的特性包括: 1.5V 至 15V 宽转换输入电压范围、所用外部组件极少、针对超快瞬变的 D-CAP™ 模式控制、自动跳跃模式运行、内部软启动控制、可选频率并且无需补偿。

转换输入电压范围为 1.5V 至 15V, 电源电压范围为 4.5V 至 25V, 输出电压范围为 0.6V 至 5.5V。

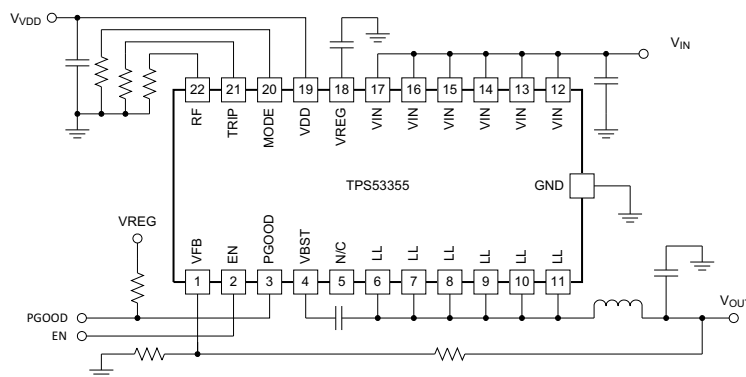
该器件采用 22 引脚 6mm x 5mm QFN 封装。

### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPS53355	LSON-CLIP (22)	6.00mm x 5.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

### 典型应用



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

### Changes from Revision E (March 2019) to Revision F Page

•	从“说明”中删除了 -40°C 至 +85°C 的温度范围 .....	1
•	Removed -40°C to +85°C temperature range from Absolute Maximum Ratings .....	5

### Changes from Revision D (November 2016) to Revision E Page

•	已添加 WEBENCH 链接 .....	1
•	Deleted "Operating free-air temperature, T <sub>A</sub> " row .....	5

### Changes from Revision C (February 2016) to Revision D Page

•	添加了特性：可选“绿色环保”（符合 RoHS 标准） .....	1
•	Added the VQP package to the <i>Thermal Infomation</i> .....	5
•	From: a SC5026-1R0 inductor is used. To: a 744355182 inductor is used. ....	8
•	Changed <a href="#">Figure 32</a> and <a href="#">Figure 33</a> .....	12
•	<i>5-V LDO and VREG Start-Up</i> , Changed the NOTE From: "The 5-V LDO is not controlled" To: "The 5-V LDO is controlled" .....	16
•	Changed 250 μs To ~550 μs in <a href="#">Figure 34</a> .....	16

### Changes from Revision B (January 2014) to Revision C Page

•	将数据表标题从“具有 Eco-mode™ 的 TPS53355 高效 30A 同步降压转换器”更改为“具有 Eco-mode™ 的 TPS53355 高效 30A 同步降压 SWIFT™ 转换器” .....	1
•	添加了特性：“如需 SWIFT™ 电源产品文档，...” .....	1

### Changes from Revision A (September 2012) to Revision B Page

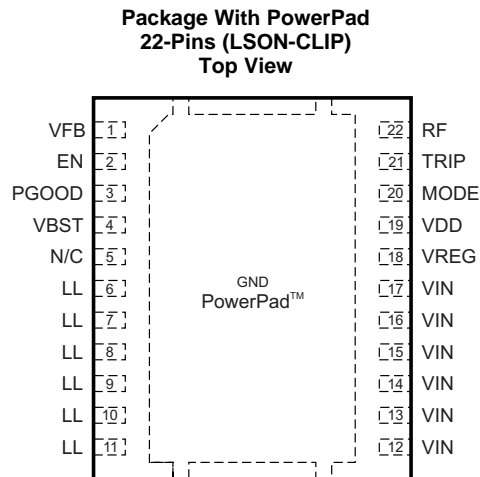
•	已添加 引脚配置和功能部分、ESD 额定值表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分 .....	1
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**Changes from Original (August 2011) to Revision A**
**Page**

• 已更改 将转换输入电压范围从“3V”改为“1.5V” .....	1
• Changed VIN input voltage range minimum from "3 V" to "1.5 V" .....	4
• Changed typographical error in THERMAL INFORMATION table .....	5
• Changed VIN (main supply) input voltage range minimum from "3 V" to "1.5 V" in <i>Recommended Operating Conditions...</i>	5
• Changed VIN pin power conversion input minimum voltage from "3 V" to "1.5 V" in ELECTRICAL CHARACTERISTICS table .....	6
• Changed conversion input voltage range from "3 V" to "1.5" in <i>Overview</i> .....	14
• Added note to the <i>Functional Block Diagram</i> .....	15
• Changed "ripple injection capacitor" to "ripple injection resistor" in <i>Layout Guidelines</i> section .....	30

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## 5 Pin Configuration and Functions



(1) N/C = no connection

### Pin Functions

PIN		I/O/P <sup>(1)</sup>	DESCRIPTION
NAME	NO		
EN	2	I	Enable pin. Typical turn-on threshold voltage is 1.2 V. Typical turn-off threshold is 0.95 V.
GND	—	—	Ground and thermal pad of the device. Use proper number of vias to connect to ground plane.
LL	6	B	Output of converted power. Connect this pin to the output Inductor.
	7		
	8		
	9		
	10		
11			
MODE	20	I	Soft-start and Skip/CCM selection. Connect a resistor to select soft-start time using <a href="#">Table 3</a> . The soft-start time is detected and stored into internal register during start-up.
N/C	5		No connect.
PGOOD	3	O	Open drain power good flag. Provides 1-ms start-up delay after VFB falls in specified limits. When VFB goes out of the specified limits PGOOD goes low after a 2-μs delay.
RF	22	I	Switching frequency selection. Connect a resistor to GND or VREG to select switching frequency using <a href="#">Table 1</a> . The switching frequency is detected and stored during the startup.
TRIP	21	I	OCL detection threshold setting pin. $I_{TRIP} = 10 \mu A$ at room temperature, 4700 ppm/°C current is sourced and set the OCL trip voltage as follows: $V_{OCL} = V_{TRIP}/32$ ( $V_{TRIP} \leq 2.4 V, V_{OCL} \leq 75 mV$ )
VBST	4	P	Supply input for high-side FET gate driver (boost terminal). Connect capacitor from this pin to LL node. Internally connected to VREG via bootstrap MOSFET switch.
VDD	19	P	Controller power supply input. VDD input voltage range is from 4.5 V to 25 V.
VFB	1	I	Output feedback input. Connect this pin to Vout through a resistor divider.
VIN	12	P	Conversion power input. VIN input voltage range is from 1.5 V to 15 V.
	13		
	14		
	15		
	16		
17			
VREG	18	P	5-V low drop out (LDO) output. Supplies the internal analog circuitry and driver circuitry.

(1) I=Input, O=Output, B=Bidirectional, P=Supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

		MIN	MAX	UNIT	
Input voltage	VIN (main supply)	-0.3	25	V	
	VDD	-0.3	28		
	VBST	-0.3	32		
	VBST (with respect to LL)	-0.3	7		
	EN, TRIP, VFB, RF, MODE	-0.3	7		
Output voltage	LL	DC	-2	25	V
		Pulse < 20 ns, E = 5 μJ	-7	27	
	PGOOD, VREG	-0.3	7		
	GND	-0.3	0.3		
Source/sink current	VBST	50		mA	
Junction temperature, T <sub>J</sub>		-40	150	°C	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			300	°C	
Storage temperature, T <sub>stg</sub>		-55	150	°C	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltage range	VIN (main supply)	1.5	15	V
	VDD	4.5	25	
	VBST	4.5	28	
	VBST (with respect to LL)	4.5	6.5	
	EN, TRIP, VFB, RF, MODE	-0.1	6.5	
Output voltage range	LL	-1	22	V
	PGOOD, VREG	-0.1	6.5	
Junction temperature range, T <sub>J</sub>		-40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS53355		UNIT
		DQP	VQP	
		22 PINS	22 PINS	
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	27.2	27.2	°C/W
θ <sub>JCtop</sub>	Junction-to-case (top) thermal resistance	17.1	17.1	°C/W
θ <sub>JB</sub>	Junction-to-board thermal resistance	5.9	5.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.8	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

**Thermal Information (continued)**

THERMAL METRIC <sup>(1)</sup>		TPS53355		UNIT
		DQP	VQP	
		22 PINS	22 PINS	
$\psi_{JB}$	Junction-to-board characterization parameter	5.8	5.8	°C/W
$\theta_{JCb\text{ot}}$	Junction-to-case (bottom) thermal resistance	1.2	1.2	°C/W

**6.5 Electrical Characteristics**

 Over recommended free-air temperature range,  $V_{VDD} = 12\text{ V}$  (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
$V_{VIN}$	VIN pin power conversion input voltage		1.5		15	V
$V_{VDD}$	Supply input voltage		4.5		25	V
$I_{VIN(\text{leak})}$	VIN pin leakage current	$V_{EN} = 0\text{ V}$			1	$\mu\text{A}$
$I_{VDD}$	VDD supply current	$T_A = 25^\circ\text{C}$ , No load, $V_{EN} = 5\text{ V}$ , $V_{VFB} = 0.630\text{ V}$		420	590	$\mu\text{A}$
$I_{VDDSDN}$	VDD shutdown current	$T_A = 25^\circ\text{C}$ , No load, $V_{EN} = 0\text{ V}$			10	$\mu\text{A}$
<b>INTERNAL REFERENCE VOLTAGE</b>						
$V_{VFB}$	VFB regulation voltage	CCM condition <sup>(1)</sup>		0.6		V
$V_{VFB}$	VFB regulation voltage	$T_A = 25^\circ\text{C}$	0.597	0.6	0.603	V
		$0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0.5952	0.6	0.6048	
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0.594	0.6	0.606	
$I_{VFB}$	VFB input current	$V_{VFB} = 0.630\text{ V}$ , $T_A = 25^\circ\text{C}$		0.01	0.20	$\mu\text{A}$
<b>LDO OUTPUT</b>						
$V_{VREG}$	LDO output voltage	$0\text{ mA} \leq I_{VREG} \leq 30\text{ mA}$	4.77	5	5.36	V
$I_{VREG}$	LDO output current <sup>(1)</sup>	Maximum current allowed from LDO			30	mA
$V_{DO}$	Low drop out voltage	$V_{VDD} = 4.5\text{ V}$ , $I_{VREG} = 30\text{ mA}$			230	mV
<b>BOOT-STRAP SWITCH</b>						
$V_{FBST}$	Forward voltage	$V_{VREG-VBST}$ , $I_F = 10\text{ mA}$ , $T_A = 25^\circ\text{C}$		0.1	0.2	V
$I_{VBSTLK}$	VBST leakage current	$V_{VBST} = 23\text{ V}$ , $V_{SW} = 17\text{ V}$ , $T_A = 25^\circ\text{C}$		0.01	1.50	$\mu\text{A}$
<b>DUTY AND FREQUENCY CONTROL</b>						
$t_{OFF(\text{min})}$	Minimum off time	$T_A = 25^\circ\text{C}$	150	260	400	ns
$t_{ON(\text{min})}$	Minimum on time	$V_{IN} = 17\text{ V}$ , $V_{OUT} = 0.6\text{ V}$ , $R_{RF} = 39\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$ <sup>(1)</sup>		35		ns
<b>SOFT START</b>						
$t_{SS}$	Internal soft-start time from $V_{OUT} = 0\text{ V}$ to 95% of $V_{OUT}$	$R_{MODE} = 39\text{ k}\Omega$		0.7		ms
		$R_{MODE} = 100\text{ k}\Omega$		1.4		
		$R_{MODE} = 200\text{ k}\Omega$		2.8		
		$R_{MODE} = 470\text{ k}\Omega$		5.6		
<b>INTERNAL MOSFETS</b>						
$R_{DS(\text{on})H}$	High-side MOSFET on-resistance	$T_A = 25^\circ\text{C}$		5		m $\Omega$
$R_{DS(\text{on})L}$	Low-side MOSFET on-resistance	$T_A = 25^\circ\text{C}$		2		m $\Omega$

(1) Ensured by design. Not production tested.

## Electrical Characteristics (continued)

Over recommended free-air temperature range,  $V_{DD} = 12\text{ V}$  (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER GOOD</b>						
$V_{THPG}$	PG threshold	PG in from lower	92.5%	95.0%	98.5%	
		PG in from higher	107.5%	110.0%	112.5%	
		PG hysteresis	2.5%	5.0%	7.5%	
$R_{PG}$	PG transistor on-resistance		15	30	55	$\Omega$
$t_{PGDEL}$	PG delay	Delay for PG in	0.8	1	1.2	ms
<b>LOGIC THRESHOLD AND SETTING CONDITIONS</b>						
$V_{EN}$	EN Voltage	Enable	1.8			V
		Disable			0.6	
$I_{EN}$	EN Input current	$V_{EN} = 5\text{ V}$			1.0	$\mu\text{A}$
$f_{SW}$	Switching frequency	$R_{RF} = 0\ \Omega$ to GND, $T_A = 25^\circ\text{C}^{(2)}$	200	250	300	kHz
		$R_{RF} = 187\text{ k}\Omega$ to GND, $T_A = 25^\circ\text{C}^{(2)}$	250	300	350	
		$R_{RF} = 619\text{ k}\Omega$ , to GND, $T_A = 25^\circ\text{C}^{(2)}$	350	400	450	
		$R_{RF} = \text{Open}$ , $T_A = 25^\circ\text{C}^{(2)}$	450	500	550	
		$R_{RF} = 866\text{ k}\Omega$ to VREG, $T_A = 25^\circ\text{C}^{(2)}$	580	650	720	
		$R_{RF} = 309\text{ k}\Omega$ to VREG, $T_A = 25^\circ\text{C}^{(2)}$	670	750	820	
		$R_{RF} = 124\text{ k}\Omega$ to VREG, $T_A = 25^\circ\text{C}^{(2)}$	770	850	930	
		$R_{RF} = 0\ \Omega$ to VREG, $T_A = 25^\circ\text{C}^{(2)}$	880	970	1070	
<b>PROTECTION: CURRENT SENSE</b>						
$I_{TRIP}$	TRIP source current	$V_{TRIP} = 1\text{ V}$ , $T_A = 25^\circ\text{C}$	9.4	10.0	10.6	$\mu\text{A}$
$TC_{ITRIP}$	TRIP current temperature coefficient	On the basis of $25^\circ\text{C}^{(1)}$		4700		ppm/ $^\circ\text{C}$
$V_{TRIP}$	Current limit threshold setting range	$V_{TRIP-GND}$	0.4		2.4	V
$V_{OCL}$	Current limit threshold	$V_{TRIP} = 2.4\text{ V}$	68.5	75.0	81.5	mV
		$V_{TRIP} = 0.4\text{ V}$	7.5	12.5	17.5	
$V_{OCLN}$	Negative current limit threshold	$V_{TRIP} = 2.4\text{ V}$	-315	-300	-285	mV
		$V_{TRIP} = 0.4\text{ V}$	-58	-50	-42	
$V_{AZCADJ}$	Auto zero cross adjustable range	Positive	3	15		mV
		Negative		-15	-3	
<b>PROTECTION: UVP and OVP</b>						
$V_{OVP}$	OVP trip threshold	OVP detect	115%	120%	125%	
$t_{OVPDEL}$	OVP propagation delay	VFB delay with 50-mV overdrive		1		$\mu\text{s}$
$V_{UVP}$	Output UVP trip threshold	UVP detect	65%	70%	75%	
$t_{UVPDEL}$	Output UVP propagation delay		0.8	1.0	1.2	ms
$t_{UVPEN}$	Output UVP enable delay	From enable to UVP workable	1.8	2.6	3.2	ms
<b>UVLO</b>						
$V_{UVVREG}$	VREG UVLO threshold	Wake up	4.00	4.20	4.33	V
		Hysteresis		0.25		
<b>THERMAL SHUTDOWN</b>						
$T_{SDN}$	Thermal shutdown threshold	Shutdown temperature <sup>(1)</sup>		145		$^\circ\text{C}$
		Hysteresis <sup>(1)</sup>		10		

(2) Not production tested. Test condition is  $V_{IN} = 12\text{ V}$ ,  $V_{OUT} = 1.1\text{ V}$ ,  $I_{OUT} = 10\text{ A}$  using application circuit shown in [Figure 47](#).

## 6.6 Typical Characteristics

For  $V_{OUT} = 5\text{ V}$ , a 744355182 inductor is used. For  $1 \leq V_{OUT} \leq 3.3\text{ V}$ , a PA0513.441 inductor is used.

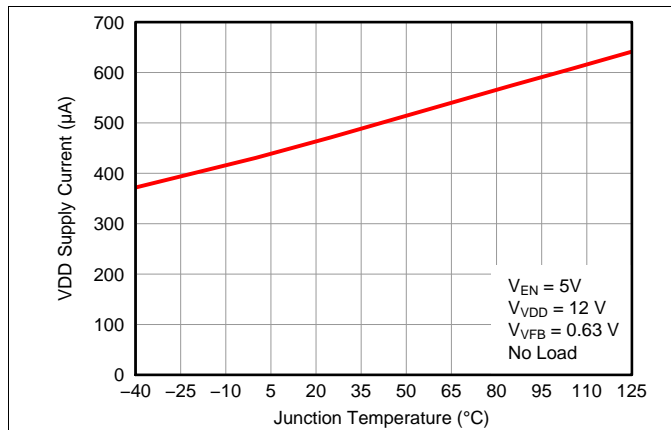


Figure 1. VDD Supply Current vs Junction Temperature

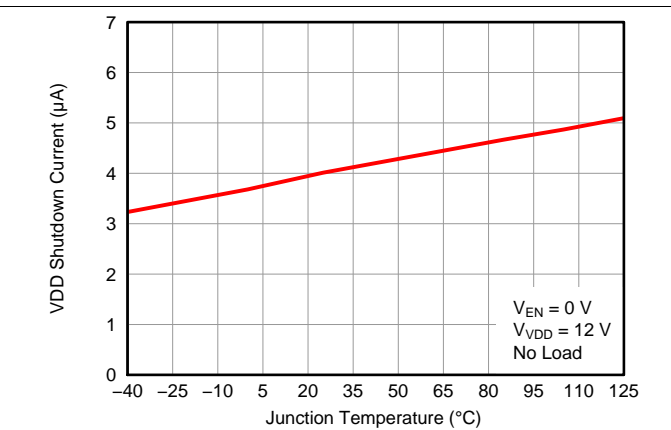


Figure 2. VDD Shutdown Current vs Junction Temperature

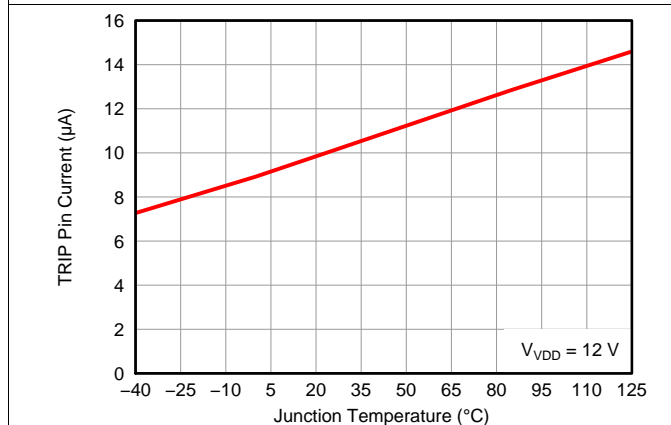


Figure 3. TRIP Pin Current vs Junction Temperature

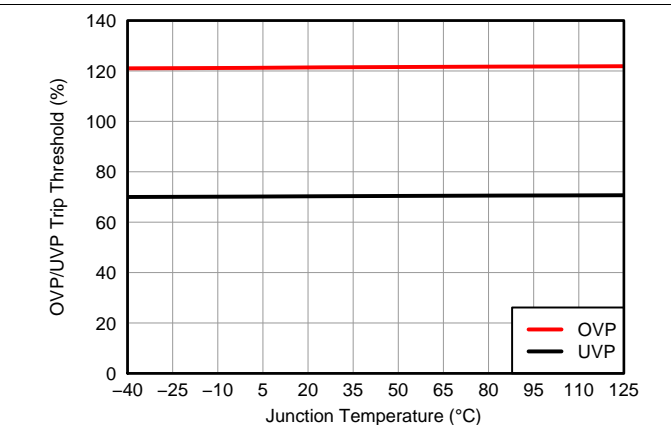


Figure 4. OVP/UVLP Trip Threshold vs Junction Temperature

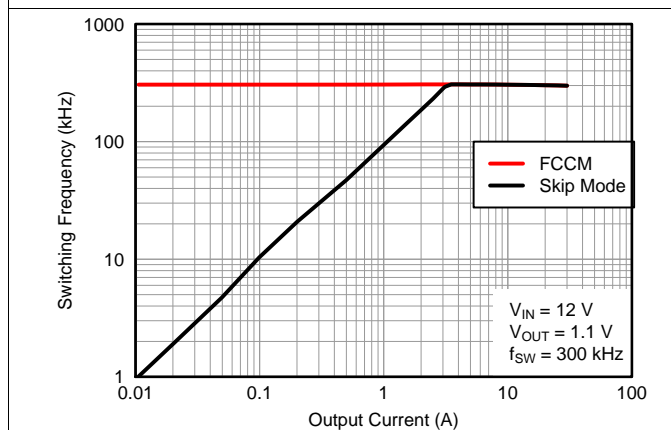


Figure 5. Switching Frequency vs Output Current

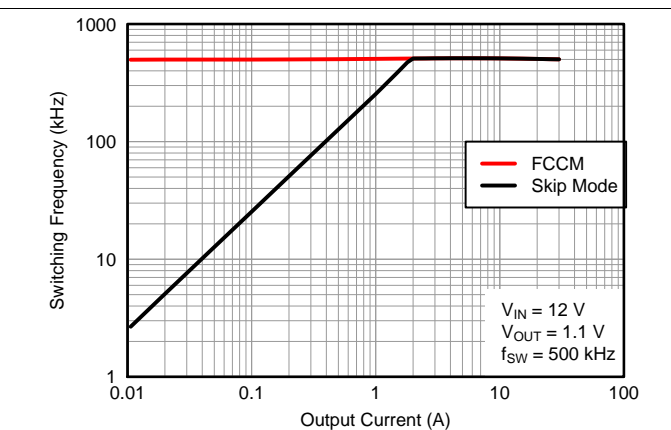


Figure 6. Switching Frequency vs Output Current



Typical Characteristics (continued)

For  $V_{OUT} = 5\text{ V}$ , a 744355182 inductor is used. For  $1 \leq V_{OUT} \leq 3.3\text{ V}$ , a PA0513.441 inductor is used.

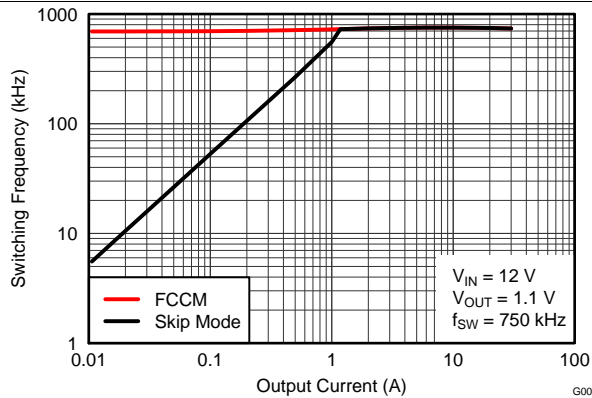


Figure 7. Switching Frequency vs Output Current

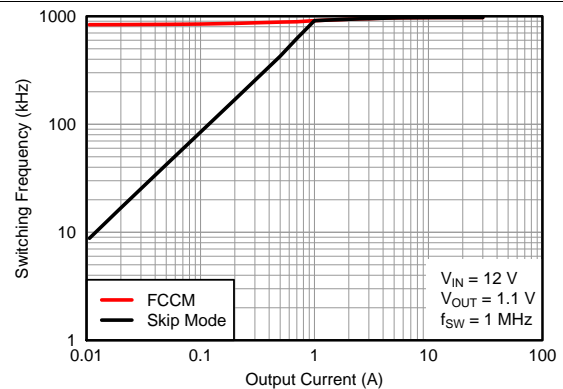


Figure 8. Switching Frequency vs Output Current

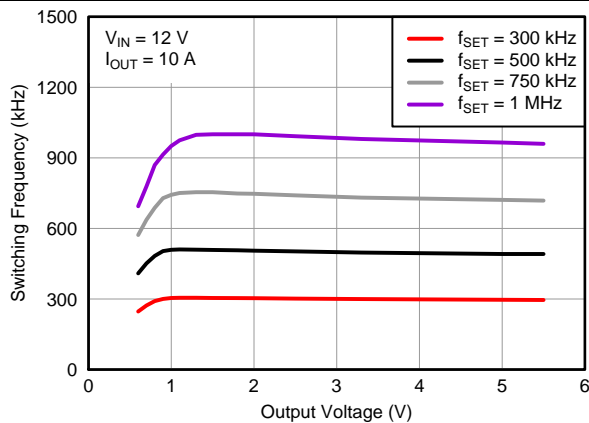


Figure 9. Switching Frequency vs Output Voltage

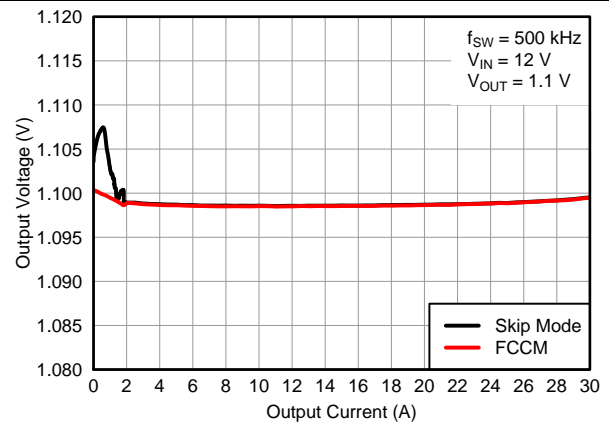


Figure 10. Output Voltage vs Output Current

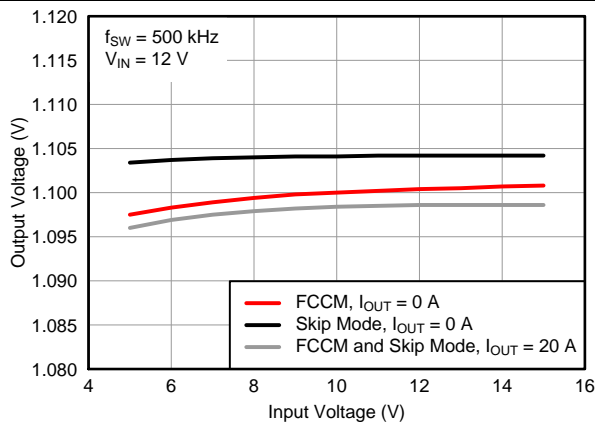


Figure 11. Output Voltage vs Input Voltage

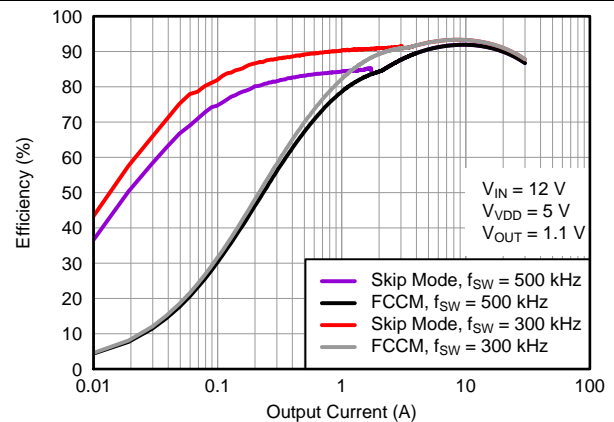
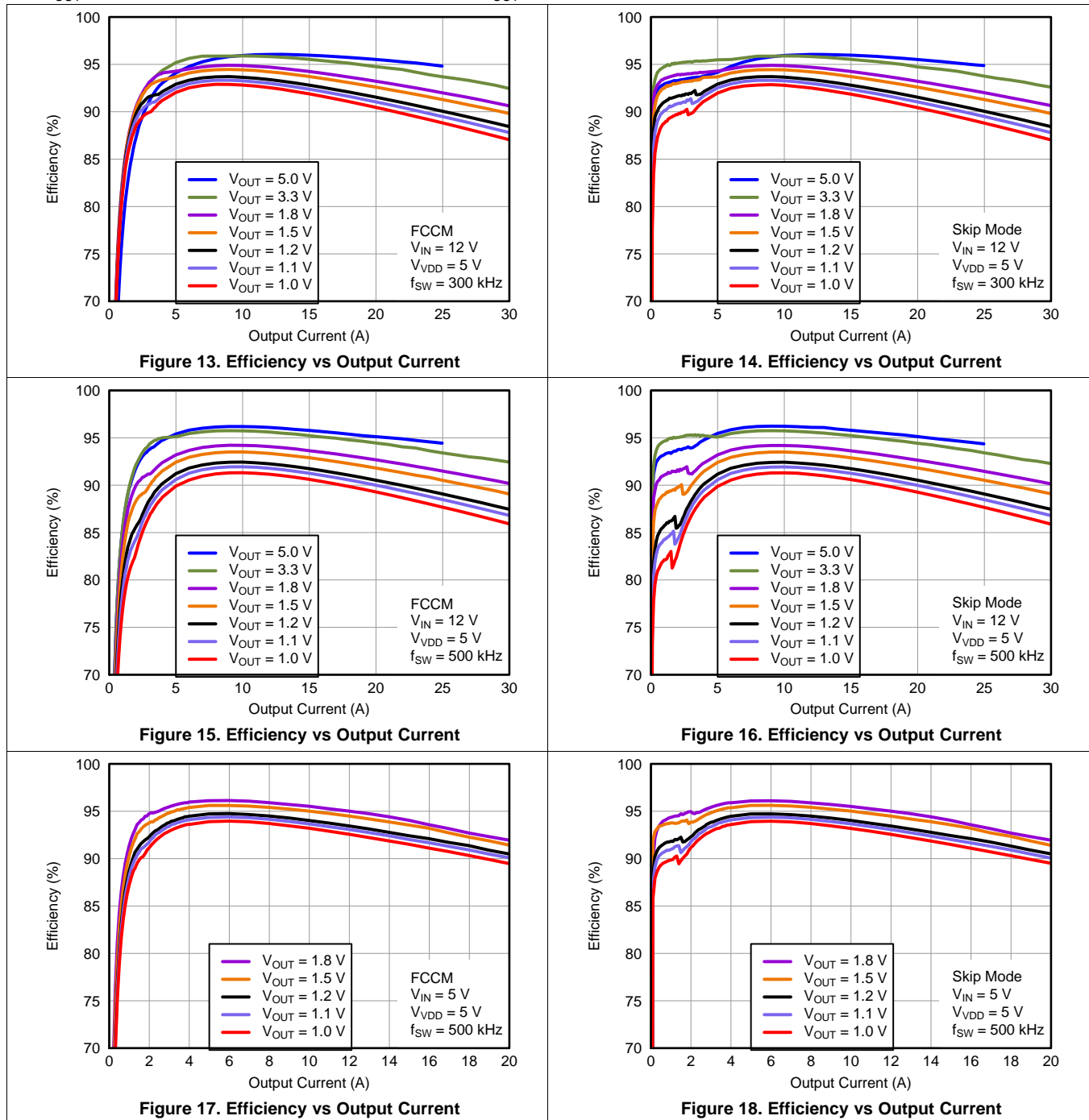


Figure 12. Efficiency vs Output Current

### Typical Characteristics (continued)

For  $V_{OUT} = 5\text{ V}$ , a 744355182 inductor is used. For  $1 \leq V_{OUT} \leq 3.3\text{ V}$ , a PA0513.441 inductor is used.



### Typical Characteristics (continued)

For  $V_{OUT} = 5\text{ V}$ , a 744355182 inductor is used. For  $1 \leq V_{OUT} \leq 3.3\text{ V}$ , a PA0513.441 inductor is used.

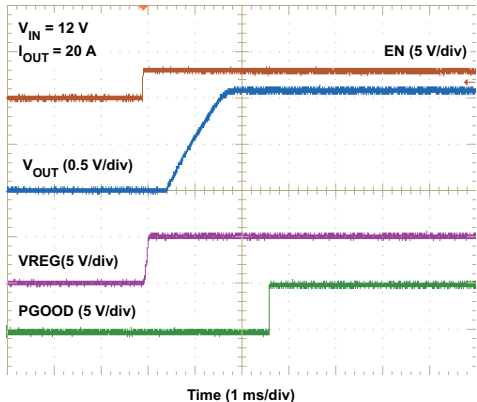


Figure 19. Start-Up Waveforms

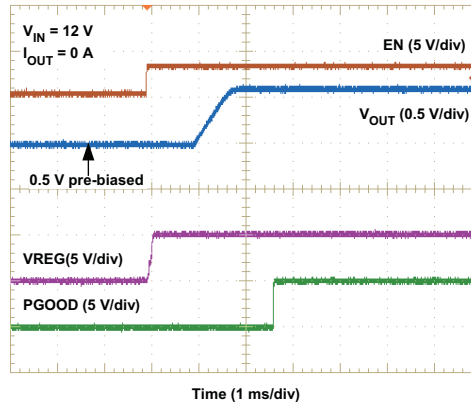


Figure 20. Pre-Bias Start-Up Waveforms

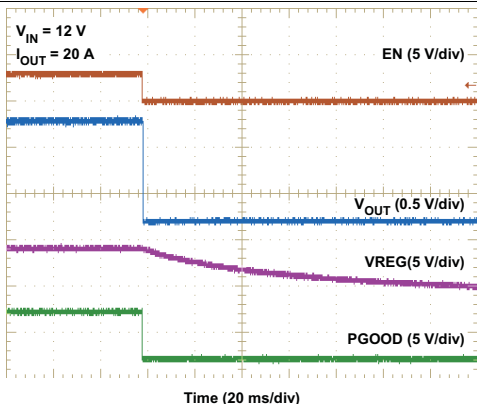


Figure 21. Shutdown Waveforms

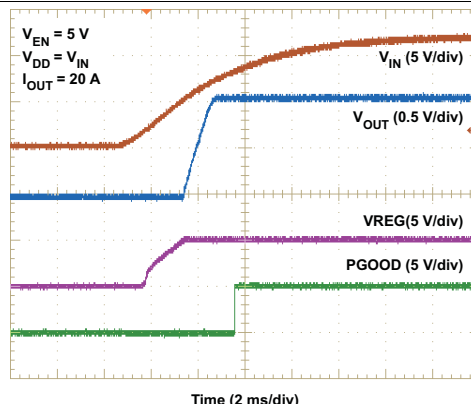


Figure 22. UVLO Start-Up Waveforms

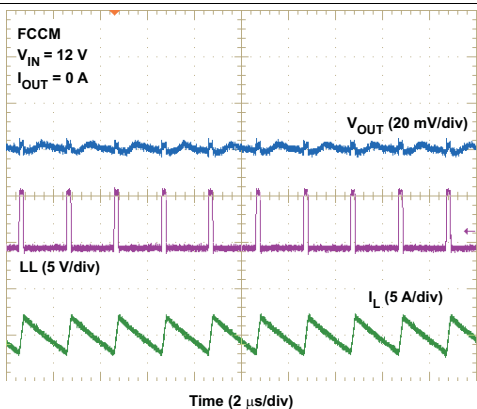


Figure 23. 1.1-V Output FCCM Mode Steady-State Operation

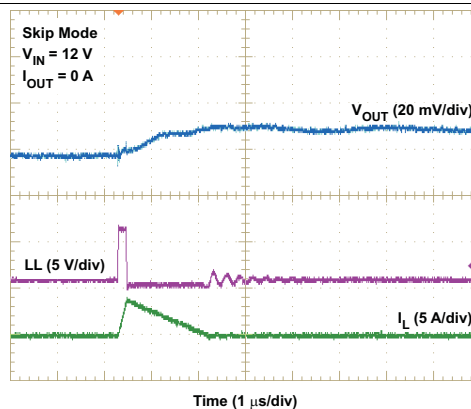


Figure 24. 1.1-V Output Skip Mode Steady-State Operation

### Typical Characteristics (continued)

For  $V_{OUT} = 5\text{ V}$ , a 744355182 inductor is used. For  $1 \leq V_{OUT} \leq 3.3\text{ V}$ , a PA0513.441 inductor is used.

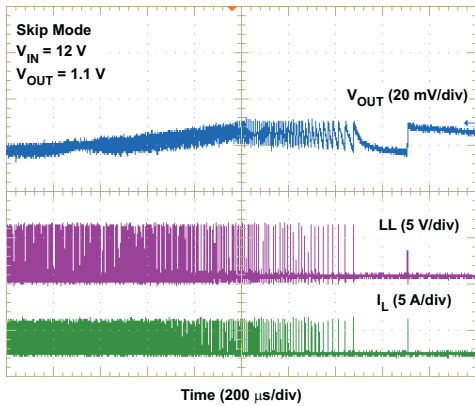


Figure 25. CCM to DCM Transition Waveforms

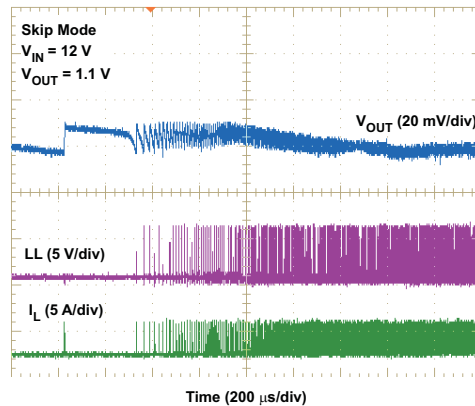


Figure 26. DCM to CCM Transition Waveforms

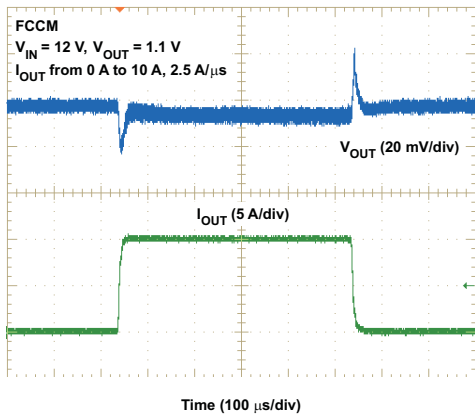


Figure 27. FCCM Load Transient

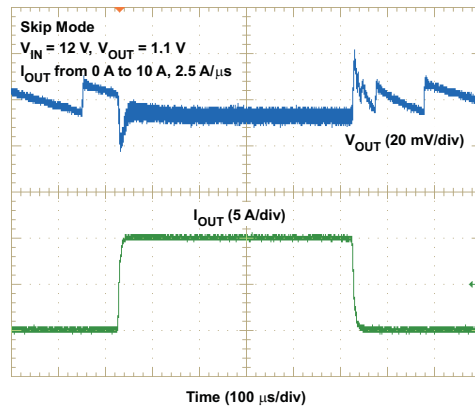


Figure 28. Skip Mode Load Transient

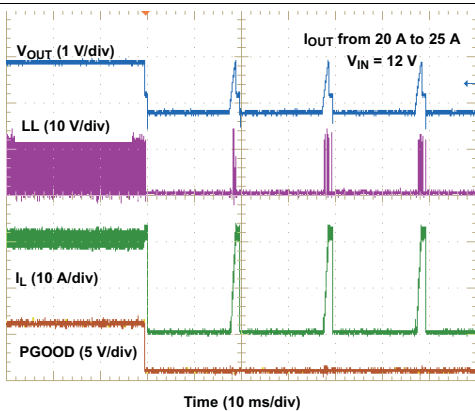


Figure 29. Overcurrent Protection Waveforms

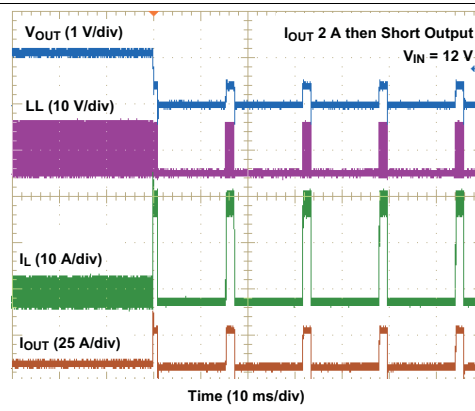


Figure 30. Output Short Circuit Protection Waveforms

Typical Characteristics (continued)

For  $V_{OUT} = 5\text{ V}$ , a 744355182 inductor is used. For  $1 \leq V_{OUT} \leq 3.3\text{ V}$ , a PA0513.441 inductor is used.

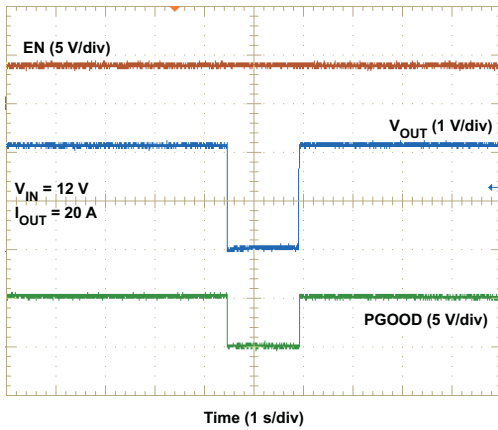


Figure 31. Over-temperature Protection Waveforms

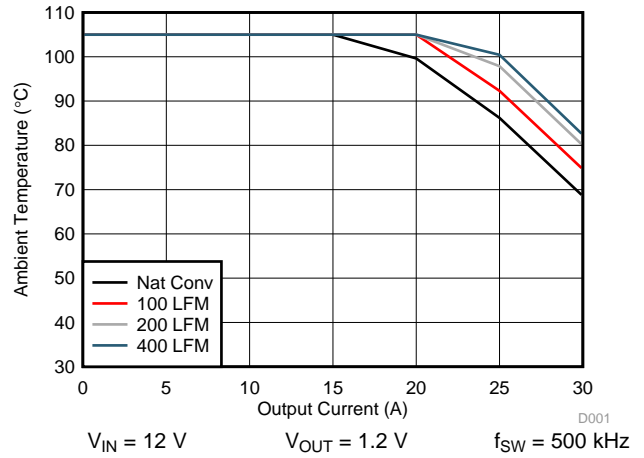


Figure 32. Safe Operating Area

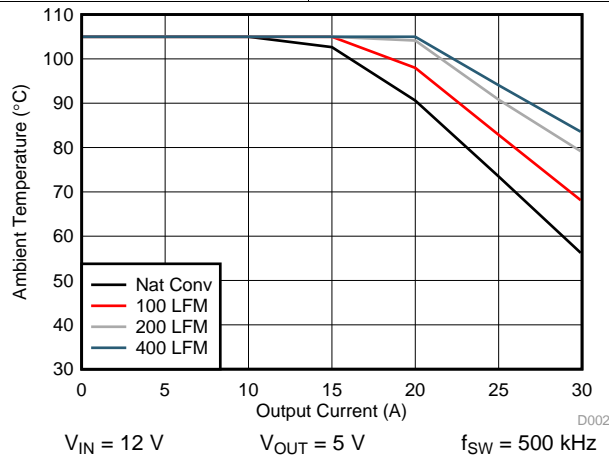


Figure 33. Safe Operating Area

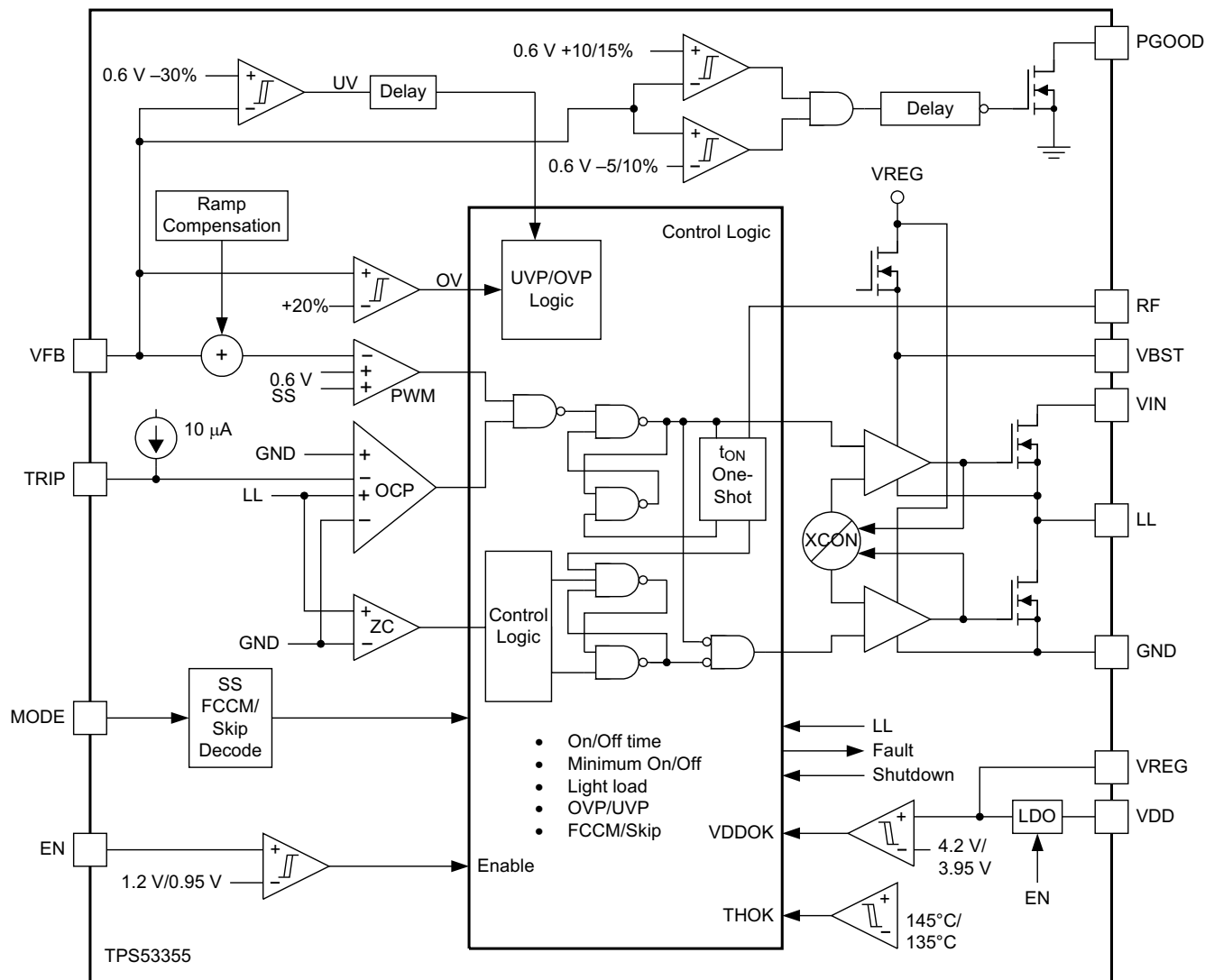
## 7 Detailed Description

### 7.1 Overview

The TPS53355 is a high-efficiency, single channel, synchronous buck converter suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP™ mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 1.5 V up to 15 V and the VDD bias voltage is from 4.5 V to 25 V. The D-CAP™ mode uses the equivalent series resistance (ESR) of the output capacitor(s) to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

The TPS53355 has a MODE pin to select between auto-skip mode and forced continuous conduction mode (FCCM) for light load conditions. The MODE pin also sets the selectable soft-start time ranging from 0.7 ms to 5.6 ms as shown in [Table 3](#).

## 7.2 Functional Block Diagram



### NOTE

The thresholds in this block diagram are typical values. Refer to the [Electrical Characteristics](#) table for threshold limits.

## 7.3 Feature Description

### 7.3.1 5-V LDO and VREG Start-Up

TPS53355 provides an internal 5-V LDO function using input from VDD and output to VREG. When the VDD voltage rises above 2 V, the internal LDO is enabled and outputs voltage to the VREG pin. The VREG voltage provides the bias voltage for the internal analog circuitry and also provides the supply voltage for the gate drives.

#### NOTE

The 5-V LDO is controlled by the EN pin. The LDO starts-up any time VDD rises to approximately 2 V. [Figure 34](#)

### 7.3.2 Adaptive On-Time D-CAP Control and Frequency Selection

The TPS53355 does not have a dedicated oscillator to determine switching frequency. However, the device operates with pseudo-constant frequency by feed-forwarding the input and output voltages into the on-time one-shot timer. The adaptive on-time control adjusts the on-time to be inversely proportional to the input voltage and proportional to the output voltage ( $t_{ON} \propto V_{OUT}/V_{IN}$ ).

This makes the switching frequency fairly constant in steady state conditions over a wide input voltage range. The switching frequency is selectable from eight preset values by a resistor connected between the RF pin and GND or between the RF pin and the VREG pin as shown in [Table 1](#). (Maintaining open resistance sets the switching frequency to 500 kHz.)

**Table 1. Resistor and Switching Frequency**

RESISTOR ( $R_{RF}$ ) CONNECTIONS		SWITCHING FREQUENCY ( $f_{sw}$ ) (kHz)
VALUE (k $\Omega$ )	CONNECT TO	
0	GND	250
187	GND	300
619	GND	400
OPEN	n/a	500
866	VREG	650
309	VREG	750
124	VREG	850
0	VREG	970

The off-time is modulated by a PWM comparator. The VFB node voltage (the mid-point of resistor divider) is compared to the internal 0.6-V reference voltage added with a ramp signal. When both signals match, the PWM comparator asserts a set signal to terminate the off time (turn off the low-side MOSFET and turn on high-side MOSFET). The set signal is valid if the inductor current level is below the OCP threshold, otherwise the off time is extended until the current level falls below the threshold.

[Figure 35](#) and [Figure 36](#) show two on-time control schemes.



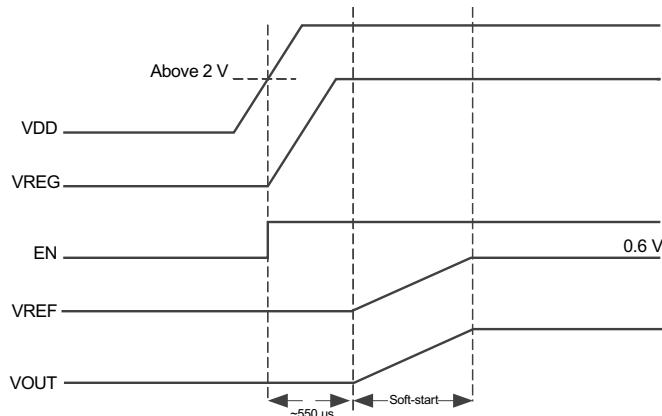


Figure 34. Power Up Sequence

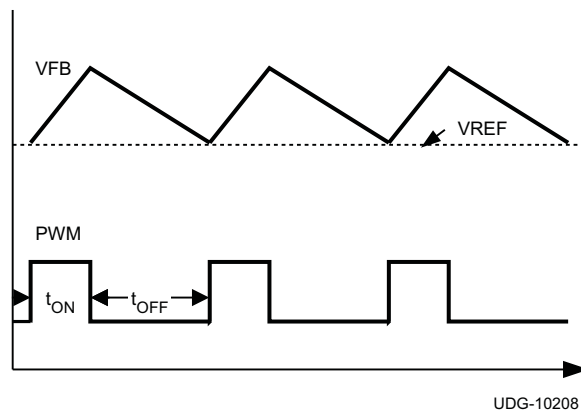


Figure 35. On-Time Control Without Ramp Compensation

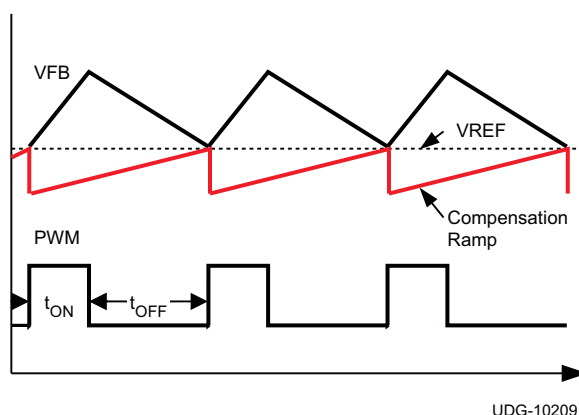


Figure 36. On-Time Control With Ramp Compensation

### 7.3.3 Ramp Signal

The TPS53355 adds a ramp signal to the 0.6-V reference in order to improve jitter performance. As described in the previous section, the feedback voltage is compared with the reference information to keep the output voltage in regulation. By adding a small ramp signal to the reference, the signal-to-noise ratio at the onset of a new switching cycle is improved. Therefore the operation becomes less jittery and more stable. The ramp signal is controlled to start with  $-7$  mV at the beginning of an on-cycle and becomes 0 mV at the end of an off-cycle in steady state.

During skip mode operation, under discontinuous conduction mode (DCM), the switching frequency is lower than the nominal frequency and the off-time is longer than the off-time in CCM. Because of the longer off-time, the ramp signal extends after crossing 0 mV. However, it is clamped at 3 mV to minimize the DC offset.

### 7.3.4 Adaptive Zero Crossing

The TPS53355 has an adaptive zero crossing circuit which performs optimization of the zero inductor current detection at skip mode operation. This function pursues ideal low-side MOSFET turning off timing and compensates inherent offset voltage of the Z-C comparator and delay time of the Z-C detection circuit. It prevents SW-node swing-up caused by too late detection and minimizes diode conduction period caused by too early detection. As a result, better light load efficiency is delivered.

### 7.3.5 Power-Good

The TPS53355 has power-good output that indicates high when switcher output is within the target. The power-good function is activated after soft-start has finished. If the output voltage becomes within  $+10\%$  and  $-5\%$  of the target value, internal comparators detect power-good state and the power-good signal becomes high after a 1-ms internal delay. If the output voltage goes outside of  $+15\%$  or  $-10\%$  of the target value, the power-good signal becomes low after two microsecond ( $2\text{-}\mu\text{s}$ ) internal delay. The power-good output is an open drain output and must be pulled up externally.

The power-good MOSFET is powered through the VDD pin.  $V_{VDD}$  must be >1 V in order to have a valid power-good logic. It is recommended to pull PGOOD up to VREG (or a voltage divided from VREG) so that the power-good logic is still valid even without VDD supply.

### 7.3.6 Current Sense, Overcurrent and Short Circuit Protection

TPS53355 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the *OFF* state and the controller maintains the *OFF* state during the period in that the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, TPS53355 supports temperature compensated MOSFET  $R_{DS(on)}$  sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor,  $R_{TRIP}$ . The TRIP terminal sources current ( $I_{TRIP}$ ) which is 10  $\mu$ A typically at room temperature, and the trip level is set to the OCL trip voltage  $V_{TRIP}$  as shown in Equation 1.

$$V_{TRIP} \text{ (mV)} = R_{TRIP} \text{ (k}\Omega\text{)} \times I_{TRIP} \text{ (}\mu\text{A)} \quad (1)$$

The inductor current is monitored by the LL pin. The GND pin is used as the positive current sensing node and the LL pin is used as the negative current sense node. The trip current,  $I_{TRIP}$  has 4700ppm/ $^{\circ}$ C temperature slope to compensate the temperature dependency of the  $R_{DS(on)}$ .

As the comparison is made during the *OFF* state,  $V_{TRIP}$  sets the valley level of the inductor current. Thus, the load current at the overcurrent threshold,  $I_{OCP}$ , can be calculated as shown in Equation 2.

$$I_{OCP} = \frac{V_{TRIP}}{(32 \times R_{DS(on)})} + \frac{I_{IND(ripple)}}{2} = \frac{V_{TRIP}}{(32 \times R_{DS(on)})} + \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

In an overcurrent or short circuit condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to decrease. Eventually, it crosses the undervoltage protection threshold and shuts down. After a hiccup delay (16 ms with 0.7 ms sort-start), the controller restarts. If the overcurrent condition remains, the procedure is repeated and the device enters hiccup mode.

Hiccup time calculation:

$$t_{HIC(wait)} = (2^n + 257) \times 4 \mu\text{s}$$

where

- $n = 8, 9, 10, \text{ or } 11$  depending on soft start time selection (3)

$$t_{HIC(dly)} = 7 \times (2^n + 257) \times 4 \mu\text{s} \quad (4)$$

**Table 2. Hiccup Delay**

SELECTED SOFT-START TIME ( $t_{SS}$ ) (ms)	n	HICCUP WAIT TIME ( $t_{HIC(wait)}$ ) (ms)	HICCUP DELAY TIME ( $t_{HIC(dly)}$ ) (ms)
0.7	8	2.052	14.364
1.4	9	3.076	21.532
2.8	10	5.124	35.868
5.6	11	9.220	64.540

### 7.3.7 Overvoltage and Undervoltage Protection

TPS53355 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 1ms, TPS53355 latches OFF both high-side and low-side MOSFETs drivers. The controller restarts after a hiccup delay (16 ms with 0.7 ms soft-start). This function is enabled 1.5-ms after the soft-start is completed.

When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches OFF the high-side MOSFET driver and latches ON the low-side MOSFET driver. The output voltage decreases. If the output voltage reaches UV threshold, then both high-side MOSFET and low-side MOSFET driver will be OFF and the device restarts after a hiccup delay. If the OV condition remains, both high-side MOSFET and low-side MOSFET driver remains OFF until the OV condition is removed.

### 7.3.8 UVLO Protection

The TPS53355 uses VREG undervoltage lockout protection (UVLO). When the VREG voltage is lower than 3.95 V, the device shuts off. When the VREG voltage is higher than 4.2 V, the device restarts. This is a non-latch protection.

### 7.3.9 Thermal Shutdown

TPS53355 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 145°C), TPS53355 is shut off. When the temperature falls about 10°C below the threshold value, the device will turn back on. This is a non-latch protection.

## 7.4 Device Functional Modes

### 7.4.1 Enable, Soft Start, and Mode Selection

When the EN pin voltage rises above the enable threshold voltage (typically 1.2 V), the controller enters its start-up sequence. The internal LDO regulator starts immediately and regulates to 5 V at the VREG pin. The controller then uses the first 250  $\mu$ s to calibrate the switching frequency setting resistance attached to the RF pin and stores the switching frequency code in internal registers. During this period, the MODE pin also senses the resistance attached to this pin and determines the soft-start time. Switching is inhibited during this phase. In the second phase, an internal DAC starts ramping up the reference voltage from 0 V to 0.6 V. Depending on the MODE pin setting, the ramping up time varies from 0.7 ms to 5.6 ms. Smooth and constant ramp-up of the output voltage is maintained during start-up regardless of load current.

**Table 3. Soft-Start and MODE Settings**

MODE SELECTION	ACTION	SOFT-START TIME (ms)	R <sub>MODE</sub> (k $\Omega$ )
Auto Skip	Pull down to GND	0.7	39
		1.4	100
		2.8	200
		5.6	475
Forced CCM <sup>(1)</sup>	Connect to PGOOD	0.7	39
		1.4	100
		2.8	200
		5.6	475

(1) Device enters FCCM after the PGOOD pin goes high when MODE is connected to PGOOD through the resistor R<sub>MODE</sub>.

After soft start begins, the MODE pin becomes the input of an internal comparator which determines auto skip or FCCM mode operation. If MODE voltage is higher than 1.3 V, the converter enters into FCCM mode. Otherwise it will be in auto skip mode at light load condition. Typically, when FCCM mode is selected, the MODE pin is connected to PGOOD through the R<sub>MODE</sub> resistor, so that before PGOOD goes high the converter remains in auto skip mode.

### 7.4.2 Auto-Skip Eco-mode™ Light Load Operation

While the MODE pin is pulled low via  $R_{MODE}$ , TPS53355 automatically reduces the switching frequency at light load conditions to maintain high efficiency. Detailed operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The synchronous MOSFET is turned off when this zero inductor current is detected. As the load current further decreases, the converter runs into discontinuous conduction mode (DCM). The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light-load operation  $I_{OUT(LL)}$  (i.e., the threshold between continuous and discontinuous conduction mode) can be calculated as shown in [Equation 5](#).

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- $f_{SW}$  is the PWM switching frequency (5)

Switching frequency versus output current in the light load condition is a function of  $L$ ,  $V_{IN}$  and  $V_{OUT}$ , but it decreases almost proportionally to the output current from the  $I_{OUT(LL)}$  given in [Equation 5](#). For example, it is 60 kHz at  $I_{OUT(LL)}/5$  if the frequency setting is 300 kHz.

### 7.4.3 Forced Continuous Conduction Mode

When the MODE pin is tied to PGOOD through a resistor, the controller keeps continuous conduction mode (CCM) in light load condition. In this mode, switching frequency is kept almost constant over the entire load range which is suitable for applications that need tight control of the switching frequency at a cost of lower efficiency.

## 8 Application and Implementation

### NOTE

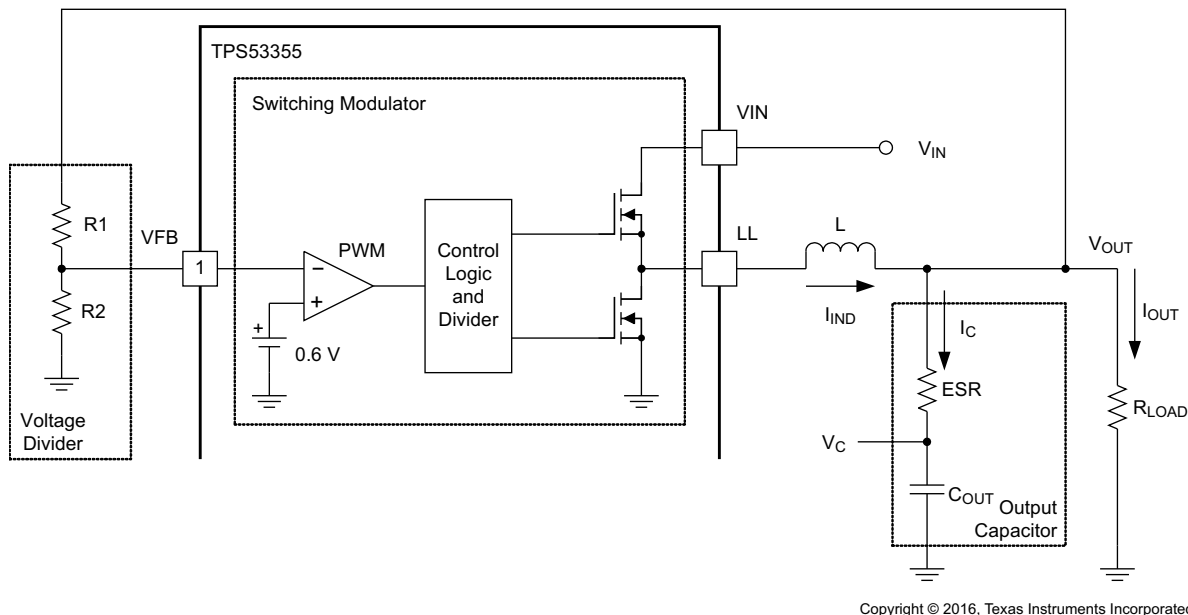
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS53355 is a high-efficiency, single channel, synchronous buck converter suitable for low output voltage point-of-load applications in computing and similar digital consumer applications. The device features proprietary D-CAP mode control combined with an adaptive on-time architecture. This combination is ideal for building modern low duty ratio, ultra-fast load step response DC-DC converters. The output voltage ranges from 0.6 V to 5.5 V. The conversion input voltage range is from 1.5 V up to 15 V and the VDD bias voltage is from 4.5 V to 25 V. The D-CAP mode uses the equivalent series resistance (ESR) of the output capacitor(s) to sense the device current. One advantage of this control scheme is that it does not require an external phase compensation network. This allows a simple design with a low external component count. Eight preset switching frequency values can be chosen using a resistor connected from the RF pin to ground or VREG. Adaptive on-time control tracks the preset switching frequency over a wide input and output voltage range while allowing the switching frequency to increase at the step-up of the load.

#### 8.1.1 Small Signal Model

From small-signal loop analysis, a buck converter using D-CAP™ mode can be simplified as shown in [Figure 37](#).



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**Figure 37. Simplified Modulator Model**

The output voltage is compared with the internal reference voltage (ramp signal is ignored here for simplicity). The PWM comparator determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator can be assumed high enough to keep the voltage at the beginning of each on cycle substantially constant.

$$H(s) = \frac{1}{s \times \text{ESR} \times C_{\text{OUT}}} \quad (6)$$

## Application Information (continued)

For loop stability, the 0-dB frequency,  $f_0$ , defined below need to be lower than 1/4 of the switching frequency.

$$f_0 = \frac{1}{2\pi \times \text{ESR} \times C_{\text{OUT}}} \leq \frac{f_{\text{SW}}}{4} \tag{7}$$

According to the equation above, the loop stability of D-CAP™ mode modulator is mainly determined by the capacitor's chemistry. For example, specialty polymer capacitors (SP-CAP) have an output capacitance in the order of several 100  $\mu\text{F}$  and ESR in range of 10  $\text{m}\Omega$ . These makes  $f_0$  on the order of 100 kHz or less, creating a stable loop. However, ceramic capacitors have an  $f_0$  at more than 700 kHz, and need special care when used with this modulator. An application circuit for ceramic capacitor is described in [External Component Selection Using All Ceramic Output Capacitors](#).

## 8.2 Typical Applications

### 8.2.1 Typical Application Circuit Diagram with Ceramic Output Capacitors

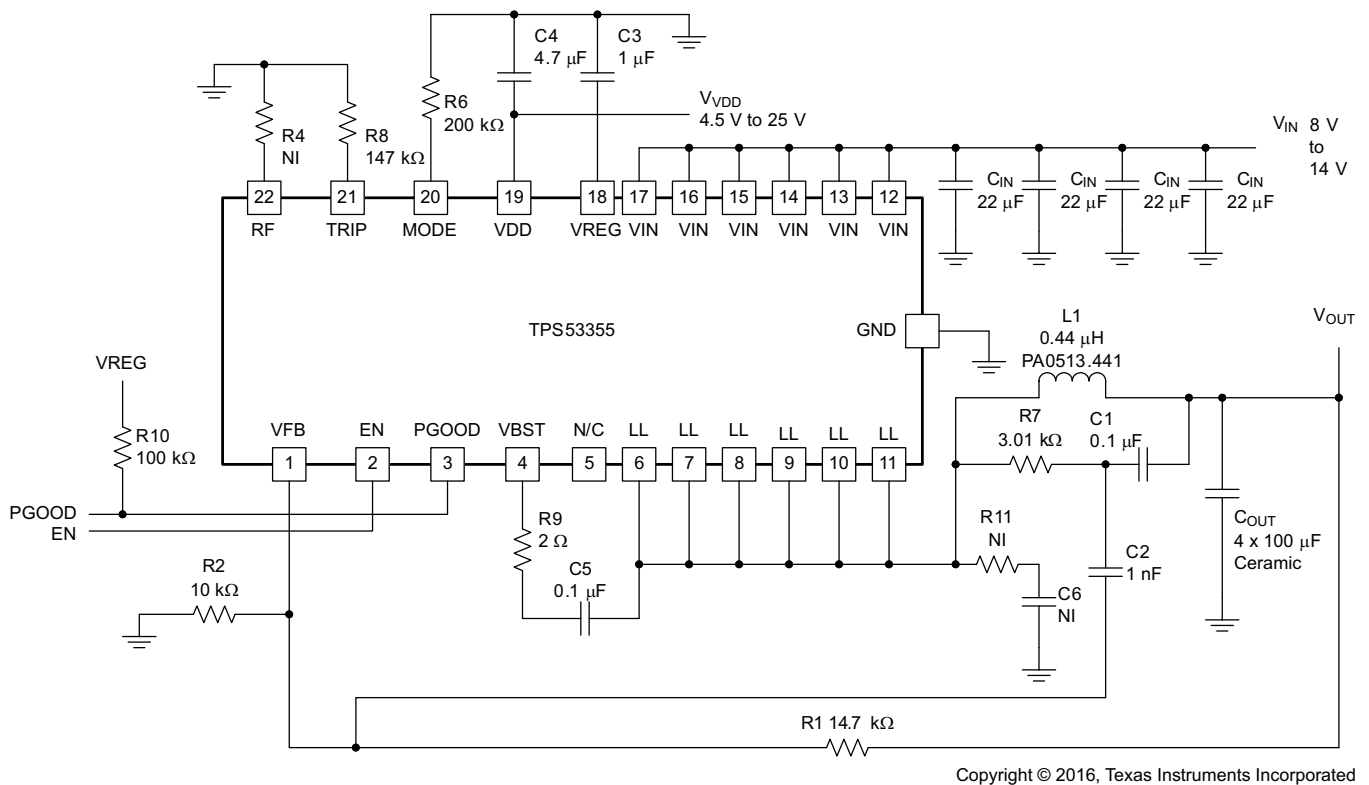


Figure 38. Typical Application Circuit Diagram with Ceramic Output Capacitors Schematic

## Typical Applications (continued)

### 8.2.1.1 Design Requirements

**Table 4. Design Parameters**

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>						
$V_{IN}$	Voltage range		8	12	14	V
$I_{MAX}$	Maximum input current	$V_{IN} = 8\text{ V}, I_{OUT} = 30\text{ A}$		6.3		A
	No load input current	$V_{IN} = 14\text{ V}, I_{OUT} = 0\text{ A}$ with auto-skip mode		1		mA
<b>OUTPUT CHARACTERISTICS</b>						
$V_{OUT}$	Output voltage			1.5		
	Output voltage regulation	Line regulation, $8\text{ V} \leq V_{IN} \leq 15\text{ V}$		0.1%		
		Load regulation, $V_{IN} = 12\text{ V}, 0\text{ A} \leq I_{OUT} \leq 30\text{ A}$ with FCCM			0.2%	
$V_{RIPPLE}$	Output voltage ripple	$V_{IN} = 12\text{ V}, I_{OUT} = 30\text{ A}$ with FCCM		20		mV <sub>PP</sub>
$I_{LOAD}$	Output load current		0		30	A
$I_{OCP}$	Output overcurrent threshold			34		A
$t_{SS}$	Soft-start time			1.4		ms
<b>SYSTEMS CHARACTERISTICS</b>						
$f_{SW}$	Switching frequency			500		kHz
$\eta$	Peak efficiency	$V_{IN} = 12\text{ V}, V_{OUT} = 1.1\text{ V}, I_{OUT} = 10\text{ A}$		91.87%		
	Full load efficiency	$V_{IN} = 12\text{ V}, V_{OUT} = 1.1\text{ V}, I_{OUT} = 30\text{ A}$		89.46%		
$T_A$	Operating temperature			25		°C

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS53355 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ( $V_{IN}$ ), output voltage ( $V_{OUT}$ ), and output current ( $I_{OUT}$ ) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

### 8.2.1.2.2 External Component Selection

The external components selection is a simple process when using organic semiconductors or special polymer output capacitors.

#### 1. Select operation mode and soft-start time

Select operation mode and soft-start time using [Table 3](#).

#### 2. Select switching frequency

Select the switching frequency from 250 kHz to 1 MHz using [Table 1](#).

#### 3. Choose the inductor

The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves signal-to-noise ratio and helps ensure stable operation, but increases inductor core loss. Using 1/3 ripple current to maximum output current ratio, the inductance can be determined by [Equation 8](#).

$$L = \frac{1}{I_{\text{IND(ripple)}} \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} = \frac{3}{I_{\text{OUT(max)}} \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} \quad (8)$$

The inductor requires a low DCR to achieve good efficiency. It also requires enough room above peak inductor current before saturation. The peak inductor current can be estimated in [Equation 9](#).

$$I_{\text{IND(peak)}} = \frac{V_{\text{TRIP}}}{32 \times R_{\text{DS(on)}}} + \frac{1}{L \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} \quad (9)$$

#### 4. External component selection with all ceramic output capacitors

Refer to [External Component Selection Using All Ceramic Output Capacitors](#) to select external components because ceramic output capacitors are used in this design.

#### 5. Choose the overcurrent setting resistor

The overcurrent setting resistor,  $R_{\text{TRIP}}$ , can be determined by [Equation 10](#).

$$R_{\text{TRIP}}(\text{k}\Omega) = \frac{\left( I_{\text{OCP}} - \left( \frac{1}{2 \times L \times f_{\text{SW}}} \right) \times \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN}}} \right) \times 32 \times R_{\text{DS(on)}}(\text{m}\Omega)}{I_{\text{TRIP}}(\mu\text{A})}$$

where

- $I_{\text{TRIP}}$  is the TRIP pin sourcing current (10  $\mu\text{A}$ )
- $R_{\text{DS(on)}}$  is the thermally compensated on-time resistance value of the low-side MOSFET (10)

Use an  $R_{\text{DS(on)}}$  value of 1.5 m $\Omega$  for an overcurrent level of approximately 30 A. Use an  $R_{\text{DS(on)}}$  value of 1.7 m $\Omega$  for overcurrent level of approximately 10 A.

### 8.2.1.2.3 External Component Selection Using All Ceramic Output Capacitors

When a ceramic output capacitor is used, the stability criteria in [Equation 7](#) cannot be satisfied. The ripple injection approach as shown in [Figure 38](#) is implemented to increase the ripple on the VFB pin and make the system stable. In addition to the selections made using steps 1 through step 6 in [External Component Selection](#), the ripple injection components must be selected. The C2 value can be fixed at 1 nF. The value of C1 can be selected between 10 nF to 200 nF.

$$\frac{L \times C_{\text{OUT}}}{R7 \times C1} > N \times \frac{t_{\text{ON}}}{2}$$

where

- N is the coefficient to account for L and  $C_{\text{OUT}}$  variation (11)



N is also used to provide enough margin for stability. It is recommended N=2 for  $V_{OUT} \leq 1.8\text{ V}$  and N=4 for  $V_{OUT} \geq 3.3\text{ V}$  or when  $L \leq 250\text{ nH}$ . The higher  $V_{OUT}$  needs a higher N value because the effective output capacitance is reduced significantly with higher DC bias. For example, a 6.3-V, 22- $\mu\text{F}$  ceramic capacitor may have only 8  $\mu\text{F}$  of effective capacitance when biased at 5 V.

Because the VFB pin voltage is regulated at the valley, the increased ripple on the VFB pin causes the increase of the VFB DC value. The AC ripple coupled to the VFB pin has two components, one coupled from SW node and the other coupled from the VOUT pin and they can be calculated using Equation 12 and Equation 13 when neglecting the output voltage ripple caused by equivalent series inductance (ESL).

$$V_{INJ\_SW} = \frac{V_{IN} - V_{OUT}}{R7 \times C1} \times \frac{D}{f_{SW}} \tag{12}$$

$$V_{INJ\_OUT} = ESR \times I_{IND(ripple)} + \frac{I_{IND(ripple)}}{8 \times C_{OUT} \times f_{SW}} \tag{13}$$

It is recommended that  $V_{INJ\_SW}$  to be less than 50 mV. If the calculated  $V_{INJ\_SW}$  is higher than 50 mV, then other parameters need to be adjusted to reduce it. For example,  $C_{OUT}$  can be increased to satisfy Equation 11 with a higher R7 value, thereby reducing  $V_{INJ\_SW}$ .

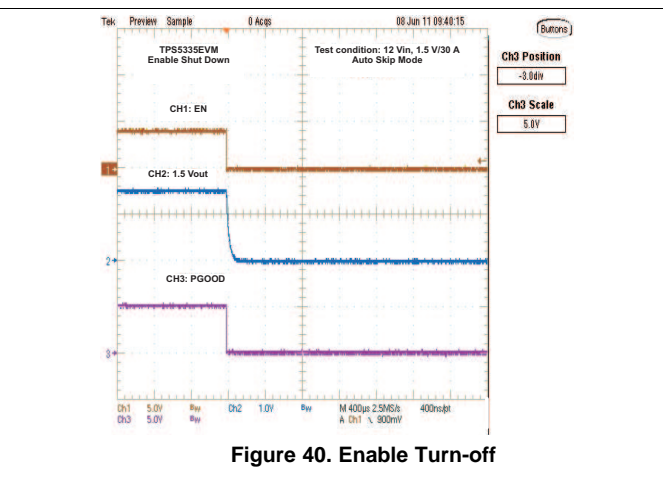
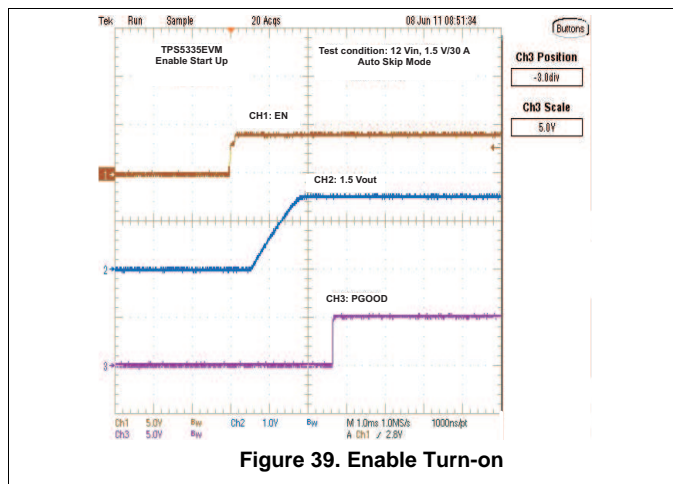
The DC voltage at the VFB pin can be calculated by Equation 14:

$$V_{VFB} = 0.6 + \frac{V_{INJ\_SW} + V_{INJ\_OUT}}{2} \tag{14}$$

And the resistor divider value can be determined by Equation 15:

$$R1 = \frac{V_{OUT} - V_{VFB}}{V_{VFB}} \times R2 \tag{15}$$

**8.2.1.3 Application Curves**



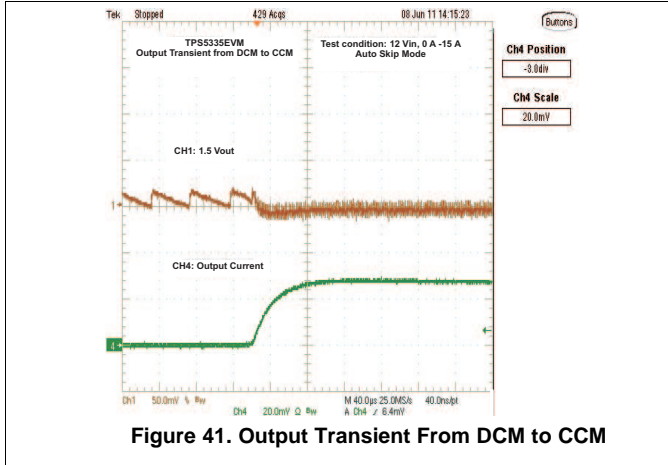


Figure 41. Output Transient From DCM to CCM

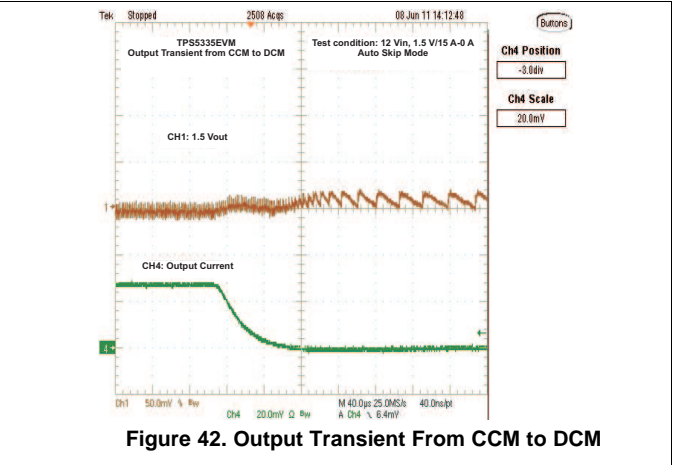


Figure 42. Output Transient From CCM to DCM

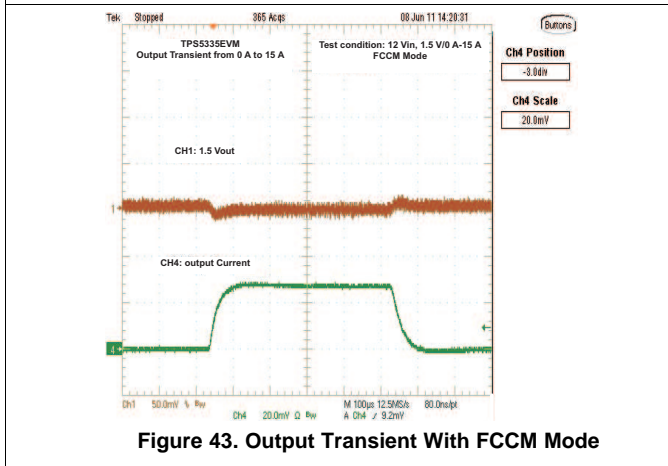


Figure 43. Output Transient With FCCM Mode

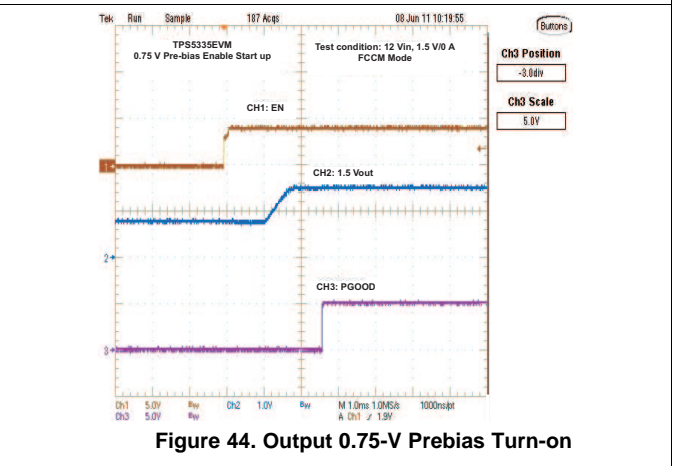


Figure 44. Output 0.75-V Prebias Turn-on

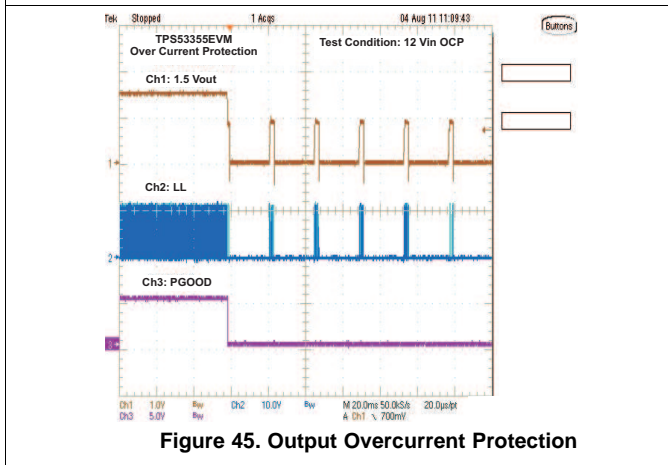


Figure 45. Output Overcurrent Protection

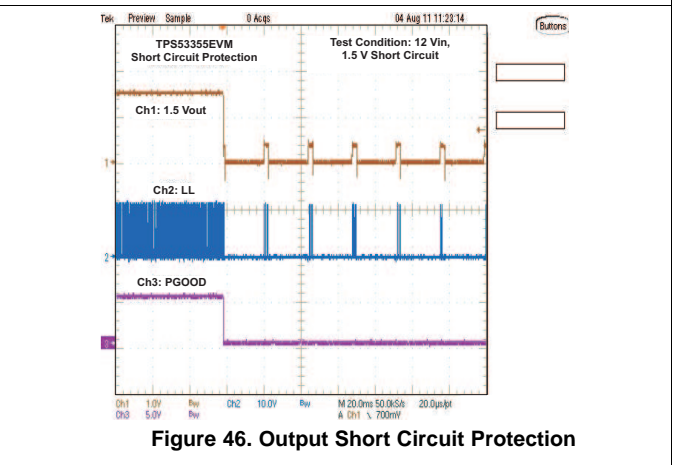


Figure 46. Output Short Circuit Protection

### 8.2.2 Typical Application Circuit

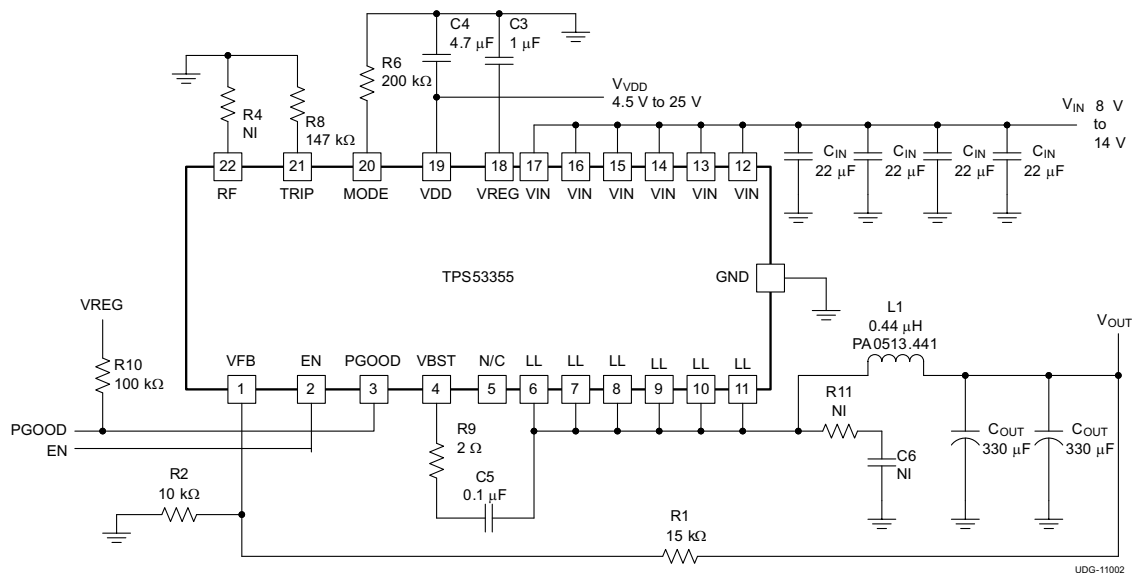


Figure 47. Typical Application Circuit Diagram

#### 8.2.2.1 Design Requirements

Table 5. Design Parameters

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>					
$V_{IN}$	Voltage range	8	12	14	V
$I_{MAX}$	Maximum input current	$V_{IN} = 8\text{ V}, I_{OUT} = 30\text{ A}$		6.3	A
	No load input current	$V_{IN} = 14\text{ V}, I_{OUT} = 0\text{ A}$ with auto-skip mode		1	mA
<b>OUTPUT CHARACTERISTICS</b>					
$V_{OUT}$	Output voltage			1.5	
	Output voltage regulation	Line regulation, $8\text{ V} \leq V_{IN} \leq 15\text{ V}$		0.1%	
Load regulation, $V_{IN} = 12\text{ V}, 0\text{ A} \leq I_{OUT} \leq 30\text{ A}$ with FCCM		0.2%			
$V_{RIPPLE}$	Output voltage ripple	$V_{IN} = 12\text{ V}, I_{OUT} = 30\text{ A}$ with FCCM		20	mV <sub>PP</sub>
$I_{LOAD}$	Output load current	0		30	A
$I_{OCP}$	Output overcurrent threshold		34		A
$t_{SS}$	Soft-start time		1.4		ms
<b>SYSTEMS CHARACTERISTICS</b>					
$f_{SW}$	Switching frequency		500		kHz
$\eta$	Peak efficiency	$V_{IN} = 12\text{ V}, V_{OUT} = 1.1\text{ V}, I_{OUT} = 10\text{ A}$		91.87%	
	Full load efficiency	$V_{IN} = 12\text{ V}, V_{OUT} = 1.1\text{ V}, I_{OUT} = 30\text{ A}$		89.46%	
$T_A$	Operating temperature		25		°C

## 8.2.2.2 Detailed Design Procedure

### 8.2.2.2.1 External Component Selection

Refer to [External Component Selection Using All Ceramic Output Capacitors](#) for guidelines for this design with all ceramic output capacitors.

The external components selection is a simple process when using organic semiconductors or special polymer output capacitors.

#### 1. Select operation mode and soft-start time

Select operation mode and soft-start time using [Table 3](#).

#### 2. Select switching frequency

Select the switching frequency from 250 kHz to 1 MHz using [Table 1](#).

#### 3. Choose the inductor

The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current. Larger ripple current increases output ripple voltage and improves signal-to-noise ratio and helps ensure stable operation, but increases inductor core loss. Using 1/3 ripple current to maximum output current ratio, the inductance can be determined by [Equation 16](#).

$$L = \frac{1}{I_{\text{IND(ripple)}} \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} = \frac{3}{I_{\text{OUT(max)}} \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} \quad (16)$$

The inductor requires a low DCR to achieve good efficiency. It also requires enough room above peak inductor current before saturation. The peak inductor current can be estimated in [Equation 9](#).

$$I_{\text{IND(peak)}} = \frac{V_{\text{TRIP}}}{32 \times R_{\text{DS(on)}}} + \frac{1}{L \times f_{\text{SW}}} \times \frac{(V_{\text{IN(max)}} - V_{\text{OUT}}) \times V_{\text{OUT}}}{V_{\text{IN(max)}}} \quad (17)$$

#### 4. Choose the output capacitors

When organic semiconductor capacitor(s) or specialty polymer capacitor(s) are used, for loop stability, capacitance and ESR should satisfy [Equation 7](#). For jitter performance, [Equation 18](#) is a good starting point to determine ESR.

$$\text{ESR} = \frac{V_{\text{OUT}} \times 10 \text{ mV} \times (1 - D)}{0.6 \text{ V} \times I_{\text{IND(ripple)}}} = \frac{10 \text{ mV} \times L \times f_{\text{SW}}}{0.6 \text{ V}} = \frac{L \times f_{\text{SW}}}{60} (\Omega)$$

where

- D is the duty factor.
- The required output ripple slope is approximately 10 mV per  $t_{\text{sw}}$  (switching period) in terms of VFB terminal voltage. (18)

**5. Determine the value of R1 and R2**

The output voltage is programmed by the voltage-divider resistor, R1 and R2 shown in Figure 37. R1 is connected between VFB pin and the output, and R2 is connected between the VFB pin and GND. Recommended R2 value is from 1 kΩ to 20 kΩ. Determine R1 using Equation 19.

$$R1 = \frac{V_{OUT} - \frac{I_{IND(ripple)} \times ESR}{2} - 0.6}{0.6} \times R2 \tag{19}$$

**6. Choose the overcurrent setting resistor**

The overcurrent setting resistor, R<sub>TRIP</sub>, can be determined by Equation 10.

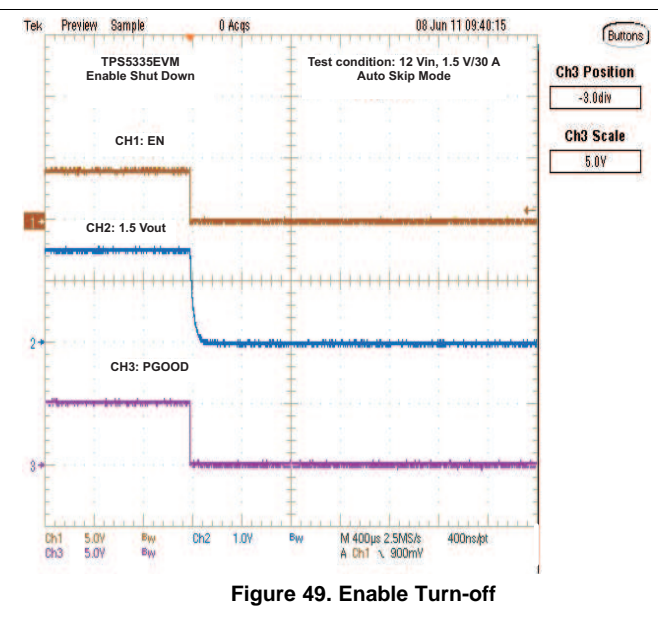
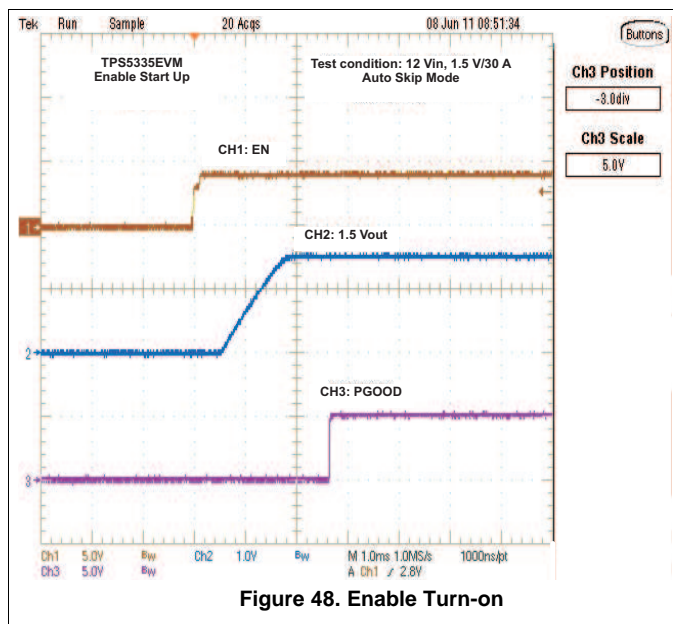
$$R_{TRIP}(k\Omega) = \frac{\left( I_{OCP} - \left( \frac{1}{2 \times L \times f_{SW}} \right) \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \right) \times 32 \times R_{DS(on)}(m\Omega)}{I_{TRIP}(\mu A)}$$

where

- I<sub>TRIP</sub> is the TRIP pin sourcing current (10 μA)
- R<sub>DS(on)</sub> is the thermally compensated on-time resistance value of the low-side MOSFET (20)

Use an R<sub>DS(on)</sub> value of 1.5 mΩ for an overcurrent level of approximately 30 A. Use an R<sub>DS(on)</sub> value of 1.7 mΩ for overcurrent level of approximately 10 A.

**8.2.2.3 Application Curves**



## 9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.5 V and 22 V (4.5-V to 25-V biased). This input supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in [Layout](#).

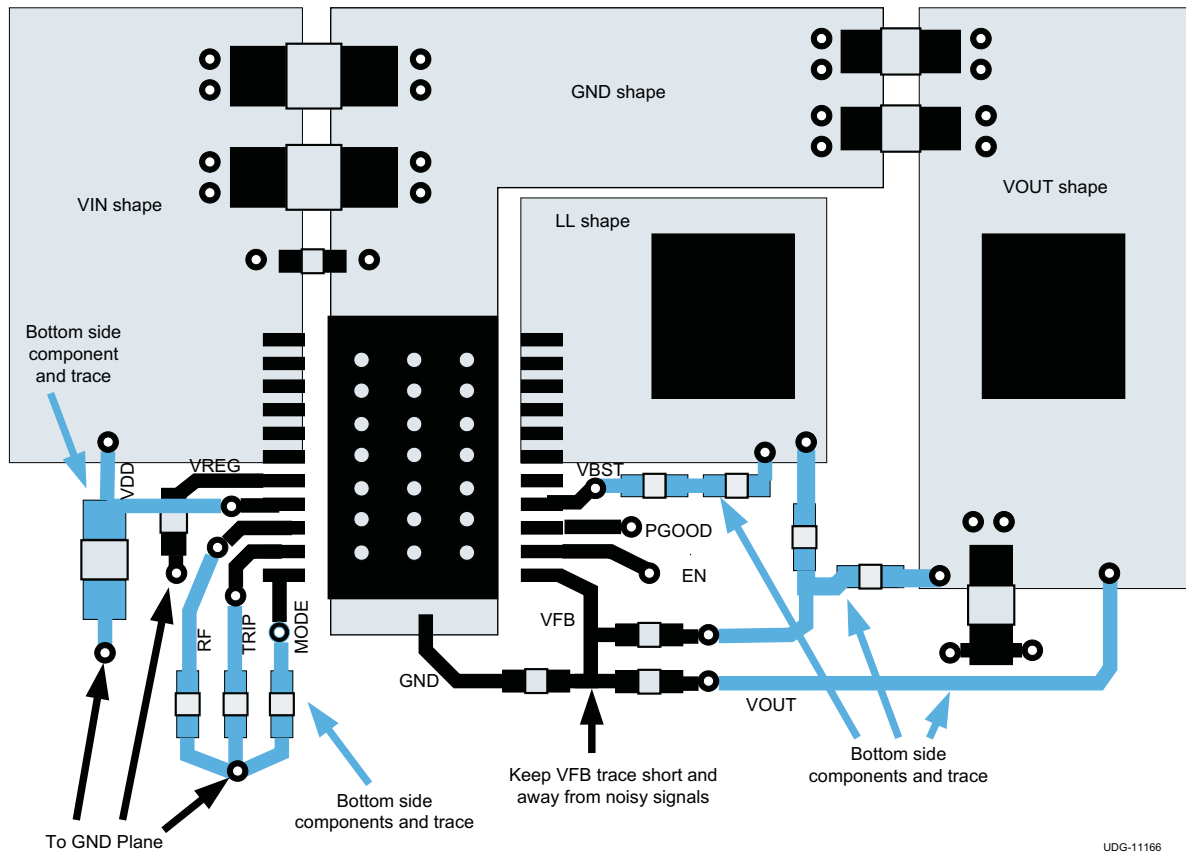
## 10 Layout

### 10.1 Layout Guidelines

Certain points must be considered before starting a layout work using the TPS53355.

- The power components (including input/output capacitors, inductor and TPS53355) must be placed on one side of the PCB (solder side). At least one inner plane should be inserted, connected to ground, in order to shield and isolate the small signal traces from noisy power lines.
- All sensitive analog traces and components such as VFB, PGOOD, TRIP, MODE and RF should be placed away from high-voltage switching nodes such as LL, VBST to avoid coupling. Use internal layer(s) as ground plane(s) and shield feedback trace from power traces and components.
- Place the VIN decoupling capacitors as close to the VIN and PGND pins as possible to minimize the input AC current loop.
- Because the TPS53355 controls output voltage referring to voltage across VOUT capacitor, the top-side resistor of the voltage divider should be connected to the positive node of the VOUT capacitor. Connect the GND of the bottom side resistor to the GND pad of the device. The trace from these resistors to the VFB pin should be short and thin.
- Place the frequency setting resistor ( $R_F$ ), OCP setting resistor ( $R_{TRIP}$ ) and mode setting resistor ( $R_{MODE}$ ) as close to the device as possible. Use the common GND via to connect them to GND plane if applicable.
- Place the VDD and VREG decoupling capacitors as close as possible to the device. Make sure GND vias are provided for each decoupling capacitor and make the loop as small as possible.
- The PCB trace defined as switch node, which connects the LL pins and high-voltage side of the inductor, should be as short and wide as possible.
- Connect the ripple injection  $V_{OUT}$  signal ( $V_{OUT}$  side of the C1 capacitor in [Figure 38](#)) from the terminal of ceramic output capacitor. The AC coupling capacitor (C2 in [Figure 38](#)) should be placed near the device, and R7 and C1 can be placed near the power stage.
- Use separate vias or trace to connect LL node to snubber, boot strap capacitor and ripple injection resistor. Do not combine these connections.

## 10.2 Layout Example



UDG-11166

Figure 50. Layout Recommendation



## 11 器件和文档支持

### 11.1 器件支持

#### 11.1.1 开发支持

##### 11.1.1.1 使用 WEBENCH® 工具创建定制设计

单击[此处](#)，使用 TPS53355 器件并借助 WEBENCH® 电源设计器创建定制设计。

1. 首先输入输入电压 ( $V_{IN}$ )、输出电压 ( $V_{OUT}$ ) 和输出电流 ( $I_{OUT}$ ) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 [www.ti.com.cn/WEBENCH](http://www.ti.com.cn/WEBENCH)。

### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的[通知我](#)进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.4 商标

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### 11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。



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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HPA01111DQPR	ACTIVE	LSON-CLIP	DQP	22	2500	Pb-Free (RoHS Exempt)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53355DQP	<a href="#">Samples</a>
TPS53355DQPR	ACTIVE	LSON-CLIP	DQP	22	2500	Pb-Free (RoHS Exempt)	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	53355DQP	<a href="#">Samples</a>
TPS53355DQPT	ACTIVE	LSON-CLIP	DQP	22	250	Pb-Free (RoHS Exempt)	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 125	53355DQP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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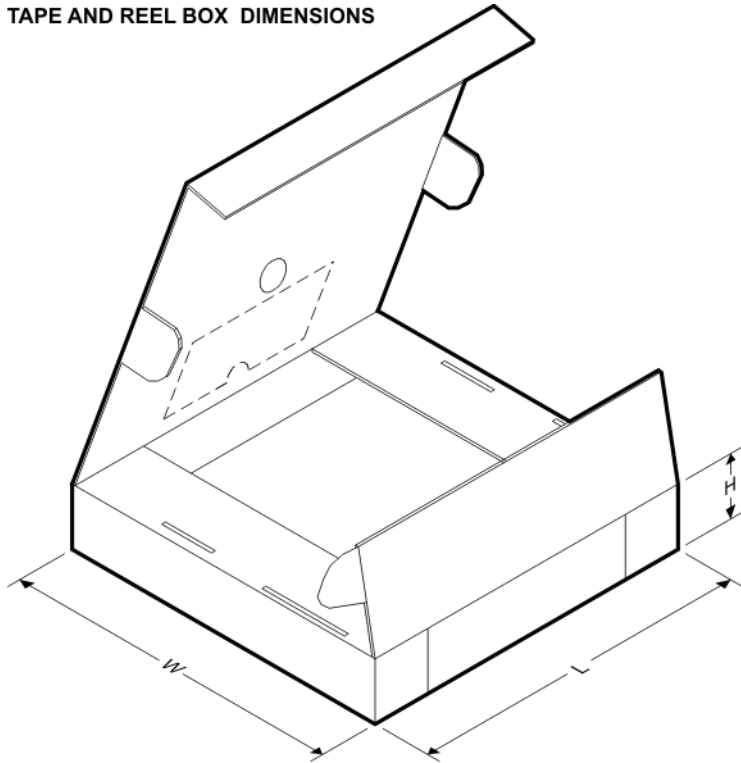
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53355DQPR	LSON-CLIP	DQP	22	2500	330.0	15.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53355DQPT	LSON-CLIP	DQP	22	250	330.0	15.4	5.3	6.3	1.8	8.0	12.0	Q1
TPS53355DQPT	LSON-CLIP	DQP	22	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q1

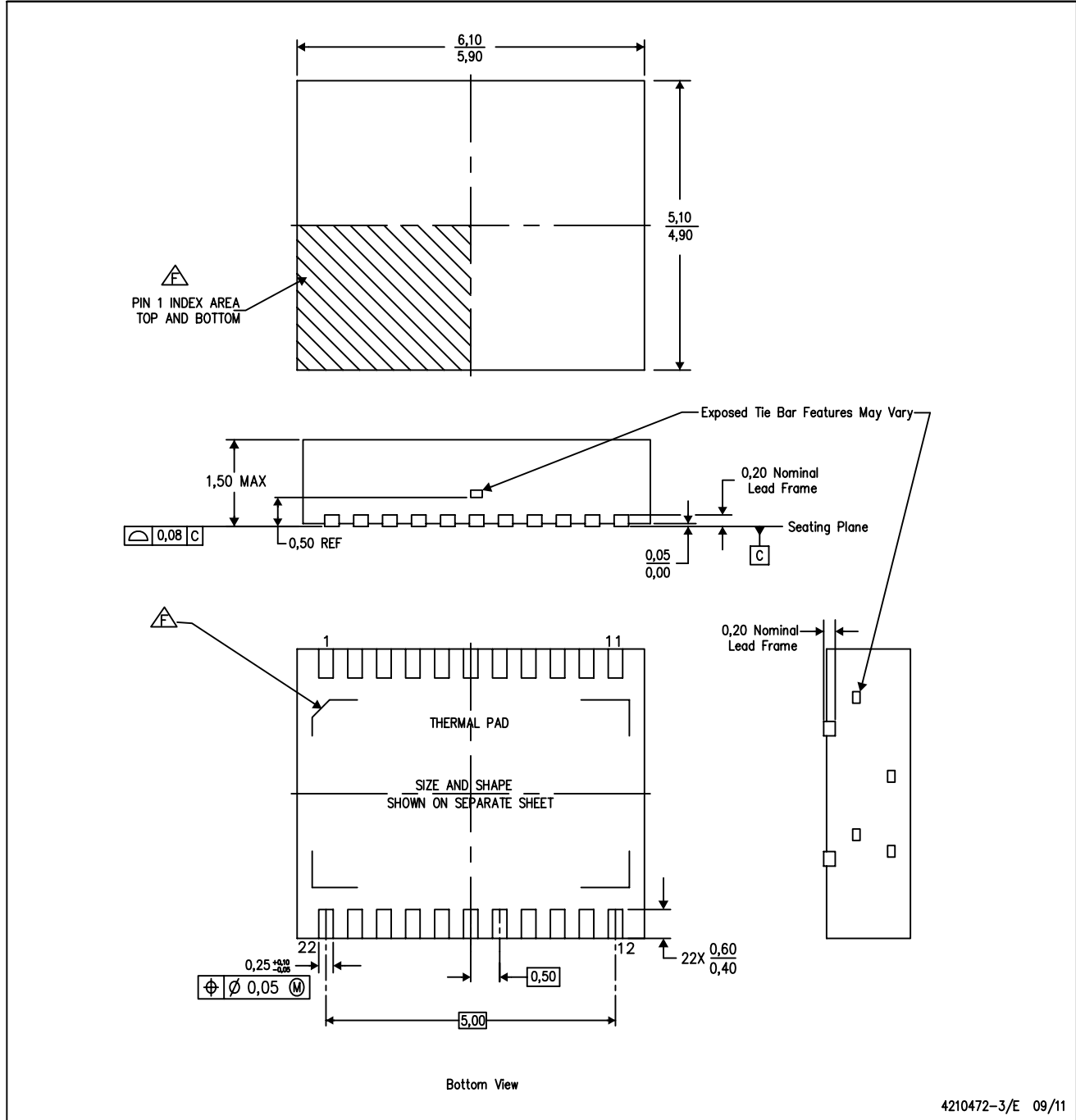
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53355DQPR	LSON-CLIP	DQP	22	2500	336.6	336.6	41.3
TPS53355DQPT	LSON-CLIP	DQP	22	250	336.6	336.6	41.3
TPS53355DQPT	LSON-CLIP	DQP	22	250	210.0	185.0	35.0

DQP (R-PSON-N22)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

# THERMAL PAD MECHANICAL DATA

DQP (R-PSO-N22)

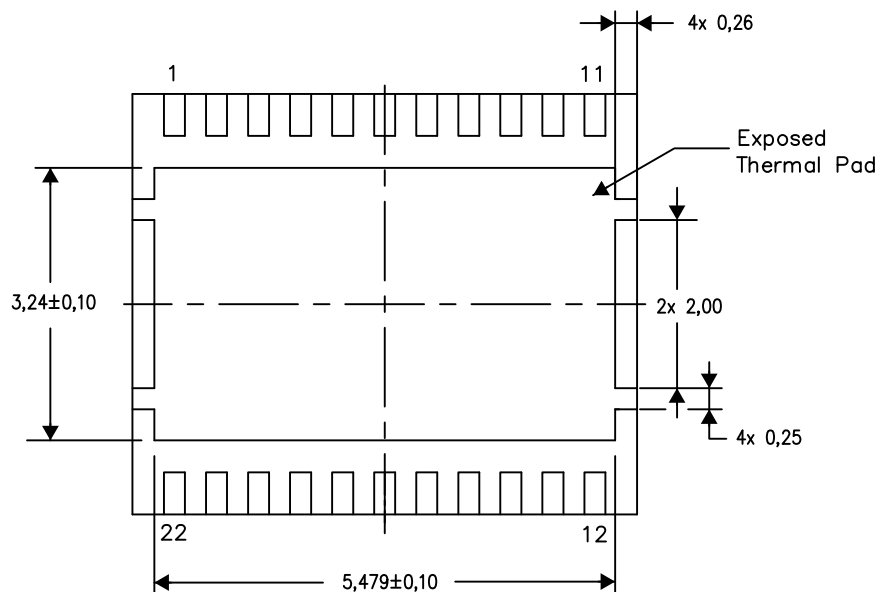
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

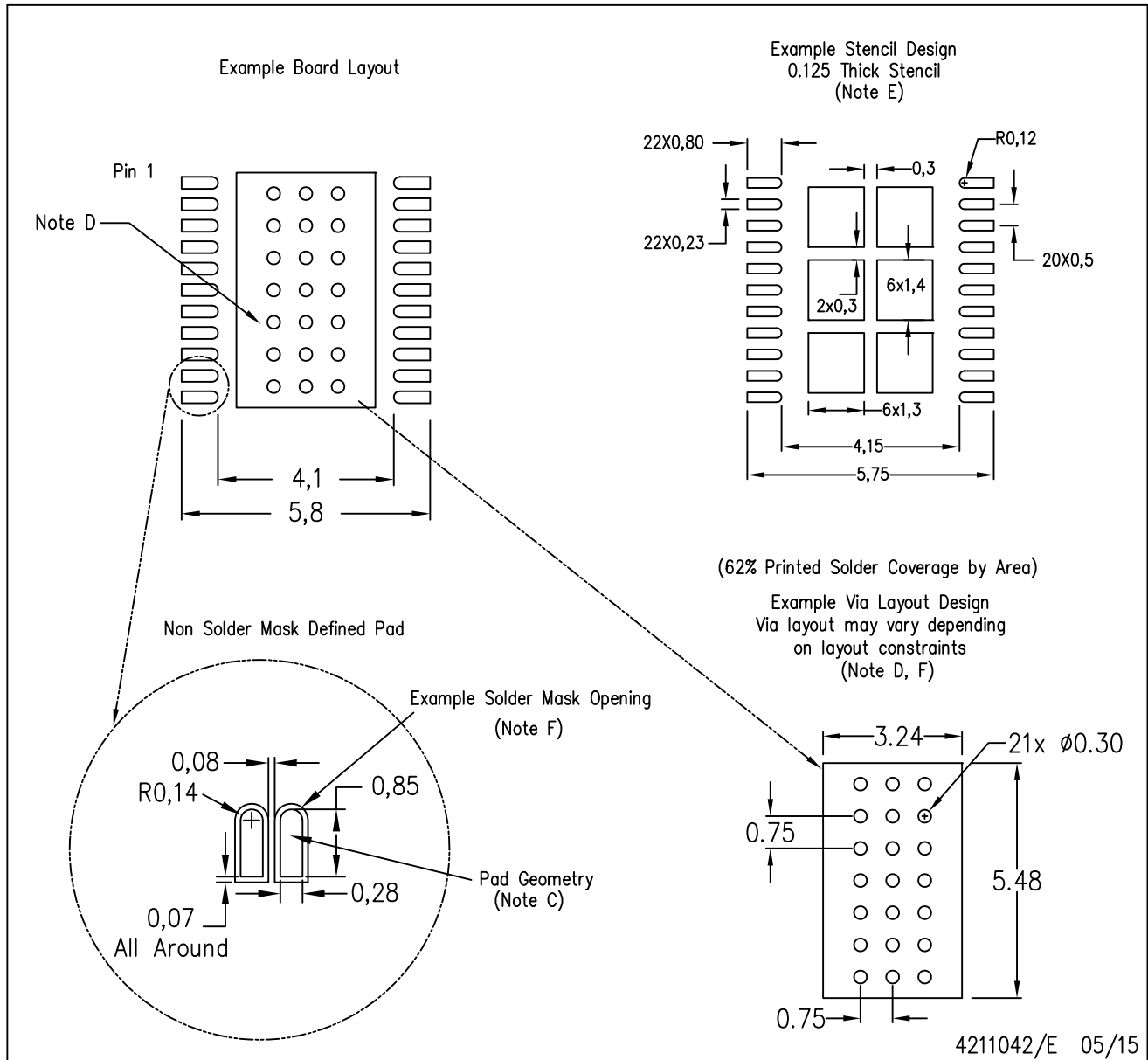
Exposed Thermal Pad Dimensions

4211024-3/H 08/15

NOTE: All linear dimensions are in millimeters

DQP (R-PSO-N22)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.



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