Features

- High Precision Reference Voltage
  0.5% Accuracy
  Optional Initial Voltage
  IIC Programmable Reference Voltage
- Optional IIC Address
- Selectable Control Mode
- Programmable Power Play Slew Rate
- Low External Component Count and Easy to use
- Small Footprint TSON8-3x3 package
- Green Product (RoHS, Lead-Free, Halogen-Free Compliant)

Applications

- Motherboards and Graphic Cards
- DC/DC Converters and Regulators

General Description

The GS8601-A is a programmable high precision voltage console. It features selectable control mode by virtue of the integrated IIC interface. The output voltage can be set by the external circuit, and also can be programmed from 0.6V to 1.875V with 5mV increments by 2-bit parallel VID interface (PVI) or series VID interface (SVI). The GS8601-A offers 3 selectable IIC address.

The GS8601-A also supports programmable output currents, and thus programmable voltage slew rate. Low external component count and space-saving package ensure the GS8601-A easy to use.

Typical Application

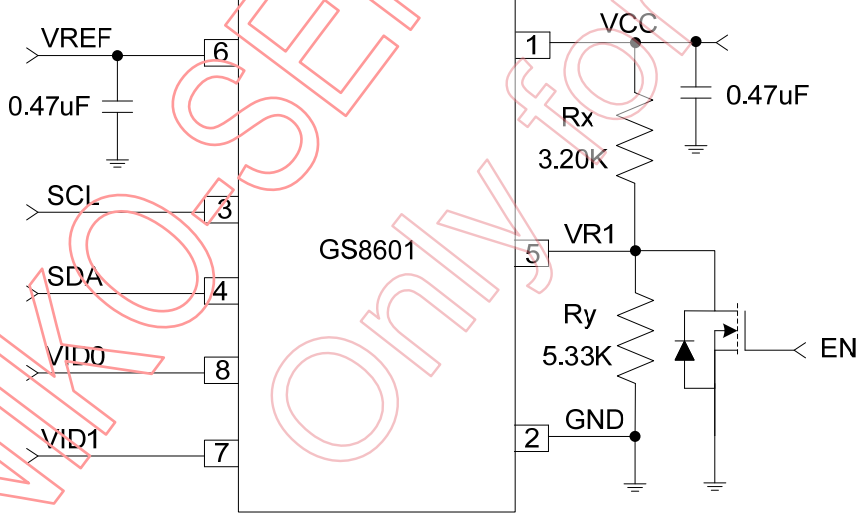


Figure 1 Typical Application of GS8601-A

Function Block Diagram

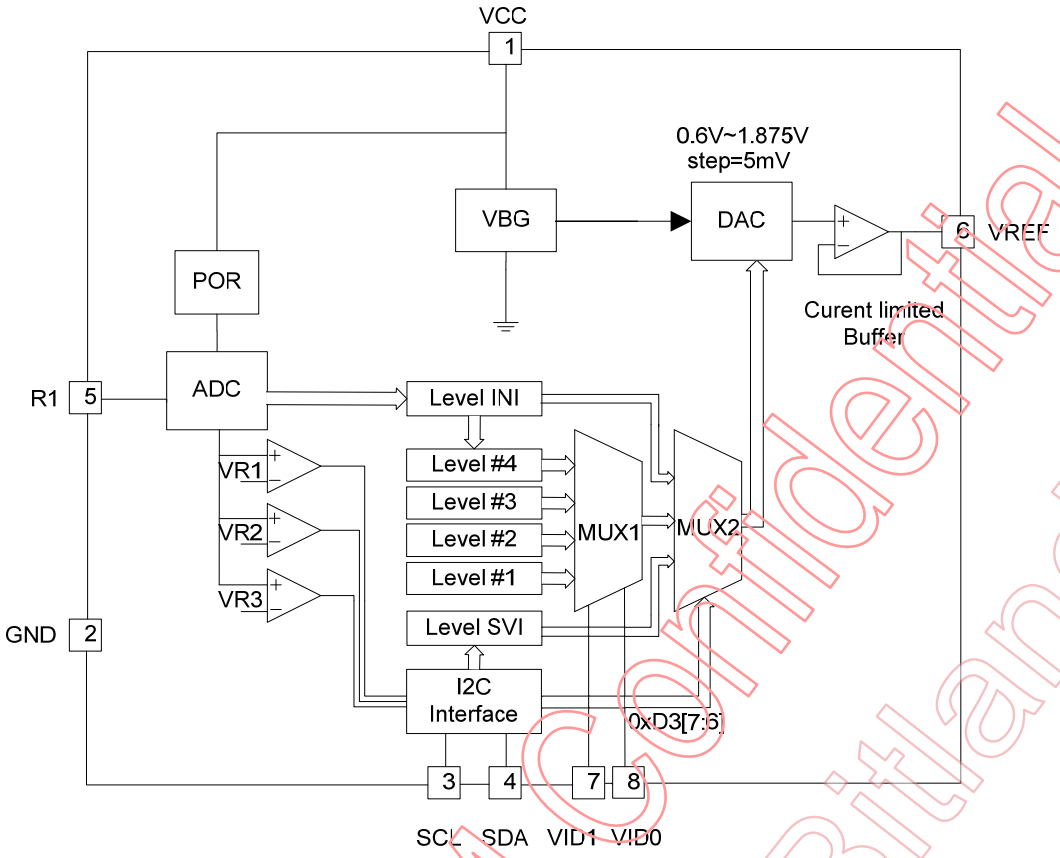


Figure 2 Function Block Diagram

Pin Configuration

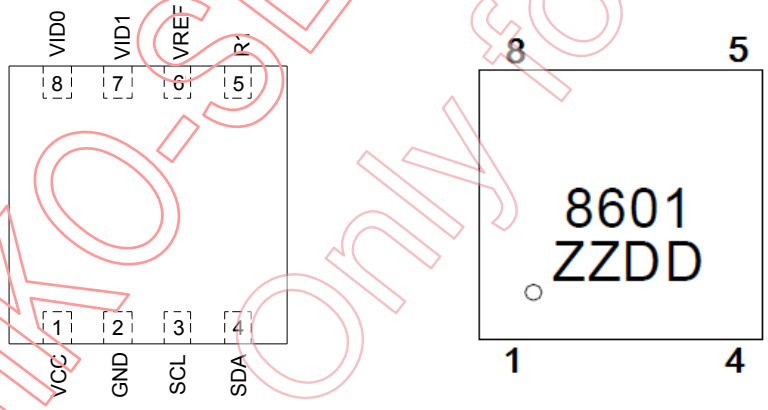


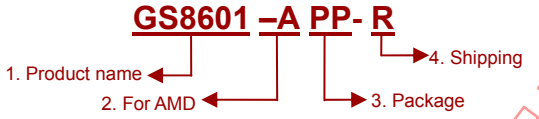
Figure 3 TSON8-3x3 Package

(Top view)

Pin Descriptions

No	Name	I/O type	Description
1	VCC	I	Supply Voltage Input. This pin is continuously monitored for POR. The POR threshold level is 2.8V with 0.2V hysteresis. Connect this pin to a 3.0V ~5.5V voltage source with a ceramic decoupling capacitor directly to GND pin.
2	GND		GND.
3	SCL	I	Serial Clock Input. This pin receives serial bus clock signal.
4	SDA	I/O	Serial Data Input and Output. This pin is input or output of serial bus data signal.
5	R1	I	Initial Output Voltage Setting and IIC Address Selecting. A voltage divider from VCC-to-R1-to-GND set the initial voltage for VREF and IIC address.
6	VREF	O	Reference Voltage Output. The reference voltage output can be programmed by IIC Bus.
7	VID1	I	VID Input 1 for PVI Mode. This pin is internally pulled low by a 10uA current source.
8	VID0	I	VID Input 0 for PVI Mode. This pin is internally pulled low by a 10uA current source.

Ordering Information



No	Item	Contents
1	Product name	GS8601
2	For AMD	-A
3	Package	TD: TSOIN8-3x3
4	Shipping	R: Tape & Reel

Example: GS8601-A TSOIN8-3x3 Tape & Reel ordering information is “GS8601-ATD-R”

Absolute Maximum Rating (Note 1)

Parameter	Symbol	Limits	Units
VCC to GND	V_{CC}	-0.3 < V_{IN}< 6	V
SDA 、SCL、VID1、VID0、R1、VREF to GND		-0.3 ~ 6	V
Package Power Dissipation at T_A≦25°C	$P_{D\_TSON8-3x3}$	952	mW
Storage Temperature	T_{STG}	- 65 ~ 150	°C
Lead Temperature (Soldering) 10S	T_{LEAD}	260	°C
ESD (Human Body Mode) (Note 2)	V_{ESD_HBM}	2K	V
ESD (Machine Mode) (Note 2)	V_{ESD_MM}	200	V

Thermal Information (Note 3)

Parameter	Symbol	Limits	Units
Thermal Resistance Junction to Ambient	$\theta_{JA\_TSON8-3x3}$	105	°C/W

Recommend Operating Condition (Note 4)

Parameter	Symbol	Limits	Units
VCC to GND	V_{CC}	3.0 to 5.5	V
Junction Temperature	T_J	- 40 ~ 125	°C
Operating Temperature Range	T_A	-40 ~ 85	°C

Electrical Characteristics

((VCC =+3V to 5V, T_A = -40°C to +85°C ,T_J= -40°C to +125°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Section						
Supply Voltage	V_{CC}		3.0		5.5	V
Supply Current	I_{CC}	VREF OPEN	0.5	1.0	1.5	mA
POR Threshold	V_{CC_RTH}		2.6	2.8	3.0	V
POR Hysteresis	V_{CC_HYS}			0.2		V
Output Section						
Initial Accuracy		0.6V to 0.8V	-10		+10	mV
		0.8V to 1.0V	-8		+8	mV
		1.0V to 1.875V	-0.5		+0.5	%
Output Load Regulation		V_{REF} = 1.0V, I_{REF} =-100uA ~ 100uA	-3		+3	mV
Output Current						
Soft Start Current		V_{REF} =0V		200		uA
Output Sourcing Current Limit		V_{REF} = 100mV under target voltage,Reg0xD3[4:2] = [0, 1, 1]		800		uA
Output Sinking Current Limit		V_{REF} = 100mV above target voltage,Reg0xD3[4:2] = [0, 1, 1]		-800		uA
Initial Voltage Setting						
V R1 = % of VCC for Initial Voltage Setting	V_{R1}	V_{REF} =750mV	29.5		31.5	%
		V_{REF} =800mV	33.5		35.5	%
		V_{REF} =850mV	37.5		39.5	%
		V_{REF} =875mV	41.5		43.5	%
		V_{REF} =900mV	45.5		47.5	%
		V_{REF} =925mV	49.5		51.5	%
		V_{REF} =950mV	53.5		55.5	%
		V_{REF} =975mV	57.5		59.5	%
		V_{REF} =1000mV	61.5		63.5	%
		V_{REF} =1050mV	65.5		67.5	%
		V_{REF} =1100mV	69.5		71.5	%
		V_{REF} =1150mV	73.5		75.5	%
		V_{REF} =1250mV	77.5		79.5	%
		V_{REF} =1350mV	81.5		83.5	%
		V_{REF} =1500mV	85.5		87.5	%

		V_{REF} =1800mV	89.5		91.5	%
VID0/1 Inputs						
High Level Threshold Level			1.2			V
Low Level Threshold Level					0.4	V
VID Pull Low Current		VID0 = VID1 =VCC		10		uA
Enable/Disable						
Enable Threshold Voltage	V_{R1}	V_{R1} rising		200		mV
Disable Threshold Voltage	V_{R1}	V_{R1} falling		150		mV

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

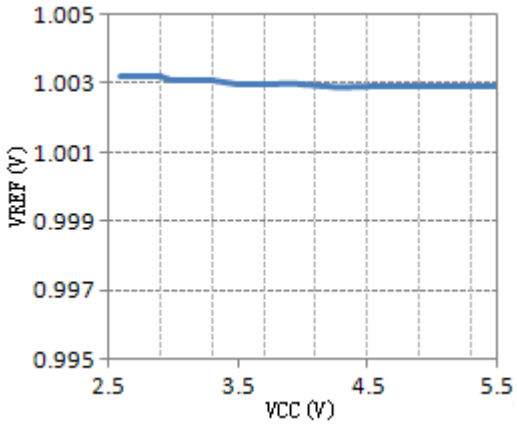
Note 3. θ_{JA} is measured in the natural convection at T_A=25°C on a high effective thermal conductivity test board (4 Layers, 2S2P) of JEDEC 51-7 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Characteristics

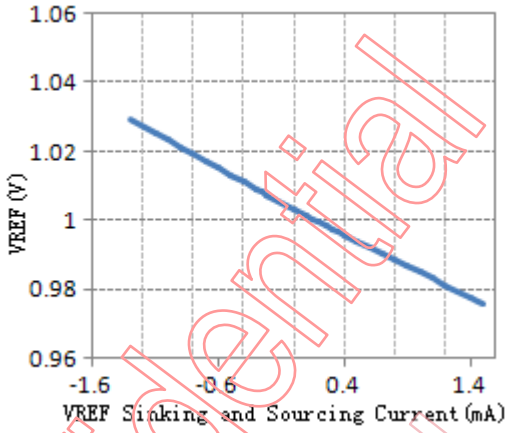
(V_{CC}=3.3V, C_{VCC}=1uF, C_{VREF}=0.47uF, T_A=25°C unless otherwise specified)

VREF Line Regulation



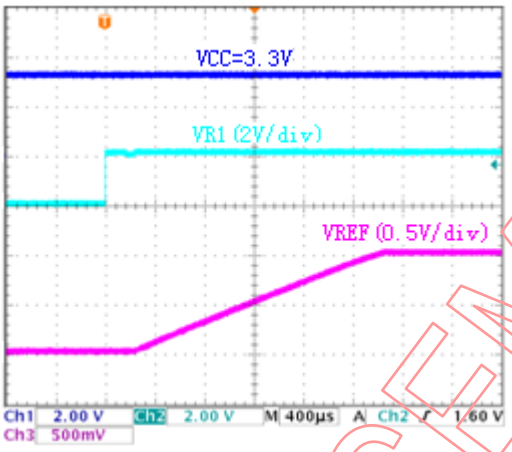
VREF=1V, No Load

VREF Load Regulation



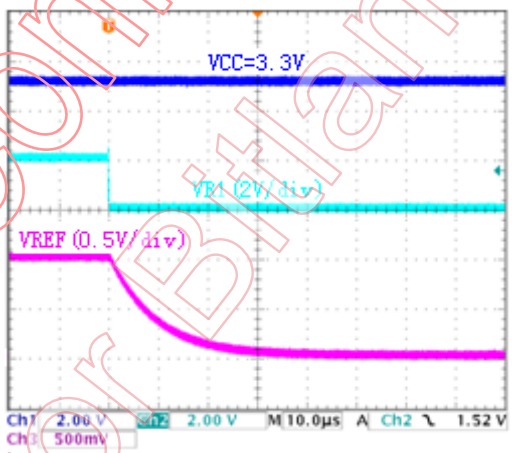
V_{CC}=3.3V, VREF=1V

Power On from EN



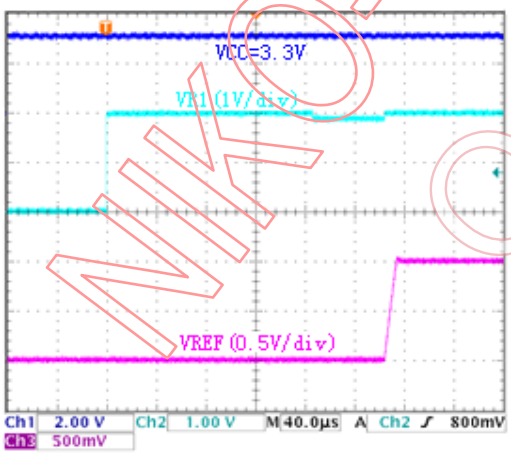
V_{CC}=3.3V, VREF=1V, No Load

Power Off from EN



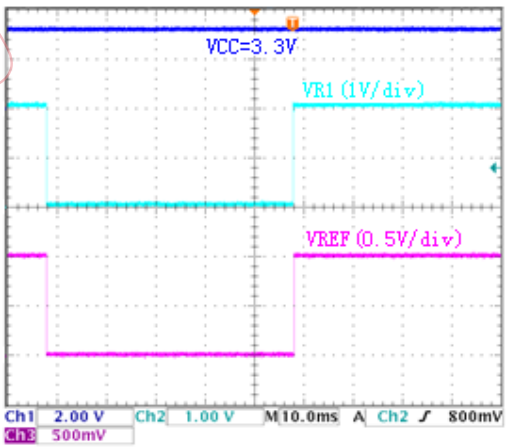
V_{CC}=3.3V, VREF=1V, No Load

Power On from EN



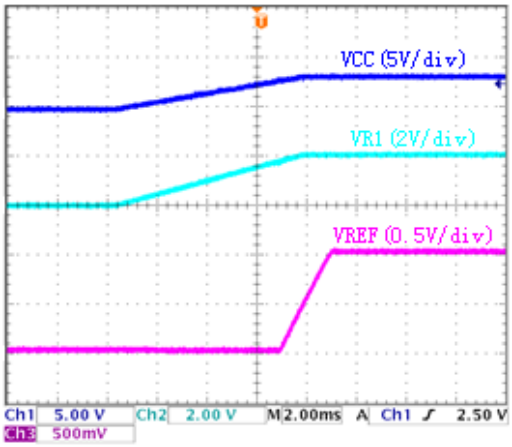
V_{CC}=3.3V, VREF=1V, C_{VREF}=2.2nF No Load

Power On/Off from EN



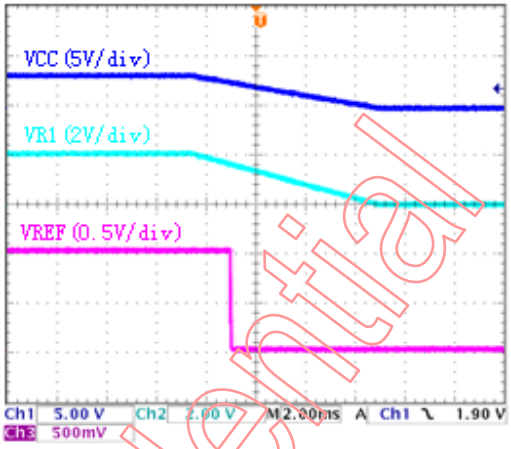
V_{CC}=3.3V, VREF=1V, C_{VREF}=2.2nF No Load

Power On from VCC



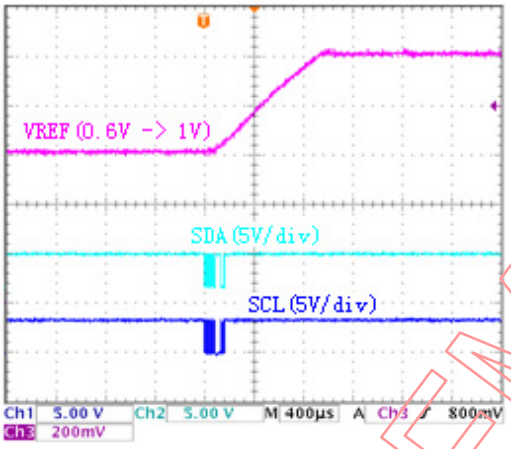
VREF=1V, No Load

Power Off from VCC



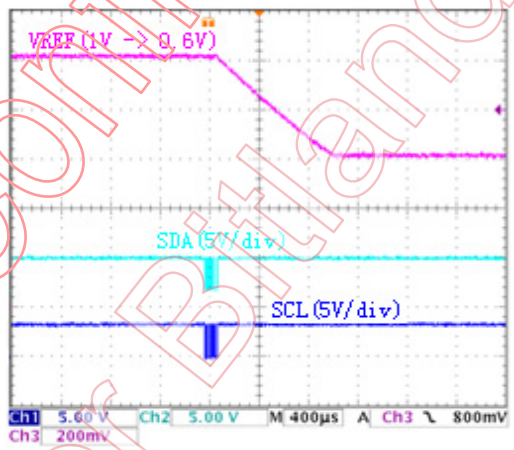
VREF=1V, No Load

VREF Ramp Up by IIC



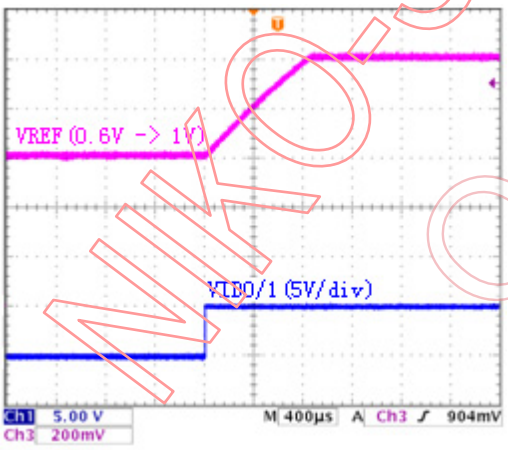
V_{CC}=3.3V, No Load

VREF Ramp Down by IIC



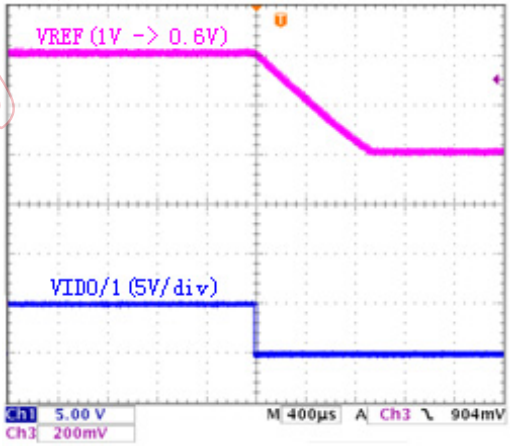
V_{CC}=3.3V, No Load

VREF Ramp Up by VID



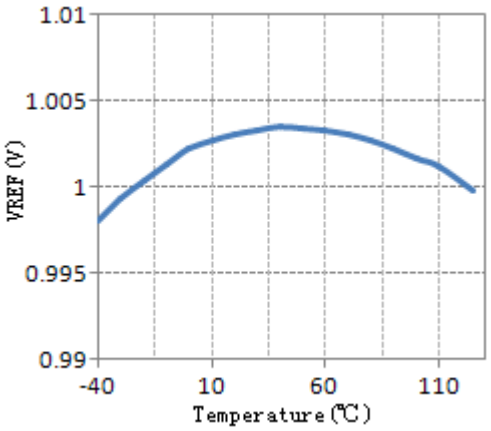
V_{CC}=3.3V, No Load

VREF Ramp Down by VID



V_{CC}=3.3V, No Load

VREF vs. Temperature



V_{CC}=3.3V, VREF=1V, No Load

Application Information

Supply Input and Enable

The GS8601-A receives the supply input through the VCC pin. This pin is continuously monitored for power on reset (POR). The threshold voltage is about 2.8V at VCC rising. When the pin is in the logic high, the GS8601-A will be turned on.

Initial Voltage and IIC Address Setting

The GS8601-A has a multiplex function pin R1 set the initial voltage and the IIC address. As shown in the following Figure 1: the pin R1 is connected to a voltage divider at VCC-R1-GND externally.

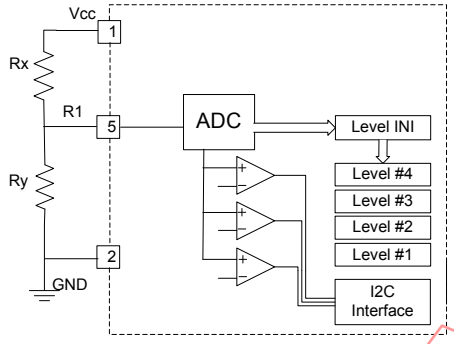


Figure 4 Initial Voltage and IIC Address Setting

Once the POR is released, the V_{R1} voltage is digitalized to determine the initial reference voltage V_{INI} by the ADC. This value is also sent to the Reg0x8B and Reg0xD4/D5/D6/D7 as initial value.

Recurs to three comparators, the GS8601-A can supply three IIC address according to the external resistances. The following table 1 shows the recommended resistance combination for each IIC address.

Mode select

The GS8601-A offers three kinds of control mode. It can set the initial voltage through the external resistance divider. It can employ the parallel VID (PVI) to determine the reference voltage. And it can also decide the reference voltage refers to the series VID (SVI). By coding the Reg0XD3[7:6], the GS8601-A can correspondingly operation in the mode illustrated in table 2.

Table 1 Initial Voltage and IIC Address Setting

V_{R1}=% of VCC	Initial V_{REF}(V)	Rx/Ry for IIC Address(kΩ)		
		0xA2	0xA4	0xA6
30.5%	0.750	6.56/2.88	19.67/8.63	39.34/17.27
34.5%	0.800	5.80/3.05	17.39/9.16	34.78/18.32
38.5%	0.850	5.19/3.25	15.58/9.76	31.17/19.51
42.5%	0.875	4.71/3.48	14.12/10.43	28.24/20.87
46.5%	0.900	4.30/3.74	12.90/11.21	25.81/22.43
50.5%	0.925	3.96/4.04	11.88/12.12	23.76/24.24
54.5%	0.950	3.67/4.40	11.01/13.19	22.02/26.37
58.5%	0.975	3.42/4.82	10.26/14.46	20.51/28.92
62.5%	1.000	3.20/5.33	9.60/16.00	19.20/32.00
66.5%	1.050	3.01/5.97	9.02/17.91	18.05/35.82
70.5%	1.100	2.84/6.78	8.51/20.34	17.02/40.68
74.5%	1.150	2.68/7.84	8.05/23.53	16.11/47.06
78.5%	1.250	2.55/9.30	7.64/27.91	15.29/55.81
82.5%	1.350	2.42/11.43	7.27/34.29	14.55/68.57
86.5%	1.500	2.31/14.82	6.94/44.44	13.87/88.89
90.5%	1.800	2.21/21.05	6.63/63.16	13.26/126.32

The Reg0x D3 [7:6] is defaulted as [0,0] that selects initial voltage, Reg0x D3 [7:6]=[0,1] selects PVI mode and Reg0x D3 [7:6]=[1,x] selects SVI mode.

Table 2 Mode Selection

Reg0xD3[7:6]	VID Mode
[0,0]	Set by R1 Pin
[0,1]	Parallel VID Selected by VID0/1
[1,0]	Serial VID by IIC
[1,1]	Serial VID by IIC

Parallel VID

The GS8601-A supports level#1~level#4 voltages that programmed by VID[1:0] under Parallel VID mode. The following table 3 gives the relevant code to each level voltage.

Table 3 Parallel VID Selection

VID[1:0]	Level #	Register
[0,0]	Level #1	Reg0xD4
[0,1]	Level #2	Reg0xD5
[1,0]	Level #3	Reg0xD6
[1,1]	Level #4	Reg0xD7

Note that the Reg0xD4/D5/D6/D7 are defaulted to Reg0X8B which assigns the level INI at VCC POR.

DAC Output

The GS8601-A contains a high precise voltage reference output to the DAC model as shown in the Function Block Diagram. According to the code of the Reg0xD3[7:6], the multiplexer (MUX2) outputs the correspondingly operation mode to the DAC. According to the R1 input, the VID0/1 inputs and IIC command, the DAC generates the reference voltage by a output buffer to drive the load.

Output Current Limit

The GS8601-A supports choose the output current to achieve smooth output voltage through programming the Reg0xD3[4:2]. The output voltage current limited default to be 200uA during start up and can be programmed as 400uA to 1600uA with 200uA steps. Adaptationally, the output voltage ramps up with a slew rate as:

$$\frac{dV_{REF}}{dt} = \frac{200\mu A}{C_{REF}}$$

C_{REF} is the output capacitor

Table 4 illustrates the current limit programming by IIC during output change.

Table 4 Output Current Limit Programming

Reg0xD3[4:2]	Current Limit
000	200uA
001	400uA
010	600uA
011	800uA
100	1000uA
101	1200uA
110	1400uA
111	1600uA

Output Disable

The GS8601-A can disable the output voltage active internally and passive externally.

Through set the bit Reg0xD3[5]=1, the GS8601-A can active disable output voltage internally.

If the R1 pin is pulled low by external open drain transistor lower than 0.15V as shown in the Function Block Diagram, the GS8601-A can be disabled and all the IIC registers can be reset. If the R1 pin can be released from the ground, the GS8601-A can performs its power on reset procedures, including initial voltage setting and IIC address selection.

Note that when release the R1 pin, the transistor MUST be completely turned off with 1us. Otherwise may cause wrong value of initial voltage and IIC address.

Power Up Sequence

The Figure 2 shows the power up sequence and power play of the GS8601-A.

At T1, the GS8601-A releases POR signal, selects the initial voltage and the IIC address and initiates the output current as 200uA.

At T2, the Reg0xD3[7:6] is set to [0,1] that selects the PVI mode. The Reg0xD3[4:2] is set to be [001] that change the output current limit to be 400uA. The output voltage ramps up to the new target

voltage which programmed by VID[1:0] and Reg0xD4/D5/D6/D7 in accordance with the new slew rate programmed by Reg0xD3[4:2].

At T3, Reg0xD4/D5/D6/D7 is changed and the output voltage ramps up/down to its new target level.

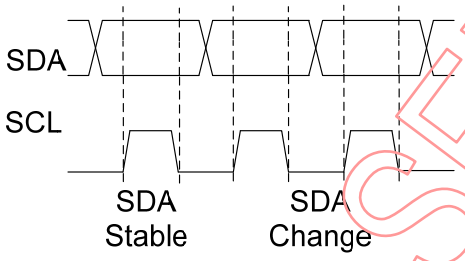
At T4, VID[1:0] is changed and the output voltage ramps up to its new target level.

At T5, the Reg0xD3[7:6] is set to [1,x] that selects the SVI mode. The output voltage ramps up to the new target voltage programmed by Reg0xD2.

At T6, Reg0xD2 is changed and the output voltage ramps up to its new target level.

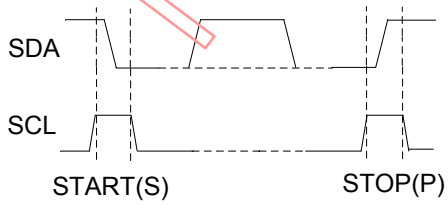
IIC Interface Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The state of the data line can only change when the clock signal on the SCL line is LOW.



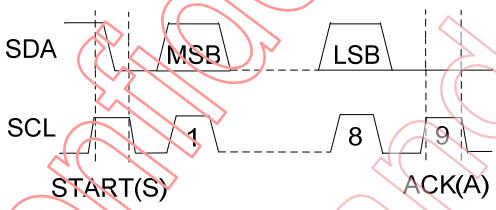
Start and Stop Conditions

A START (S) condition is a HIGH to LOW transition of SDA while SCL is HIGH. The STOP (P) condition is a LOW to HIGH transition of SDA while SCL is HIGH. A STOP condition must be sent before each START condition.



Acknowledge

Each address and data transmission uses 9 clock pulses. The ninth pulse is the acknowledge bit (A). After the start condition, the master sends 7 slave address bits and a R/W bit during the next 8 clock pulses. During the ninth clock pulse, the device that recognizes its own address pulls SDA low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data.



IIC Address

The IIC address 0xA2, 0xA4, 0xA6 is selected by the resistor divider connected to the R1 pin as shown in the table 1.

IIC Registers

Table 5 shows the IIC registers of the GS8601-A, including read/write type, default and description.

INI (0x8B)

This register supports read only and storages the initial voltage.

V_{INI}=600mV+INI×5mV=600mV+Reg0x8B[7:0] ×5mV

Note that the V_{INI} is decided by the externally resistor divider as illustrated in table 1. Table 5 shows the possible Reg0x8B values with corresponding initial voltages. The value out of the table is not recommended.

Table 5 Possible Reg0x8B Values

Initial V_{REF}(V)	Reg0x8B	Initial V_{REF}(V)	Reg0x8B
0.750	0x1E	1.000	0x50

0.800	0x28	1.050	0x5A
0.850	0x32	1.100	0x64
0.875	0x37	1.150	0x6E
0.900	0x3C	1.250	0x82
0.925	0x41	1.350	0x96
0.950	0x46	1.500	0xB4
0.975	0x4B	1.800	0xF0

CHIPID (Reg0xD0)

This register supports read only and storages the chip ID of the GS8601-A. Its default value is 0x12.

MISC (Reg0xD1)

This deliberate register is defined for watch dog timer.

MISC[7]=0; disable the watch dog timer

MISC[7]=1; enable the watch dog timer

MISC[6]=0; read only. This bit is set to 1 if time-out happens and is set to 0 if it is read.

The time-out can be programmed by IIC as illustrated in table 6.

Table 6 Time out Programming

MISC[5:4]	Time-out(ms)
00	400
01	800
10	1600
11	3200

SVI (Reg0xD2)

This register sets the output voltage if SVI mode is selected.

V_{REF}=600mV+Reg0xD2[7:0]×5mV

The range of V_{REF} is from 600mV to 1875mV.

ILIM (Reg0xD3)

This register can set on/off, the control mode, and current limit. And the Reg0xD3 supports read back of the level of output voltage of the PVI mode.

Reg0xD3[7:6] choose the control mode of the GS8601-A as the Table 6 illustrated.

Reg0xD3[5] can set on/off of the output voltage. Reg0xD3[5]=1 turns off the output voltage.

Reg0xD3[4:2] sets the current limit of the output voltage as shown in the Table 6.

Reg0xD3[1:0] are the read backs for VID1 and VID0.

Reg0xD3[1:0]=[0,0] means VID[1:0]= [0,0]

Reg0xD3[1:0]=[0,1] means VID[1:0]= [0,1]

Reg0xD3[1:0]=[1,0] means VID[1:0]= [1,0]

Reg0xD3[1:0]=[1,1] means VID[1:0]= [1,1]

PVI (Reg0xD4/D5/D6/D7)

These registers set the output voltage if the PVI mode is selected.

V_{REF}=600mV+Reg0xD4[7:0]×5mV, VID[1:0]= [0,0]

V_{REF}=600mV+Reg0xD5[7:0]×5mV, VID[1:0]= [0,0]

V_{REF}=600mV+Reg0xD6[7:0]×5mV, VID[1:0]= [0,0]

V_{REF}=600mV+Reg0xD7[7:0]×5mV, VID[1:0]= [0,0]

The range of V_{REF} is from 600mV to 1875mV.

Table 7 is the VID table of Reg0x8B, Reg0xD2, and Reg0xD4/D5/D6/D7

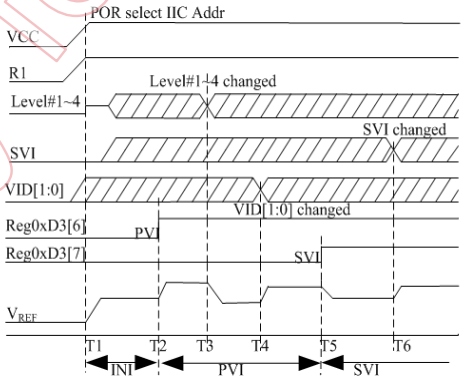


Figure 5 Power up Sequence

Table 6 IIC Registers Summary

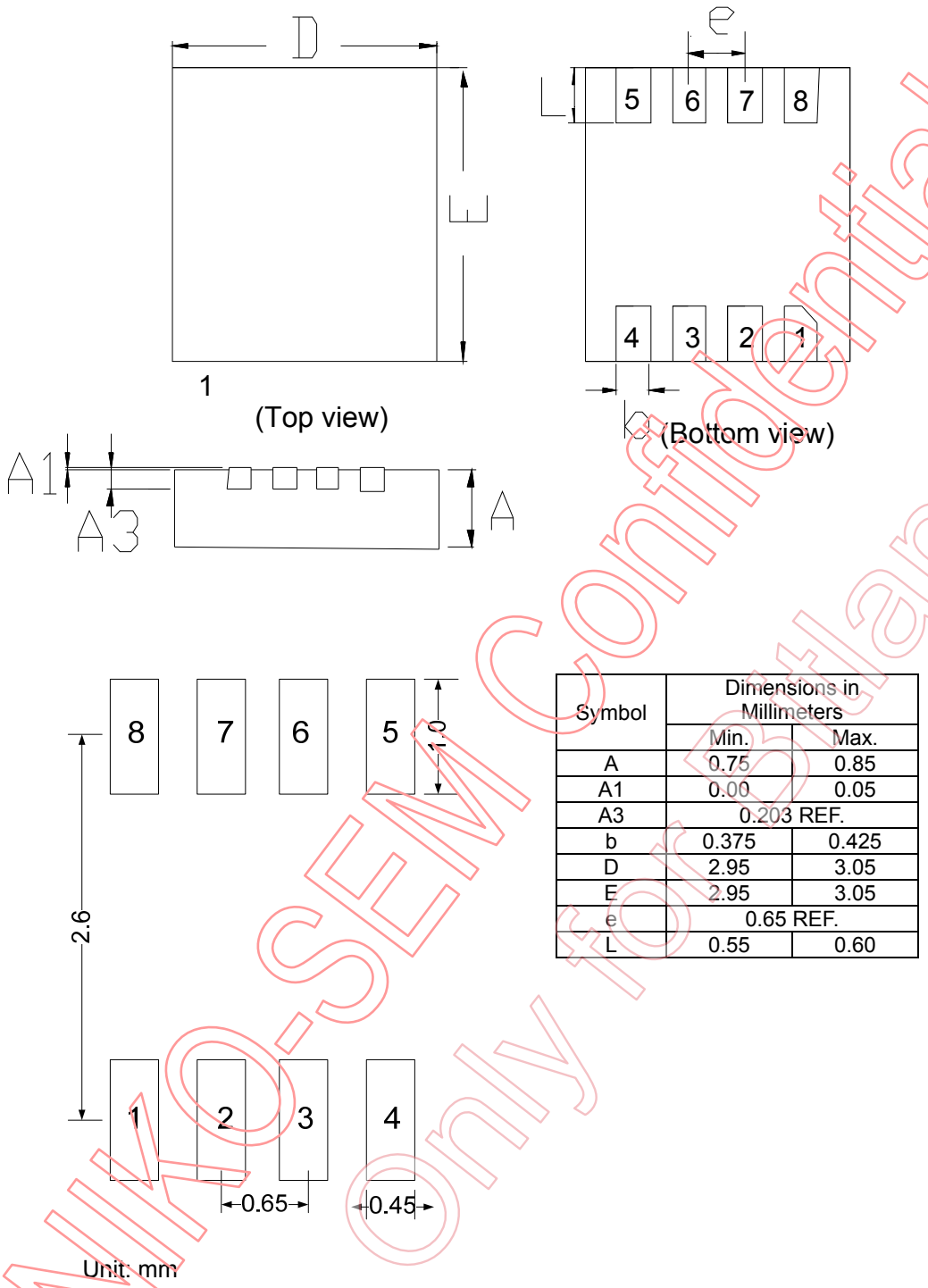
Reg. Address.	Type	Name	Deault	Description
0x8B	R	INI	Set by R1	Initial voltage read back(0.75V~1.80V, 16 level)
0xD0	R	ID	0x12	Chip ID
0xD1	R/W	MISC	0x00	
0xD2	R/W	SVI	0x00	V_{REF} set by SVI(0.6v~1.875V, 5mV increment)
0xD3	R/W	ILIM	0x00	Mode, current limit setting and on/off control
0xD4	R/W	Level #1	Set by R1	V_{REF} set by SVI(0.6v~1.875V, 5mV increment)
0xD5	R/W	Level #2	Set by R1	V_{REF} set by SVI(0.6v~1.875V, 5mV increment)
0xD6	R/W	Level #3	Set by R1	V_{REF} set by SVI(0.6v~1.875V, 5mV increment)
0xD7	R/W	Level #4	Set by R1	V_{REF} set by SVI(0.6v~1.875V, 5mV increment)

Table 7 VID table for 0x8B, 0xD2, and 0xD4/D5/D6/D7 registers

Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)	Reg Code	Vol (V)
0x00	0.600	0x20	0.760	0x40	0.920	0x60	1.080	0x80	1.240	0xA0	1.400	0xC0	1.560	0xE0	1.720
0x01	0.605	0x21	0.765	0x41	0.925	0x61	1.085	0x81	1.245	0xA1	1.405	0xC1	1.565	0xE1	1.725
0x02	0.610	0x22	0.770	0x42	0.930	0x62	1.090	0x82	1.250	0xA2	1.410	0xC2	1.570	0xE2	1.730
0x03	0.615	0x23	0.775	0x43	0.935	0x63	1.095	0x83	1.255	0xA3	1.415	0xC3	1.575	0xE3	1.735
0x04	0.620	0x24	0.780	0x44	0.940	0x64	1.100	0x84	1.260	0xA4	1.420	0xC4	1.580	0xE4	1.740
0x05	0.625	0x25	0.785	0x45	0.945	0x65	1.105	0x85	1.265	0xA5	1.425	0xC5	1.585	0xE5	1.745
0x06	0.630	0x26	0.790	0x46	0.950	0x66	1.110	0x86	1.270	0xA6	1.430	0xC6	1.590	0xE6	1.750
0x07	0.635	0x27	0.795	0x47	0.955	0x67	1.115	0x87	1.275	0xA7	1.435	0xC7	1.595	0xE7	1.755
0x08	0.640	0x28	0.800	0x48	0.960	0x68	1.120	0x88	1.280	0xA8	1.440	0xC8	1.600	0xE8	1.760
0x09	0.645	0x29	0.805	0x49	0.965	0x69	1.125	0x89	1.285	0xA9	1.445	0xC9	1.605	0xE9	1.765
0x0A	0.650	0x2A	0.810	0x4A	0.970	0x6A	1.130	0x8A	1.290	0xAA	1.450	0xCA	1.610	0xEA	1.770
0x0B	0.655	0x2B	0.815	0x4B	0.975	0x6B	1.135	0x8B	1.295	0xAB	1.455	0xCB	1.615	0xEB	1.775
0x0C	0.660	0x2C	0.820	0x4C	0.980	0x6C	1.140	0x8C	1.300	0xAC	1.460	0xCC	1.620	0xEC	1.780
0x0D	0.665	0x2D	0.825	0x4D	0.985	0x6D	1.145	0x8D	1.305	0xAD	1.465	0xCD	1.625	0xED	1.785
0x0E	0.670	0x2E	0.830	0x4E	0.990	0x6E	1.150	0x8E	1.310	0xAE	1.470	0xCE	1.630	0xEE	1.790
0x0F	0.675	0x2F	0.835	0x4F	0.995	0x6F	1.155	0x8F	1.315	0xAF	1.475	0xCF	1.635	0xEF	1.795
0x10	0.680	0x30	0.840	0x50	1.000	0x70	1.160	0x80	1.320	0xB0	1.480	0xD0	1.640	0xF0	1.800
0x11	0.685	0x31	0.845	0x51	1.005	0x71	1.165	0x91	1.325	0xB1	1.485	0xD1	1.645	0xF1	1.805
0x12	0.690	0x32	0.850	0x52	1.010	0x72	1.170	0x92	1.330	0xB2	1.490	0xD2	1.650	0xF2	1.810
0x13	0.695	0x33	0.855	0x53	1.015	0x73	1.175	0x93	1.335	0xB3	1.495	0xD3	1.655	0xF3	1.815
0x14	0.700	0x34	0.860	0x54	1.020	0x74	1.180	0x94	1.340	0xB4	1.500	0xD4	1.660	0xF4	1.820

0x15	0.705	0x35	0.865	0x55	1.025	0x75	1.185	0x95	1.345	0xB5	1.505	0xD5	1.665	0xF5	1.825
0x16	0.710	0x36	0.870	0x56	1.030	0x76	1.190	0x96	1.350	0xB6	1.510	0xD6	1.670	0xF6	1.830
0x17	0.715	0x37	0.875	0x57	1.035	0x77	1.195	0x97	1.355	0xB7	1.515	0xD7	1.675	0xF7	1.835
0x18	0.720	0x38	0.880	0x58	1.040	0x78	1.200	0x98	1.360	0xB8	1.520	0xD8	1.680	0xF8	1.840
0x19	0.725	0x39	0.885	0x59	1.045	0x79	1.205	0x99	1.365	0xB9	1.525	0xD9	1.685	0xF9	1.845
0x1A	0.730	0x3A	0.890	0x5A	1.050	0x7A	1.210	0x9A	1.370	0xBA	1.530	0xDA	1.690	0xFA	1.850
0x1B	0.735	0x3B	0.895	0x5B	1.055	0x7B	1.215	0x9B	1.375	0xBB	1.535	0xDB	1.695	0xFB	1.855
0x1C	0.740	0x3C	0.900	0x5C	1.060	0x7C	1.220	0x9C	1.380	0xBC	1.540	0xDC	1.700	0xFC	1.860
0x1D	0.745	0x3D	0.905	0x5D	1.065	0x7D	1.225	0x9D	1.385	0xBD	1.545	0xDD	1.705	0xFD	1.865
0x1E	0.750	0x3E	0.910	0x5E	1.070	0x7E	1.230	0x9E	1.390	0xBE	1.550	0xDE	1.710	0xFE	1.870
0x1F	0.755	0x3F	0.915	0x5F	1.075	0x7F	1.235	0x9F	1.395	0xBF	1.555	0xDF	1.715	0xFF	1.875

Package Dimensions, TSON8-3x3



Symbol	Dimensions in Millimeters	
	Min.	Max.
A	0.75	0.85
A1	0.00	0.05
A3	0.203 REF.	
b	0.375	0.425
D	2.95	3.05
E	2.95	3.05
e	0.65 REF.	
L	0.55	0.60

Note

1. Min.: Minimum dimension specified.
2. Max.: Maximum dimension specified.
3. REF.: Reference. Normal/Regular dimension specified for reference.

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