TECH PUBLIC
台舟电子

TPLC03-3.3LC
Low Capacitance 3.3 TVS

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Features

- Low capacitance for high speed interfaces
- Ultra low leakage: nA level
- Low operating voltage: 3.3V
- Ultra low clamping voltage
- Protects two lines in common and differential mode
- JEDEC SO-8 package
- Complies with following standards:
  - – IEC 61000-4-2 (ESD) immunity test
    - Air discharge: ±30kV
    - Contact discharge: ±30kV
  - – IEC61000-4-5 (Lightning) 55A (8/20 μs)
- RoHS Compliant

Mechanical Characteristics

- Package: SO-8
- Lead Finish: Matte Tin
- Case Material: “Green” Molding Compound.
- Moisture Sensitivity: Level 3 per J-STD-020
- Terminal Connections: See Diagram Below

RoHS

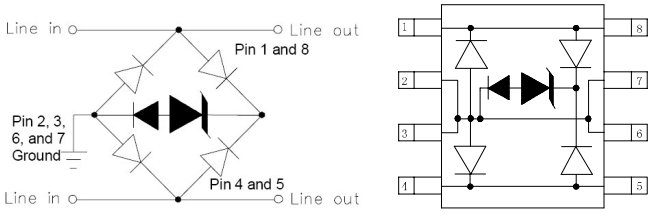
Applications

- T1/E1 Line Cards
- T3/E3 and DS3 Interfaces
- STS-1 Interfaces
- 10/100/1000 BaseT Ethernet
- Set Top Box
- ISDN Interfaces
- Low Voltage Interfaces

Ordering Information

Part Number	Qty per Reel	Reel Size
TPLC03-3.3LC	2500	13Inch

Dimensions and Pin Configuration



Absolute Maximum Ratings (T_A=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power(8/20μs)	Ppk	1500	W
Peak Pulse Current(8/20μs)	I_{PP}	55	A
ESD per IEC 61000−4−2 (Air) ESD per IEC 61000−4−2 (Contact)	V_{ESD}	±30 ±30	kV
Operating Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

Electrical Characteristics (T_A=25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			3.3	V	
Punch-Through Voltage	V_{PT}	3.5			V	I_T = 2μA
Snap-Back Voltage	V_{SB}	2.8			V	I_T = 50mA
Reverse Leakage Current	I_R			0.5	μA	V_{RWM} = 3.3V
Clamping Voltage	V_C			7	V	I_{PP} = 1A (8 x 20□s pulse), any I/O pin to ground
Clamping Voltage	V_C			22	V	I_{PP} = 50A (8 x 20□s pulse), between I/O pins
Clamping Voltage	V_C			25	V	I_{PP} = 55A (8 x 20□s pulse), any I/O pin to ground
Junction Capacitance	C_J		3	5	pF	VR = 0V, f = 1MHz, between I/O pins and ground
Junction Capacitance	C_J		1.5	2.5	pF	VR = 0V, f = 1MHz, between I/O pins

Note 1: I/O pins are Pin 1, 4, 5 and 8

PROTECTION PRODUCTS
Typical charateristics

Fig1. 8/20μs Pulse Waveform

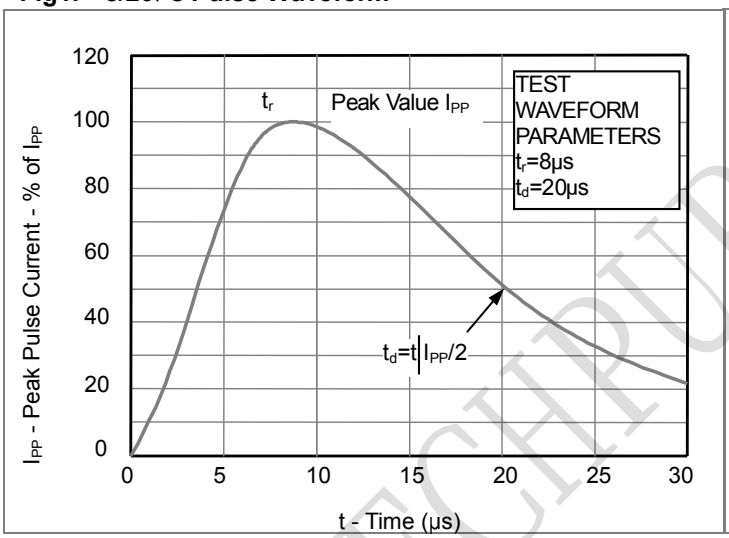


Fig2. ESD Pulse Waveform (according to IEC 61000-4-2)

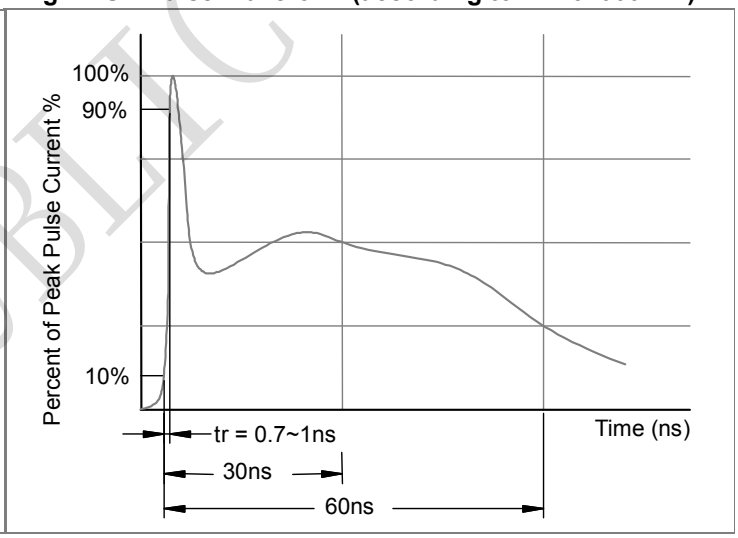
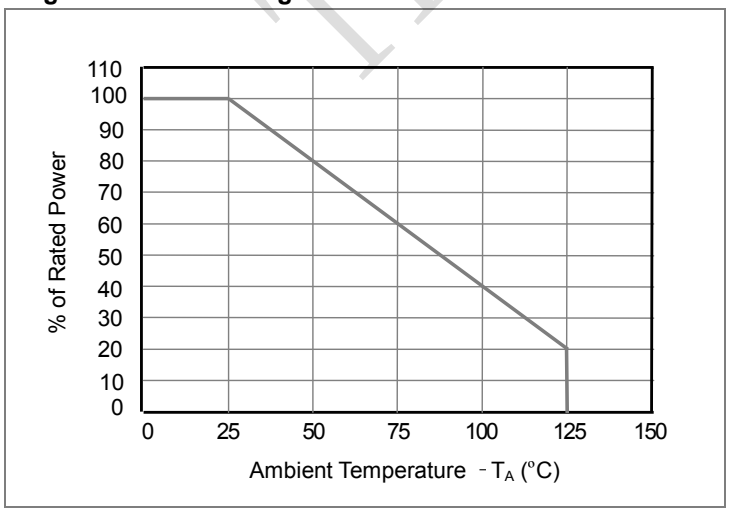
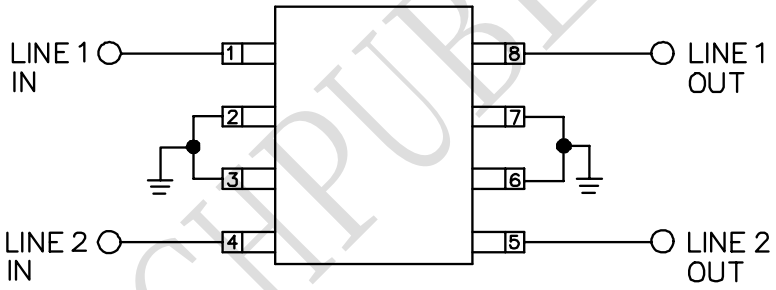


Fig3. Power Derating Curve

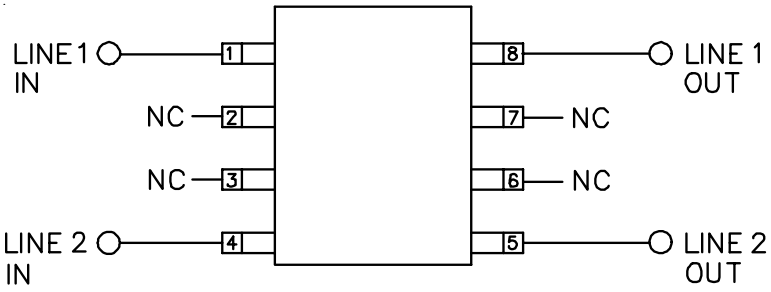


Typical Application

The TPLC03-3.3LC is designed to protect two high speed data lines (one differential pair) from transient over - voltages which result from lightning and ESD. The device can be configured to protect in differential (Line to Line) and common (Line to Ground) mode. Data line inputs/outputs are connected at pins 1 to 8, and 4 to 5 as shown below. Pins 2, 3, 6, 7 are connected to ground. These pins should be connected directly to a ground plane on the board for the best results, the path length is kept as short as possible to minimize parasitic inductance. In applications where high common voltages are present, differential protection is achieved by leaving pins 2, 3, 6, and 7 not connected.

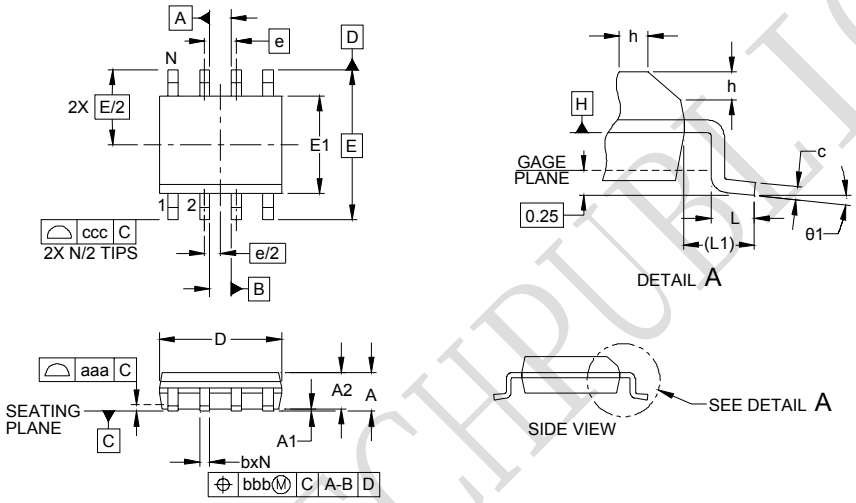


Connection for differential (Line to Line) and common mode protection (Line to Ground)



Connection for differential protection (Line to Line)

Outline Drawing - SOP-8(SO-8)



DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		

Land Pattern - SOP-8