Features

- Low Supply Current~55uA (Typ.)
- Low Shutdown Current ~0.1uA (Typ.)
- Output Current ~300mA
- High Power Supply Rejection Ratio ~75dB@1KHz
- 1.7~5.5V Operation
- ±1.5% Initial Voltage Accuracy
- Low Temperature Drift Coefficient ~50ppm
- Line Regulation ~0.02%/V(Typ.)
- Low ESR Capacitor ~1.0uF ceramic capacitor
- WDFN4-1.2x1.6 \cdot TDFN6-1.8x2 \cdot SOT-23-5 \cdot SOT-89-3 \cdot MSOT-23 and SOT-353 package

VDD

 Green Product (RoHS, Lead-Free, Halogen-Free Compliant)

Applications

- Portable communication equipment
- Notebook Computer
- Battery Powered Systems

Typical Application

General Description

The GS7119 is a CMOS linear regulator. It is featuring ultra-high power supply rejection ratio, low output voltage noise, low dropout voltage, low quiescent current and fast transient response. It guarantees delivery of 300mA output current, and supports preset 1.2V, 1.3V, 1.5V, 1.7V, 1.8V, 1.85V, 1.9V, 2.0V, 2.3V, 2.5V, 2.6V, 2.7V, 2.8V, 2.85V, 2.9V, 3.0V, 3.1V, 3.3V output voltage versions.

Based on its low quiescent current consumption and its less than 1uA shutdown mode, the GS7119 is ideal for battery- powered applications. The high power supply rejection ratio of the GS7119 holds well for low input voltages typically encountered in battery- operated systems. The regulator is stable with small ceramic capacitive loads (1µF typical).



VDD VOUT

GS7119

GND

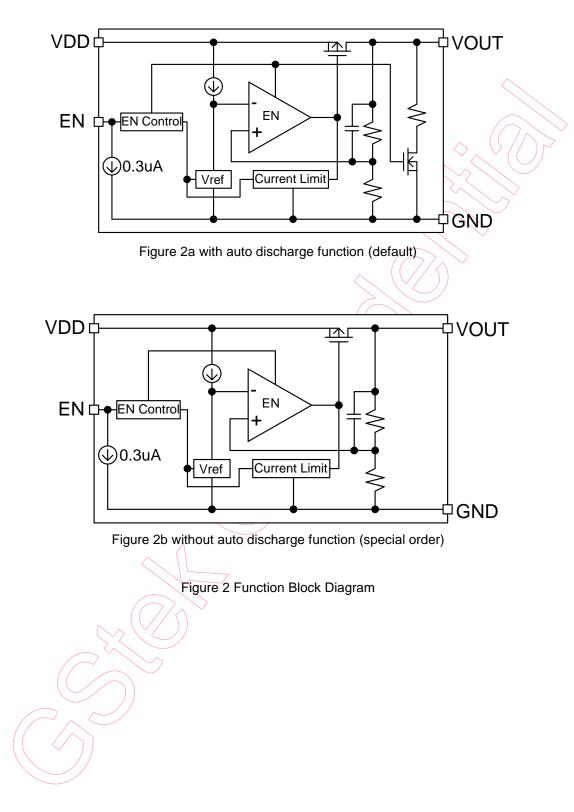
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3 FN

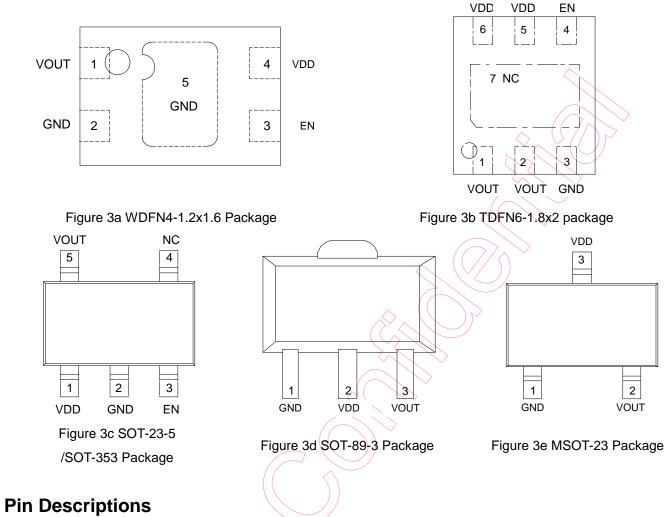
EN

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Function Block Diagram



Pin Configuration



No								
WDFN4-1.2x1.6	TDFN6-1.8x2	SOT-23-5/ SOT-353	SOT-89-3	MSOT-23	Name	I/O type	Description	
1	1, 2	5	3	2	VOUT	0	Output pin	
2, 5	3	2	1	1	GND	0	Ground pin	
3	4	3			EN	I	Enable Pin	
4	5,6) 1	2	3	VDD	I	Input Pin	
		4			NC			

Ordering Information

	GS7119 <u>PP</u> -	XXX- R 3. Shipping 2. Output Voltage
No	ltem	Contents
		UD: WDFN4-1.2x1.6
		TD: TDFN6-1.8x2
	Package	ST: SOT-23-5
1	Fackage	S9: SOT-89-3
		SR: MSOT-23
		C5: SOT-353(SC-75)
		1P2: 1.2V, 1P3: 1.3V, 1P5: 1.5V, 1P7:1.7V, 1P8: 1.8V, 185: 1.85V, 1P9: 1.9V,
2	Output Voltage	2P0: 2.0V, 2P3: 2.3V, 2P5: 2.5V, 2P6: 2.6V, 2P7: 2.7V, 2P8: 2.8V, 285: 2.85V,
		2P9: 2.9V, 3P0: 3.0V, 3P1: 3.1V, 3P3: 3.3V
3	Shipping	R: Tape & Reel

Example: GS7119 2.5V SOT-23-5 Tape & Reel ordering information is "GS7119ST-2P5-R"

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Absolute Maximum Rating (Note 1)

Parameter	Symbol	Limits	Units
VIN to GND	V _{IN}	-0.3 < V _{IN} < 6	V
VEN to GND	V _{EN}	-0.3 < V _{EN} < 6	V
Output Voltage	V _{OUT}	-0.3 < V _{OUT} <v<sub>IN+0.3</v<sub>	V
Output Current	Ι _{ουτ}	300	mA
Package Power Dissipation at $T_A \leq 25^{\circ}C$	P _{D_WDFN4-1.2x1.6}	500	mW
Package Power Dissipation at $T_A \leq 25^{\circ}C$	P _{D_TDFN6-1.8x2}	880	mW
Package Power Dissipation at $T_A \leq 25^{\circ}C$	P _{D_SOT-23-5}	420	mW
Package Power Dissipation at $T_A \leq 25^{\circ}C$	P _{D_SOT-89-3}	571	mW
Package Power Dissipation at $T_A \leq 25^{\circ}C$	P _{D_MSOT-23}	380	mW
Package Power Dissipation at $T_A \leq 25^{\circ}C$	P _{D_SOT-353}	300	mW
Storage Temperature	T _{STG}	- 65 ~ 150	°C
Lead Temperature (Soldering) 10S	TLEAD	260	°C
ESD (Human Body Mode) (Note 2)	Vesd_hbm	2K	V
ESD (Machine Mode) (Note 2)	Vesd_mm	200	V

Thermal Information (Note 3)

Parameter	Symbol	Limits	Units
Thermal Resistance Junction to Ambient	θJA_WDFN4-1.2x1.6	200	°C/W
Thermal Resistance Junction to Ambient	θJA_TDFN6-1.8x2	114	°C/W
Thermal Resistance Junction to Ambient	$\theta_{\text{JA}_\text{SOT-23-5}}$	238	°C/W
Thermal Resistance Junction to Ambient	$\theta_{JA_SOT-89-3}$	182	°C/W
Thermal Resistance Junction to Ambient	$\theta_{JA_MSOT-23}$	263	°C/W
Thermal Resistance Junction to Ambient	$\theta_{\text{JA}_{\text{SOT-353}}}$	333	°C/W
$(\sim \langle \mathcal{O} \rangle)$	-		

Recommend Operating Condition (Note 4)

Parameter	Symbol	Limits	Units
VIN to GND	V _{IN}	1.7 to 5.5	V
Junction Temperature	TJ	- 40 ~ 125	°C
Operating Temperature Range	T _A	-40 ~ 85	°C

Low Noise 300mA LDO Regulator

Electrical Characteristics

 $(V_{IN} = V_{OUT} + 1V, T_A = 25^{\circ}C, C_{IN} = C_L = 0.47 uF, I_{OUT} = 1mA$, unless otherwise specified)

Parameter	Symbol	Conditions		Min	Тур	Max	Units
SUPPLY VOLTAGE S		~		1			
Supply Voltage	V _{IN}			1.7		5.5	V
Supply Current	I _{VIN}	Unload			55	70	uA
Standby Current	I _{STBY}	V _{EN} =0		\diamond	0.1	1.0	uA
EN Input Current	I _{EN}	$V_{EN}=V_{IN}=5.5V$		\bigtriangledown	0.3		uA
Output Current(Note 5)	Ι _{ουτ}			300 (Note 6)	$\langle \zeta_{\zeta}$		mA
OUTPUT SECTION					\checkmark		1
Output Voltage	V _{OUT}	T _A = 25°C		-1.5		+1.5	%
Dropout Voltage (Note 7)		I _{OUT} =300mA (For WDFN4-1.2x1.6, , SOT-23-5, SOT-89-3 package)	V _{OUT} =1.2V		495	650	- mV
	V _{DROP}		V _{OUT} =1.5V		375	490	
			V _{OUT} =2.5V		235	295	
			V _{OUT} =2.8V		220	275	
			V _{OUT} =3.3V		195	245	
		I _{OUT} =300mA (For MSOT-23 package)	V _{OUT} =1.5V		500	680	
			V _{OUT} =1.8V		400	490	
			V _{OUT} =2.8V		260	340	
Line Regulation	$ riangle V_{LNR}$	$V_{IN} = V_{OUT} + 0.5V \text{ to } 5.5V$	/, I _{OUT} =1mA		0.02	0.20	%/V
Load Regulation	$\triangle V_{LDR}$	$V_{IN} = V_{OUT}$ +1V, I _{OUT} =1mA to 150mA			15	40	mV
Ripple Rejection Rate	PSRR	V _{IN} =MAX{V _{OUT} +1.0V, 3∖ 0.2Vp-p, I _{OUT} =30mA, f=			78		dB
Limit Current	llim	V _{EN} =V _{IN}			460		mA
Short Current	Ishort	V _{OUT} =0V			40		mA
EN Input Voltage High	VENH			1.2			V
EN Input Voltage Low	V _{ENL}					0.3	V
CL Auto-Discharge Resistance (Note 8)	Rdischg	V _{IN} =5.0V, V _{EN} =0V			95		Ω
Temperature Drift	$\triangle V_{OUT} / \triangle T_A$	I_{OUT} =1mA, T _A = -40°C to +85°C			40		ppm/°C

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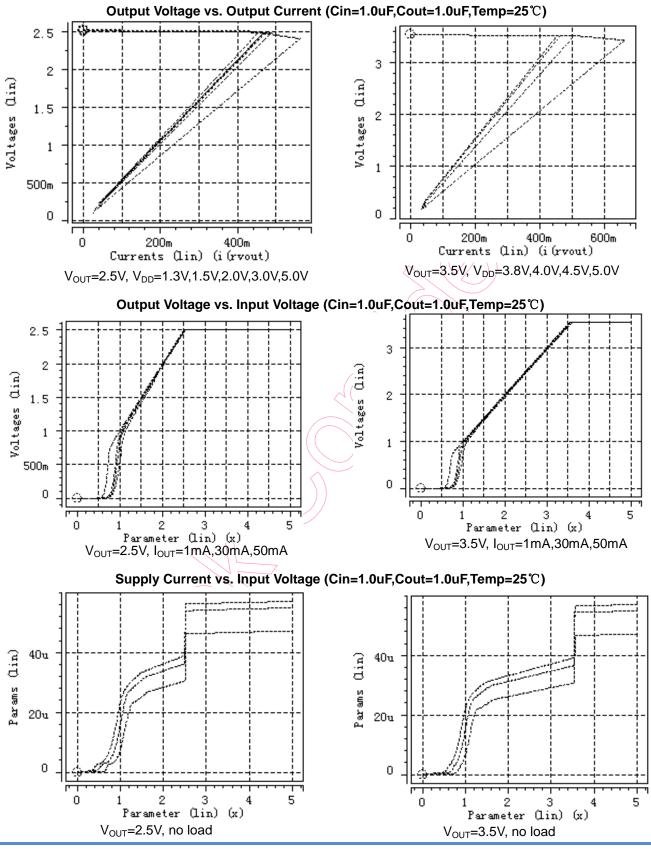
Low Noise 300mA LDO Regulator

Thermal Shutdown Temperature	T _{SD}	T_J Rising	165	°C
Thermal Shutdown			 1 1 5	°C
Returned Temperature			145	C

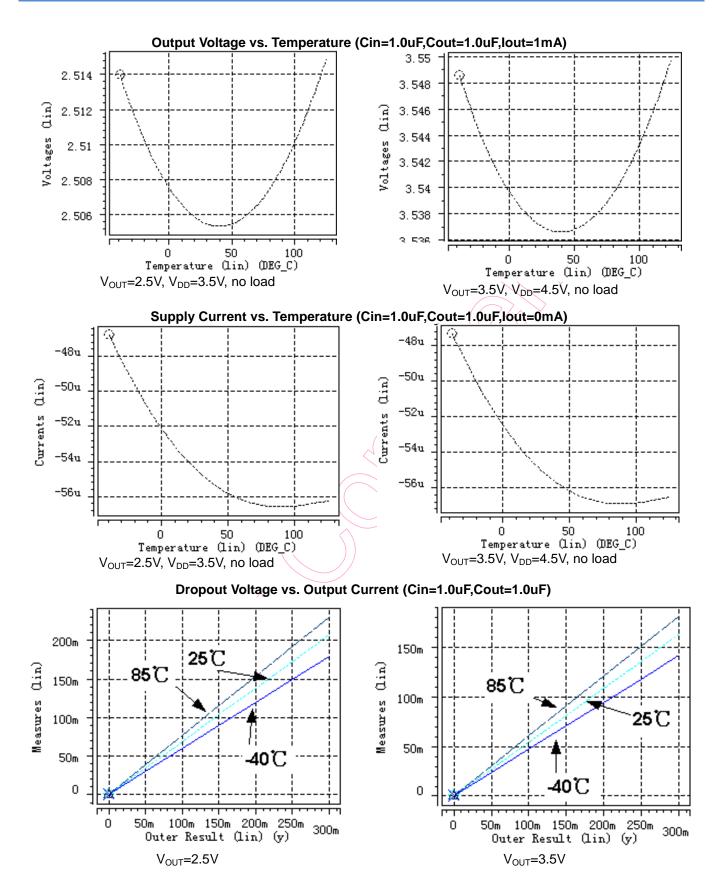
- Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.
- Note 2. Devices are ESD sensitive. Handling precaution recommended.
- Note 3. θ_{JA} is measured in the natural convection at T_A=25°C on a high effective thermal conductivity test board (40mm x 40mm x 1.6mm double sided board with 2oz, copper ratio: approx. 50%) of JEDEC 51-7 thermal measurement standard.
- Note 4. The device is not guaranteed to function outside its operating conditions.
- Note 5. The output current at which the output voltage becomes 95% of V_{OUT} after gradually increasing the output current.
- Note 6. The output current can be at least this value. Due to restrictions on the package power dissipation, this value may not be satisfied. Attention should be paid to the power dissipation of the package when the output current is large. The specification is guaranteed by design.
- **Note 7.** The dropout voltage is defined as V_{IN}^2 V_{OUT}, which is measured when V_{OUT} is 98%*V_{OUT}.
- Note 8. The output voltage Auto discharge function is optional.

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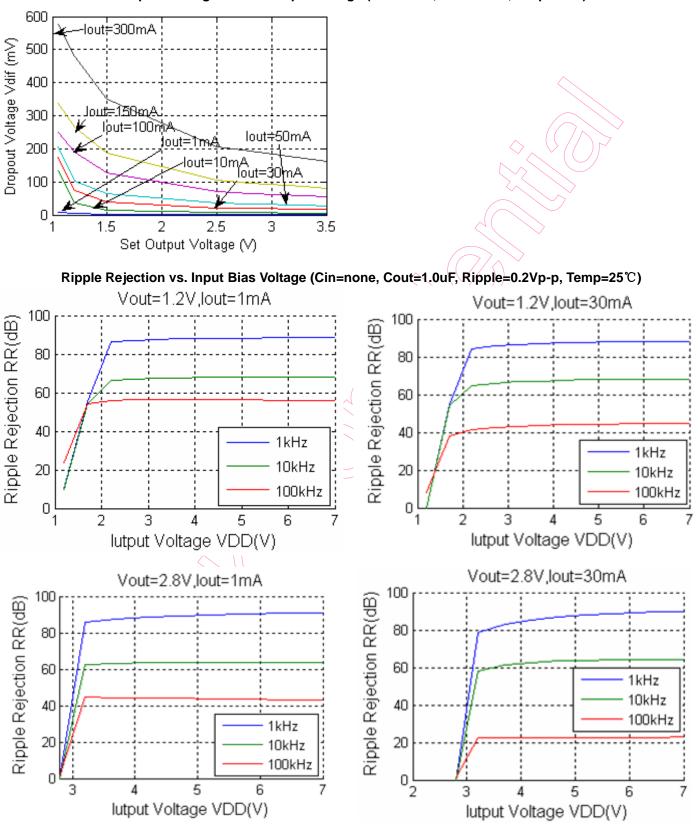
Typical Characteristics



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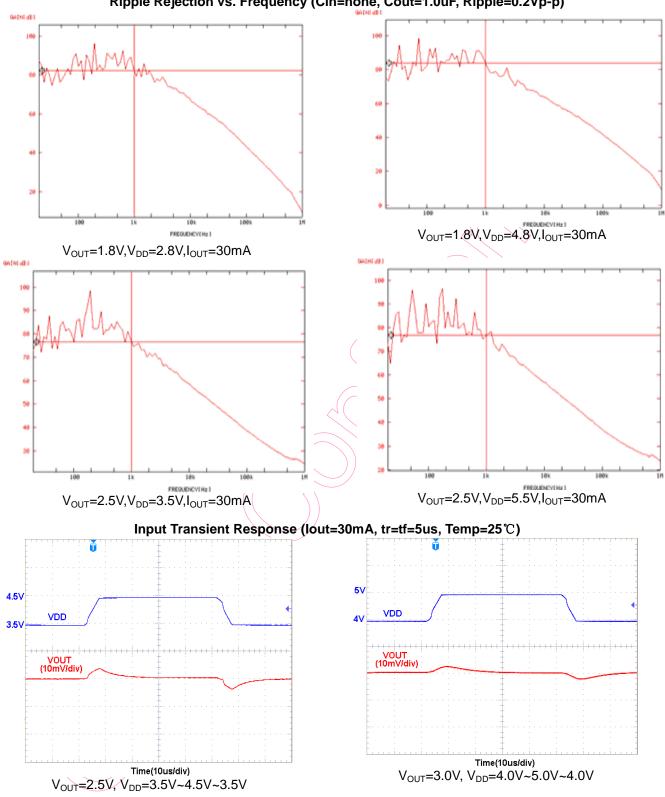


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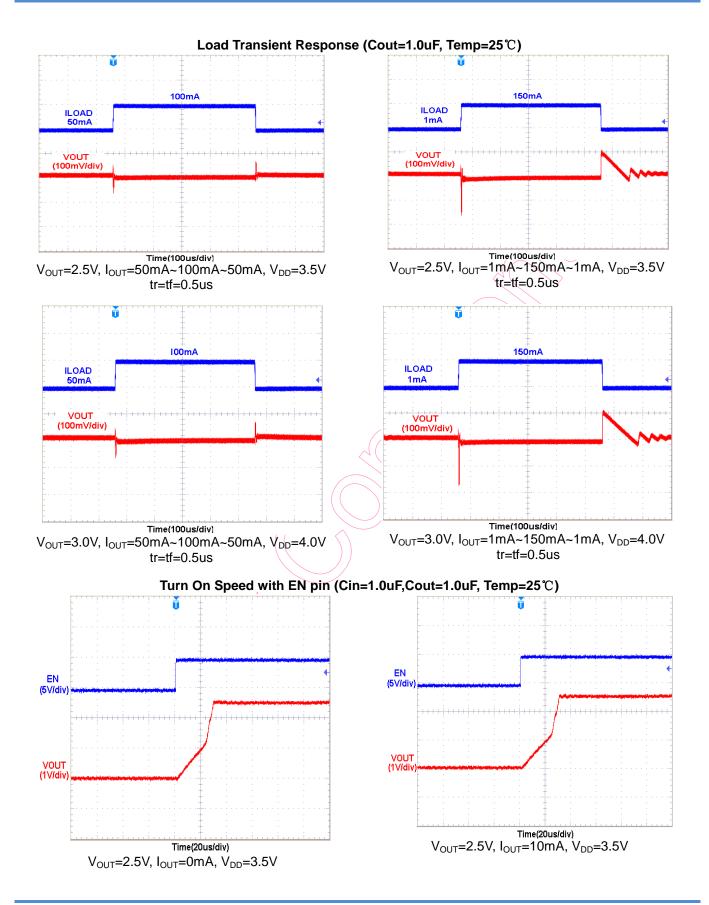


Dropout Voltage vs. Set Output Voltage (Cin=1.0uF,Cout=1.0uF,Temp=25℃)

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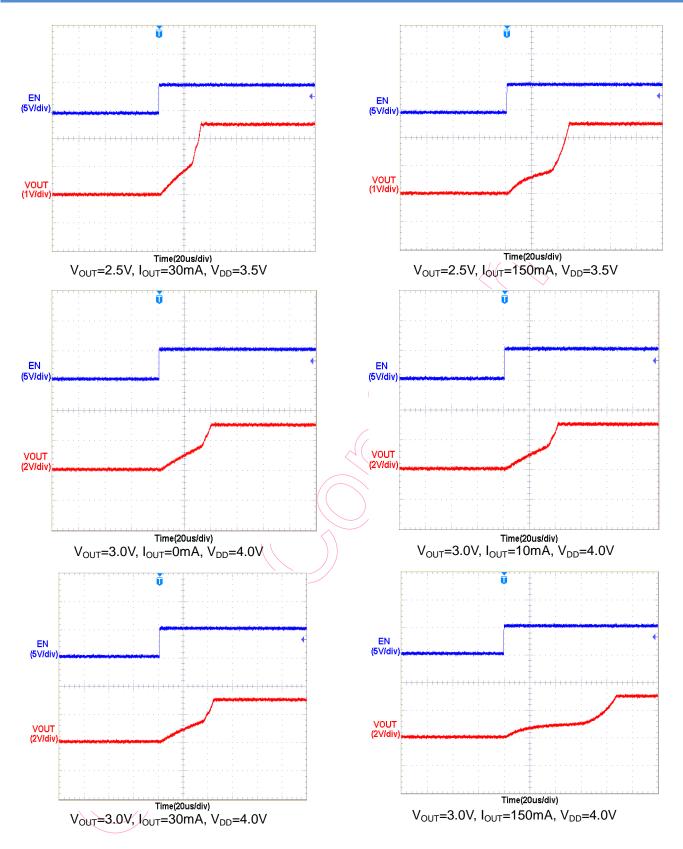


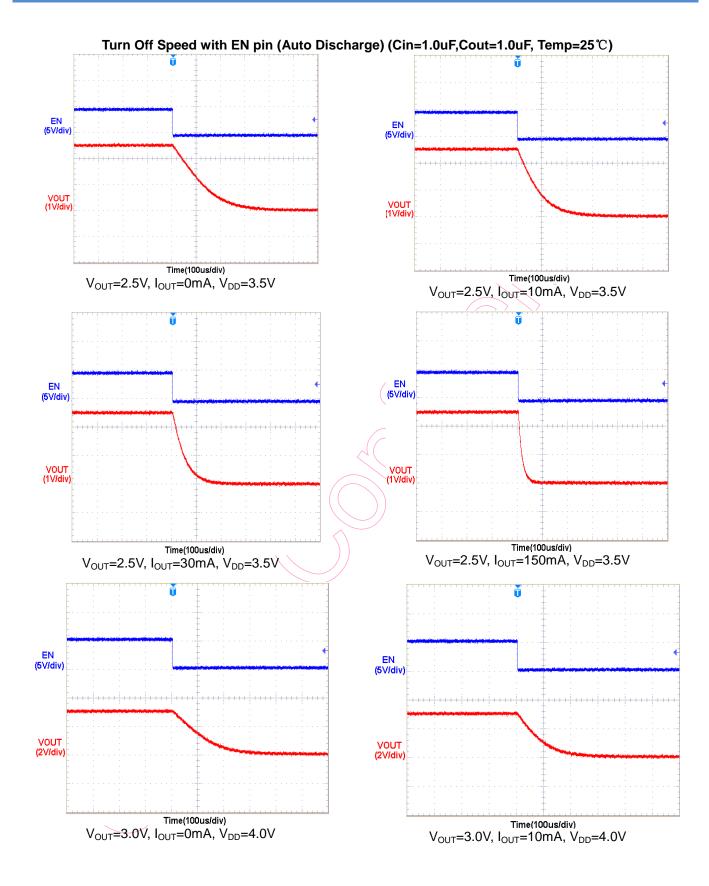
Ripple Rejection vs. Frequency (Cin=none, Cout=1.0uF, Ripple=0.2Vp-p)



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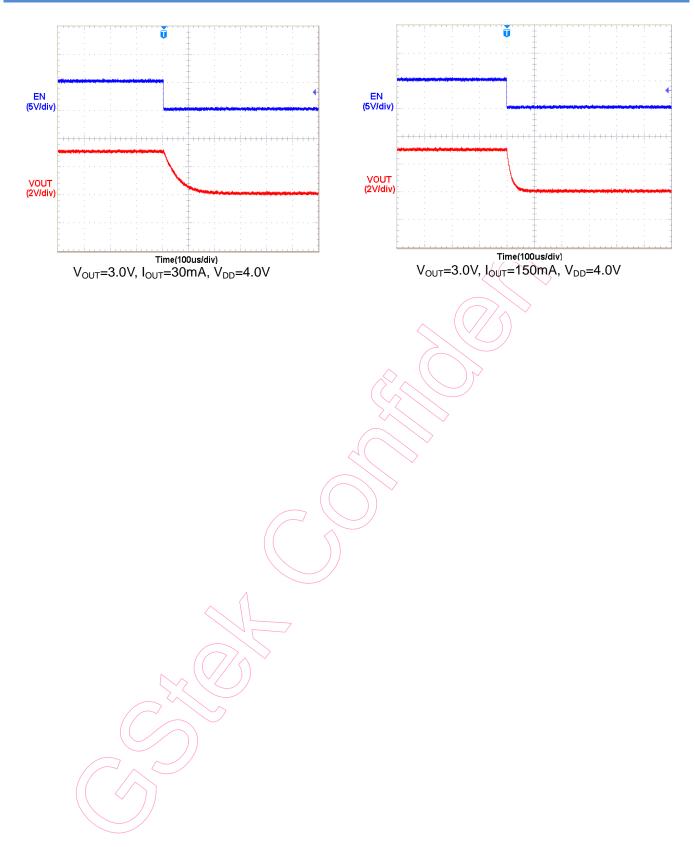
Low Noise 300mA LDO Regulator





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Low Noise 300mA LDO Regulator



Application Information Enable

The GS7119 has a dedicated enable pin(EN). When the EN pin is in the logic low (V_{EN} <0.3V), the regulator will be turned off, reducing the supply current to less than 1uA.

When the EN pin is in the logic high (V_{EN} >1.2V), the regulator will be turned on. Left open, the EN pin is pulled down by a internal resistor to shut down the regulator.

Current Limit and Short circuit current protection

The GS7119 use a current mirror to monitor the output current. A small portion of the PMOS output transistor's current is mirrored onto a resistor such that the voltage across this resistor is proportional to the output current; this voltage is compared against the feedback voltage. Once the output current cannot exceeds the limit. The current is set to 480mA typically.

When the output voltage is less than 0.2V, the short circuit current protection starts and maintains the loading current to 40mA. The output can be shorted to ground without damaging the device.

Output Capacitor

The GS7119 is specifically designed to employ ceramic output capacitors as low as 1uF (X7R). The ceramic capacitors offer significant cost and space savings, along with high frequency noise filtering. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

Ceramic capacitors have different temperature characteristics and bias characteristics which depend on their dimensions and manufacturers. If the setting voltage is 2.5V or more and the capacitor's dimensions for V_{OUT} equal to 1.0mm by 0.5mm or smaller than that, the capacitance value might be extremely low. As a result, the capacitance might be much less than expected value. In such cases, the operation might be unstable at low temperature (-25°C or less). In that case, use a larger capacity, or a large dimensions' capacitor. (For example 1.6mm by 0.8mm)

Input Capacitor

Good bypassing is recommended from input to ground to help improve AC performance. A 1uF (X7R) input capacitor or greater located as close as possible to the IC is recommended. Place the capacitors physically as close as possible to the device with wide and direct PCB traces.

Power Dissipation and Layout Considerations Excessive power dissipation may cause thermal overload, and hence the increase of the IC junction temperature beyond a safe operating level. For continuous operation, it is highly recommended to keep the junction temperature below the maximum operation junction temperature 125°C for maximum reliability.

The relationship between θ_{JA} and $T_{J(MAX)}$ can be calculated as:

$\mathsf{P}_{\mathsf{D}(\mathsf{MAX})} = (\mathsf{T}_{\mathsf{J}(\mathsf{MAX})} - \mathsf{T}_{\mathsf{A}}) \: / \: \theta_{\mathsf{JA}}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

The power dissipation definition in device is:

 $\mathsf{P}_\mathsf{D} = (\mathsf{V}_\mathsf{IN} - \mathsf{V}_\mathsf{OUT}) \times \mathsf{I}_\mathsf{OUT} + \mathsf{V}_\mathsf{DD} \times \mathsf{I}_\mathsf{Q}$

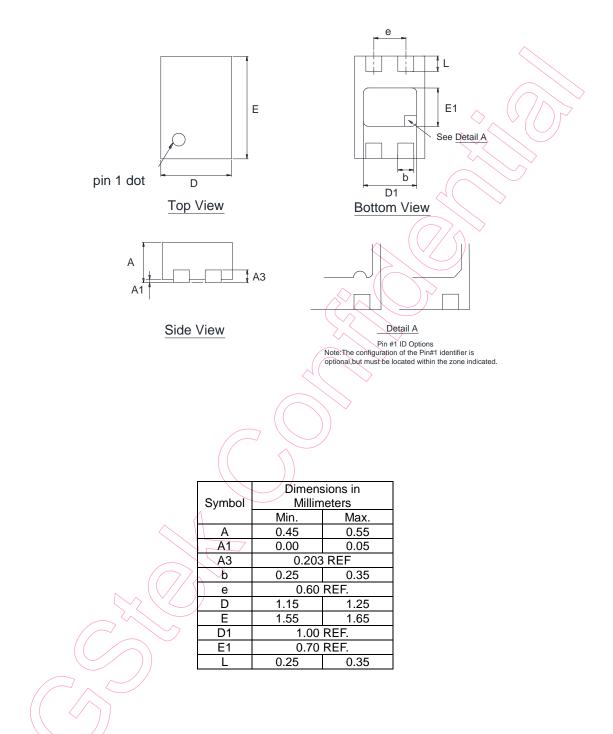
As the above equations indicate, it is desirable to

Low Noise 300mA LDO Regulator

work ICs whose θ_{JA} values are small such that $T_{J(MAX)}$ does not increase strongly with P_D . To avoid thermally overloading the GS7119, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating condition. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

GS7119

Package Dimensions, WDFN4-1.2x1.6



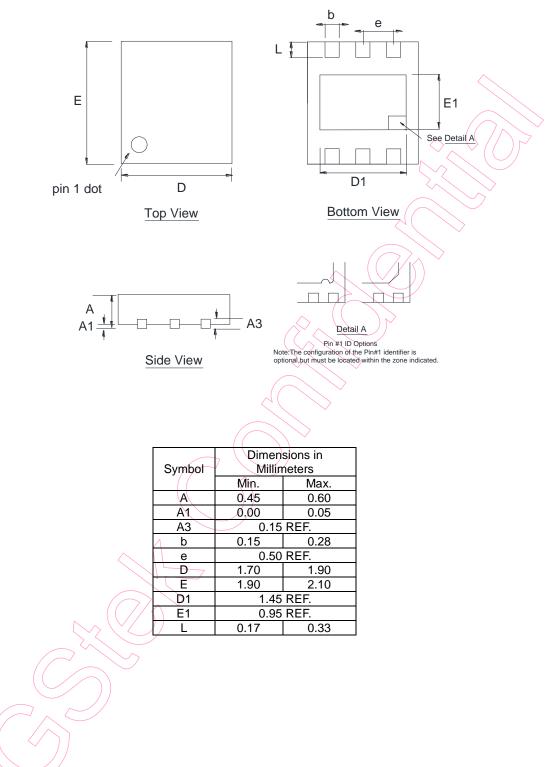
Note .

1.Min.: Minimum dimension specified.

2.Max.: Maximum dimension specified.

3.REF.: Reference. Normal/Regular dimension specified for reference.

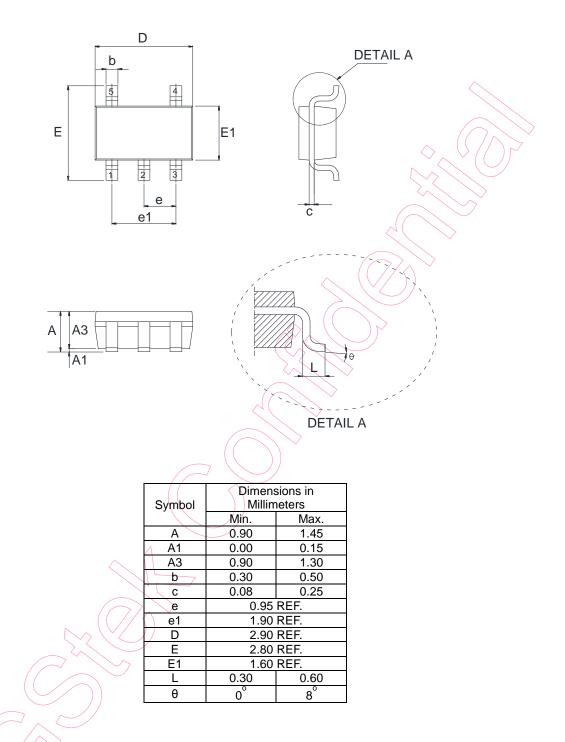
Package Dimensions, TDFN6-1.8x2



Note:

- 1. Min.: Minimum dimension specified.
- 2. Max.: Maximum dimension specified.
- 3. REF.: Reference. Normal/Regular dimension specified for reference.

Package Dimensions, SOT-23-5



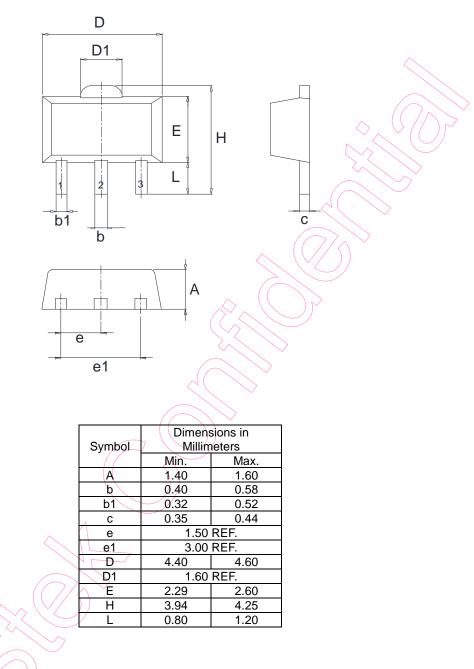
Note .

1.Min.: Minimum dimension specified.

2.Max.: Maximum dimension specified.

3.REF.: Reference. Normal/Regular dimension specified for reference.

Package Dimensions, SOT-89-3



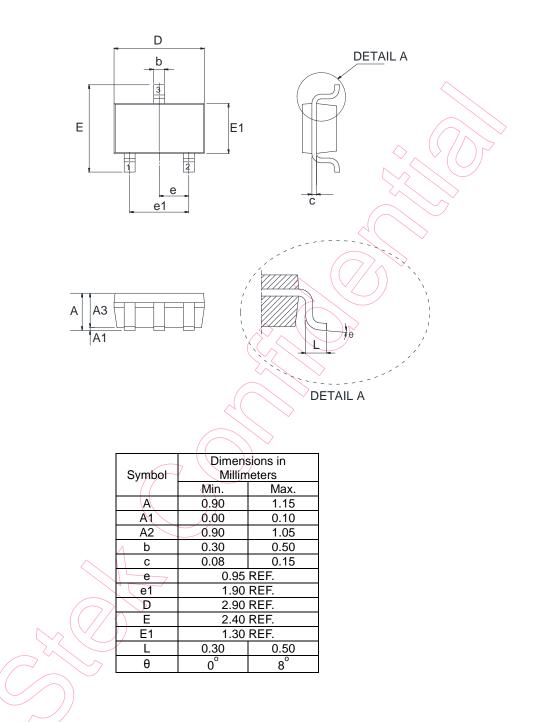
Note .

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2.Max.: Maximum dimension specified.

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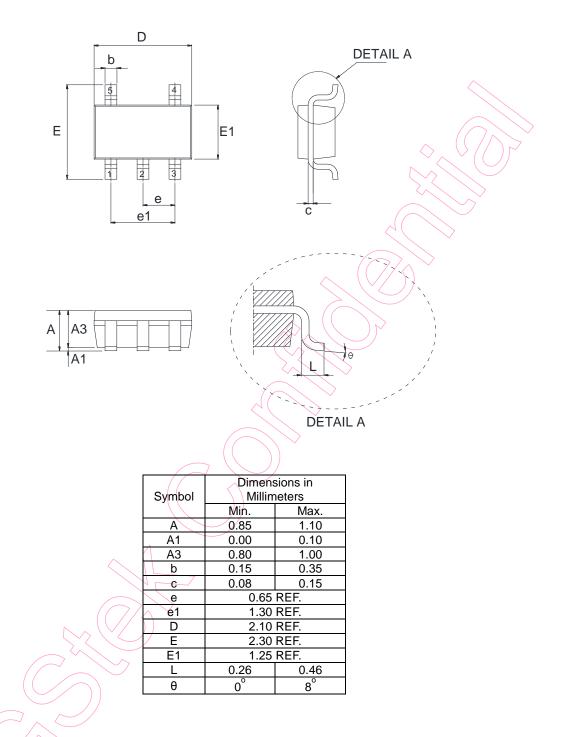
Package Dimensions, MSOT-23



Note:

- 1. Min.: Minimum dimension specified.
- 2. Max.: Maximum dimension specified.
- 3. REF.: Reference. Normal/Regular dimension specified for reference.

Package Dimensions, SOT-353(SC-75)



Note .

1.Min.: Minimum dimension specified.

2.Max.: Maximum dimension specified.

3.REF.: Reference. Normal/Regular dimension specified for reference.

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