

# HCNW4502/3

## HCPL-0452/0453/4502/4503

### Single Channel, High Speed Optocouplers



## Data Sheet



Lead (Pb) Free  
RoHS 6 fully compliant

RoHS 6 fully compliant options available;  
-xxxE denotes a lead-free product

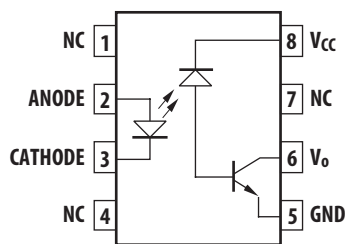
### Description

These diode-transistor optocouplers use an insulating layer between a LED and an integrated photodetector to provide electrical insulation between input and output. Separate connections for the photodiode bias and output-transistor collector increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

These single channel optocouplers are available in 8-Pin DIP, SO-8 and Widebody package configurations.

The HCPL-4502/4503 and HCNW4502/4503 are designed for high speed TTL/TTL applications. A standard 16 mA TTL sink current through the input LED will provide enough output current for 1 TTL load and a 5.6 kΩ pull-up resistor. CTR for these devices is 19% minimum at  $I_F = 16$  mA.

### Functional Diagram



TRUTH TABLE  
(POSITIVE LOGIC)

LED	$V_o$
ON	LOW
OFF	HIGH

A 0.1  $\mu$ F bypass capacitor must be connected between pins 5 and 8.

### Features

- 15 kV/ $\mu$ s minimum common mode transient immunity at  $V_{CM} = 1500$  V
- High speed: 1 Mb/s
- TTL compatible
- Available in 8-Pin DIP, SO-8, widebody packages
- Open collector output
- Guaranteed performance from temperature: 0°C to 70°C
- Safety approval
  - UL Recognized – 3750  $V_{rms}$  for 1 minute (5000  $V_{rms}$  for 1 minute for HCNW and Option 020 devices) per UL1577
  - CSA Approved
  - IEC/EN/DIN EN 60747-5-5 Approved
    - $V_{IORM} = 630$  V peak for HCPL-4503#060
    - $V_{IORM} = 1414$  V peak for HCNW devices
- Dual channel version available (4534/0534)
- MIL-PRF-38534 hermetic version available (55XX/65XX/4N55)

### Applications

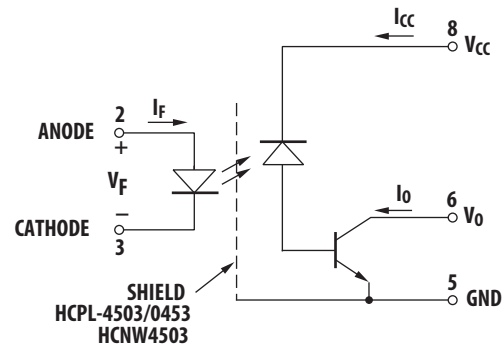
- High voltage insulation
- Video signal isolation
- Power transistor isolation in motor drives
- Line receivers
- Feedback element in switched mode power supplies
- High speed logic ground isolation
  - TTL/TTL, TTL/CMOS, TTL/LSTTL
- Replaces pulse transformers
- Replaces slow phototransistor isolators
- Analog signal ground isolation

**CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The HCPL-4502, HCPL-0452, and HCNW4502 provide the electrical and switching performance of the 6N136, HCPL-0501, and HCNW136 with increased ESD protection.

The HCPL-4503, HCPL-0453, and HCNW4503 are similar to the HCPL-4502, HCPL-0452, and HCNW4502 optocouplers but have increased common mode transient immunity of 15 kV/ $\mu$ s minimum at  $V_{CM} = 1500V$  guaranteed.

### Schematic



### Selection Guide

Minimum CMR		8-Pin DIP (300 Mil)		Small-Outline SO-8 (400 Mil)		Widebody Hermetic		
$dV/dt$ (V/ $\mu$ s)	$V_{CM}$ (V)	Current Transfer Ratio (%)	Single Channel Package	Dual Channel Package*	Single Channel Package	Dual Channel Package*	Single Channel Package	Single and Dual Channel Packages*
10	1500	19	HCPL-4502		HCPL-0452		HCNW4502	
15,000	1500	19	HCPL-4503	HCPL-4534	HCPL-0453	HCPL-0534	HCNW4503	
1,000	10	9						HCPL-55XX HCPL-65XX 4N55

\*Technical data for these products are on separate Avago publications.

## Ordering Information

HCPL-4502 and HCPL-4503, HCPL-0452, HCPL-0453 are UL Recognized with 3750 V<sub>rms</sub> for 1 minute per UL1577.

HCNW4502 and HCNW4503 are UL Recognized with 5000 V<sub>rms</sub> for 1 minute per UL1577. All devices listed above are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	UL 5000 V <sub>rms</sub> / 1 Minute rating	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant	Non RoHS Compliant							
HCPL-4502 HCPL-4503	-000E	No option	300mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	#520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-360E	#360		X	X			X	50 per tube
	-560E	#560		X	X	X		X	1000 per reel
HCPL-0452 HCPL-0453	-000E	No option	SO-8						100 per tube
	-500E	#500		X	X	X			1500 per reel
	-060E	#060						X	100 per tube
	-560E	#560		X	X	X		X	1500 per reel
HCNW4502 HCNW4503	-000E	No option	400mil Widebody DIP-8				X	X	42 per tube
	-300E	#300		X	X		X	X	42 per tube
	-500E	#500		X	X	X	X	X	750 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-4502-560E to order product of 300mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

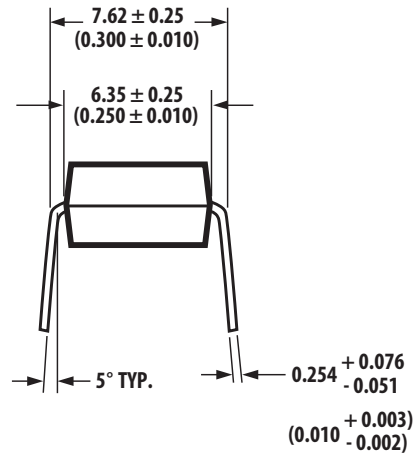
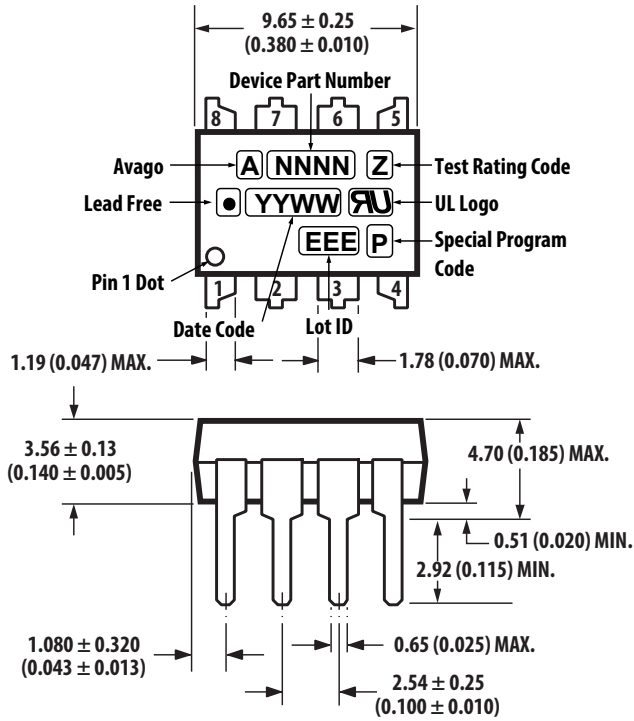
HCPL-4502 to order product of 300mil DIP package in tube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since 15th July 2001 and RoHS compliant option will use '-XXXE'.

## Package Outline Drawings

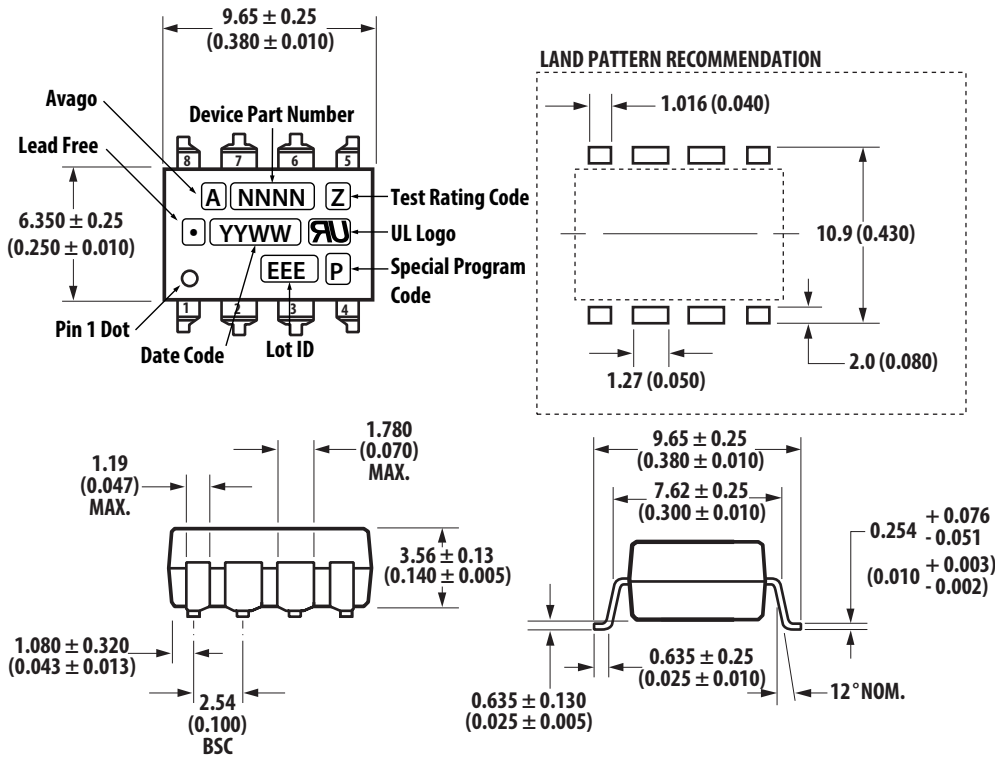
### 8-Pin DIP Package (HCPL-4502/3)



Dimensions in millimeters and (inches).  
 \*marking code letter for option numbers  
 "L" = option 020  
 "V" = option 060  
 Option numbers 300 and 500 not marked.

Note: Floating lead protrusion is 0.25 mm (10 mils) max.

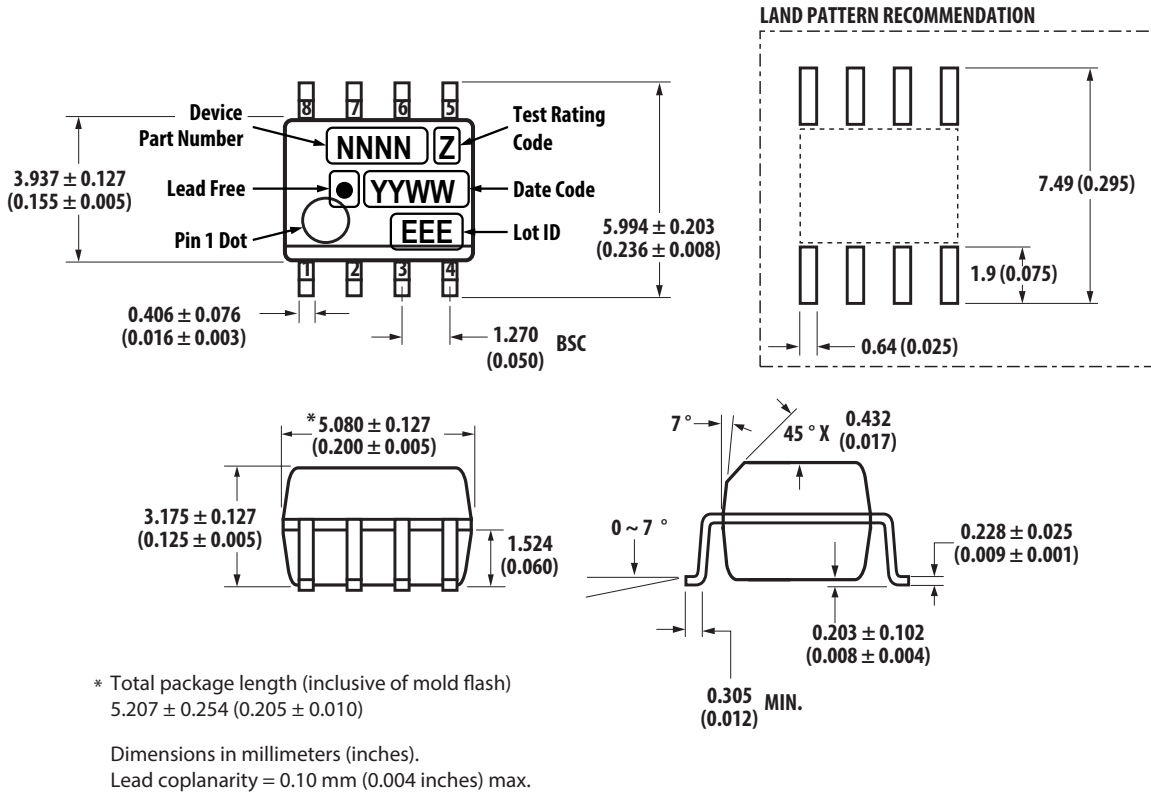
### 8-Pin DIP Package with Gull Wing Surface Mount Option 300 (HCPL-4502/3)



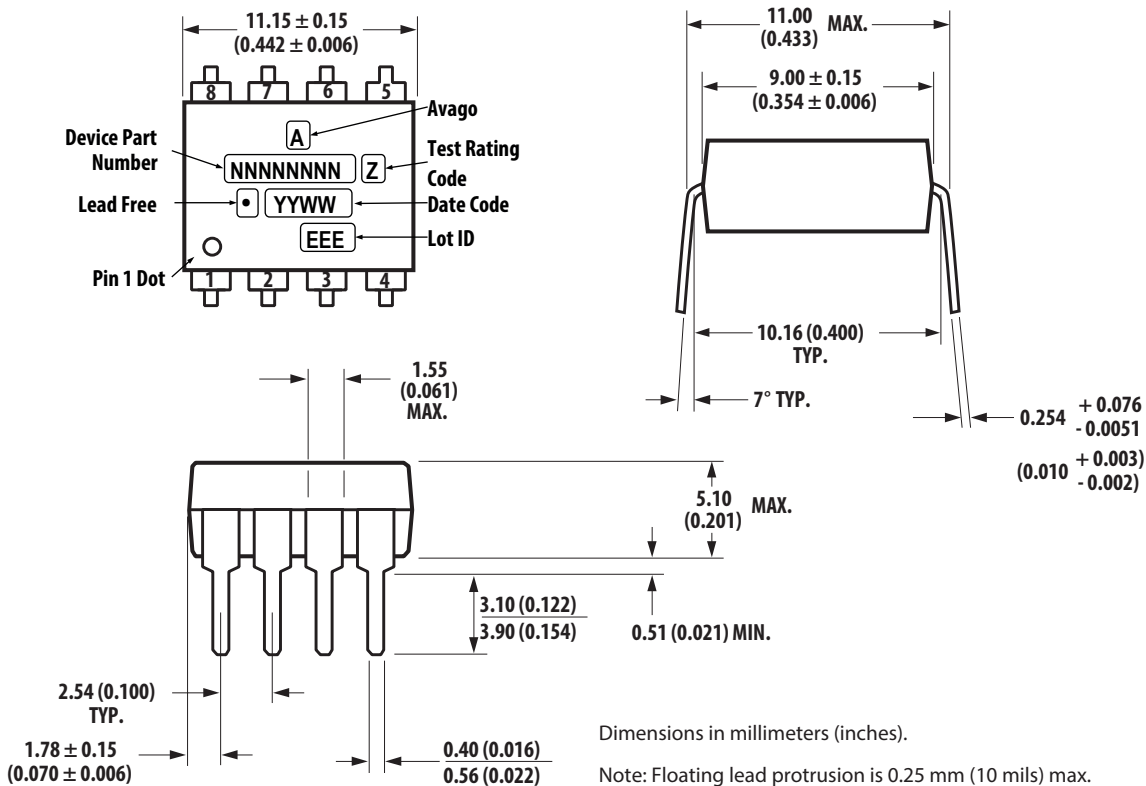
Dimensions in millimeters (inches).  
 Lead coplanarity = 0.10 mm (0.004 inches).

Note: Floating lead protrusion is 0.25 mm (10 mils) max.

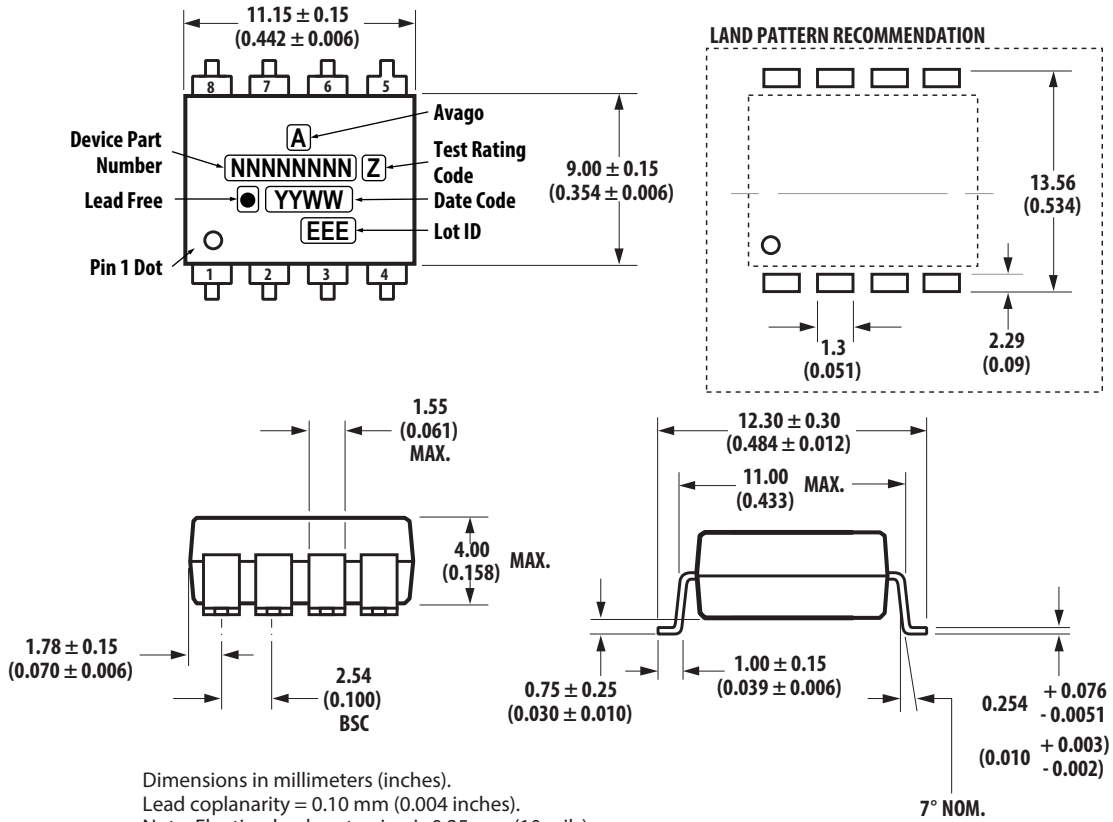
### Small Outline SO-8 Package (HCPL-0452/3)



### 8-Pin Widebody DIP Package (HCNW4502/3)



### 8-Pin Widebody DIP Package with Gull Wing Surface Mount Option 300 (HCNW4502/3)



## Solder Reflow Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-Halide Flux should be used.

## Regulatory Information

The devices contained in this data sheet have been approved by the following organizations:

### UL

Recognized under UL 1577, Component Recognition Program, File E55361.

**IEC/EN/DIN EN 60747-5-5** (HCNW and option 060 only)

Approved with Maximum Working Insulation Voltage

$V_{\text{ioirm}} = 560 V_{\text{peak}}$  for HCPL-0452/0453,

$V_{\text{ioirm}} = 630 V_{\text{peak}}$  for HCPL-4502/4503, and

$V_{\text{ioirm}} = 1414 V_{\text{peak}}$  for HCNW4502/4503.

### CSA

Approved under CSA Component Acceptance Notice #5, File CA 88324.

## Insulation and Safety Related Specifications

Parameter	Symbol	8-Pin DIP (300 Mil) Value	SO-8 Value	Widebody (400 Mil) Value	Unit	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	> 175	> 175	> 175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 - surface mount classification is Class A in accordance with CECC 00802.

### IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics (OPTION 060 ONLY)

Description	Symbol	Characteristic		Units
		HCPL-4502/4503	HCPL-0452/0453	
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage $\leq 300 V_{rms}$		I-IV	I-IV	
for rated mains voltage $\leq 600 V_{rms}$		I-IV	I-III	
Climatic Classification		55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/39)		2	2	
Maximum Working Insulation Voltage	$V_{IORM}$	630	560	$V_{peak}$
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	1181	1050	$V_{peak}$
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.6 = V_{PR}$ , Type and sample test, $t_m = 10$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	1008	896	$V_{peak}$
Highest Allowable Overvoltage* (Transient Overvoltage, $t_{ini} = 60$ sec)	$V_{IOTM}$	8000	6000	$V_{peak}$
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 9, Thermal Derating curve.)				
Case Temperature	$T_s$	175	175	$^{\circ}C$
Input Current	$I_{S,INPUT}$	230	150	mA
Output Power	$P_{S,OUTPUT}$	600	600	mW
Insulation Resistance at $T_s, V_{IO} = 500$ V	$R_s$	$\geq 10^9$	$\geq 10^9$	$\Omega$

### IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics (HCNW4502/3 ONLY)

Description	Symbol	Characteristic	Units
Installation classification per DIN VDE 0110/39, Table 1 for rated mains voltage $\leq 600$ V rms		I-IV	
for rated mains voltage $\leq 1000$ V rms		I-III	
Climatic Classification		55/85/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	$V_{IORM}$	1414	$V_{peak}$
Input to Output Test Voltage, Method b* $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	2652	$V_{peak}$
Input to Output Test Voltage, Method a* $V_{IORM} \times 1.6 = V_{PR}$ , Type and sample test, $t_m = 10$ sec, Partial Discharge $< 5$ pC	$V_{PR}$	2262	$V_{peak}$
Highest Allowable Overvoltage* (Transient Overvoltage, $t_{ini} = 60$ sec)	$V_{IOTM}$	8000	$V_{peak}$
Safety Limiting Values (Maximum values allowed in the event of a failure, also see Figure 9, Thermal Derating curve.)			
Case Temperature	$T_s$	150	$^{\circ}C$
Input Current	$I_{S,INPUT}$	400	mA
Output Power	$P_{S,OUTPUT}$	700	mW
Insulation Resistance at $T_s, V_{IO} = 500$ V	$R_s$	$\geq 10^9$	$\Omega$

\*Refer to the front of the optocoupler section of the current catalog, under Product Safety Regulations section IEC/EN/DIN EN 60747-5-5, for a detailed description.

Note: Isolation characteristics are guaranteed only within the safety maximum ratings which must be ensured by protective circuits in application.



## Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units	Note
Storage Temperature	$T_S$		-55	125	°C	
Operating Temperature	$T_A$	8-Pin DIP SO-8	-55	100	°C	
		Widebody	-55	85		
Average Forward Input Current	$I_{F(AVG)}$			25	mA	1
Peak Forward Input Current (50% duty cycle, 1 ms pulse width)	$I_{F(PEAK)}$	8-Pin DIP SO-8		50	mA	2
		Widebody		40		
Peak Transient Input Current ( $\leq 1 \mu\text{s}$ pulse width, 300 pps)	$I_{F(TRANS)}$	8-Pin DIP SO-8		1	A	
		Widebody		0.1		
Reverse LED Input Voltage (Pin 3-2)	$V_R$	8-Pin DIP SO-8		5	V	
		Widebody		3		
Input Power Dissipation	$P_{IN}$	8-Pin DIP SO-8		45	mW	3
		Widebody		40		
Average Output Current (Pin 6)	$I_{O(AVG)}$			8	mA	
Peak Output Current	$I_{O(PEAK)}$			16	mA	
Emitter-Base Reverse Voltage (Pin 5-7, except 4502/3, 0452/3)	$V_{EBR}$			5	V	
Supply Voltage (Pin 8-5)	$V_{CC}$		-0.5	30	V	
Output Voltage (Pin 6-5)	$V_O$		-0.5	20	V	
Base Current (Pin 7, except 4502/3, 0452/3)	$I_B$			5	mA	
Output Power Dissipation	$P_O$			100	mW	4
Lead Solder Temperature (Through-Hole Parts Only)						
1.6 mm below seating plane, 10 seconds up to seating plane, 10 seconds	$T_{LS}$	8-Pin DIP		260	°C	
		Widebody		260	°C	
Reflow Temperature Profile	$T_{RP}$	SO-8 and Option 300	See <b>Package Outline Drawings</b> section			

## Electrical Specifications (DC)

Over recommended temperature ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ) unless otherwise specified. See note 13.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	HCPL-4502/3 HCPL-0452/3 HCNW4502/3	19 15	24 24	50	%	$T_A = 25^\circ\text{C}$ $V_O = 0.4\text{ V}$ $V_O = 0.5\text{ V}$	$I_F = 16\text{ mA}$ $V_{CC} = 4.5\text{ V}$	1, 2, 5 4
Logic Low Output Voltage	$V_{OL}$	HCPL-4502/3 HCPL-0452/3 HCNW4502/3		0.1 0.1	0.4 0.5	V	$T_A = 25^\circ\text{C}$ $I_O = 3.0\text{ mA}$ $I_O = 2.4\text{ mA}$	$I_F = 16\text{ mA}$ $V_{CC} = 4.5\text{ V}$	
Logic High Output Current	$I_{OH}$			0.003 0.01	0.5 1	$\mu\text{A}$	$T_A = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$	$V_O = V_{CC} = 5.5\text{ V}$ $V_O = V_{CC} = 15\text{ V}$ $V_O = V_{CC} = 15\text{ V}$	$I_F = 0\text{ mA}$ 7
Logic Low Supply Current	$I_{CCL}$			50	200	$\mu\text{A}$	$I_F = 16\text{ mA}$ , $V_O = \text{Open}$ , $V_{CC} = 15\text{ V}$		10
Logic High Supply Current	$I_{CCH}$			0.02	1	$\mu\text{A}$	$T_A = 25^\circ\text{C}$ $I_F = 16\text{ mA}$ , $V_O = \text{Open}$ , $V_{CC} = 15\text{ V}$		10
Input Forward Voltage	$V_F$	8-Pin DIP SO-8 Widebody		1.5 1.45 1.35	1.7 1.8 1.85 1.95	V	$T_A = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$	$I_F = 16\text{ mA}$ $I_F = 16\text{ mA}$	3
Input Reverse Breakdown Voltage	$BV_R$	8-Pin DIP SO-8 Widebody	5 3			V	$I_R = 10\text{ }\mu\text{A}$ $I_R = 100\text{ }\mu\text{A}$		
Temperature Coefficient of Forward Voltage	$\Delta V_F / \Delta T_A$	8-Pin DIP SO-8 Widebody		-1.6 -1.9		$\text{mV}/^\circ\text{C}$	$I_F = 16\text{ mA}$		
Input Capacitance	$C_{IN}$	8-Pin DIP SO-8 Widebody		60 90		pF	$f = 1\text{ MHz}$ , $V_F = 0\text{ V}$		
Transistor DC Current Gain	$h_{FE}$	8-Pin DIP SO-8 Widebody		150 130 180 160			$V_O = 5\text{ V}$ , $I_O = 3\text{ mA}$ $V_O = 0.4\text{ V}$ , $I_B = 20\text{ }\mu\text{A}$ $V_O = 0.4\text{ V}$ , $I_B = 20\text{ }\mu\text{A}$ $V_O = 5\text{ V}$ , $I_O = 3\text{ mA}$		

\*All typicals at  $T_A = 25^\circ\text{C}$ .

## Switching Specifications (AC)

Over recommended temperature ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ),  $V_{CC} = 5\text{ V}$ ,  $I_F = 16\text{ mA}$  unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note	
Propagation Delay Time to Logic Low at Output	$t_{\text{PHL}}$	HCPL-4502/3	0.2	0.8		$\mu\text{s}$	$T_A = 25^\circ\text{C}$ $R_L = 1.9\text{ k}\Omega$	5, 6,	8	
		HCPL-0452/3		1.0						
		HCNW4502/3								
Propagation Delay Time to Logic High at Output	$t_{\text{PLH}}$	HCPL-4502/3	0.6	0.8		$\mu\text{s}$	$T_A = 25^\circ\text{C}$ $R_L = 1.9\text{ k}\Omega$	5, 6,	8	
		HCPL-0452/3		1.0						
		HCNW4502/3								
Common Mode Transient Immunity at Logic High Level Output	$ CM_H $	HCPL-4502		1		$\text{kV}/\mu\text{s}$	$R_L = 1.9\text{ k}\Omega$ $I_F = 0\text{ mA}$ , $T_A = 25^\circ\text{C}$ , $V_{CM} = 10\text{ V}_{\text{p-p}}$ $C_L = 15\text{ pF}$	11	7, 8	
		HCPL-0452								
		HCNW4502								
		HCPL-4503	15	30						$R_L = 1.9\text{ k}\Omega$ $I_F = 0\text{ mA}$ , $T_A = 25^\circ\text{C}$ , $V_{CM} = 1500\text{ V}_{\text{p-p}}$ $C_L = 15\text{ pF}$
		HCPL-0453								
HCNW4503										
Common Mode Transient Immunity at Logic Low Level Output	$ CM_L $	HCPL-4502		1		$\text{kV}/\mu\text{s}$	$R_L = 1.9\text{ k}\Omega$ $I_F = 16\text{ mA}$ , $T_A = 25^\circ\text{C}$ , $V_{CM} = 10\text{ V}_{\text{p-p}}$ $C_L = 15\text{ pF}$	11	7, 8	
		HCPL-0452								
		HCNW4502								
		HCPL-4503	15	30						$R_L = 1.9\text{ k}\Omega$ $I_F = 16\text{ mA}$ , $T_A = 25^\circ\text{C}$ , $V_{CM} = 1500\text{ V}_{\text{p-p}}$ $C_L = 15\text{ pF}$
		HCPL-0453								
HCNW4503										

\*All typicals at  $T_A = 25^\circ\text{C}$ .

## Package Characteristics

Over recommended temperature ( $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ) unless otherwise specified.

Parameter	Sym.	Device	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Input-Output Momentary Withstand Voltage**	$V_{ISO}$	8-Pin DIP	3750			V rms	RH < 50%, t = 1 min., $T_A = 25^\circ\text{C}$		6, 11
		SO-8							6, 12
		Widebody	5000						6, 9, 12
		8-Pin DIP (Option 020)	5000						6, 9, 12
	$I_{I-O}$	8-Pin DIP			1	$\mu\text{A}$	45% RH, t = 5 s, $V_{I-O} = 3 \text{ kVdc}$ , $T_A = 25^\circ\text{C}$		6, 13
Input-Output Resistance	$R_{I-O}$	8-Pin DIP		$10^{12}$		$\Omega$	$V_{I-O} = 500 \text{ Vdc}$		6
		SO-8							
		Widebody	$10^{12}$	$10^{13}$			$T_A = 25^\circ\text{C}$		
			$10^{11}$				$T_A = 100^\circ\text{C}$		
Input-Output Capacitance	$C_{I-O}$	8-Pin DIP		0.6		pF	f = 1 MHz		6
		SO-8							
		Widebody		0.5	0.6				

\*All typicals at  $T_A = 25^\circ\text{C}$ .

\*\*The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage," publication number 5963-2203E.

### Notes:

- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $0.8 \text{ mA}/^\circ\text{C}$  (8-Pin DIP).  
Derate linearly above  $85^\circ\text{C}$  free-air temperature at a rate of  $0.5 \text{ mA}/^\circ\text{C}$  (SO-8).
- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $1.6 \text{ mA}/^\circ\text{C}$  (8-Pin DIP).  
Derate linearly above  $85^\circ\text{C}$  free-air temperature at a rate of  $1.0 \text{ mA}/^\circ\text{C}$  (SO-8).
- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $0.9 \text{ mW}/^\circ\text{C}$  (8-Pin DIP).  
Derate linearly above  $85^\circ\text{C}$  free-air temperature at a rate of  $1.1 \text{ mW}/^\circ\text{C}$  (SO-8).
- Derate linearly above  $70^\circ\text{C}$  free-air temperature at a rate of  $2.0 \text{ mW}/^\circ\text{C}$  (8-Pin DIP).  
Derate linearly above  $85^\circ\text{C}$  free-air temperature at a rate of  $2.3 \text{ mW}/^\circ\text{C}$  (SO-8).
- CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current,  $I_{O'}$  to the forward LED input current,  $I_F$ , times 100.
- Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
- Common mode transient immunity in a Logic High level is the maximum tolerable (positive)  $dV_{CM}/dt$  on the leading edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a Logic High state (i.e.,  $V_O > 2.0 \text{ V}$ ). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative)  $dV_{CM}/dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a Logic Low state (i.e.,  $V_O < 0.8 \text{ V}$ ).
- The  $1.9 \text{ k}\Omega$  load represents 1 TTL unit load of  $1.6 \text{ mA}$  and the  $5.6 \text{ k}\Omega$  pull-up resistor.
- See Option 020 data sheet for more information.
- Use of a  $0.1 \mu\text{F}$  bypass capacitor connected between pins 5 and 8 is recommended.
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 4500 \text{ V rms}$  for 1 second (leakage detection current limit,  $I_{I-O} \leq 5 \mu\text{A}$ ). This test is performed before the 100% Production test shown in the IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics Table if applicable.
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage  $\geq 6000 \text{ V rms}$  for 1 second (leakage detection current limit,  $I_{I-O} \leq 5 \mu\text{A}$ ). This test is performed before the 100% Production test shown in the IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristics Table if applicable.
- This rating is equally validated by an equivalent ac proof test.



Figure 1. DC and pulsed transfer characteristics.

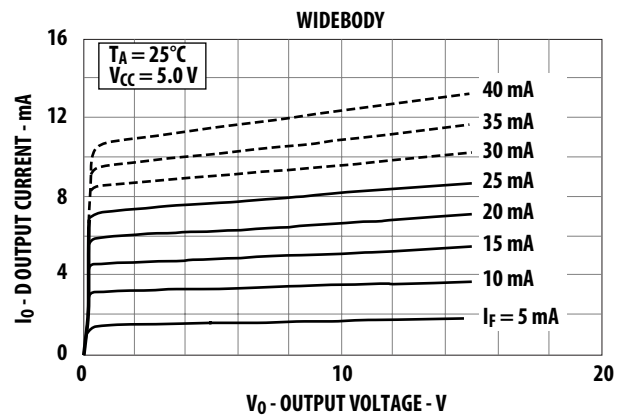


Figure 2. Current transfer ratio vs. input current.

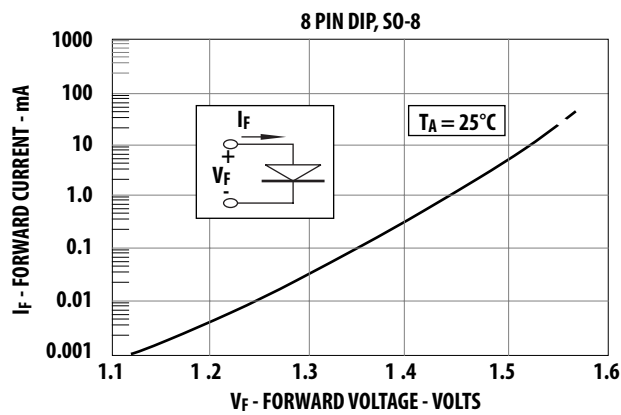
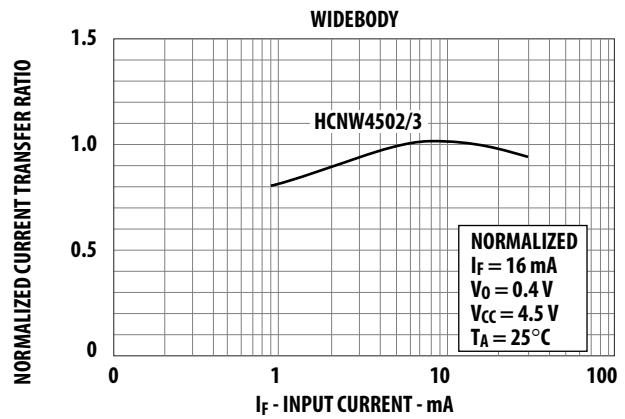


Figure 3. Input current vs. forward voltage.

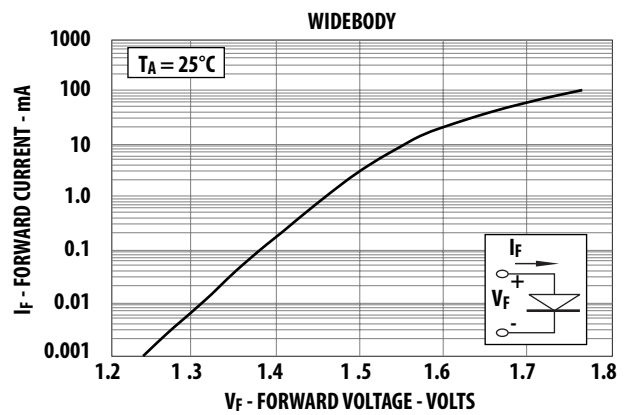




Figure 4. Current transfer ratio vs. temperature.



Figure 5. Propagation delay vs. temperature.



Figure 6. Propagation delay time vs. load resistance.



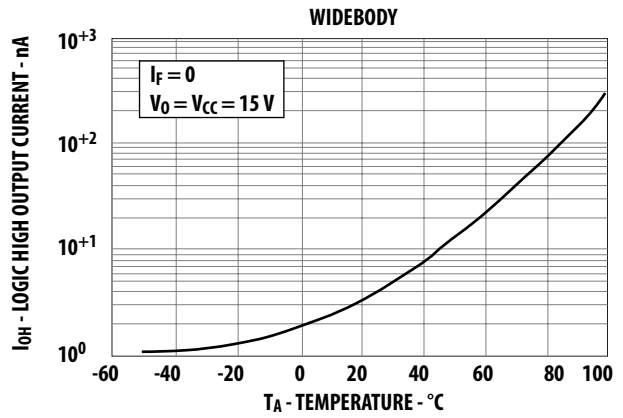
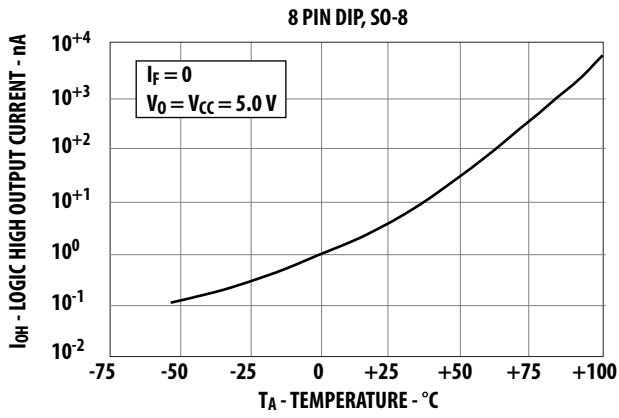


Figure 7. Logic high output current vs. temperature.

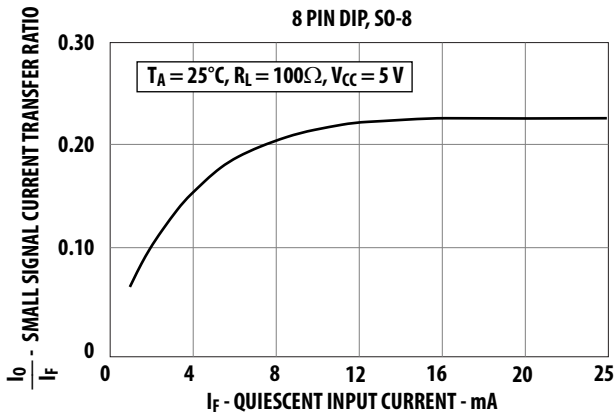


Figure 8. Small-signal current transfer ratio vs. quiescent input current.

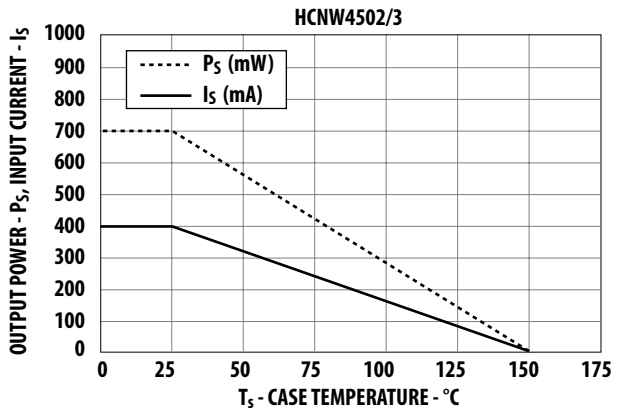
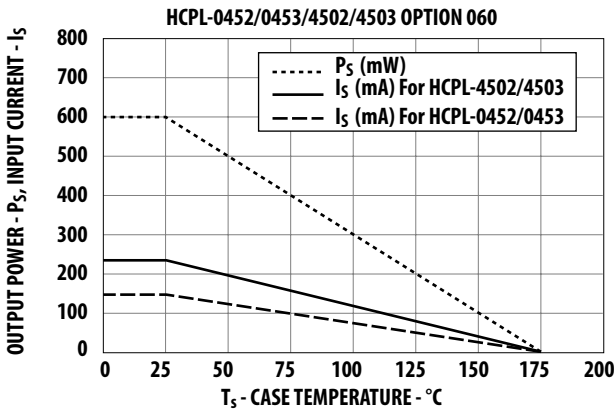


Figure 9. Thermal derating curve, dependence of safety limiting value with case temperature per IEC/EN/DIN EN 60747-5-5.

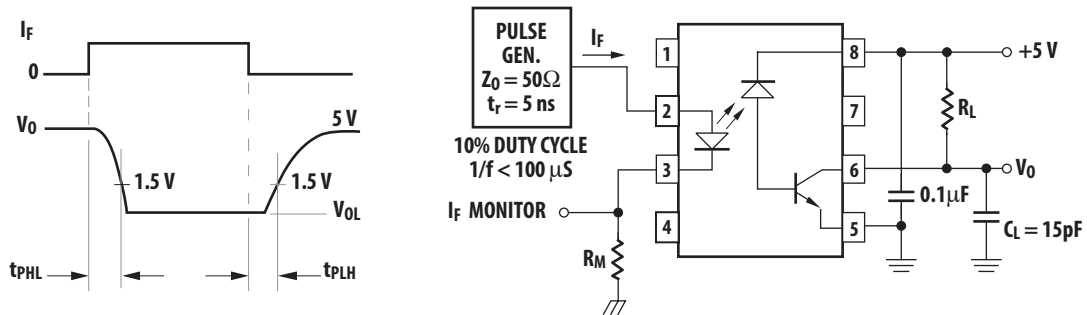


Figure 10. Switching test circuit.

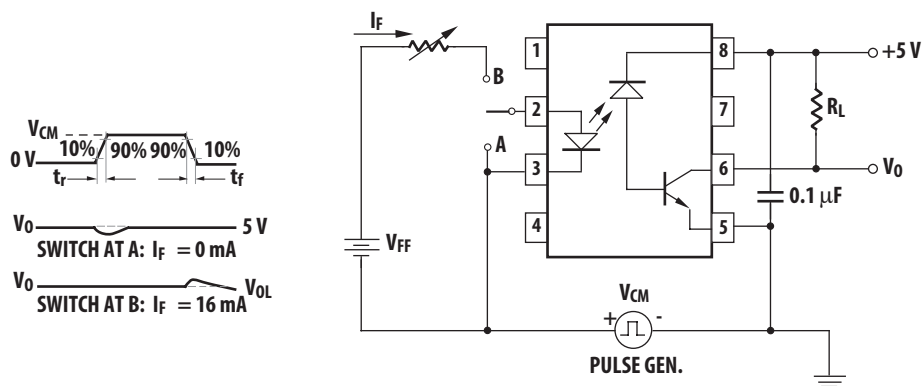


Figure 11. Test circuit for transient immunity and typical waveforms.

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