TLC5925 Low-Power 16-Channel Constant-Current LED Sink Driver

1 Features

- 16 Constant-Current Output Channels
- Constant Output Current Invariant to Load Voltage Change
- Excellent Output Current Accuracy:
  - Between Channels: < ±4% (Max)
  - Between ICs: < ±6% (Max)
- Constant Output Current Range: 3 mA to 45 mA
- Output Current Adjusted By External Resistor
- Fast Response of Output Current, $\overline{OE}$ (Min): 100 ns
- 30-MHz Clock Frequency
- Schmitt-Trigger Inputs
- 3.3-V to 5-V Supply Voltage
- Thermal Shutdown for Overtemperature Protection
- ESD Performance: 1-kV HBM

2 Applications

- Gaming Machine and Entertainment
- General LED Applications
- LED Display Systems
- Signs LED Lighting
- White Goods

3 Description

The TLC5925 is designed for LED displays and LED lighting applications. The TLC5925 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC5925 output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of VF variations. Used in system design for LED display applications (such as, LED panels), the TLC5925 provides great flexibility and device performance. Users can adjust the output current from 3 mA to 45 mA through an external resistor, R_{ext}, which gives flexibility in controlling the light intensity of LEDs. TLC5925 is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

The serial data is transferred into TLC5925 via SDI, shifted in the shift register, and transferred out via SDO. LE can latch the serial data in the shift register to the output latch. $\overline{OE}$ enables the output drivers to sink current.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC5925	SSOP (24)	8.65 mm × 3.90 mm
	SOIC (24)	15.40 mm × 7.50 mm
	TSSOP (24)	7.80 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application

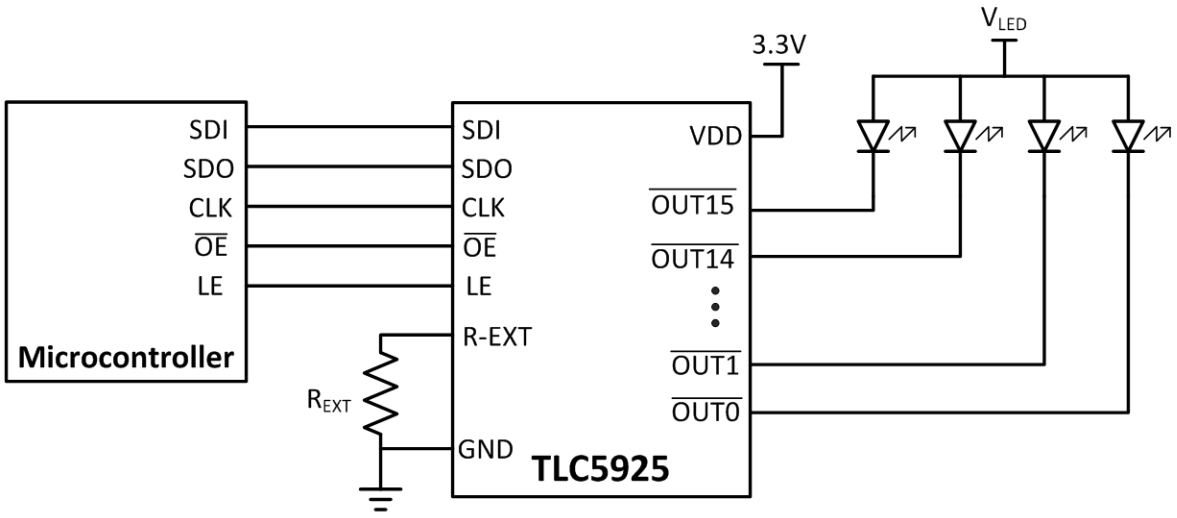


Table of Contents

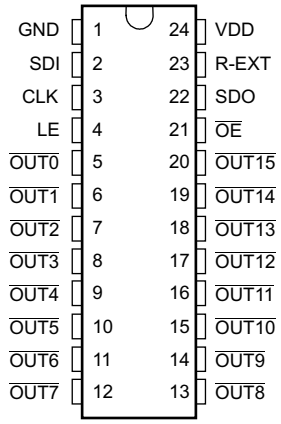
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2013) to Revision B	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

DBQ, DW, or PWP Package
24-Pin SSOP, SOIC, or TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CLK	3	I	Clock input for data shift on rising edge
GND	1	—	Ground for control logic and current sink
LE	4	I	Data strobe input Serial data is transferred to the respective latch when LE is high. The data is latched when LE goes low. LE has an internal pull-down resistor.
$\overline{OE}$	21	I	Output enable When $\overline{OE}$ is active (low), the output drivers are enabled. When $\overline{OE}$ is high, all output drivers are turned OFF (blanked). $\overline{OE}$ has an internal pullup resistor.
$\overline{OUT0}$	5	O	Constant-current outputs
$\overline{OUT1}$	6		
$\overline{OUT2}$	7		
$\overline{OUT3}$	8		
$\overline{OUT4}$	9		
$\overline{OUT5}$	10		
$\overline{OUT6}$	11		
$\overline{OUT7}$	12		
$\overline{OUT8}$	13		
$\overline{OUT9}$	14		
$\overline{OUT10}$	15		
$\overline{OUT11}$	16		
$\overline{OUT12}$	17		
$\overline{OUT13}$	18		
$\overline{OUT14}$	19		
$\overline{OUT15}$	20		
R-EXT	23	I	Input used to connect an external resistor (R_{ext}) for setting output currents
SDI	2	I	Serial-data input to the Shift register
SDO	22	O	Serial-data output to the following SDI of next driver IC or to the microcontroller
VDD	24	I	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	0	7	V
V_I	Input voltage	–0.4	V_{DD} + 0.4	V
V_O	Output voltage	–0.5	20	V
I_{OUT}	Output current		45	mA
I_{GND}	GND terminal current		750	mA
T_A	Free-air operating temperature range	–40	125	°C
T_J	Operating junction temperature range	–40	150	°C
T_{stg}	Storage temperature range	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_{DD}	Supply voltage			3	5.5	V
V_O	Output voltage	$\overline{OUT0}$ to $\overline{OUT15}$			17	V
I_O	Output current	DC test circuit	$V_O \geq 0.6$ V	3		mA
			$V_O \geq 1$ V		45	
I_{OH}	High-level output current	SDO		–1		mA
I_{OL}	Low-level output current	SDO		1		mA
V_{IH}	High-level input voltage	CLK, $\overline{OE}$, LE, and SDI		0.7 × V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage	CLK, $\overline{OE}$, LE, and SDI		GND	0.3 × V_{DD}	V
t_R	Rise Time	CLK			500	ns
t_F	Fall Time	CLK			500	ns

6.4 Thermal Information

THERMAL METRIC (1)			TLC5925 DBQ (SSOP) 24 PINS	TLC5925 DW (SOIC) 24 PINS	TLC5925 PW (TSSOP) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Mounted on JEDEC 1-layer board (JESD 51-3), No airflow	99.8	80.5	118.8	°C/W
		Mounted on JEDEC 4-layer board (JESD 51-7), No airflow	61	45.5	87.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		52.9	45.0	44.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		41.5	44.8	52.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter		16.4	21.7	6.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter		41.2	44.4	52.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: V_{DD} = 3 V

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Input voltage			3		5.5	V
V_O	Output voltage					17	V
I_O	Output current	$V_O \geq 0.6$ V		3			mA
		$V_O \geq 1$ V				45	
I_{OH}	High-level output current, source			-1			mA
I_{OL}	Low-level output current, sink			1			
V_{IH}	High-level input voltage			0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage			GND		0.3 × V_{DD}	
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	µA
			T_J = 125°C			2	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 1680 Ω			13		mA
	Output current error, die-die	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1680 Ω, T_J = 25°C			±3%	±6%	
	Output current error, channel-to-channel	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1680 Ω, T_J = 25°C			±1.5%	±4%	
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 840 Ω			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 840 Ω, T_J = 25°C			±3%	±6%	
	Output current error, channel-to-channel	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 840 Ω, T_J = 25°C			±1.5%	±4%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V, I_O = 13 mA			±0.1		%/V
		V_{DD} = 3.0 V to 5.5 V, I_O = 13 mA to 45 mA			±1		
	Pullup resistance	$\overline{OE}$			500		kΩ
	Pulldown resistance	LE			500		kΩ
T_{sd}	Overtemperature shutdown (1)			150	175	200	°C
T_{hys}	Restart temperature hysteresis				15		°C
I_{DD}	Supply current	R_{ext} = Open			7	10	mA
		R_{ext} = 1680 Ω			9	12	
		R_{ext} = 840 Ω			11	13	
C_{IN}	Input capacitance	V_I = V_{DD} or GND, CLK, SDI, SDO, $\overline{OE}$				10	pF

(1) Specified by design

6.6 Electrical Characteristics: V_{DD} = 5.5 V

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DD}	Input voltage			3		5.5	V
V_O	Output voltage					17	V
I_O	Output current	$V_O \geq 0.6$ V		3			mA
		$V_O \geq 1$ V				45	
I_{OH}	High-level output current, source			-1			mA
I_{OL}	Low-level output current, sink			1			
V_{IH}	High-level input voltage			0.7 × V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage			GND		03 × V_{DD}	
I_{leak}	Output leakage current	V_{OH} = 17 V	T_J = 25°C			0.5	µA
			T_J = 125°C			2	
V_{OH}	High-level output voltage	SDO, I_{OL} = –1 mA		V_{DD} – 0.4			V
V_{OL}	Low-level output voltage	SDO, I_{OH} = 1 mA				0.4	V
$I_{O(1)}$	Output current 1	V_{OUT} = 0.6 V, R_{ext} = 1680 Ω			13		mA
	Output current error, die-die	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1680 Ω, T_J = 25°C			±3$	±6$	
	Output current error, channel-to-channel	I_{OL} = 13 mA, V_O = 0.6 V, R_{ext} = 1680 Ω, T_J = 25°C			±1.5$	±4$	
$I_{O(2)}$	Output current 2	V_O = 0.8 V, R_{ext} = 840 Ω			26		mA
	Output current error, die-die	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 840 Ω, T_J = 25°C			±3%	±6%	
	Output current error, channel-to-channel	I_{OL} = 26 mA, V_O = 0.8 V, R_{ext} = 840 Ω, T_J = 25°C			±1.5%	±4%	
I_{OUT} vs V_{OUT}	Output current vs output voltage regulation	V_O = 1 V to 3 V , I_O = 26 mA			±0.1		%/V
		V_{DD} = 3.0 V to 5.5 V, I_O = 13 mA to 45 mA			±1		
	Pullup resistance	$\overline{OE}$			500		kΩ
	Pulldown resistance	LE			500		kΩ
T_{sd}	Overtemperature shutdown (1)			150	175	200	°C
T_{hys}	Restart temperature hysteresis				15		°C
I_{DD}	Supply current	R_{ext} = Open			9	11	mA
		R_{ext} = 1680 Ω			12	14	
		R_{ext} = 840 Ω			14	16	
C_{IN}	Input capacitance	V_I = V_{DD} or GND, CLK, SDI, SDO, $\overline{OE}$				10	pF

(1) Specified by design

6.7 Power Dissipation and Thermal Impedance

				MIN	MAX	UNIT
P_D	Power dissipation	Mounted on JEDEC 4-layer board (JESD 51-7), No airflow, T_A = 25°C, T_J = 125°C	DBQ package		1.6	W
			DW package		2.2	
			PW package		1.1	

6.8 Timing Requirements

V_{DD} = 3 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
$t_{w(L)}$	LE pulse duration	15		ns
$t_{w(CLK)}$	CLK pulse duration	15		ns
$t_{w(OE)}$	$\overline{OE}$ pulse duration	300		ns
$t_{su(D)}$	Setup time for SDI	3		ns
$t_{h(D)}$	Hold time for SDI	2		ns
$t_{su(L)}$	Setup time for LE	5		ns
$t_{h(L)}$	Hold time for LE	5		ns
f_{CLK}	Clock frequency, Cascade operation		30	MHz

6.9 Switching Characteristics: V_{DD} = 3 V

V_{DD} = 3 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	V_{IH} = V_{DD}, V_{IL} = GND, R_{ext} = 840 Ω, V_L = 4 V, R_L = 88 Ω, C_L = 10 pF	30	45	60	ns
t_{PLH2}	Low-to-high propagation delay time, LE to $\overline{OUTn}$		30	45	60	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		30	45	60	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO			30	40	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$		40	65	100	ns
t_{PHL2}	High-to-low propagation delay time, LE to $\overline{OUTn}$		40	65	100	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		40	65	100	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO			30	40	ns
$t_{w(CLK)}$	Pulse duration, CLK		15			ns
$t_{w(L)}$	Pulse duration LE		15			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$		300			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D)}$	Setup time, SDI		3			ns
$t_{h(L)}$	Hold time, LE		5			ns
$t_{su(L)}$	Setup time, LE		5			ns
t_r	Rise time, CLK (1)				500	ns
t_f	Fall time, CLK (1)				500	ns
t_{or}	Rise time, outputs (off)		35	50	70	ns
t_{of}	Rise time, outputs (on)		15	50	120	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

6.10 Switching Characteristics: V_{DD} = 5.5 V

V_{DD} = 5.5 V, T_J = –40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH1}	Low-to-high propagation delay time, CLK to $\overline{OUTn}$	V_{IH} = V_{DD}, V_{IL} = GND, R_{ext} = 840 Ω, V_L = 4 V, R_L = 88 Ω, C_L = 10 pF	20	35	55	ns
t_{PLH2}	Low-to-high propagation delay time, LE to $\overline{OUTn}$		20	35	55	ns
t_{PLH3}	Low-to-high propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		20	35	55	ns
t_{PLH4}	Low-to-high propagation delay time, CLK to SDO			20	30	ns
t_{PHL1}	High-to-low propagation delay time, CLK to $\overline{OUTn}$		15	28	42	ns
t_{PHL2}	High-to-low propagation delay time, LE to $\overline{OUTn}$		15	28	42	ns
t_{PHL3}	High-to-low propagation delay time, $\overline{OE}$ to $\overline{OUTn}$		15	28	42	ns
t_{PHL4}	High-to-low propagation delay time, CLK to SDO			20	30	ns
$t_{w(CLK)}$	Pulse duration, CLK		10			ns
$t_{w(L)}$	Pulse duration LE		10			ns
$t_{w(OE)}$	Pulse duration, $\overline{OE}$		200			ns
$t_{h(D)}$	Hold time, SDI		2			ns
$t_{su(D)}$	Setup time, SDI		3			ns
$t_{h(L)}$	Hold time, LE		5			ns
$t_{su(L)}$	Setup time, LE		5			ns
t_r	Rise time, CLK (1)				500	ns
t_f	Fall time, CLK (1)				500	ns
t_{or}	Rise time, outputs (off)		25	45	65	ns
t_{of}	Rise time, outputs (on)		7	12	20	ns
f_{CLK}	Clock frequency	Cascade operation			30	MHz

(1) If the devices are connected in cascade and t_r or t_f is large, it may be critical to achieve the timing required for data transfer between two cascaded devices.

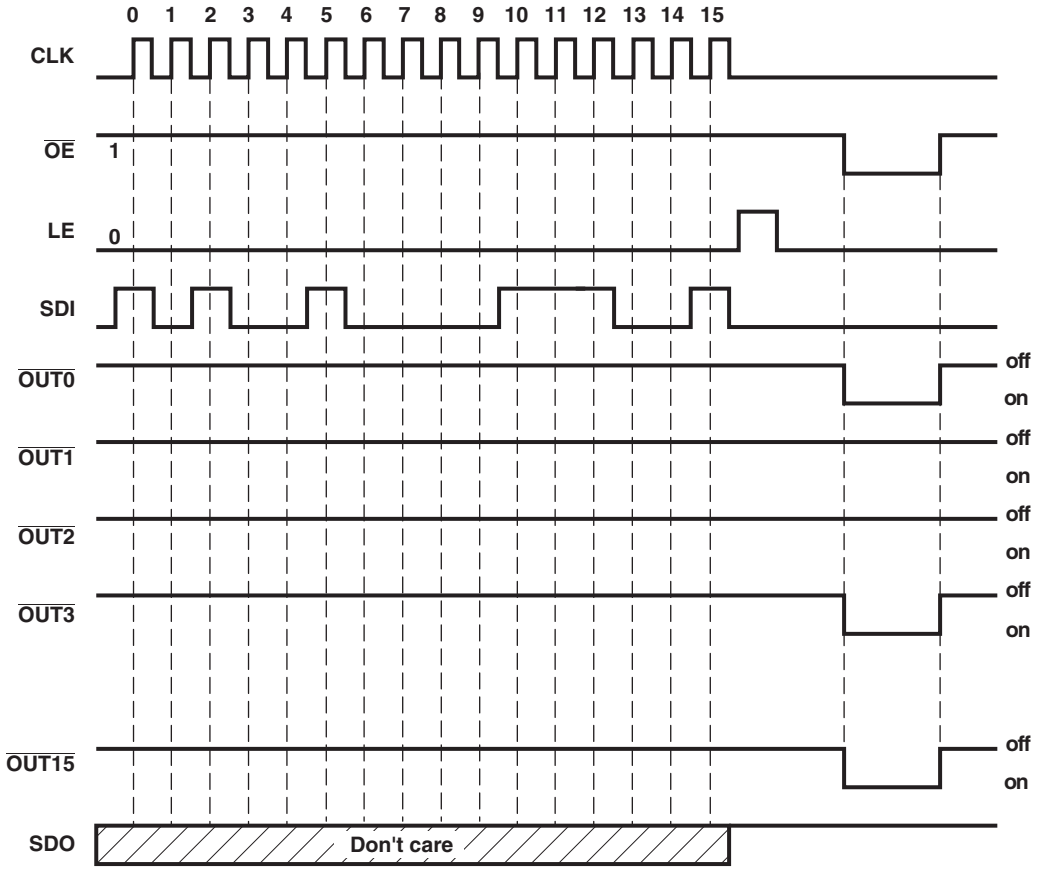


Figure 1. Timing Diagram

6.11 Typical Characteristics

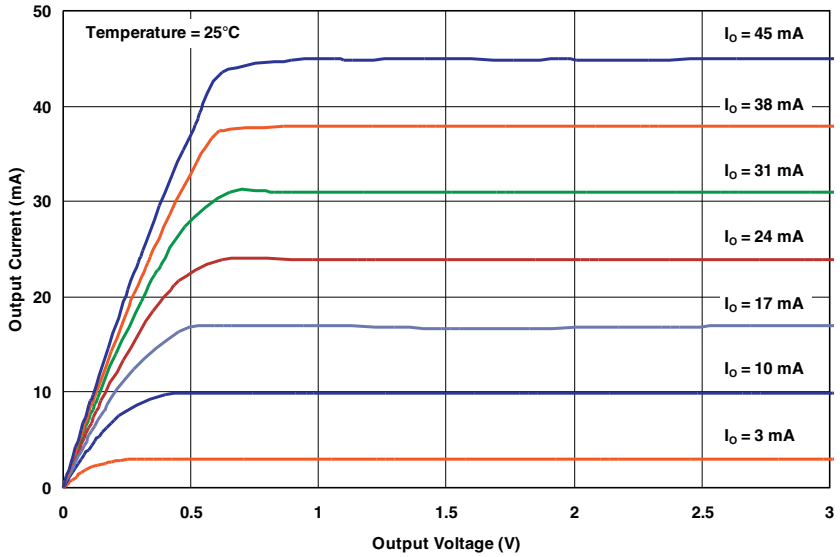


Figure 2. Output Current vs Output Voltage

7 Parameter Measurement Information

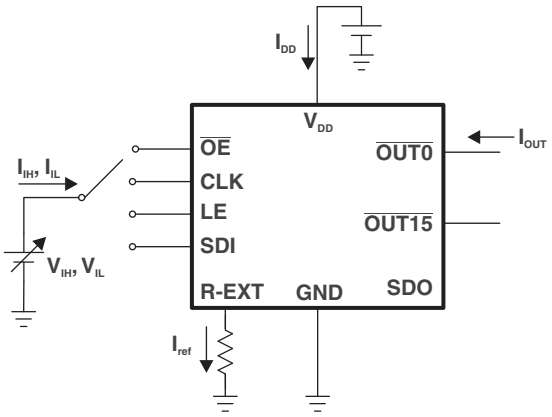


Figure 3. Test Circuit for Electrical Characteristics

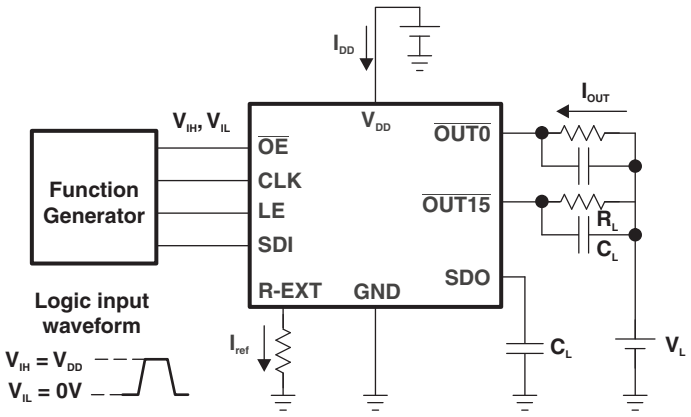


Figure 4. Test Circuit for Switching Characteristics

Parameter Measurement Information (continued)

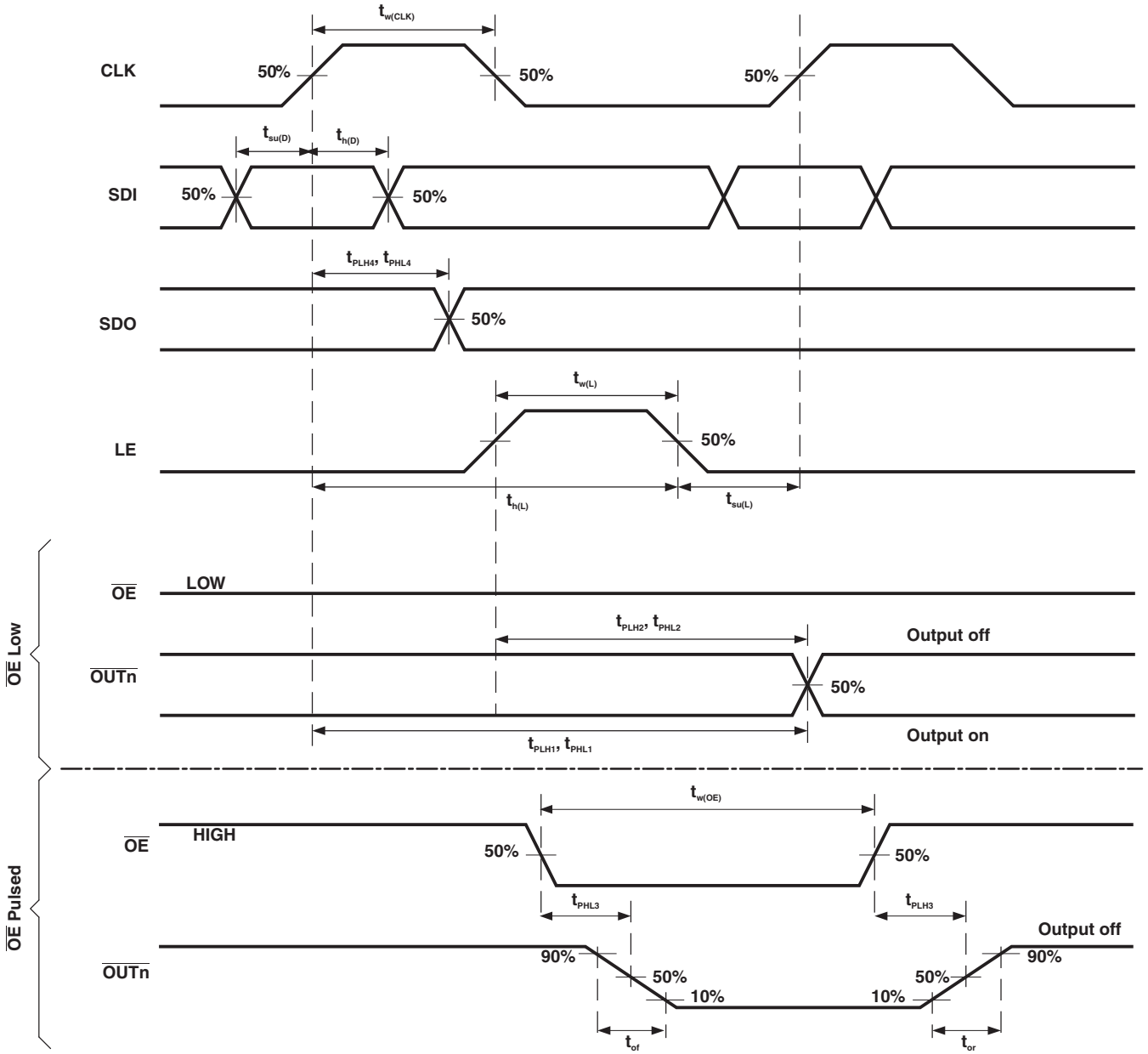


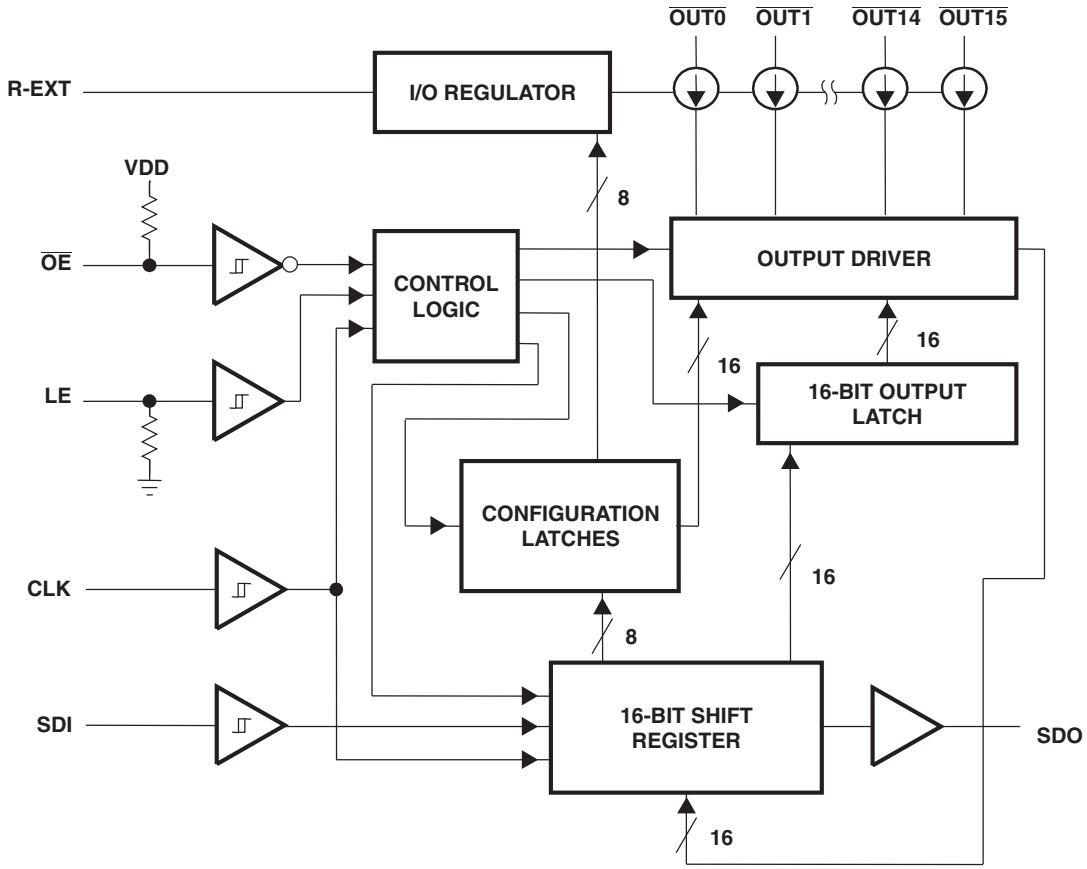
Figure 5. Normal Mode Timing Waveforms

8 Detailed Description

8.1 Overview

The TLC5925 is a 16-channel LED driver designed for LED displays and LED lighting applications. The TLC5925 contains a 16-bit shift register and data latches, which convert serial input data into parallel output format. At the TLC5925 output stage, 16 regulated-current ports provide uniform and constant current for driving LEDs within a wide range of VF variations. Used in system design for LED display applications (for example, LED panels), the TLC5925 provides great flexibility and device performance. Users can adjust the output current from 3 mA to 45 mA through an external resistor, REXT, which gives flexibility in controlling the light intensity of LEDs. TLC59025 is designed for up to 17 V at the output port. The high clock frequency, 30 MHz, also satisfies the system requirements of high-volume data transmission.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Constant Current

In LED display applications, TLC5925 provides nearly no current variations from channel to channel and from IC to IC. While I_{OUT} ≤ 45 mA, the maximum current skew between channels is less than ±5% and between ICs is less than ±6%.

8.4 Device Functional Modes

The table below lists the functional modes for the TLC5925.

Table 1. Truth Table in Normal Operation

CLK	LE	$\overline{OE}$	SDI	$\overline{OUT0}$...$\overline{OUT15}$...$\overline{OUT15}$	SDO
↑	H	L	Dn	Dn...Dn – 7...Dn – 15	Dn – 15
↑	L	L	Dn + 1	No change	Dn – 14
↑	H	L	Dn + 2	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	L	Dn + 3	Dn + 2...Dn – 5...Dn – 13	Dn – 13
↓	X	H	Dn + 3	off	Dn – 13

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Turning on the LEDs

To turn on an LED connected to one of the outputs of the device, the output must be pulled low. To do this, the SDI signal must let the device know which outputs should be activated. Using the rising edge of CLK, the logic level of the SDI signal latches the desired state of each output into the shift register. Once this is complete, the LE signal must be toggled from low to high then back to low. Once /OE is pulled down, the corresponding outputs will be pulled low and the LEDs will be turned on. The below diagram shows outputs 0, 3, 4, 5, 10, 13, and 15 being activated.

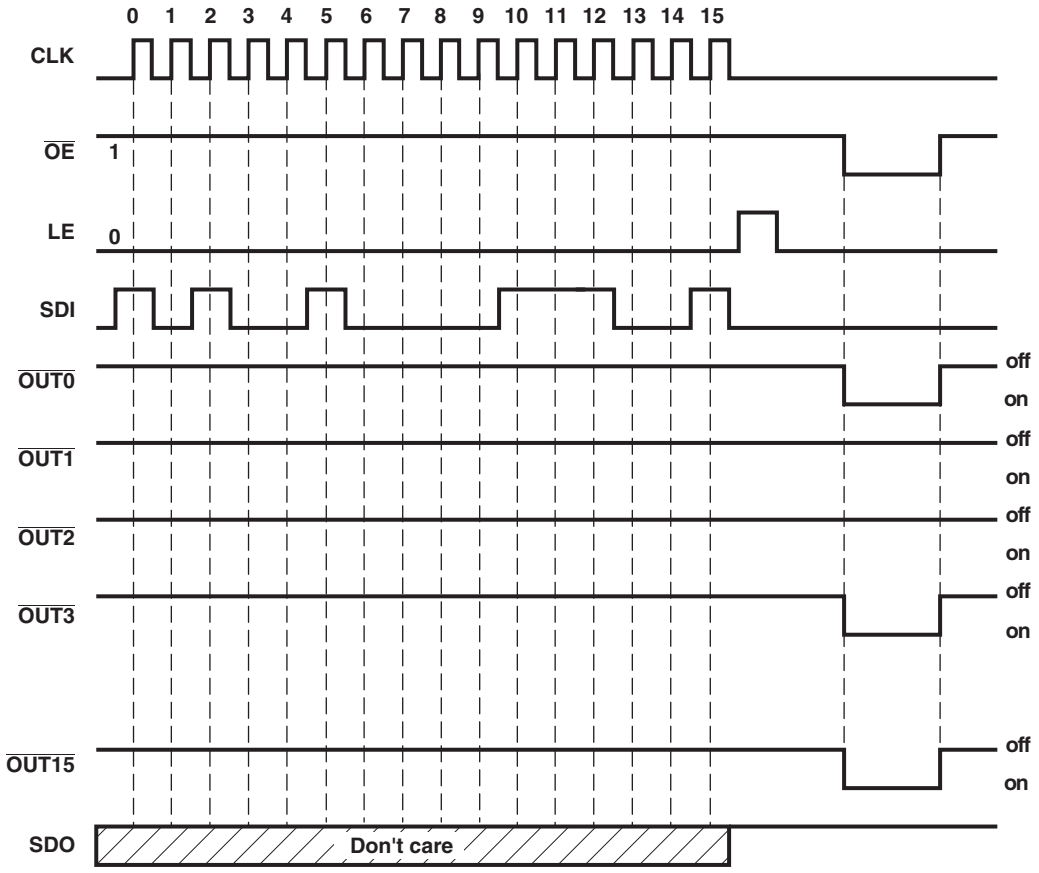


Figure 6. Timing Diagram

Application Information (continued)

9.1.2 Propagation Delay Times

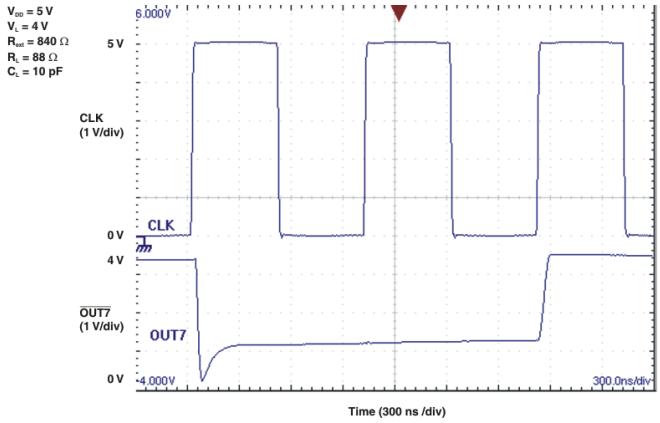


Figure 7. CLK to $\overline{OUT7}$

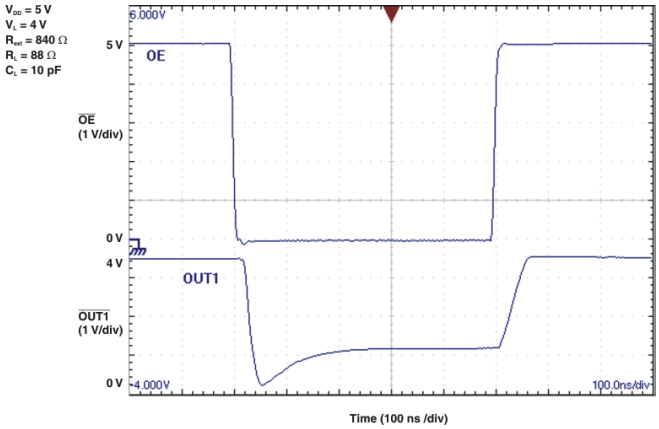


Figure 8. $\overline{OE}$ to $\overline{OUT1}$

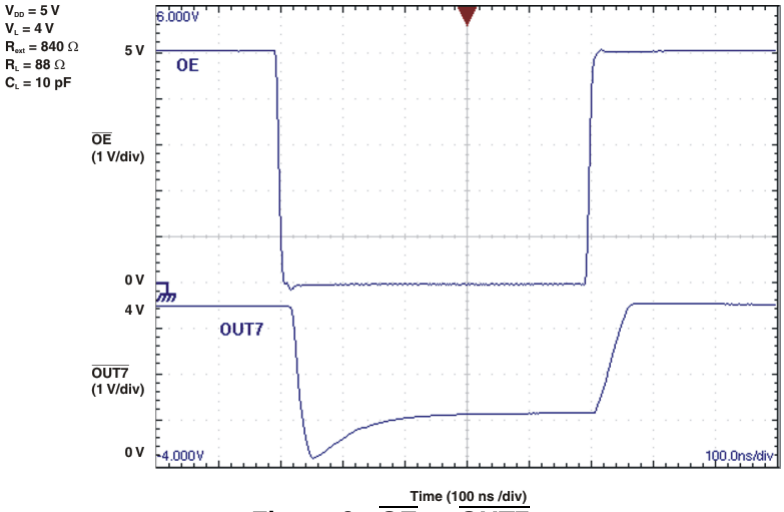
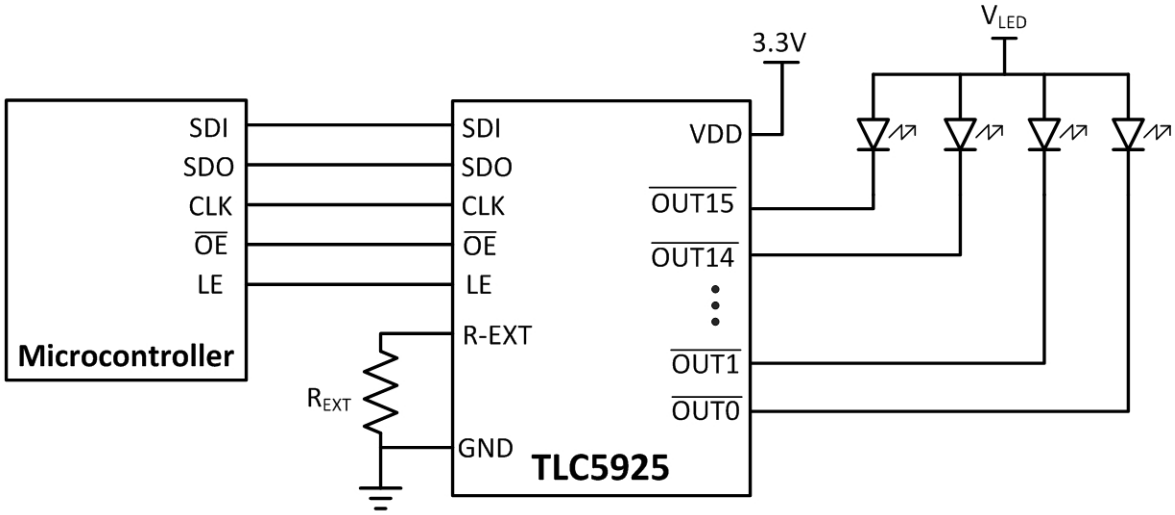


Figure 9. $\overline{OE}$ to $\overline{OUT7}$

9.2 Typical Application



Typical Application (continued)

9.2.1 Design Requirements

For the following design procedure, the input voltage (VDD) is between 3 V and 5.5 V.

9.2.2 Detailed Design Procedure

9.2.2.1 Adjusting Output Current

TLC5925 sets I_{OUT} based on the external resistor R_{ext}. Users can follow the below formulas to calculate the target output current $I_{OUT,target}$ in the saturation region:

$I_{OUT,target}$ = (1.21 V / R_{ext}) × 18, where R_{ext} is the external resistance connected between R-EXT and GND.

Therefore, the default current is approximately 26 mA at 840 Ω and 13 mA at 1680 Ω.

9.2.3 Application Curve

The default relationship after power on between $I_{OUT,target}$ and R_{ext} is shown in Figure 10.

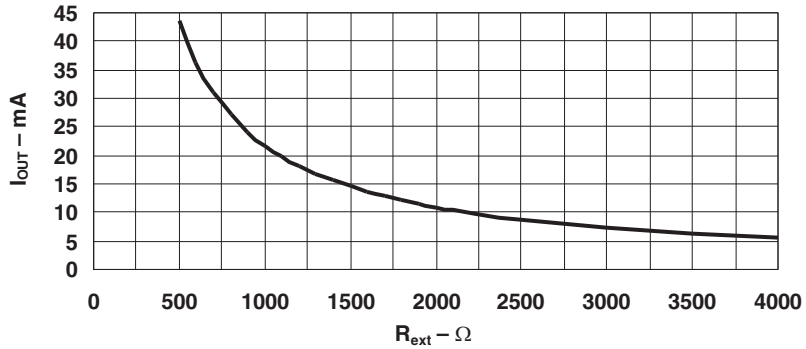


Figure 10. Default Relationship Curve Between $I_{OUT,target}$ and R_{ext} After Power Up

10 Power Supply Recommendations

The TLC5925 is designed to operate with a VDD range between 3 V and 5.5 V.

11 Layout

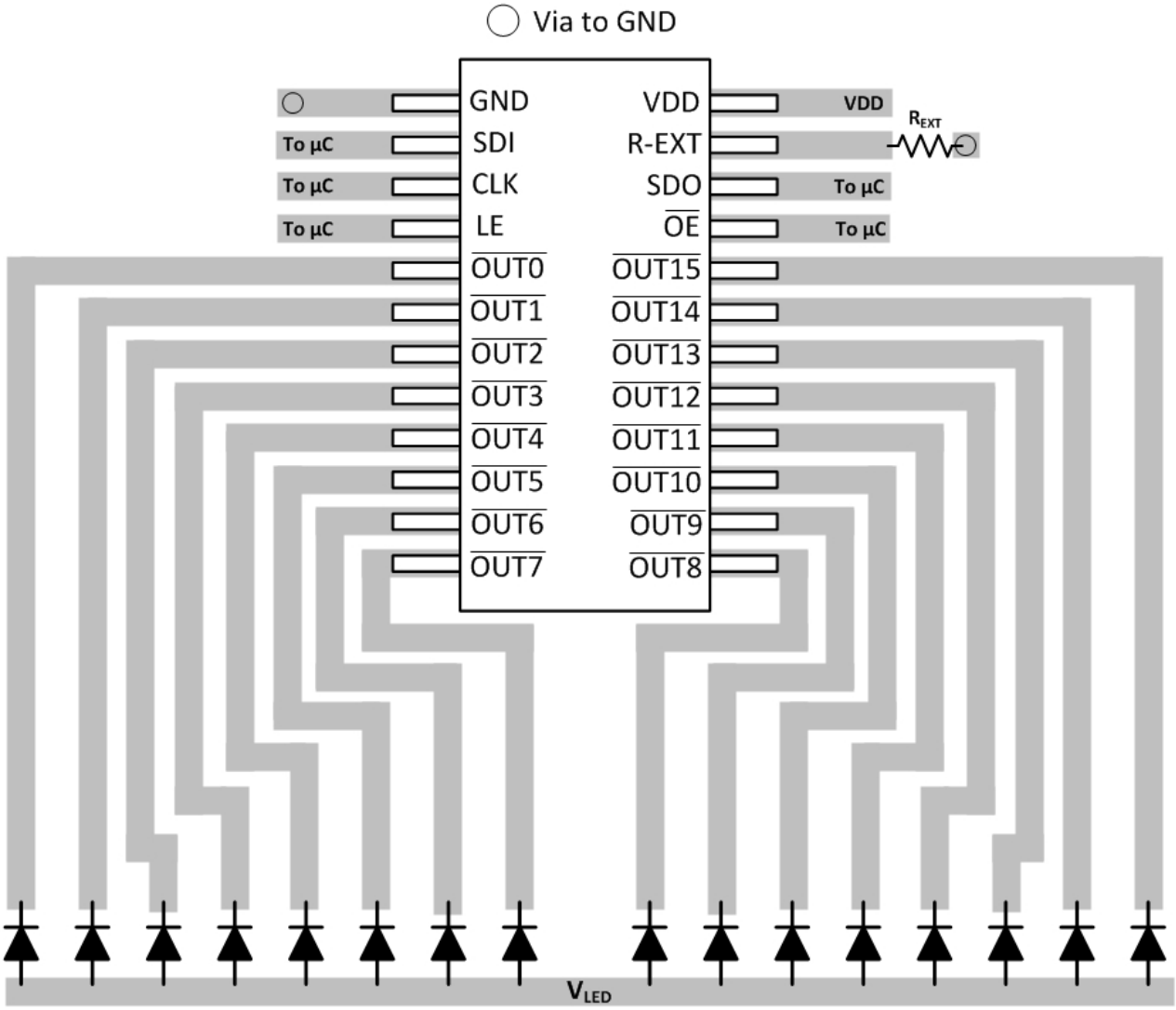
11.1 Layout Guidelines

The SDI, CLK, SDO, LE, and OE signals should all be kept from potential noise sources.

All traces carrying power through the LEDs should be wide enough to handle necessary currents.

All LED current passes through the device and into the ground node. There must be a strong connection between the device ground and the circuit board ground.

11.2 Layout Example



12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5925IDBQR	ACTIVE	SSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLC5925I	Samples
TLC5925IDWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5925I	Samples
TLC5925IDWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLC5925I	Samples
TLC5925IPWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5925	Samples
TLC5925IPWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Y5925	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

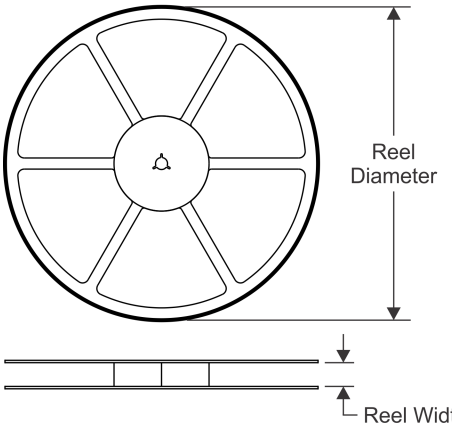
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

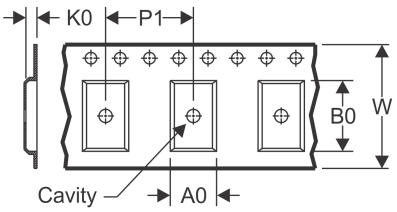
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

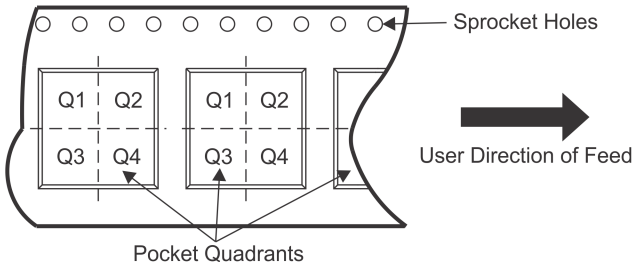


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

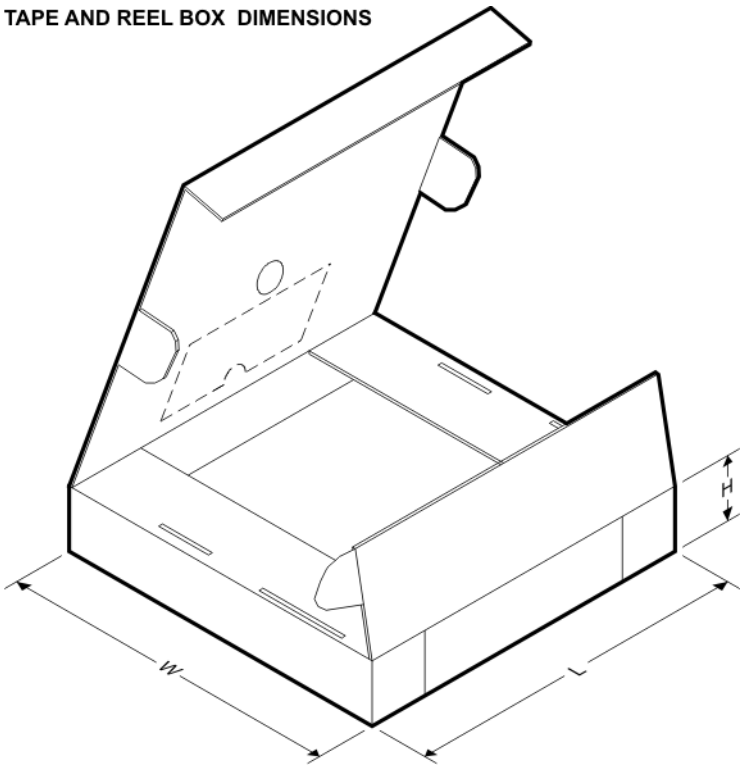
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5925IDBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5925IDWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
TLC5925IPWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

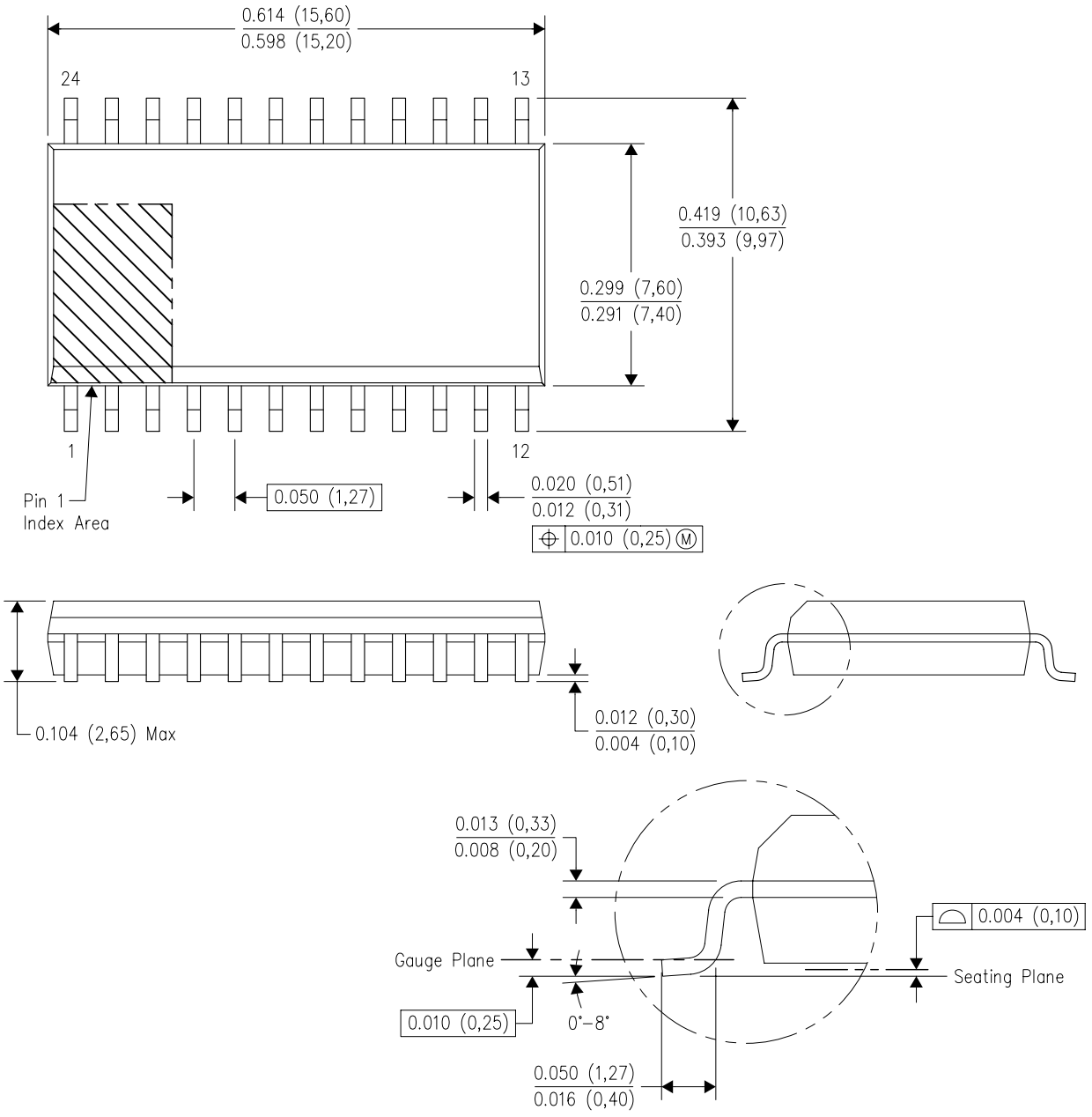
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

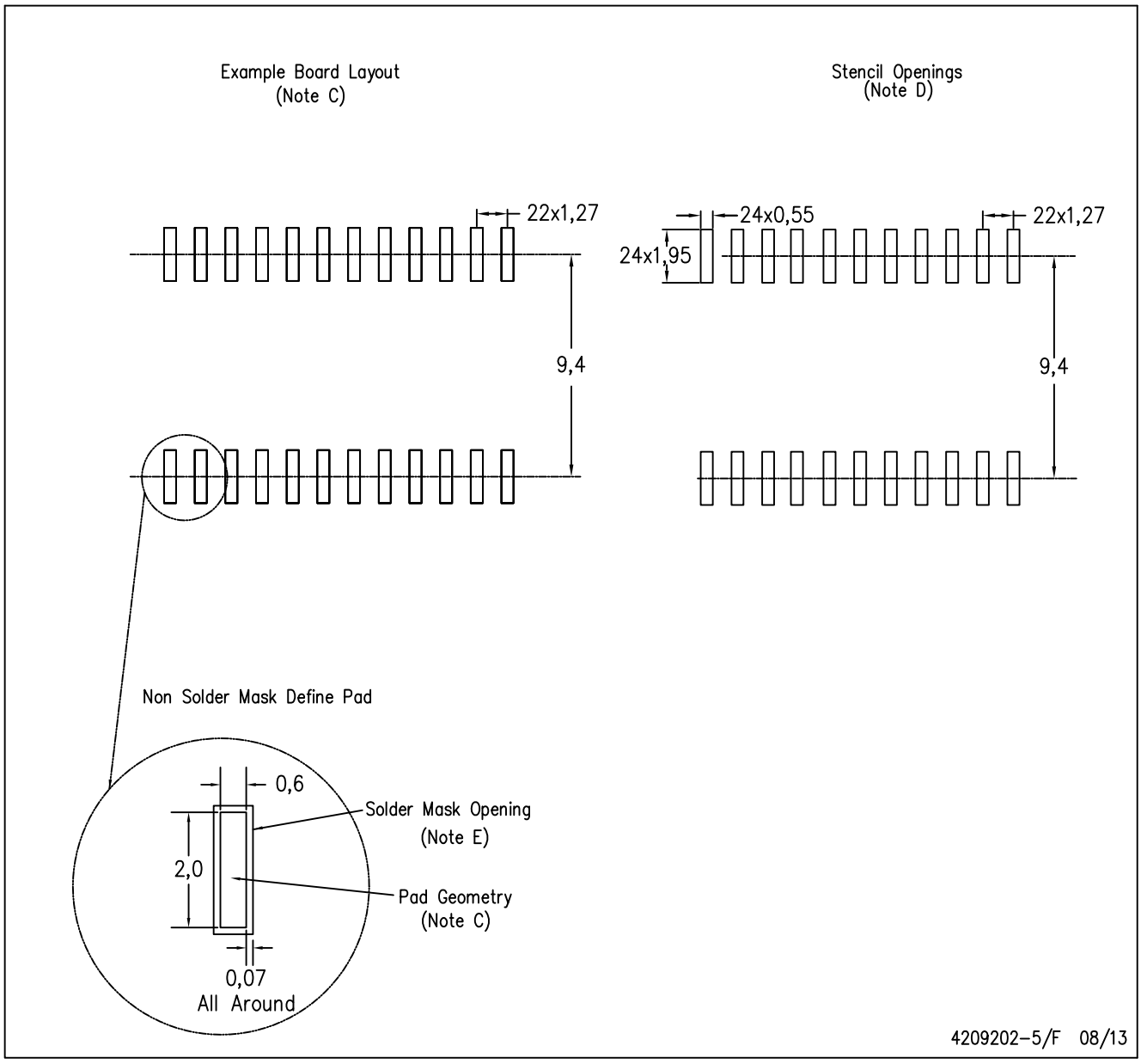
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5925IDBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
TLC5925IDWR	SOIC	DW	24	2000	350.0	350.0	43.0
TLC5925IPWR	TSSOP	PW	24	2000	367.0	367.0	38.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



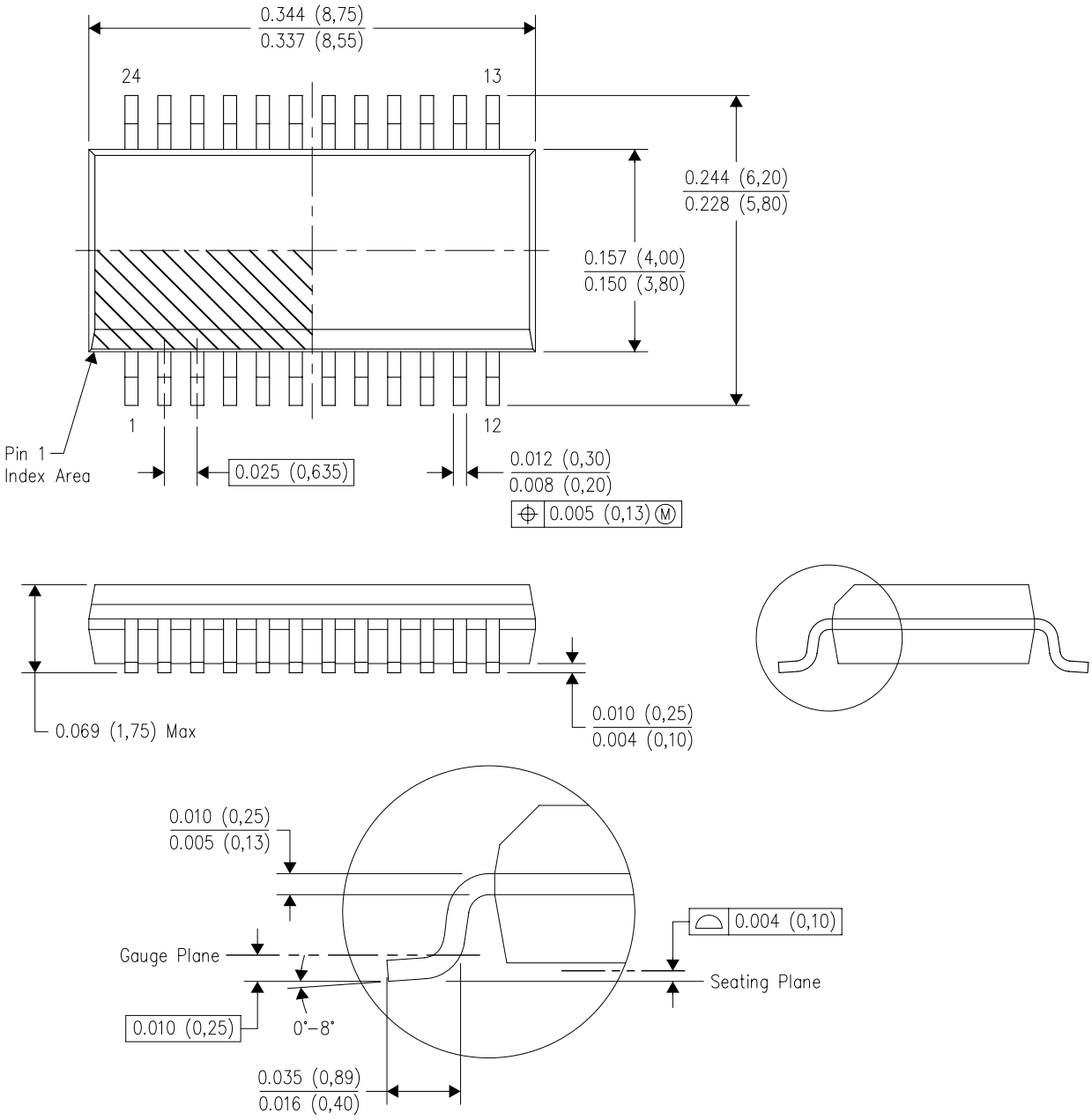
NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



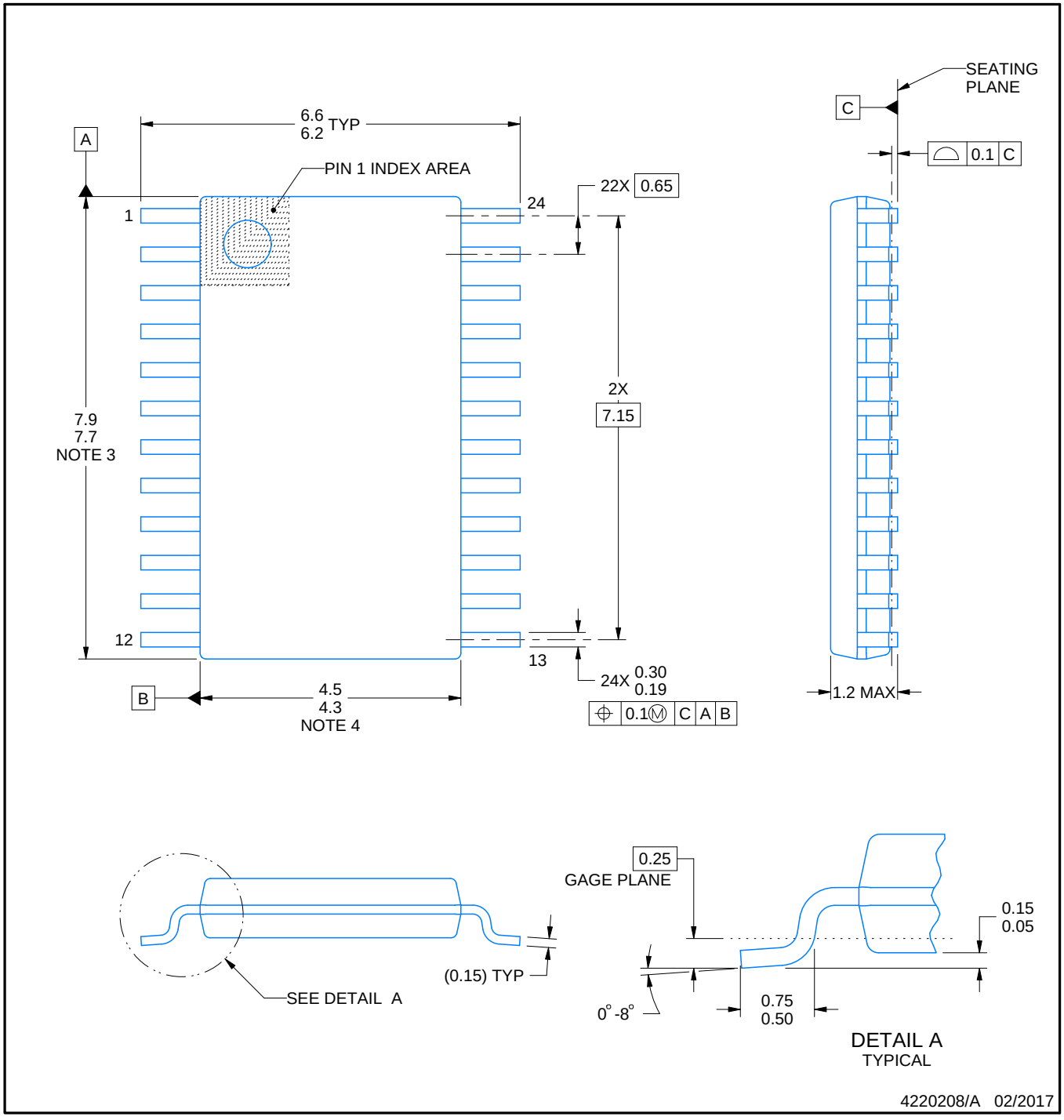
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

PACKAGE OUTLINE

PW0024A

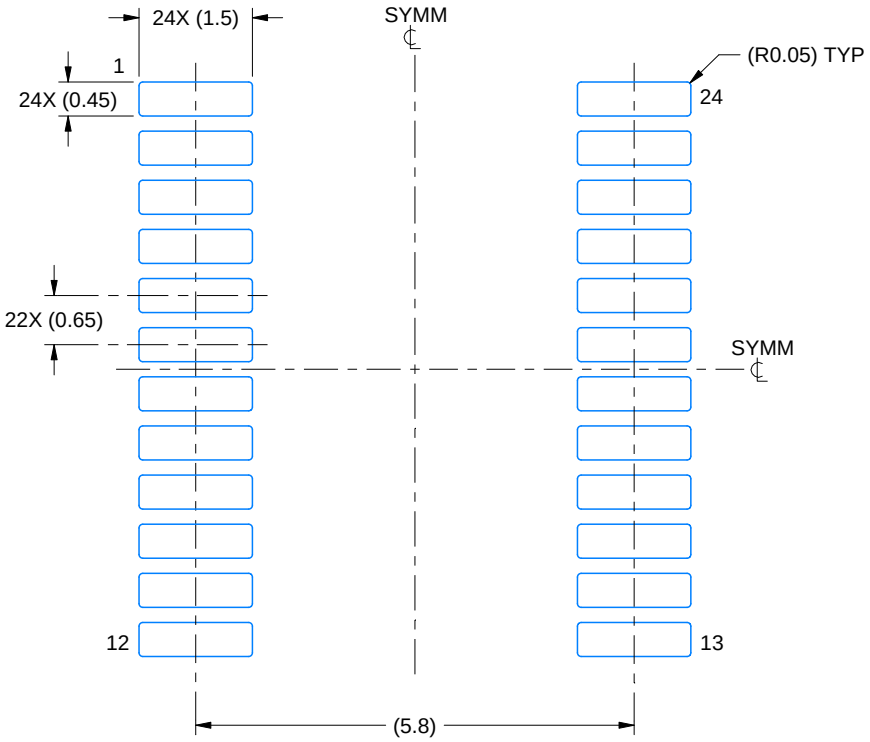
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

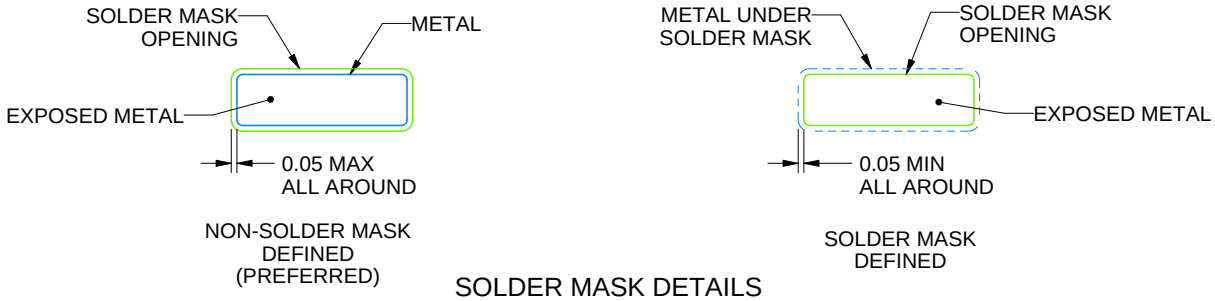


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

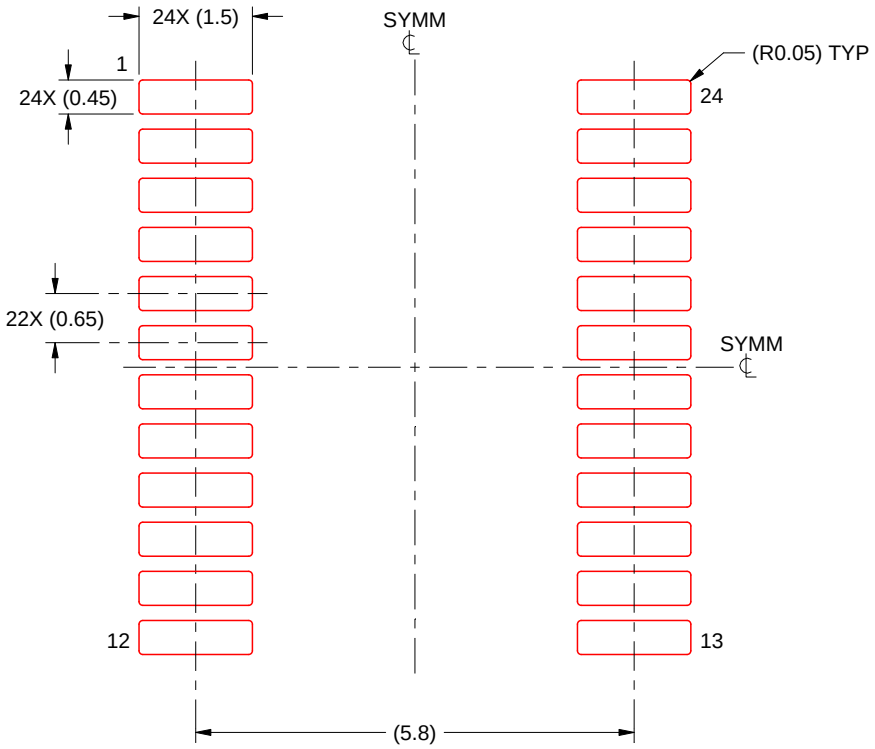


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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