# TCA9617B 电平转换 FM+ I²C 总线中继器

## 1 特性

- 双通道双向 I²C 缓冲器
- 支持标准模式、快速模式 (400kHz) 和快速模式+ (1MHz) I²C 操作
- 在 A 侧上，运行电源电压范围为 0.8V 至 5.5V
- 在 B 侧上，运行电源电压范围为 2.2V 至 5.5V
- 从 0.8V 至 5.5V 和 2.2V 至 5.5V 的电压电平转换
- 针对 TCA9517 的封装和功能替代产品
- 高电平有效中继器启用输入
- 漏极开路 I²C I/O
- 5.5V 电压容错 I²C 和启用输入支持
- 无闭锁操作
- 断电高阻抗 I²C 总线引脚
- 器件上支持时钟扩展和多主机仲裁
- 闩锁性能超出 JESD 78 II 类规范要求的 100mA
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
  - 4000V 人体放电模式 (A114-A)
  - 1500V 充电器件模型 (C101)

## 2 应用

- 服务器
- 路由器（电信交换设备）
- 工业设备
- 具有多个 I²C 从器件和/或印刷电路板 (PCB) 走线较长的产品

## 3 说明

TCA9617B 是一款专门用于 I²C 总线和 SMBus 系统的 BiCMOS 双路双向缓冲器。此器件可在混合应用中提供低电压（低至 0.8V）和较高电压（2.2V 至 5.5V）间的双向电压水平转换（上行转换模式和 下行转换模式）。电平转换期间，这个器件在不损失系统性能的情况下可扩展 I²C 和相似的总线系统。

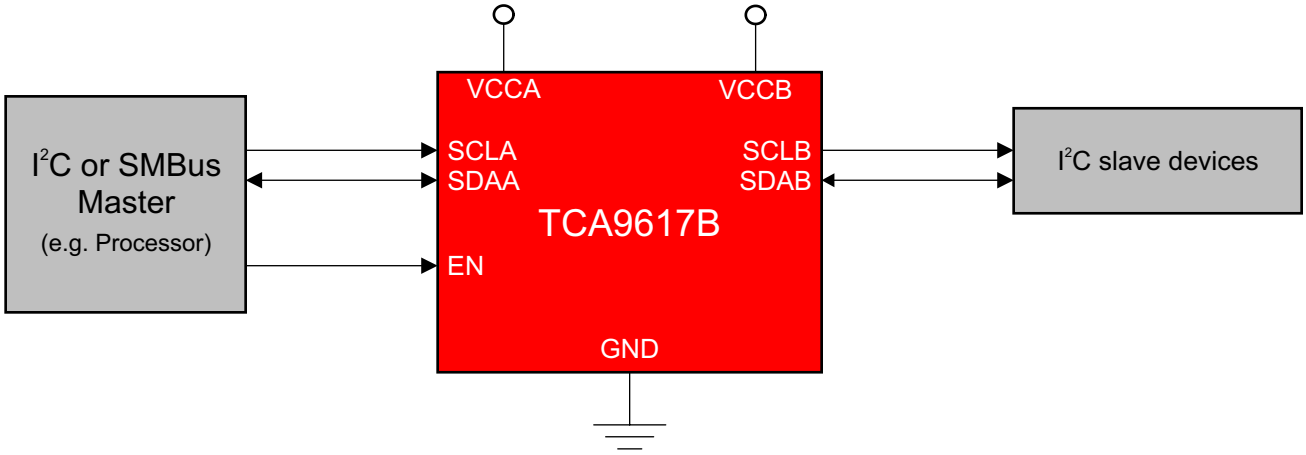
TCA9617B 缓冲 I²C 总线上的串行数据 (SDA) 和串行时钟 (SCL) 信号，从而将 550pF 的两条总线连接至一个 I²C 应用。这款器件也可用于将总线隔离为电压和电容两部分。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TCA9617B | VSSOP (8) | 3.00mm × 3.00mm |

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



# 目录



## 4 修订历史记录

**Changes from Revision A (December 2014) to Revision B** **Page**

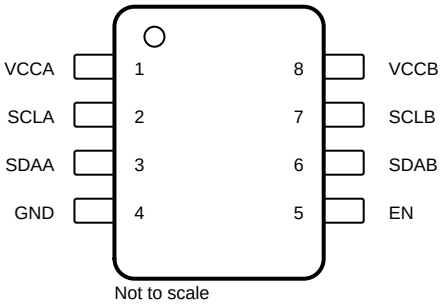
- Changed the appearance of the DGK pin out image ... 3
- Changed $V_{CCA} < V_{CCB}$ To: $V_{CCA} \leq V_{CCB}$ in the Design Requirements list ... 12

**Changes from Original (December 2014) to Revision A** **Page**

- 初始完整版。 ... 1

# 5 Pin Configuration and Functions

**DGK Package**
**8-Pin VSSOP**
**Top View**




Not to scale

**Pin Functions**

| PIN | | DESCRIPTION |
|---|---|---|
| NAME | NO. | |
| VCCA | 1 | A-side supply voltage (0.8 V to 5.5 V) |
| SCLA | 2 | $I^2C$ SCL line, A side. Connect to $V_{CCA}$ through a pull-up resistor. |
| SDAA | 3 | $I^2C$ SDA line, A side. Connect to $V_{CCA}$ through a pull-up resistor. |
| GND | 4 | Supply ground |
| EN | 5 | Active-high repeater enable input |
| SDAB | 6 | $I^2C$ SDA line, B side. Connect to $V_{CCB}$ through a pull-up resistor. |
| SCLB | 7 | $I^2C$ SCL line, B side. Connect to $V_{CCB}$ through a pull-up resistor. |
| VCCB | 8 | B-side and device supply voltage (2.2 V to 5.5 V) |

# 6 Specifications

## 6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCB}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_{CCA}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Enable input voltage range(2) | | –0.5 | 7 | V |
| $V_{I/O}$ | $I^2C$ bus voltage range(2) | | –0.5 | 7 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 (2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage, A-side bus | 0.8 | $V_{CCB}$ | V |
| $V_{CCB}$ | Supply voltage, B-side bus | 2.2 | 5.5 | V |
| $I_{OLA}$ | Low-level output current | | 30 | mA |
| $I_{OLB}$ | Low-level output current | 0.1 | 30 | mA |
| $T_A$ | Operating free-air temperature | –40 | 85 | °C |

## 6.4 Thermal Information

| THERMAL METRIC (1) | | TCA9617B | UNIT |
|---|---|---|---|
| | | DGK | |
| | | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 171.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 61.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 93.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 7.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 91.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

$V_{CCB}$ = 2.2 V to 5.5 V, GND = 0 V, $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | $V_{CCB}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | | $I_I$ = –18 mA | 2.2 V to 5.5 V | | | –1.2 | V |
| $V_{OL}$ | Low-level output voltage | SDAB, SCLB | $I_{OL}$ = 100 µA or 30 mA, $V_{ILA}$ = 0 V | 2.2 V to 5.5 V | 0.48 | 0.53 | 0.58 | V |
| | | SDAA, SCLA | $I_{OL}$ = 30 mA | | | 0.1 | 0.23 | |
| $V_{IH}$ | High-level input voltage | SDAA, SCLA | | 2.2 V to 5.5 V | 0.7 × $V_{CCA}$ | | 5.5 | V |
| | | SDAB, SCLB | | | 0.7 × $V_{CCB}$ | | 5.5 | |
| | | EN | | | 0.7 × $V_{CCB}$ | | 5.5 | |
| $V_{IL}$ | Low-level input voltage | SDAA, SCLA | | 2.2 V to 5.5 V | | | 0.3 × $V_{CCA}$ | V |
| | | SDAB, SCLB | | | | | 0.4 | |
| | | EN | | | | | 0.3 × $V_{CCB}$ | |
| $I_{CCA}$ | Quiescent supply current for $V_{CCA}$ | | Both channels low, SDAA = SCLA = GND and $I_{OLB}$ =100 µA, or SDAA = SCLA = open and SDAB = SCLB = GND | 2.2 V to 5.5 V | | | 13 | µA |
| $I_{CCB}$ | Quiescent supply current | | Both Channels high, SDAA = SCLA = $V_{CCA}$ B-side pulled up to $V_{CCB}$ with pull-up resistors | 5.5 V | | +4.5 | +7 | mA |
| | | | Both channels low, SDAA = SCLA = GND, $I_{OLB}$ = 100 µA | | | +5.7 | +8.1 | |
| $I_I$ | Input leakage current | SDAB, SCLB | $V_I$ = $V_{CCB}$ | 2.2 V to 5.5 V | –1 | | +1 | µA |
| | | | $V_I$ = 0.2 V, EN = 0 | | –10 | | +10 | |
| | | | $V_I$ = $V_{CCB}$ – 0.2 V | | –1 | | +1 | |
| | | | $V_I$ = 5.5 V,$V_{CCA}$ = 0 V | 0 V | –10 | | +10 | |
| | | SDAA, SCLA | $V_I$ = $V_{CCA}$ | 2.2 V to 5.5 V | –1 | | +1 | |
| | | | $V_I$ = 0.2 V, EN = 0 | | –10 | | +10 | |
| | | | $V_I$ = $V_{CCA}$ – 0.2 V | | –1 | | +1 | |
| | | | $V_I$ = 5.5 V, $V_{CCA}$ = 0 V | 0 V | –10 | | +10 | |
| | | EN | $V_I$ = $V_{CCB}$ | | –1 | | +1 | |
| | | | $V_I$ = 0.2 V | | –25 | | | |
| $C_I$ | Input capacitance | EN | $V_I$ = 3 V or 0 V | 3.3 V | | | 7 | pF |
| $C_{I/O}$ | Input/output capacitance | SCLA, SDAA | $V_I$ = 3 V or 0 V | 3.3 V | | | 9 | |
| | | | | 0 V | | | 9 | |
| | | SCLB, SDAB | $V_I$ = 3 V or 0 V | 3.3 V | | | 14 | |
| | | | | 0 V | | | 14 | |

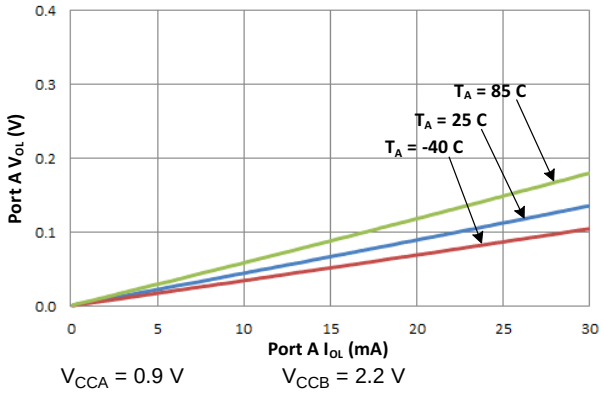
## 6.6 Timing Requirements

$V_{CCA}$ = 0.8 V to 5.5 V, $V_{CCB}$ = 2.2 V to 5.5 V, GND = 0 V, $T_A$ = –40°C to 85°C (unless otherwise noted)(1)(2)(3)

| PARAMETER | | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay | | SDAB, SCLB | SDAA, SCLA | | 42 | 55 | 90 | ns |
| | | | SDAA, SCLA | SDAB, SCLB | $V_{CCB}$ ≤ 3 V | 61 | 88 | 137 | |
| | | | | | $V_{CCB}$ > 3 V | 61 | 94 | 250 | |
| $t_{PHL}$ | Propagation delay | | SDAB, SCLB | SDAA, SCLA | | 69 | 93 | 144 | ns |
| | | | SDAA, SCLA | SDAB, SCLB | | 68 | 90 | 140 | |
| $t_{TLH}$(4) | Transition time | B side | 30% | 70% | | | 88 | | ns |
| | | A side | | | | | 37 | | |
| $t_{THL}$ | Transition time | B side | 70% | 30% | | 5.40 | 6.41 | 13.8 | ns |
| | | A side | | | | 1.40 | 4.71 | 11.3 | |
| $t_{su,en}$ | Setup time, EN high before Start condition(5) | | | | | 100 | | | ns |

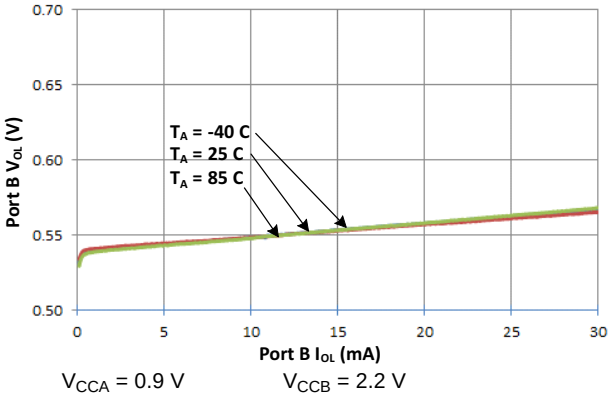
(1) Times are specified with loads of 240 Ω ±1% and 400 pF ±10% on B-side and 240 Ω ±1% and 200 pF ±10% on A-side. Different load resistance and capacitance alter the rise time, thereby changing the propagation delay and transition times.
(2) Times are specified with A-side signals pulled up to $V_{CCA}$ and B-side signals pulled up to $V_{CCB}$.
(3) Typical values were measured with $V_{CCA}$ = 0.9 V and $V_{CCB}$ = 2.5 V at $T_A$ = 25°C, unless otherwise noted.
(4) $T_{TLH}$ is determined by the pull-up resistance and load capacitance.
(5) EN should change state only when the global bus and the repeater port are in an idle state.

## 6.7 Typical Characteristics




$V_{CCA}$ = 0.9 V $V_{CCB}$ = 2.2 V

**图 1. Port A $V_{OL}$ vs $I_{OL}$**




$V_{CCA}$ = 0.9 V $V_{CCB}$ = 2.2 V

**图 2. Port B $V_{OL}$ vs $I_{OL}$**

# 7 Parameter Measurement Information

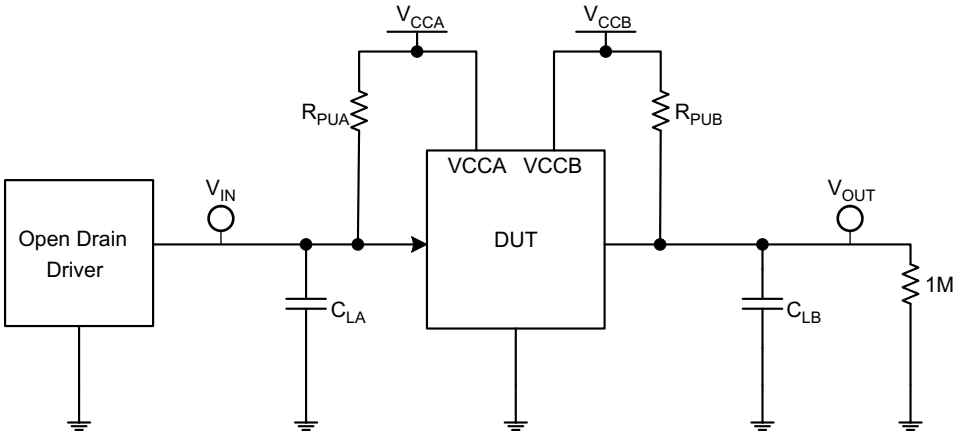
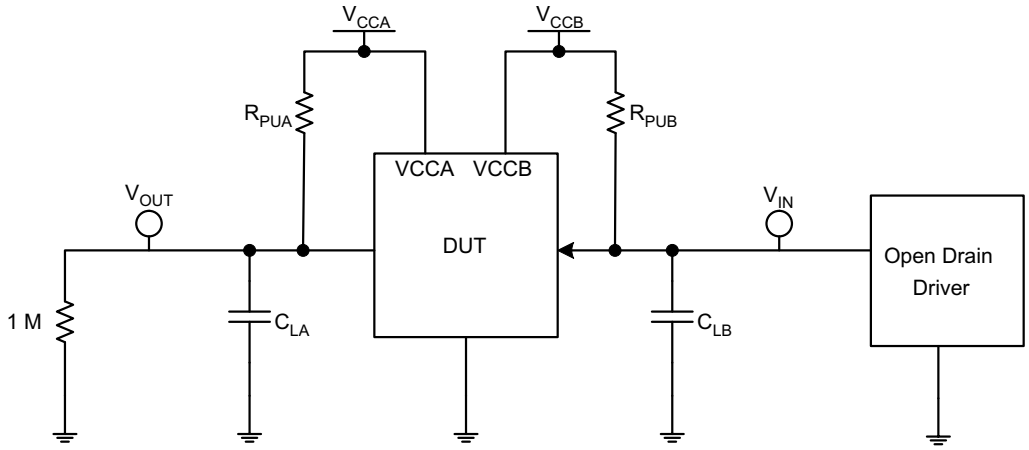



**图 3. Test Circuit for Open-Drain Output from A to B**




A. $V_{CCA}$ = 0.9 V

B. $V_{CCB}$ = 2.5 V

C. $R_{PUA}$ = $R_{PUB}$ = 240 Ω on the A-side and the B-side

D. $C_{LA}$ = 200 pF on A-side and $C_{LB}$ = 400 pF on B-side (includes probe and jig capacitance)

E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, slew rate ≥ 1 V/ns

F. The outputs are measured one at a time, with one transition per measurement.

**图 4. Test Circuit for Open-Drain Output from B to A**

## Parameter Measurement Information (接下页)

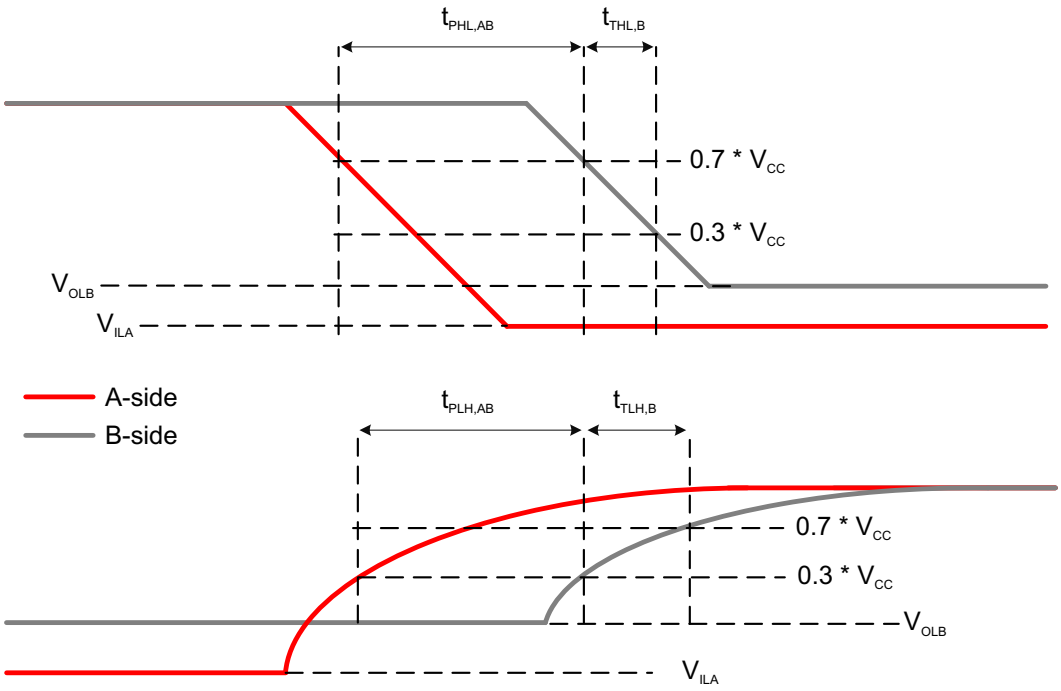



**图 5. Propagation Delay And Transition Times (A to B)**

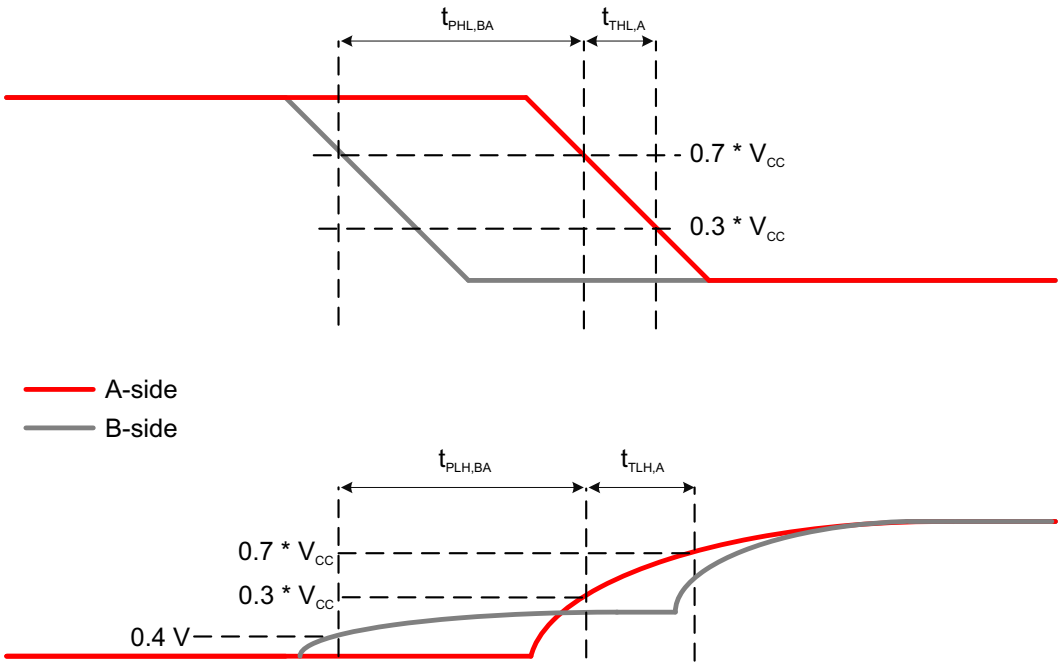



**图 6. Propagation Delay And Transition Times (B to A)**

# 8 Detailed Description

## 8.1 Overview

The TCA9617B is a BiCMOS dual bidirectional buffer intended for $I^2C$ bus and SMBus systems. As with the standard $I^2C$ system, pull-up resistors are required to provide the logic high levels on the buffered bus. The TCA9617B has standard open-drain configuration of the $I^2C$ bus. The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. The device is designed to work with Standard mode, Fast mode and Fast Mode+ $I^2C$ devices. The SCL and SDA lines shall be at high-impedance when either one of the supplies is powered off.

The TCA9617B B-side drivers operate from 2.2 V to 5.5 V. The output low level for this internal buffer is approximately 0.5 V, but the input voltage must be below $V_{IL}$ when the output is externally driven low. The higher-voltage low signal is called a buffered low. When the B-side I/O is driven low internally, the low is not recognized as a low by the input. This feature prevents a lockup condition from occurring when the input low condition is released. This type of design on the B side prevents it from being used in series with another TCA9617B B-side or other buffers that incorporate a static or dynamic offset voltage. This is because these devices do not recognize buffered low signals as a valid low and do not propagate it as a buffered low again.

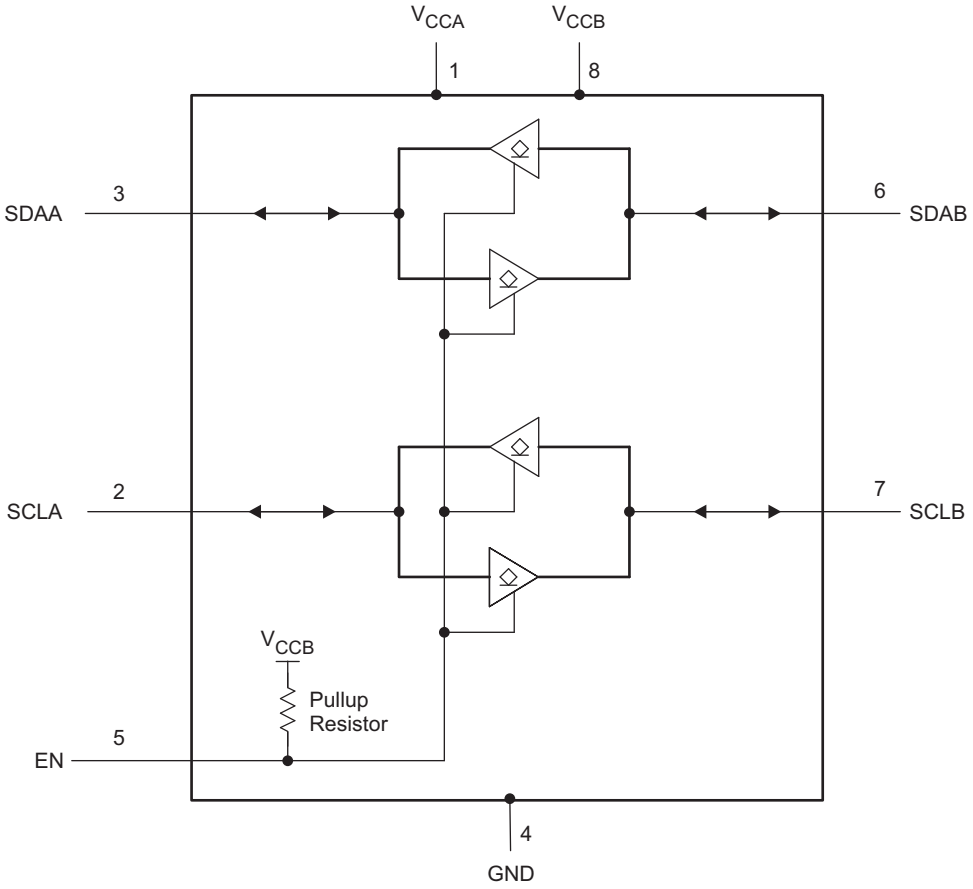
The TCA9617B A-side drivers operate from 0.8 V to 5.5 V and do not have the buffered low feature (or the static offset voltage). This means that a low signal on the B side translates to a nearly 0-V low on the A side, which accommodates smaller voltage swings of low-voltage logic. The output pull-down on the A side drives a hard low, and the input level is set to 0.3 $V_{CCA}$ to accommodate the need for a lower low level in systems where the low-voltage-side supply voltage is as low as 0.8 V.

The A side of two or more TCA9617Bs can be connected together to allow a star topology, with the A side on the common bus. Also, the A side can be connected directly to any other buffer with static or dynamic offset voltage. Multiple TCA9617Bs can be connected in series, A side to B side, with no buildup in offset voltage with only time-of-flight delays to consider.

The TCA9617B includes a power-up circuit that keeps the output drivers turned off until $V_{CCB}$ is above 2.0 V and $V_{CCA}$ is above 0.7 V. $V_{CCA}$ is only used to provide references for the A-side input comparators and the power-good-detect circuit. The TCA9617B internal circuitry and all I/Os are powered by the $V_{CCB}$ pin.

After power up and with the EN high, the A side falling below 0.7 $V_{CCA}$ turns on the corresponding B-side driver (either SDA or SCL) and drives the B-side down momentarily to 0 V before settling to approximately 0.5 V. When the A-side rises above 0.3 $V_{CCA}$, the B-side pull-down driver is turned off and the external pull-up resistor pulls the pin high. If the B side falls first and goes below 0.7 $V_{CCB}$, the A-side driver is turned on and drives the A-side to 0 V. When the B-side rises above 0.45 V, the A-side pull-down driver is turned off and the external pull-up resistor pulls the pin high.

## 8.2 Functional Block Diagram






## 8.3 Feature Description

### 8.3.1 Bidirectional Level Translation

The TCA9617B can provide bidirectional voltage level translation (up-translation and down-translation) between low voltages (down to 0.8 V) and higher voltages (2.2 V to 5.5 V) in mixed-mode applications.

### 8.3.2 Low to High Transition Characteristics

图 8 depicts the offset voltage on the B side of the device. As shown in 图 8 the slave releases and the B-side rises, and it will rise to 0.5 V and stay there until the A-side rises above 0.3 $V_{CCA}$. This effect can cause the low level signal to have a "pedestal." Once the voltage on the A-side crosses 0.3 $V_{CCA}$, the B-side will continue to rise to $V_{CCB}$.

Due to nature of the B-side pedestal and the static offset voltage, there will be a slight overshoot as the B-side rises from being externally driven low to the 0.5 V offset. The TCA9617B is designed to control this behavior provided the system is designed with rise times greater than 20 ns. Therefore, care should be taken to limit the pull-up strength when devices with rise time accelerators are present on the B side. Excessive overshoot on the B-side pedestal may cause devices with rise time accelerators to trip prematurely if the overshoot is more than accelerator thresholds. Since the A-side does not have a static offset low voltage, no pedestal is seen on the A-side as shown in 图 7.

## Feature Description (接下页)

### 8.3.3 High to Low Transition Characteristics

When the A side of the bus is driven to 0.7 $V_{CCA}$, the B side driver will turn on. This will drive the B-side to 0 V for a short period (see 图 8) and then the B-side will rise to the static offset voltage of 0.5 V ($V_{OL}$ of TCA9617B). This effect, called an inverted pedestal, allows the B-side to drive to logic low much faster than driving to the static offset. Driving to the static offset voltage requires that the fall time be slowed to prevent ringing.

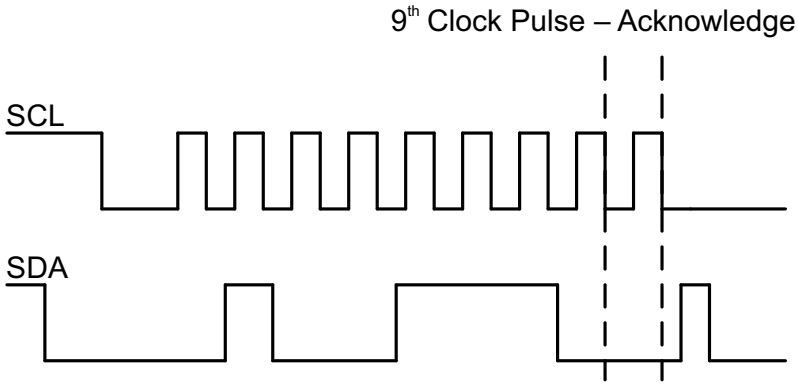



**图 7. Bus A (0.8 V to 5.5 V Bus) Waveform**

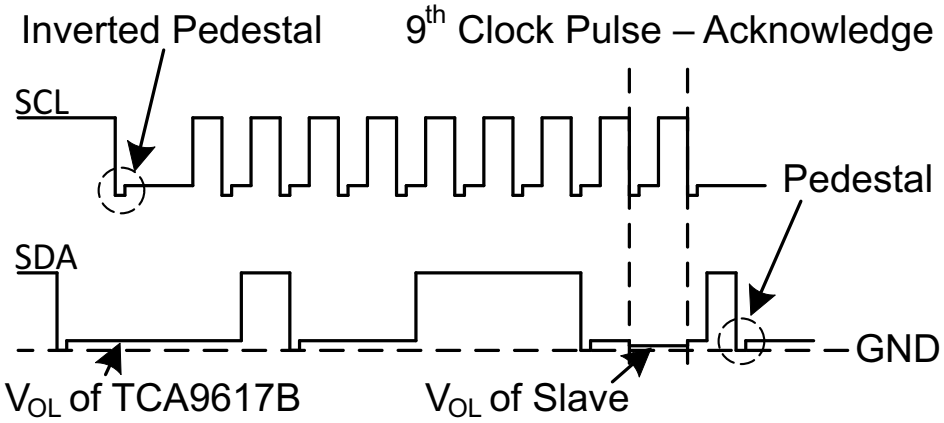



**图 8. Bus B (2.2 V to 5.5 V Bus) Waveform**

## 8.4 Device Functional Modes

The TCA9617B has an active-high enable (EN) input with an internal pull-up to $V_{CCB}$, which allows the user to select when the repeater is active. This can be used to isolate a badly behaved slave on power-up reset. It should never change state during an $I^2C$ operation, because disabling during a bus operation may hang the bus, and enabling part way through the bus cycles could confuse the $I^2C$ parts being enabled. The EN input should change state only when the global bus and repeater port are in the idle state to prevent system failures.

**表 1. Function Table**

| INPUT EN | FUNCTION |
|---|---|
| L | Outputs disabled |
| H | SDAA = SDAB<br>SCLA = SCLB |

# 9 Application and Implementation

## 9.1 Application Information

A typical application is shown in 图 9. In this example, the system master is running on a 0.9-V $I^2C$ bus, and the slave is connected to a 2.5-V bus. Both buses are running at 400 kHz. Decoupling capacitors are required but are not shown in 图 14 for simplicity.

The TCA9617B is 5-V tolerant so no additional circuits are required to translate between 0.8-V to 5.5-V bus voltages and 2.7-V to 5.5-V bus voltages.

When the A side of the TCA9617B is pulled low by a driver on the $I^2C$ bus, a comparator detects the falling edge when it goes below 0.7 $V_{CCA}$ and cause the internal driver on the B side to turn on. The B-side will first pull down to 0 V and then settle to 0.5 V. When the B side of the TCA9617B falls below 0.45 V, the TCA9617B will detect the falling edge, turn on the internal driver on the A side and pull the A-side pin down to ground.

On the B-side bus of the TCA9617B, the clock and data lines will have a positive offset from ground equal to the $V_{OL}$ of the TCA9617B. After the eighth clock pulse, the data line is pulled to the $V_{OL}$ of the slave device, which is close to ground in this example. At the end of the acknowledge, the level rises only to the low level set by the driver of the TCA9617B for a short delay (approximately 0.5 V), while the A-side bus rises above 0.3 $V_{CCA}$ and then continues high.

Although the TCA9617 has a single application, the device can exist in multiple configurations. 图 9 shows the standard configuration for the TCA9617. Multiple TCA9617s can be connected either in star configuration (图 12) or in series configuration (图 13). The design requirements , detailed design procedure, and application curves in *Standard Application* are valid for all three configurations.

## 9.2 Typical Application

### 9.2.1 Standard Application

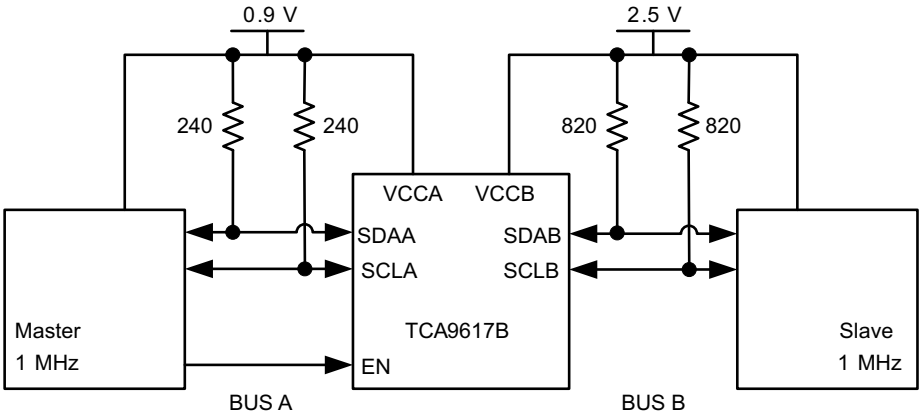



**图 9. Bidirectional Voltage Level Translator**

#### *9.2.1.1 Design Requirements*

For the level-translating application, the following should be true:

- $V_{CCA}$ = 0.8 V to 5.5 V
- $V_{CCB}$ = 2.2 V to 5.5 V
- $V_{CCA} \leq V_{CCB}$
- $I_{OL} > I_O$

## Typical Application (接下页)

### *9.2.1.2 Detailed Design Procedure*

#### 9.2.1.2.1 Pullup Resistor Sizing

For the TCA9617B to function correctly, all devices on the B-side must be able to pull the B-side below the voltage input low contention level (0.45 V). This means that the $V_{OL}$ of any device on the B-side must be below 0.4 V to ensure proper operation.

The $V_{OL}$ of a device can be adjusted by changing the $I_{OL}$ through the device which is set by the pull-up resistor value. The pull-up resistor on the B-side must be carefully selected to ensure that logic levels will be transferred correctly to the A-side.

The B-side pull-up resistor sizing must also ensure that the rise time is greater than 20 ns. Shorter rise times will increase the pedestal overshoot shown in point 2 of 图 10.

### *9.2.1.3 Application Curves*

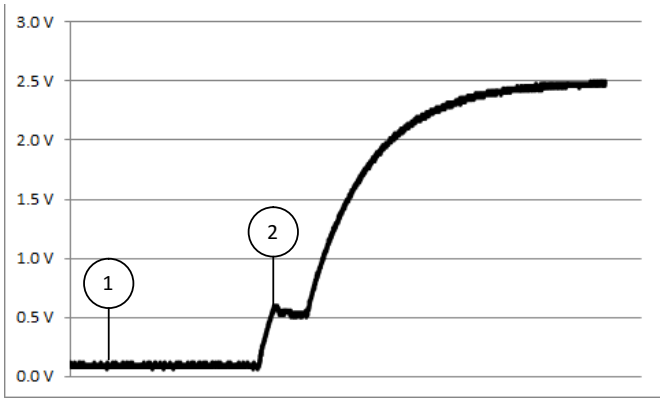



**图 10. B-side Pedestal**

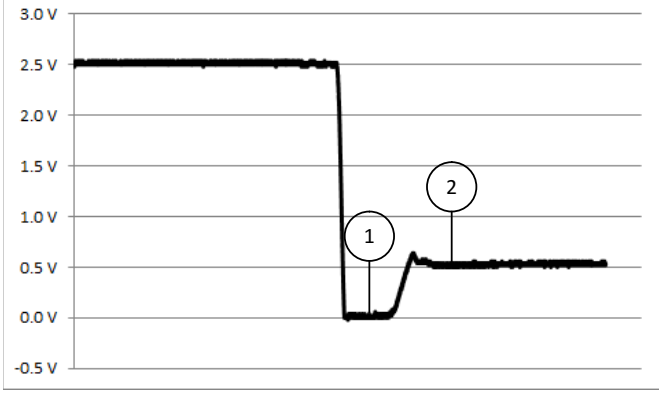



**图 11. B-side Inverted Pedestal**

## Typical Application (接下页)

### 9.2.2 Star Application

Multiple TCA9617B A sides can be connected in a star configuration, allowing all nodes to communicate with each other.

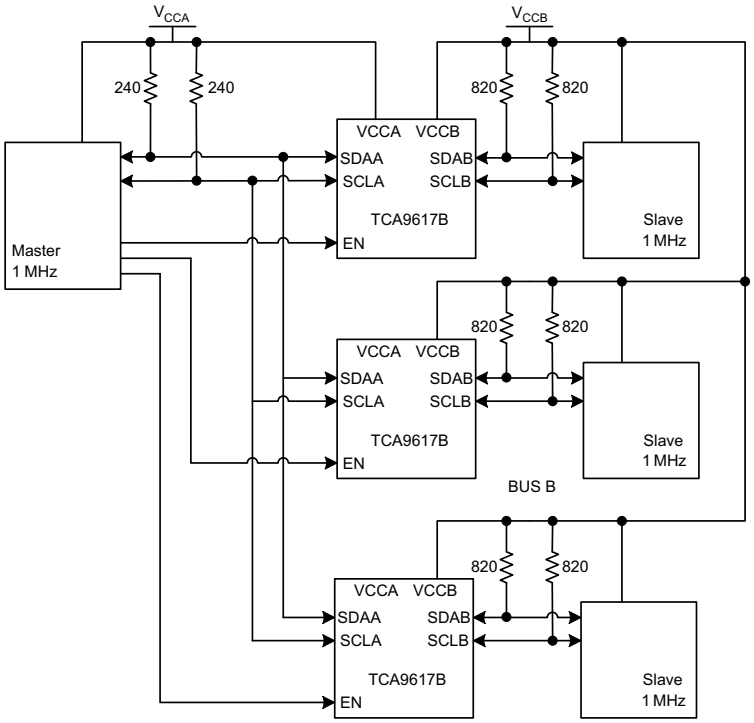



**图 12. Typical Star Application**

#### *9.2.2.1 Design Requirements*

Refer to *Design Requirements*.

#### *9.2.2.2 Detailed Design Procedure*

Refer to *Detailed Design Procedure*.

#### *9.2.2.3 Application Curves*

Refer to *Application Curves*.

## Typical Application (接下页)

### 9.2.3 Series Application

Multiple TCA9617Bs can be connected in series as long as the A side is connected to the B side. $I^2C$ bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

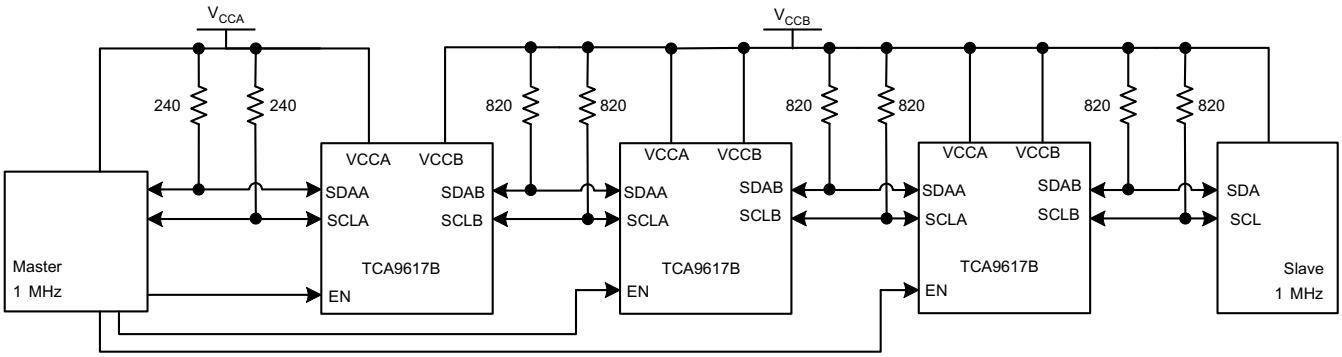



**图 13. Typical Series Application**

#### *9.2.3.1 Design Requirements*

Refer to *Design Requirements*.

#### *9.2.3.2 Detailed Design Procedure*

Refer to *Detailed Design Procedure*.

#### *9.2.3.3 Application Curves*

Refer to *Application Curves*.

## 10 Power Supply Recommendations

For VCCA, an 0.8-V to 5.5-V power supply is required. For VCCB, a 2.2-V to 5.5-V power supply is required.

Standard decoupling capacitors are recommended. These capacitors typically range from 0.1 µF to 1 µF, but the ideal capacitance depends on the amount of noise from the power supply.

# 11 Layout

## 11.1 Layout Guidelines

The recommended decoupling capacitors should be placed as close to the VCCA and VCCB pins of the TCA9617B as possible.

## 11.2 Layout Example

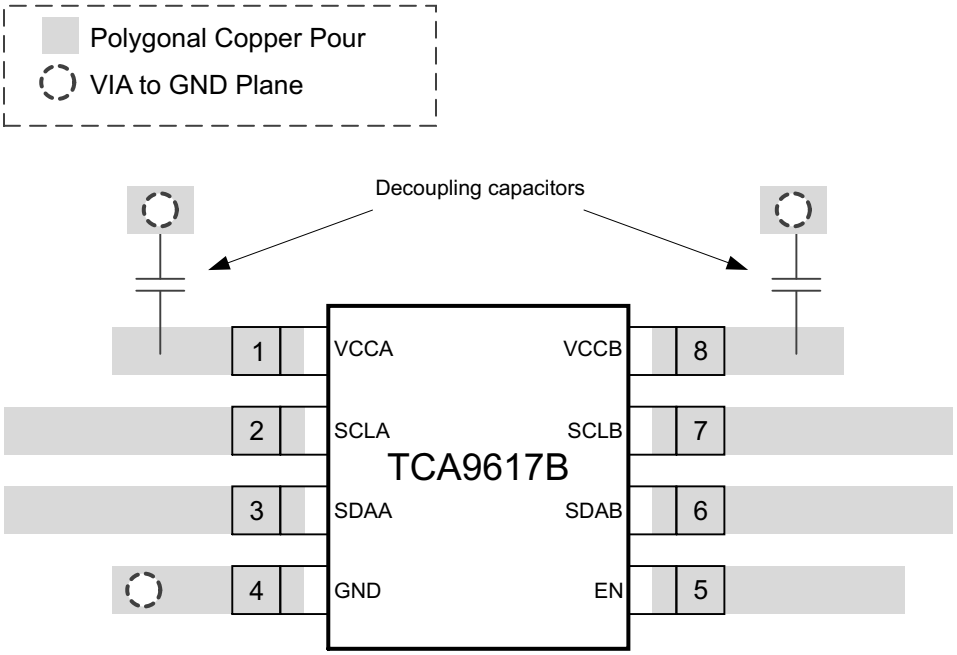



**图 14. Layout Schematic**

# 12 器件和文档支持

## 12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

## 12.2 社区资源

**下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。**

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**设计支持** ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

## 12.3 商标

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## 12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

# 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TCA9617BDGKR | ACTIVE | VSSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | NIPDAUAG | Level-1-260C-UNLIM | -40 to 85 | ZBOK | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

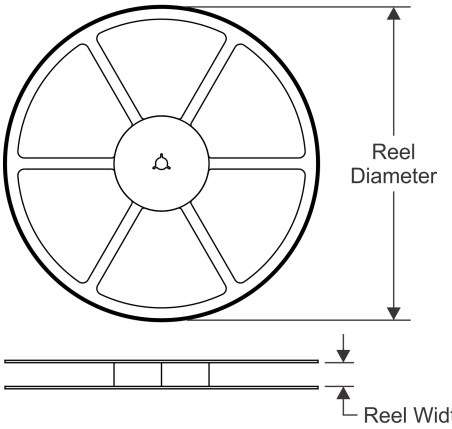
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

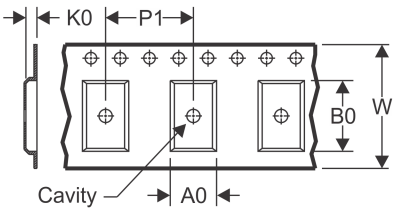
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

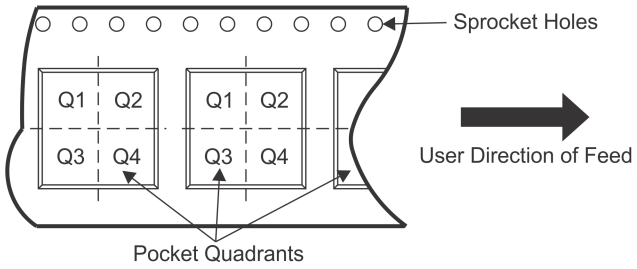



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

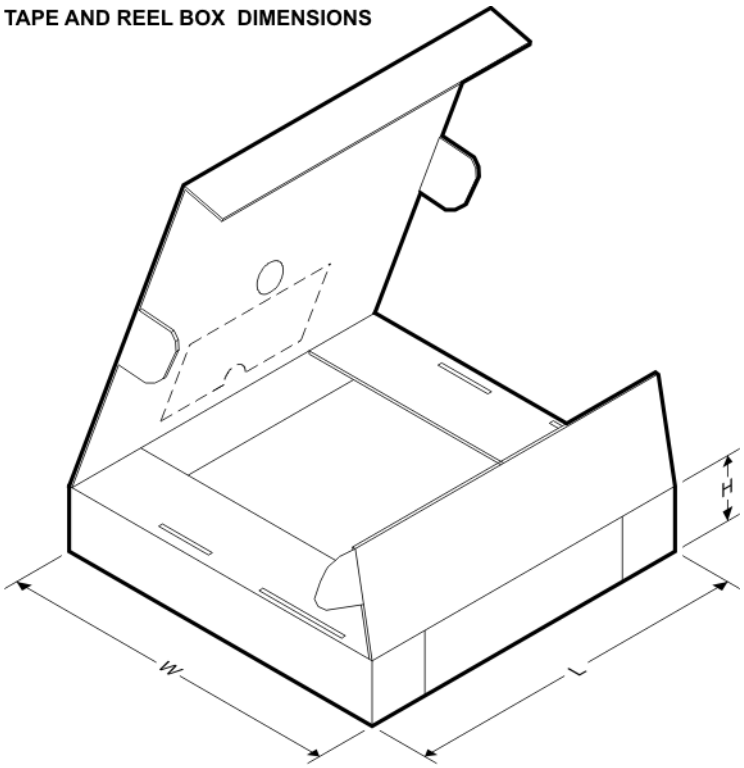
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TCA9617BDGKR | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

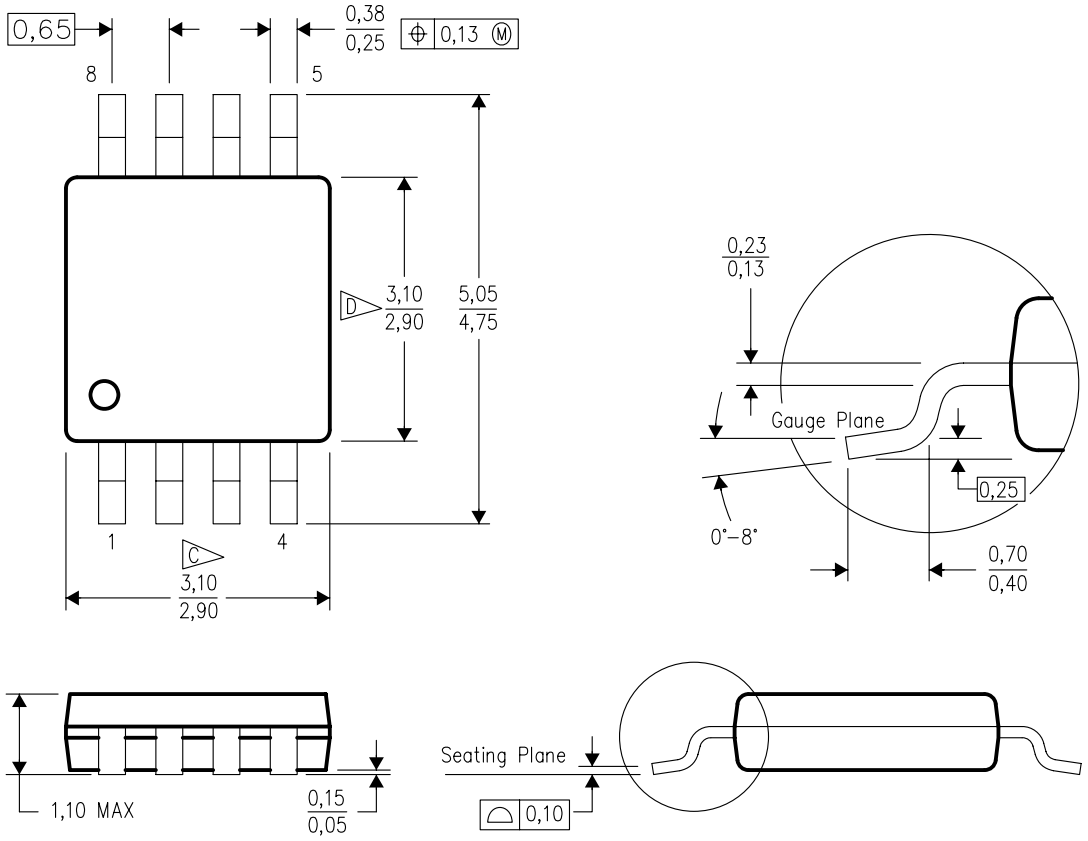
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TCA9617BDGKR | VSSOP | DGK | 8 | 2500 | 364.0 | 364.0 | 27.0 |

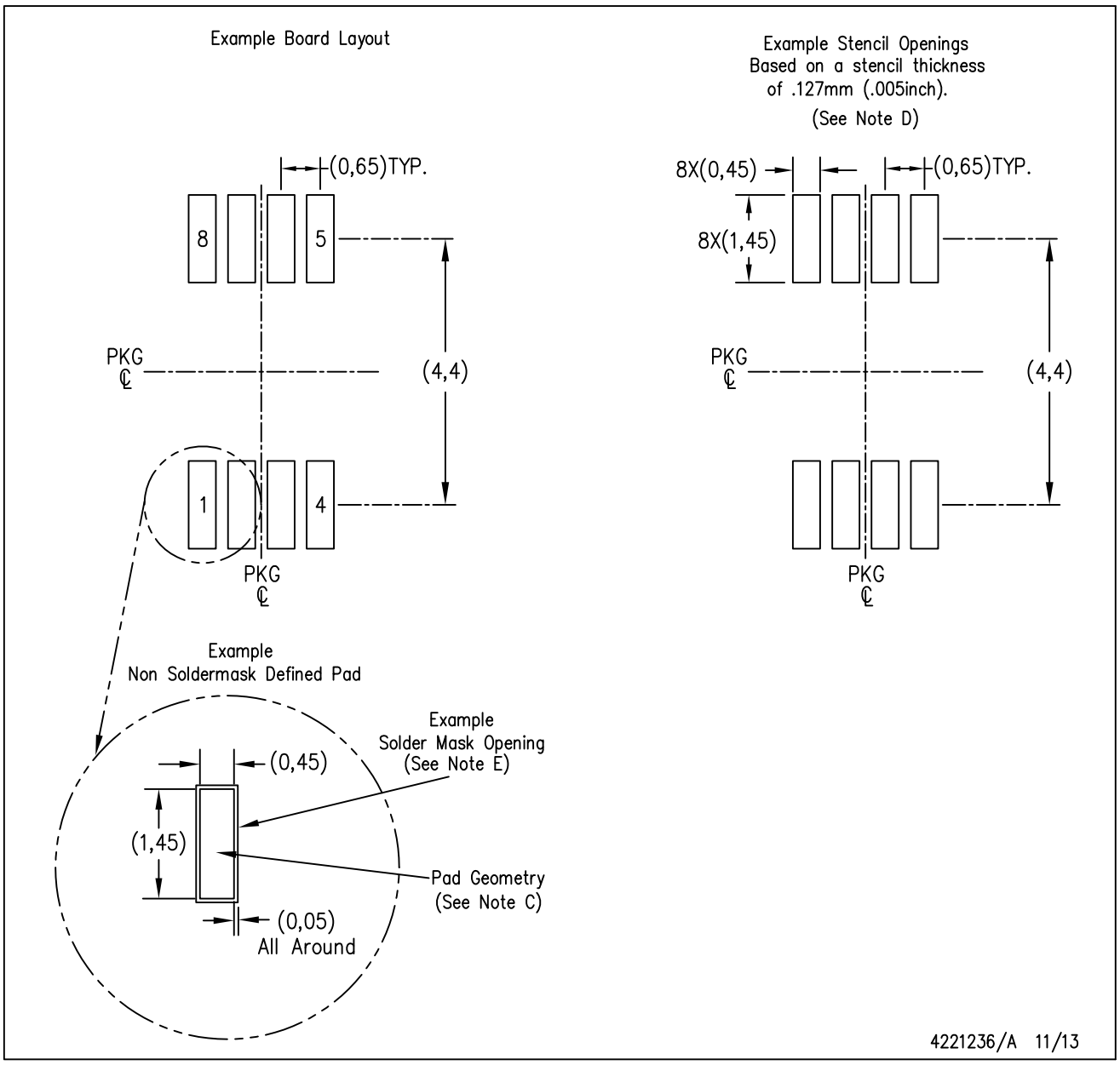
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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