Si8931/32 Data Sheet

Isolated Amplifier for Voltage Measurement

The Si8931/32 is a galvanically isolated analog amplifier optimized for voltage sensing. Its 2.5 V input range is ideal for isolated voltage sensing applications. The output is a differential analog signal (Si8931) or single-ended signal (Si8932) that is proportional to the input voltage.

The Si8931/32 provides excellent linearity with low offset and gain drift to ensure that accuracy is maintained over the entire operating temperature range. Exceptionally high common-mode transient immunity means that the Si8931/32 delivers accurate measurements even in the presence of high-power switching as is found in motor drive systems and inverters.

The Si8931/32 isolated voltage sensing amplifier utilizes Silicon Labs' proprietary isolation technology. It supports up to 5.0 kVrms withstand voltage per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and longer lifetimes compared to other isolation technologies.

Applications:

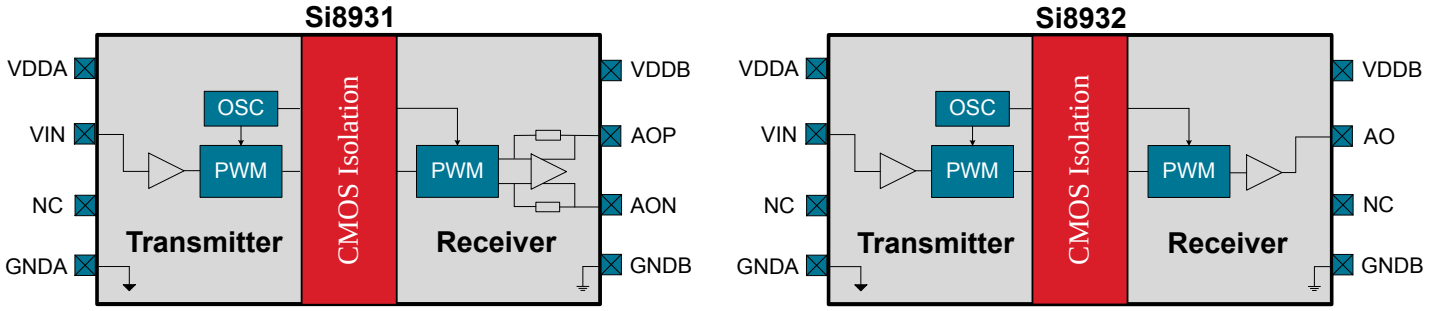
- Industrial, HEV and renewable energy inverters
- AC, Brushless, and DC motor controls and drives
- Variable speed motor control in consumer white goods
- Isolated switch mode and UPS power supplies
- Automotive BMS and charging
- General industrial data acquisition and sensor interface

Safety Approvals (pending):

- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA component notice 5A approval
  - IEC 60950-1 (reinforced insulation)
- VDE certification conformity
  - VDE0884 Part 10 (basic/reinforced insulation)
- CQC certification approval
  - GB4943.1

KEY FEATURES

- 0 to 2.5 V nominal input voltage
- Low signal delay: 1 µs
- Typical input offset: 0.2 mV
- Typical gain error: ±0.1%
- Excellent drift specifications
  - 0.75 µV/°C offset drift
  - 6 ppm/°C typical gain drift
- Typical nonlinearity: 0.004%
- Typical SNR: 76 dB
- High common-mode transient immunity: 75 kV/µs
- Compact packages
  - 8-pin wide body stretched SOIC
  - 8-pin narrow body SOIC
- –40 to 125 °C



1. Ordering Guide

New Ordering Part Number (OPN)	Ordering Options			
	Input Range	Isolation Rating	Output	Package Type
Si8931D-IS4	0 to 2.5 V nominal	5.0 kVrms	Differential	WB Stretched SOIC-8
Si8931B-IS	0 to 2.5 V nominal	2.5 kVrms	Differential	NB SOIC-8
Si8932D-IS4	0 to 2.5 V nominal	5.0 kVrms	Single-ended	WB Stretched SOIC-8
Si8932B-IS	0 to 2.5 V nominal	2.5 kVrms	Single-ended	NB SOIC-8

Note:

1. All packages are RoHS-compliant.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 pending qualification.

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2. System Overview

The input to the Si8931/32 is designed for 0 to 2.5 V nominal input.

The Si8931/32 modulates the analog signal in a unique way for transmission across the semiconductor based isolation barrier. The input signal is first converted to a pulse-width modulated digital signal. On the other side of the isolation barrier, the signal is demodulated to faithfully reproduce the analog signal. This solution provides exceptional signal bandwidth and accuracy. The Si8931 provides a differential voltage output while the Si8932 provides a single-ended voltage output.

The Si8931/32 implements a fail-safe output when the high-side supply voltage VDDA goes away. The fail-safe output is nominally 2.8 V which can be differentiated from the maximum clipping output voltage of 2.6 V to simplify diagnostics on the system level. The Si8931 outputs a negative differential output voltage while the single-ended Si8932 outputs a positive voltage.

When a loss of VDDA supply occurs the part will automatically move into a lower power mode that reduces IDDB current to approximately 1 mA. Similarly, a loss of VDDB supply will reduce IDDA current to approximately 1 mA. When the supply voltage is returned, normal operation begins in approximately 250 µs.

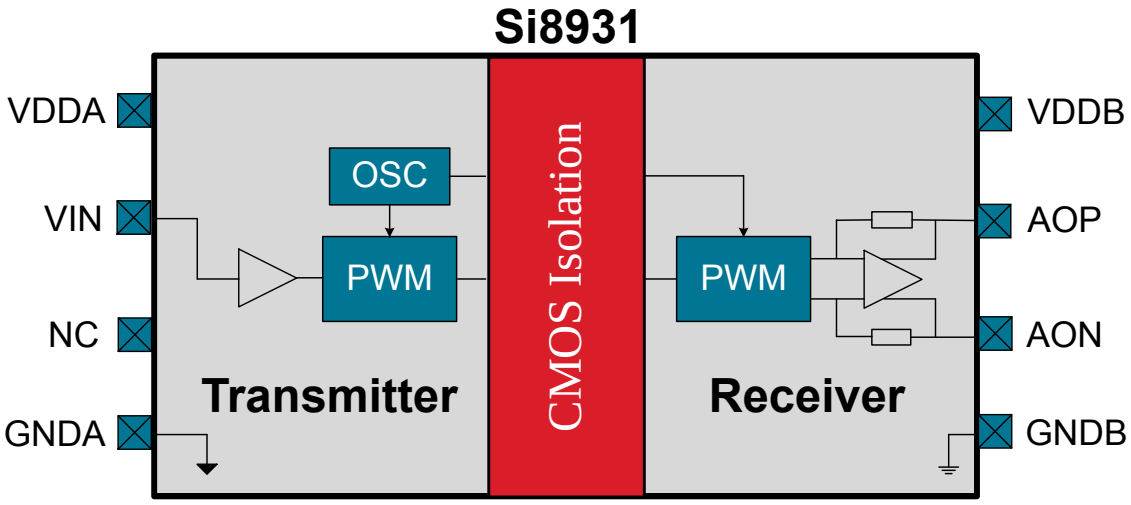


Figure 2.1. Si8931 Functional Block Diagram

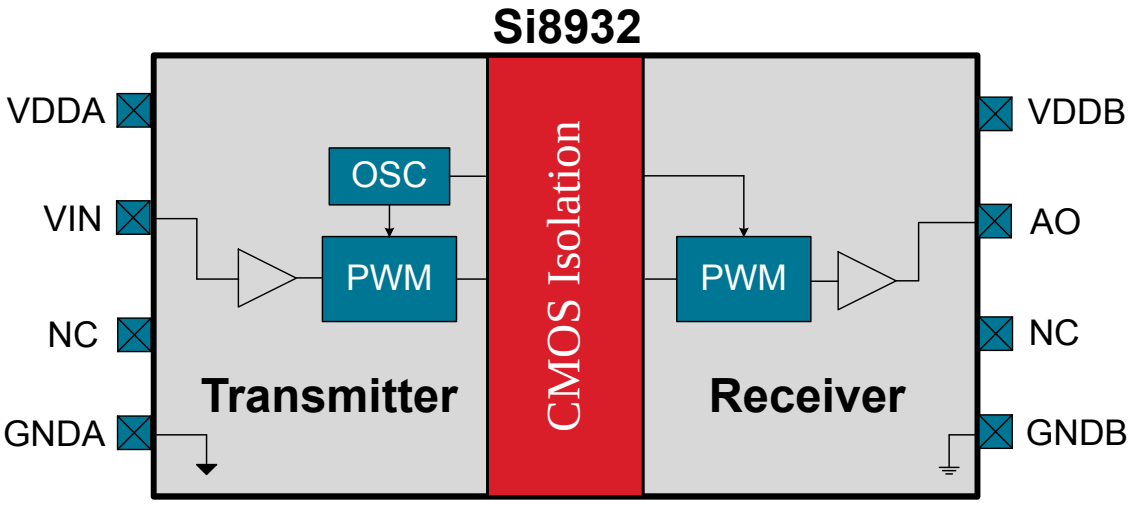


Figure 2.2. Si8932 Functional Block Diagram

3. Voltage Sense Application

A typical isolated voltage sensing application circuit is shown below. In this example, a high voltage is divided down to produce a voltage (VIN) within the optimum input signal range of the Si8931/32. Numerous alternative inputs configurations are possible with the flexibility of a high impedance input isolator. The Si8931 senses the single-ended input voltage and reproduces it as a differential (or single-ended with the Si8932) output voltage across the galvanic isolation barrier. The Si8931 differential outputs (AOP, AON) can be routed directly to a differential ADC as shown below. The Si8932 senses the single-ended input voltage and reproduces it as a single-ended output voltage across the galvanic isolation barrier. The single-ended output can be routed directly to a standard ADC (not shown). If the voltage sensed is > 2.5 V, a simple voltage divider consisting of R1 and R2 can be used to scale down any voltage to fit the input range of the Si8931/32. R2 < 10 kΩ is recommended for best performance.

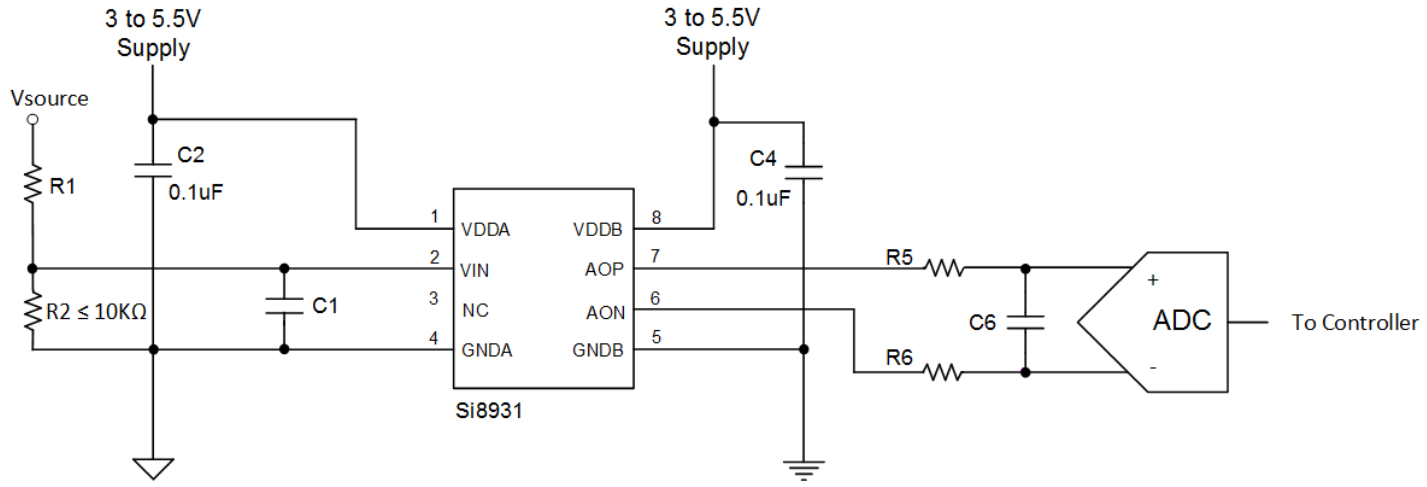


Figure 3.1. Voltage Sense Application

The amplifier bandwidth of the Si8931/32 is approximately 600 kHz. For applications where input filtering is required, a passive, differential RC low-pass filter can be placed at the input pin. Consider the source resistance of the signal measured (or the parallel combination of R1 and R2 if using a voltage divider) as it should be included in the filter calculation. Capacitor C1 should be sized to make a band limiting filter at the desired frequency.

C4, the local bypass capacitor for the B-side of Si8931/32, should be placed closed to VDDB supply pin with its return close to GNDB. The output signal at AOP and AON is differential with unity gain and common mode of 1.4 V. The outputs are sampled by a differential input ADC. Depending on the sample rate of the ADC, an anti-aliasing filter may be required. A simple anti-aliasing filter can be made from the passive components, R5, C6, and R6. The characteristics of this filter are dictated by the input topology and sampling frequency of the ADC. However, to ensure the Si8931/32 outputs are not overloaded, R5 = R6 > 5 kΩ and C6 can be calculated by the following equation:

$$C6 = \frac{1}{2 \times \pi \times (R5 + R6) \times f_{3dB}}$$

4. Electrical Specifications

Table 4.1. Electrical Specifications

V_{DDA}, V_{DDB} = 5 V, T_A = –40 to +125 °C; typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Input Side Supply Voltage	VDDA		3.0		5.5	V
Input Supply Current	IDDA	VDDA = 3.3 V	4.2	5.2	6.5	mA
Output Side Supply Voltage	VDDB		3.0		5.5	V
Output Supply Current	IDDB	VDDB = 3.3 V	2.3	3.2	5.5	mA
Amplifier Bandwidth				600		kHz
Amplifier Input						
Specified Linear Input Range	VIN		0.25		2.25	V
Maximum Input Voltage Before Clipping	VIN			2.5		V
Input Referred Offset	VOS	T_A = 25 °C	–1	0.2	1	mV
Input Offset Drift	VOS_T		–40	±0.75	5	µV/°C
Input Impedance	RIN			500		MΩ
Amplifier Output						
Full-scale Output	VAOP – VAON			2.5		Vpk
Gain				1		
Gain Error		T_A = 25 °C	–0.3	±0.1	0.3	%
Gain Error Drift			–40	6	20	ppm/°C
Output Common Mode Voltage (Si8931)	(VAOP + VAON)/2		1.36	1.39	1.42	V
Nonlinearity (Si8931)		T_A = 25 °C	–0.04	0.004	0.04	%
Nonlinearity (Si8932)		T_A = 25 °C	–0.08	0.01	0.08	%
Nonlinearity Drift		T_A = 25 °C	–7		7	ppm/°C
Signal-to-Noise Ratio (Si8931)	SNR	Over 100 kHz	74	76		dB
Signal-to-Noise Ratio (Si8932)	SNR	Over 100 kHz	71	75		dB
Total Harmonic Distortion (Si8931)	THD	F_{IN} = 1 kHz		–80	–70	dB
Total Harmonic Distortion (Si8932)	THD	F_{IN} = 1 kHz		–74	–66	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Power Supply Rejection Ratio	PSRR	PSRR vs. VDDA at DC		–100		dB
		PSRR vs. VDDA at 100 mV and 10 kHz ripple		–100		dB
		PSRR vs. VDDB at DC		–100		dB
		PSRR vs. VDDB at 100 mV and 10 kHz ripple		–100		dB
Output Resistive Load	RLOAD	Between AON and AOP (Si8931) Between AO and GND (Si8932)	5			kΩ
Output Capacitive Load	CLOAD	Each pin to ground			100	pF
Timing						
Signal Delay	t_{PD}	50% to 50%		1		µs
Rise Time	t_R	10% to 90%		1.6		µs
Common-Mode Transient Immunity[1]	CMTI	VIN = GNDA, VCM = 1500 V	50	75		kV/µs

Note:
1. An analog CMTI failure is defined as an output error of more than 100 mV persisting for at least 1 µs.

Figure 4.1. Common-Mode Transient Immunity Characterization Circuit

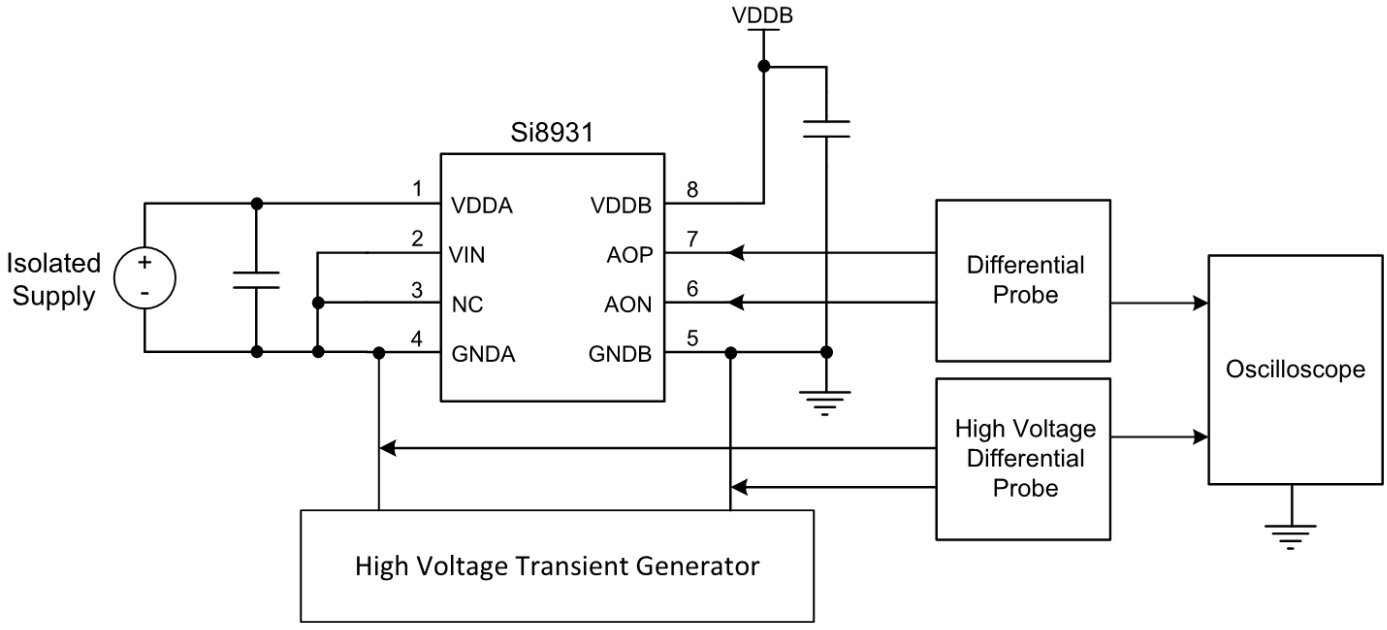


Table 4.2. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
Safety Temperature	T_S		150	°C
Safety Input Current (WB Stretched SOIC-8)	I_S	θ_{JA} = 90 °C/W VDD = 5.5 V T_J = 150 °C T_A = 25 °C	253	mA
		θ_{JA} = 90 °C/W VDD = 3.6 V T_J = 150 °C T_A = 25 °C	386	mA
Safety Input Current (NB Stretched SOIC-8)	I_S	θ_{JA} = 112 °C/W VDD = 5.5 V T_J = 150 °C T_A = 25 °C	310	mA
		θ_{JA} = 112 °C/W VDD = 3.6 V T_J = 150 °C T_A = 25 °C	203	mA
Safety Input Power (WB Stretched SOIC-8)	P_S	θ_{JA} = 90 °C/W T_J = 150 °C T_A = 25 °C	1389	mW
Safety Input Power (NB SOIC-8)	P_S	θ_{JA} = 112 °C/W T_J = 150 °C T_A = 25 °C	1116	mW
Device Power Dissipation (WB Stretched SOIC-8)	P_D		1.39	W
Device Power Dissipation (NB SOIC-8)			1.12	W

Note:
1. Maximum value allowed in the event of a failure. Refer to the thermal derating curves below.

Table 4.3. Thermal Characteristics

Parameter	Symbol	WB Stretched SOIC-8	NB SOIC-8	Unit
IC Junction-to-Air Thermal Resistance	θ_{JA}	90	112	°C/W

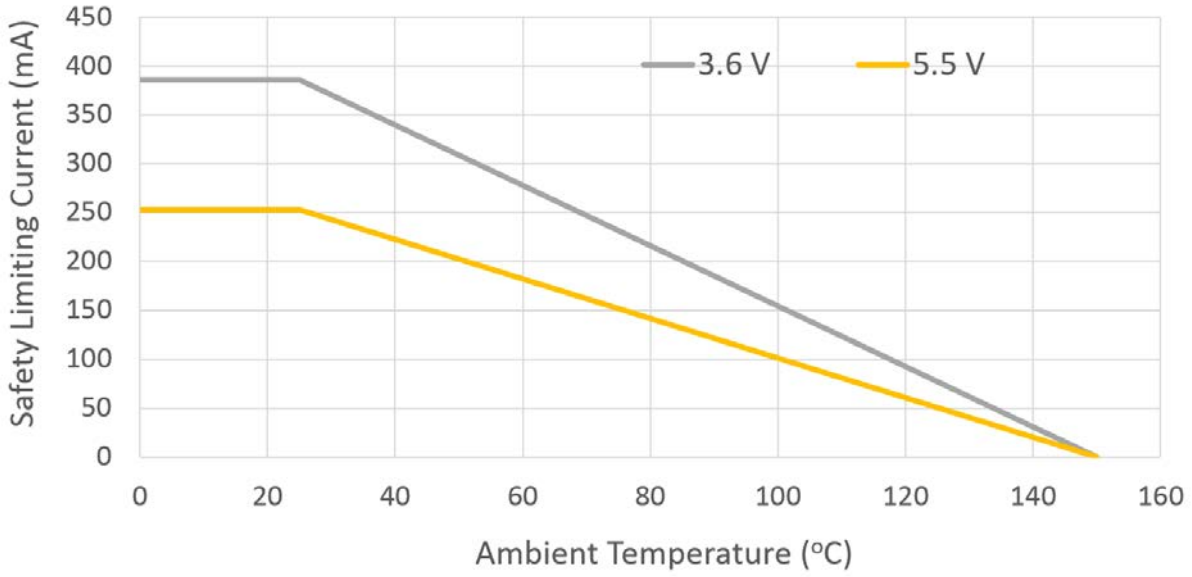


Figure 4.2. WB Stretched SOIC-8 Thermal Derating Curve for Safety Limiting Current

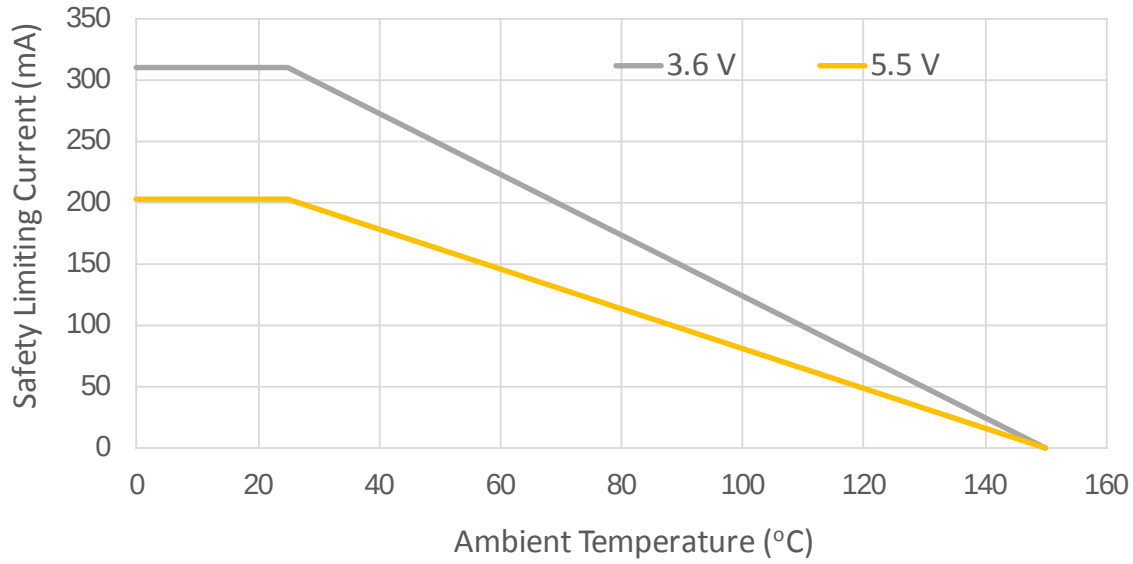


Figure 4.3. NB SOIC-8 Thermal Derating Curve for Safety Limiting Current

Table 4.4. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	–65	150	°C
Ambient Temperature Under Bias	T_A	–40	125	°C
Junction Temperature	T_J	—	150	°C
Supply Voltage	VDDA, VDDB	–0.5	6.0	V
Input Voltage respect to GNDA	VIN	–0.5	VDDx + 0.5	V
Output Sink or Source Current	$\|I_O\|$	—	5	mA
Total Power Dissipation	P_T	—	212	mW
Lead Solder Termperature (10 s)		—	260	°C
Human Body Model ESD Rating		6000	—	V
Capacitive Discharge Model ESD Rating		2000	—	V
Maximum Isolation (WB Stretched SOIC-8 Input to Output) (1 s)		—	6500	V_{RMS}
Maximum Isolation (NB SOIC-8 package Input to Output) (1 s)		—	3250	V_{RMS}

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of the data sheet.

4.1 Regulatory Information

Table 4.5. Regulatory Information (Pending)[1, 2]

CSA
The Si8931/32 is certified under CSA Component Acceptance Notice 5A. For more details, see Master Contract File 232873.
60950-1, 62368-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si8931/32 is certified according to VDE 0884-10. For more details, see File 5006301-4880-0001.
VDE 0884-10: Up to 1414 V_{peak} for reinforced insulation working voltage.
UL
The Si8931/32 is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si8931/32 is certified under GB4943.1-2011.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Note: 1. Regulatory Certifications apply to 5 kV_{RMS} rated devices which are production tested to 6.0 kV_{RMS} for 1 sec. 2. Regulatory Certifications apply to 2.5 kVRMS rated devices which are production tested to 3.0 kVRMS for 1 sec.

Table 4.6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			WB Stretched SOIC-8	NB SOIC-8	
Nominal External Air Gap (Clearance)	CLR		9.0[1]	4.9	mm
Nominal External Tracking (Creepage)	CPG		8.0[1]	4.01	mm
Minimum Internal Gap (Internal Clearance)	DTI		0.762	0.254	mm
Tracking Resistance (Proof Tracking Index)	PTI or CTI	IEC60112	600	600	V
Erosion Depth	ED		0.04	0.04	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1	1	pF

Note:

1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as x.x mm minimum for the WB Stretched SOIC-8 package. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage limits as x.x mm minimum for the WB Stretched SOIC-8 package.
2. To determine resistance and capacitance, the Si8931/32 is converted into a two-terminal device. Pins 1–4 are shorted together to form the first terminal, and pins 5–8 are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 4.7. IEC 60664-1 (VDE 0884) Ratings

Parameter	Test Conditions	Specification
		WB Stretched SOIC-8
Basic Isolation Group	Material Group	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 450 V_{RMS}	I-III
	Rated Mains Voltages ≤ 600 V_{RMS}	I-III

Table 4.8. VDE 0884-10 Insulation Characteristics[1]

Parameter	Symbol	Test Condition	Characteristic	Unit
			WB Stretched SOIC-8	
Maximum Working Insulation Voltage	V_{IORM}		1414	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	2650	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	8000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

Note:

1. This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si8931/32 provides a climate classification of 40/125/21.

4.2 Typical Operating Characteristics

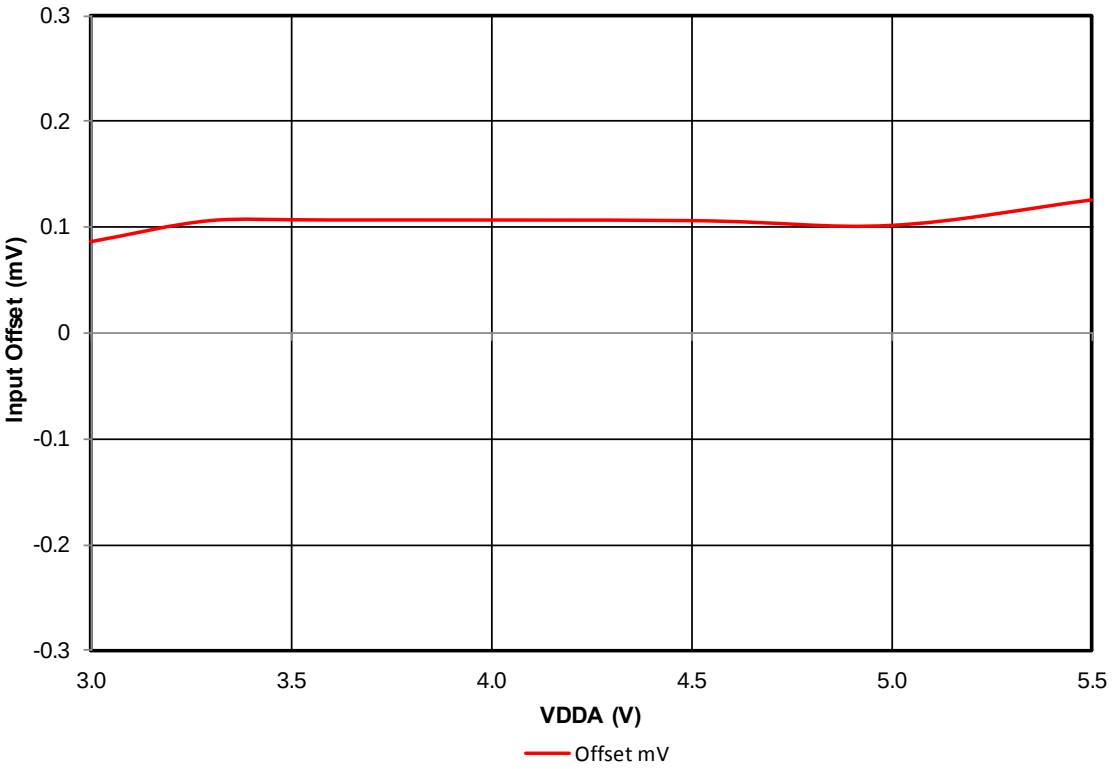


Figure 4.4. Input Offset vs. VDDA

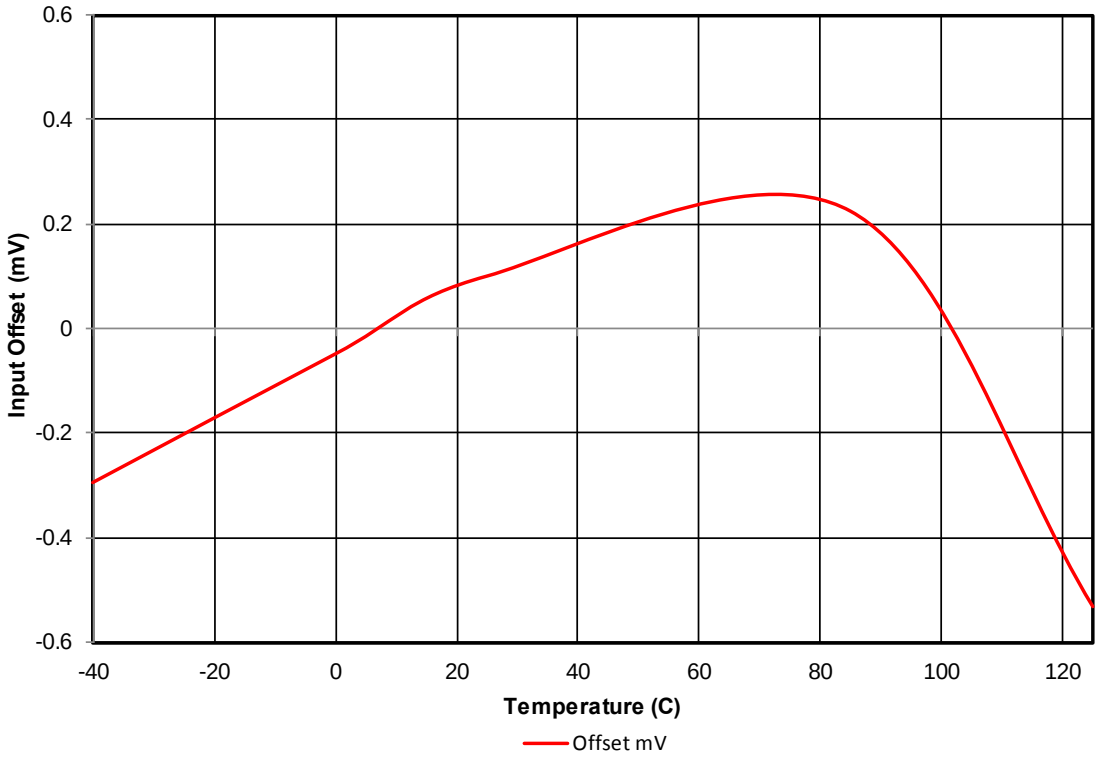


Figure 4.5. Input Offset vs. Temperature

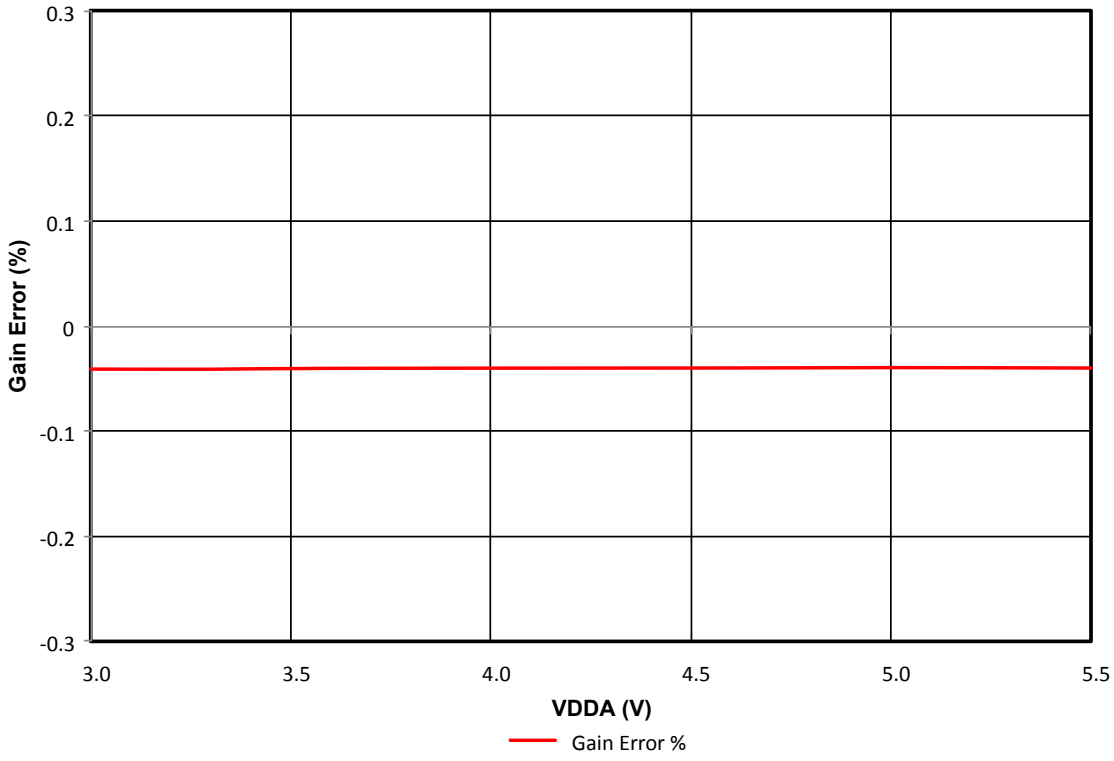


Figure 4.6. Gain Error vs. VDDA

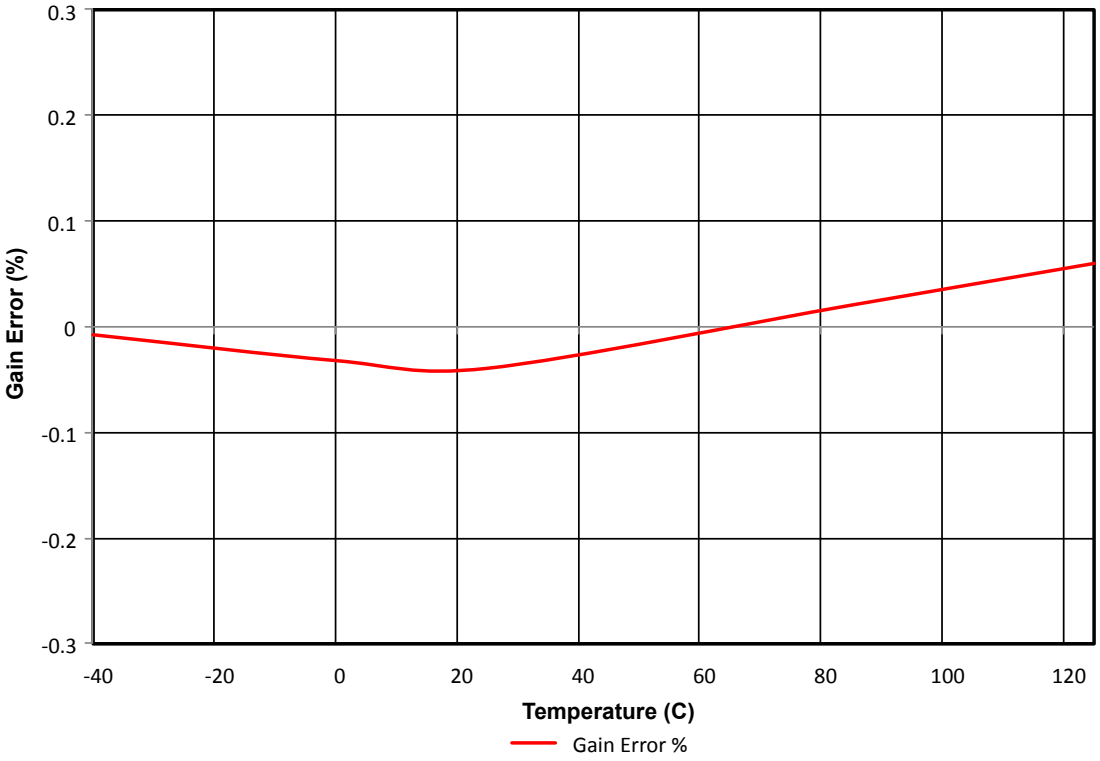


Figure 4.7. Gain Error vs. Temperature

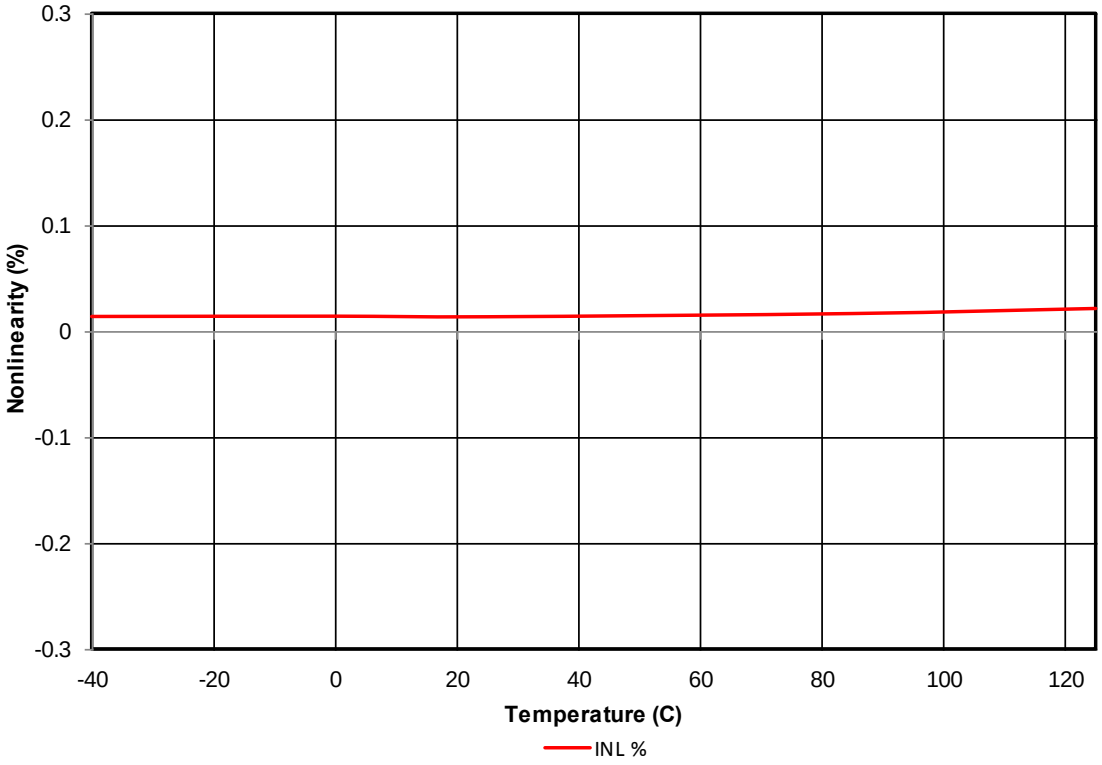


Figure 4.8. Nonlinearity vs. Temperature

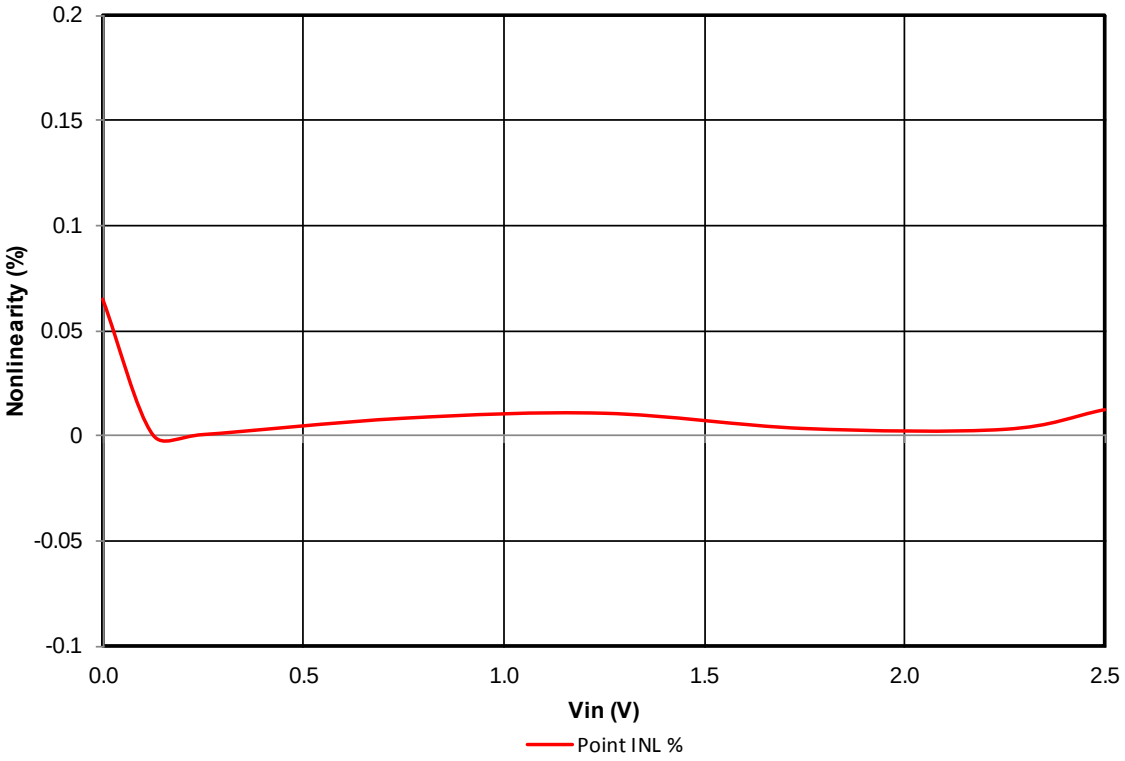


Figure 4.9. Si893x Nonlinearity vs. Input Signal Amplitude

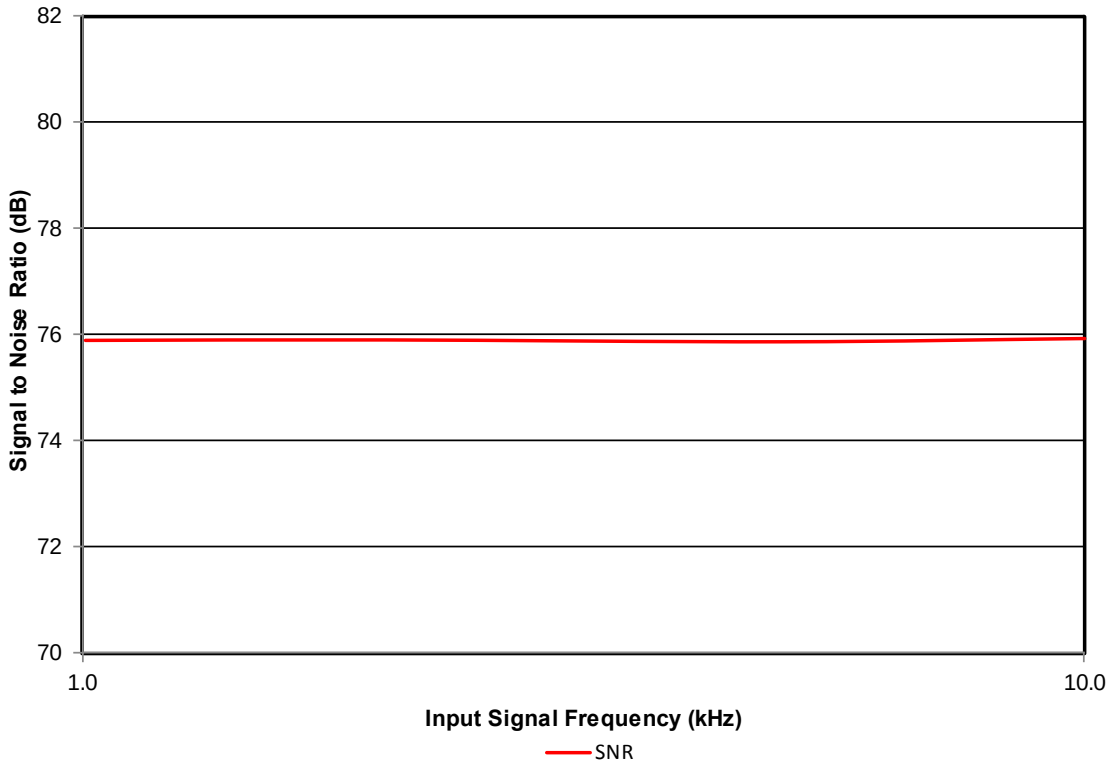


Figure 4.10. Si8931 Signal-to-Noise Ratio vs. Frequency

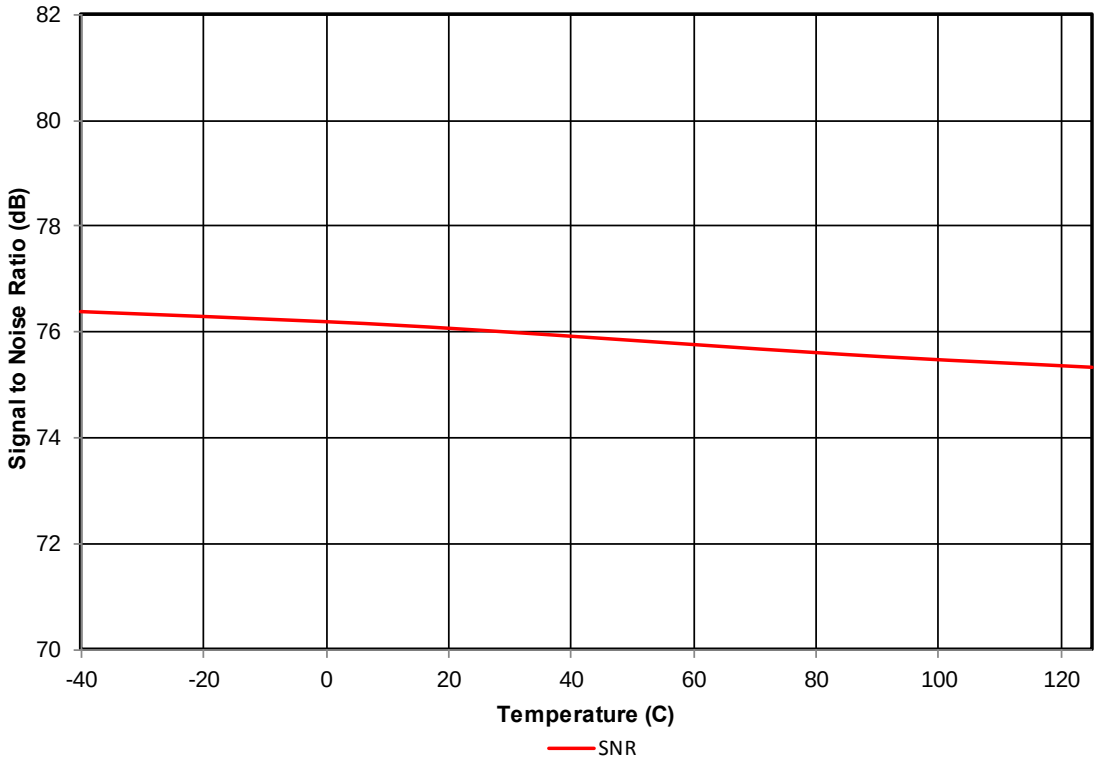


Figure 4.11. Si8931 Signal-to-Noise Ratio vs. Temperature

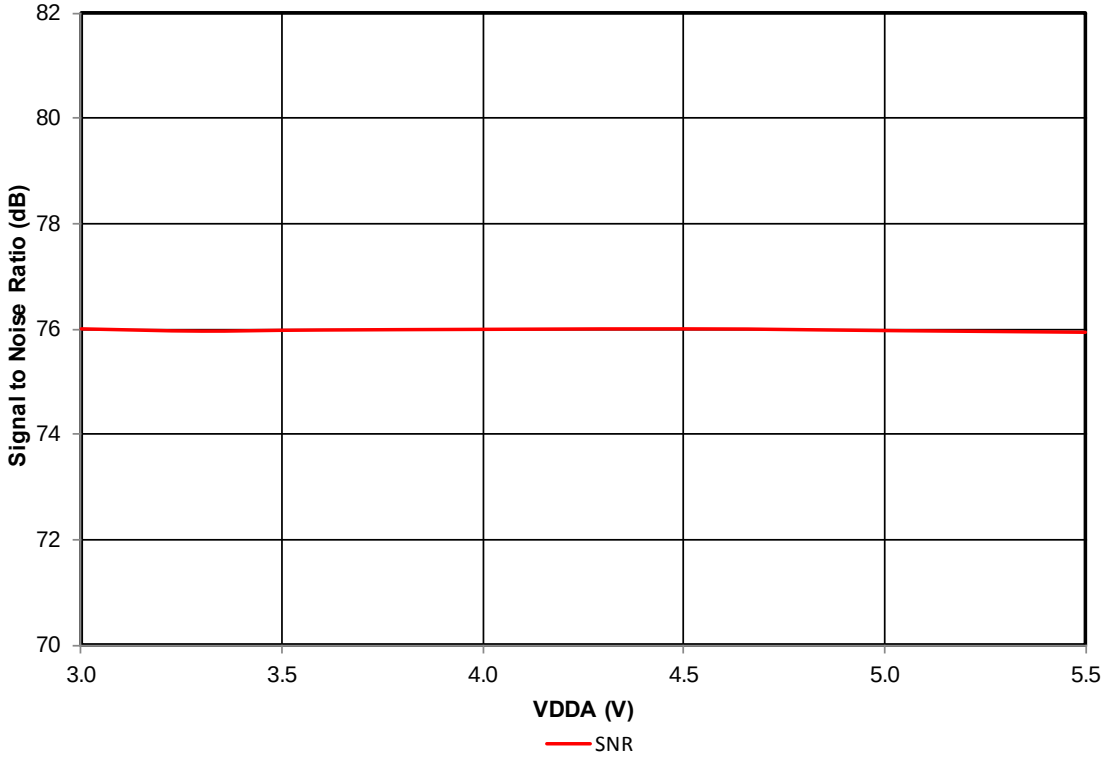


Figure 4.12. Si8931 Signal-to-Noise Ratio vs. Supply Voltage

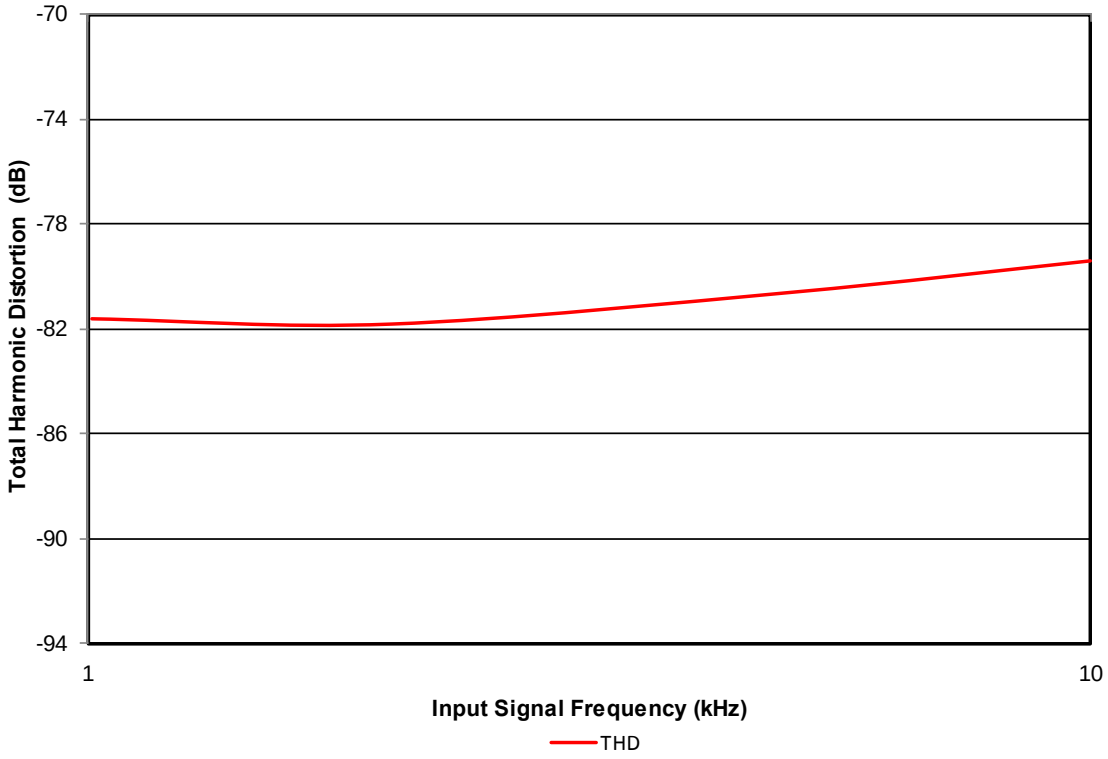


Figure 4.13. Si8931 Total Harmonic Distortion vs. Input Signal Frequency

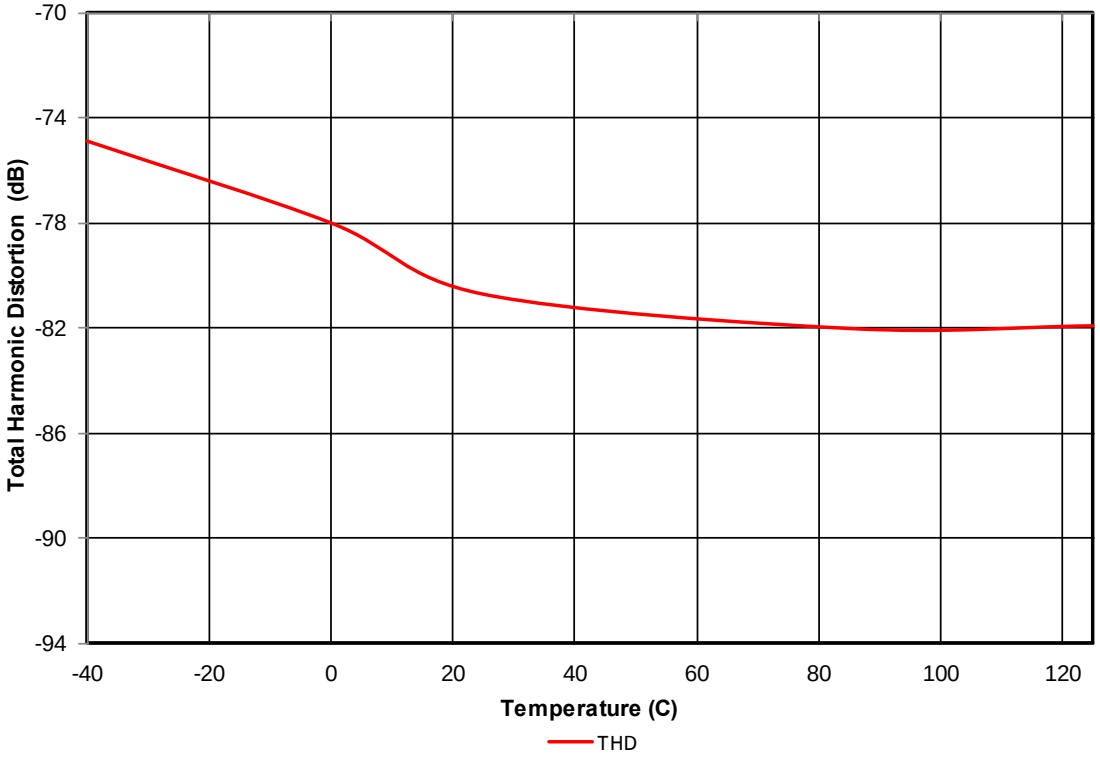


Figure 4.14. Si8931 Total Harmonic Distortion vs. Temperature

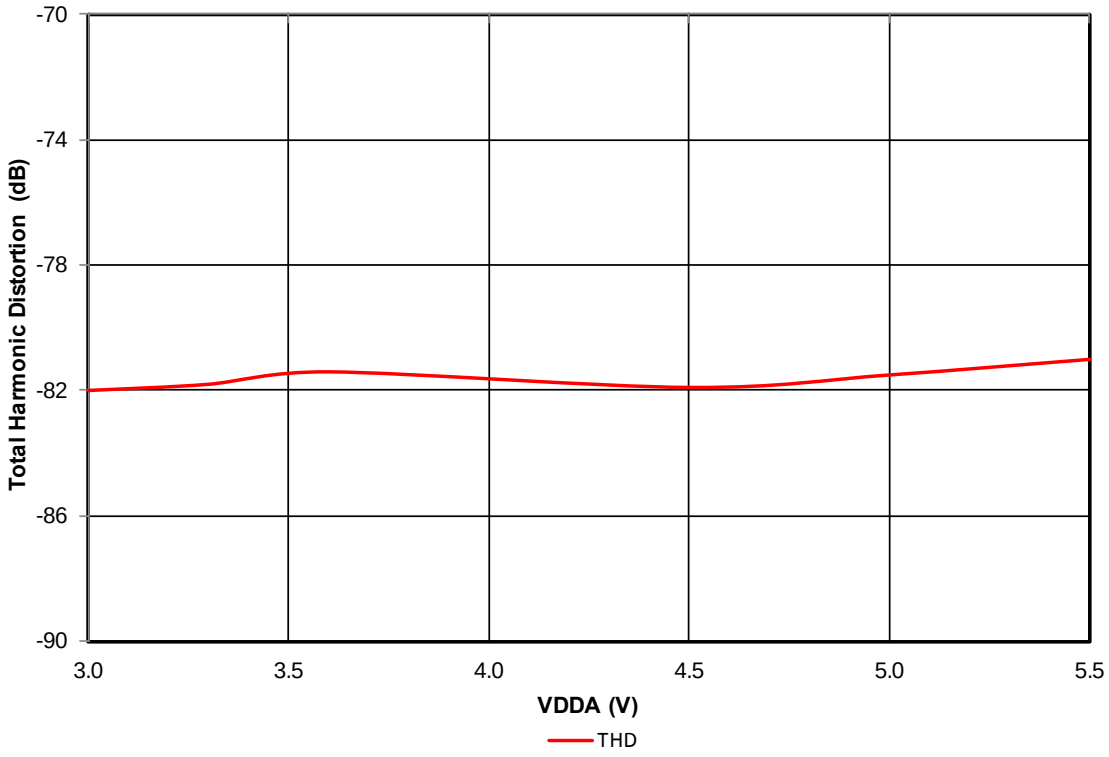


Figure 4.15. Si8931 Total Harmonic Distortion vs. VDD

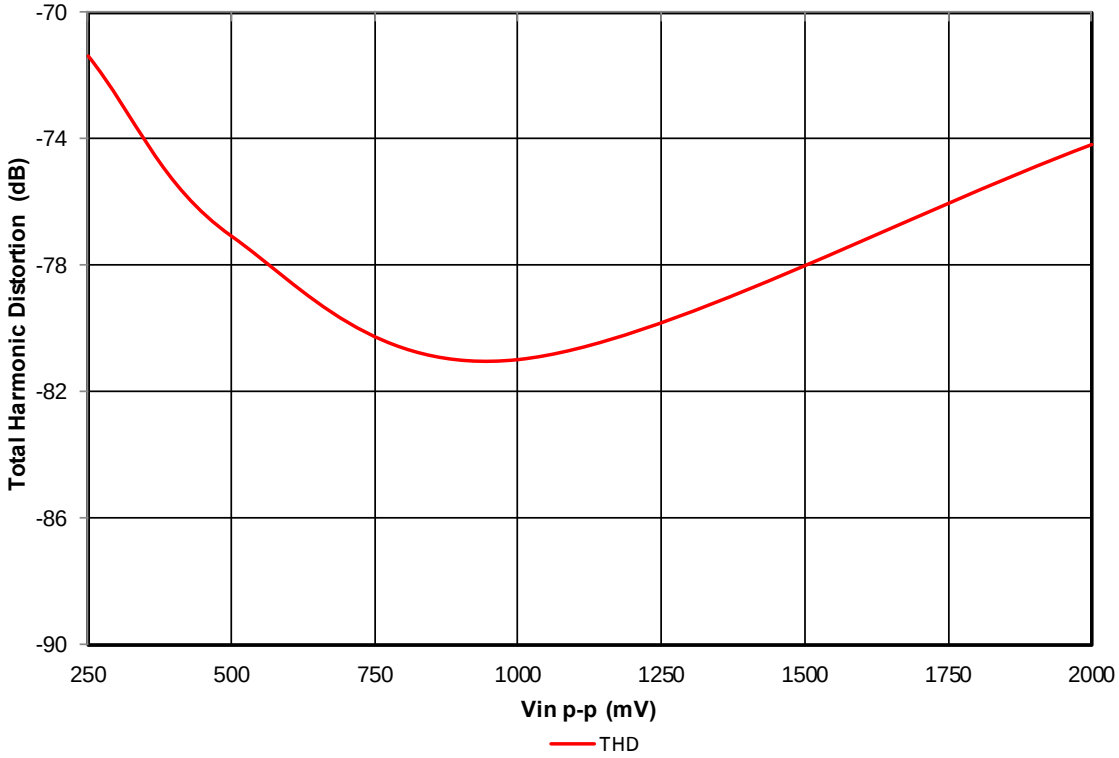


Figure 4.16. Si8931 Total Harmonic Distortion vs. Input Signal Amplitude

5. Pin Descriptions

5.1 Si8931 Pin Descriptions

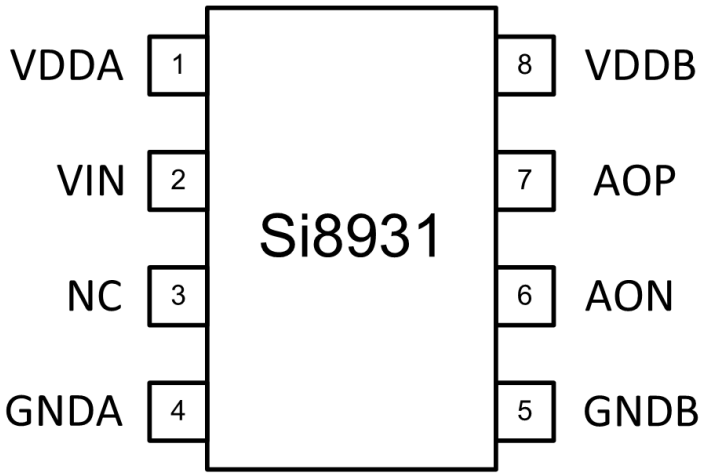


Table 5.1. Si8931 Pin Descriptions

Name	GW DIP-8 Pin #	Description
VDDA	1	Input side power supply
VIN	2	Voltage input
NC[1]	3	No Connect
GNDA	4	Input side ground
GNDB	5	Output side ground
AON	6	Analog output low
AOP	7	Analog output high
VDDB	8	Output power supply

Note:

1. No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

5.2 Si8932 Pin Descriptions

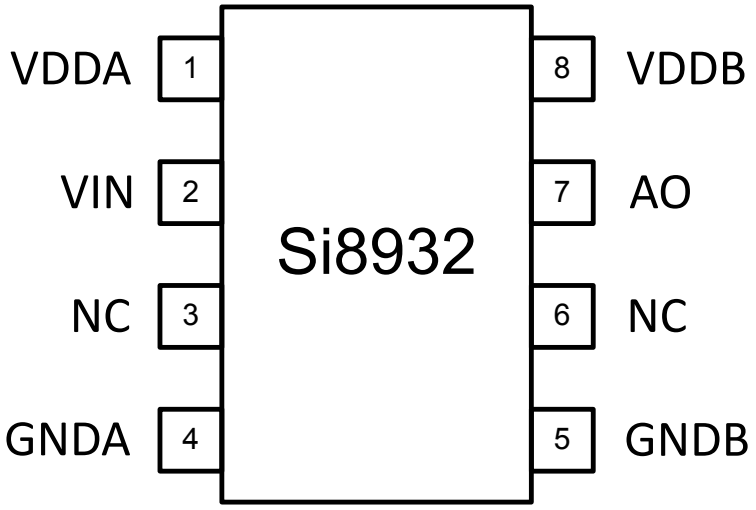


Table 5.2. Si8932 Pin Descriptions

Name	GW DIP-8 Pin #	Description
VDDA	1	Input side power supply
VIN	2	Voltage input
NC[1]	3	No Connect
GNDA	4	Input side ground
GNDB	5	Output side ground
AO	6	Analog output
NC	7	No connect
VDDB	8	Output power supply

Note:

1. No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

6. Packaging

6.1 Package Outline: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the package details for the Si8931/32 in a 8-Pin Wide Body Stretched SOIC package. The table lists the values for the dimensions shown in the illustration.

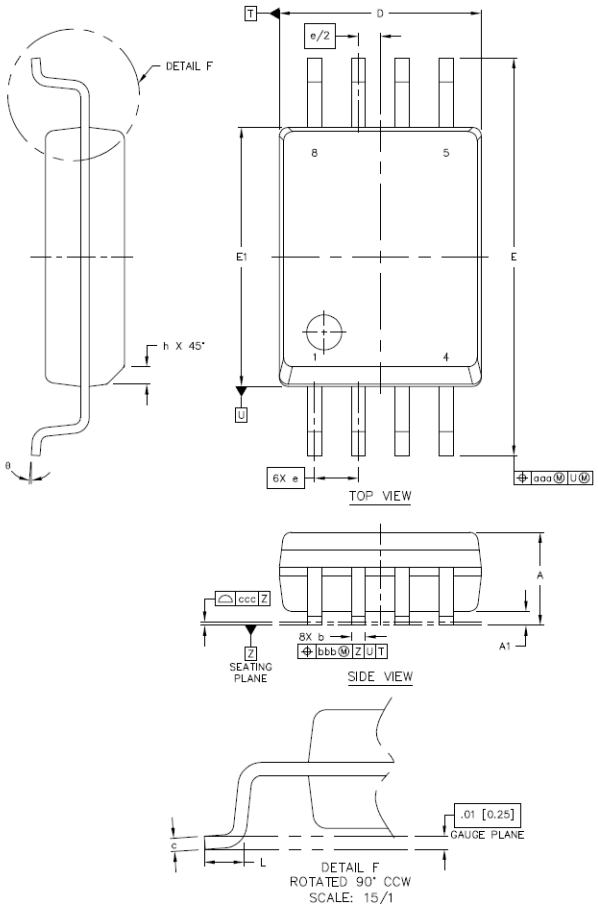


Figure 6.1. 8-Pin Wide Body Stretched SOIC Package

Table 6.1. 8-Pin Wide Body Stretched SOIC Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	2.49	2.79
A1	0.36	0.46
b	0.30	0.51
c	0.20	0.33
D	5.74	5.94
E	11.25	11.76
E1	7.39	7.59
e	1.27 BSC	
L	0.51	1.02
h	0.25	0.76

Symbol	Millimeters	
	Min	Max
θ	0°	8°
aaa	—	0.25
bbb	—	0.25
ccc	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

6.2 Package Outline: 8-Pin Narrow Body SOIC

The figure below illustrates the package details for the Si8931/32 in an 8-Pin Narrow Body SOIC package. The table lists the values for the dimensions shown in the illustration.

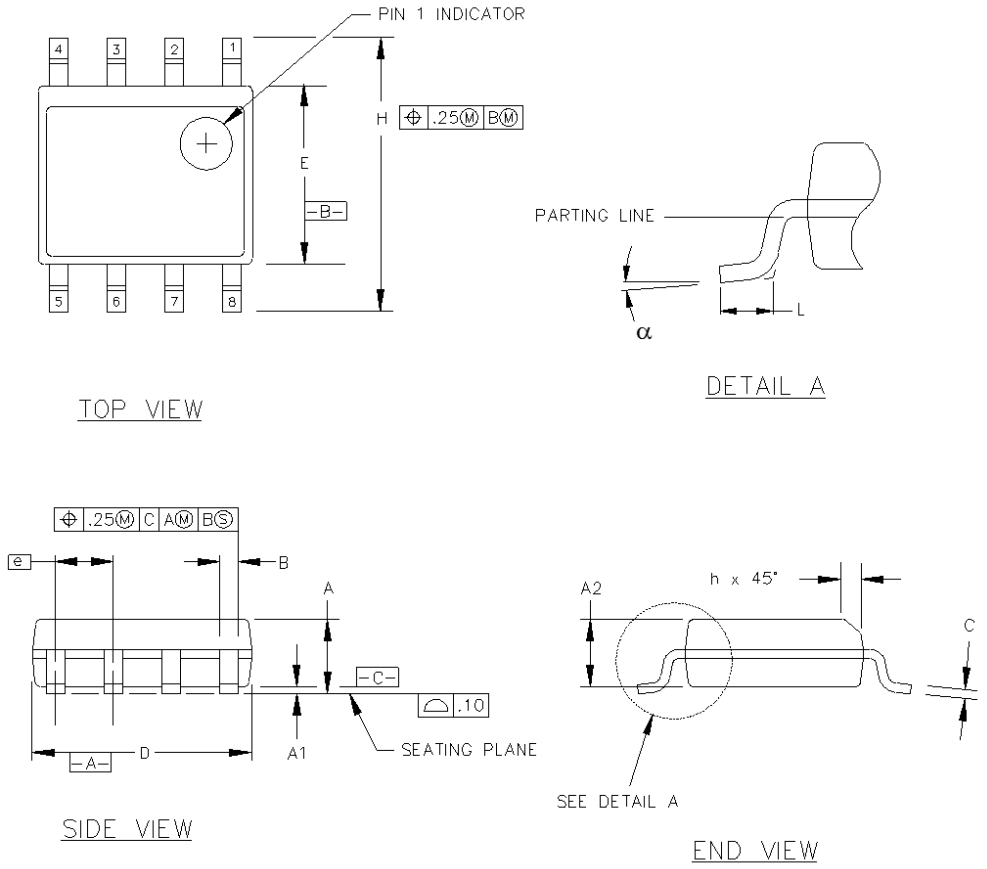


Figure 6.2. 8-Pin Narrow Body SOIC Package

Table 6.2. 8-Pin Narrow Body SOIC Package Diagram Dimensions

Dimension	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.40 REF	1.55 REF
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Dimension	Min	Max

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020B specification for Small Body Components.

6.3 Land Pattern: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the recommended land pattern details for the Si8931/32 in a 8-Pin Wide Body Stretched SOIC package. The table lists the values for the dimensions shown in the illustration.

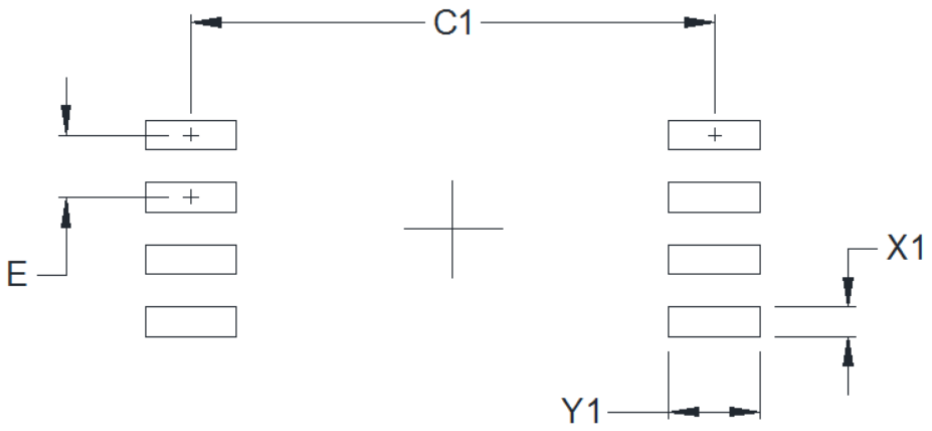


Figure 6.3. 8-Pin Wide Body Stretched SOIC Land Pattern

Table 6.3. 8-Pin Wide Body Stretched SOIC Land Pattern Dimensions[1]

Dimension	(mm)
C1	10.60
E	1.27
X1	0.60
Y1	1.85

Note:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60mm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.4 Land Pattern: 8-Pin Narrow Body SOIC

The figure below illustrates the recommended land pattern details for the Si8931/32 in an 8-Pin Narrow Body SOIC package. The table lists the values for the dimensions shown in the illustration.

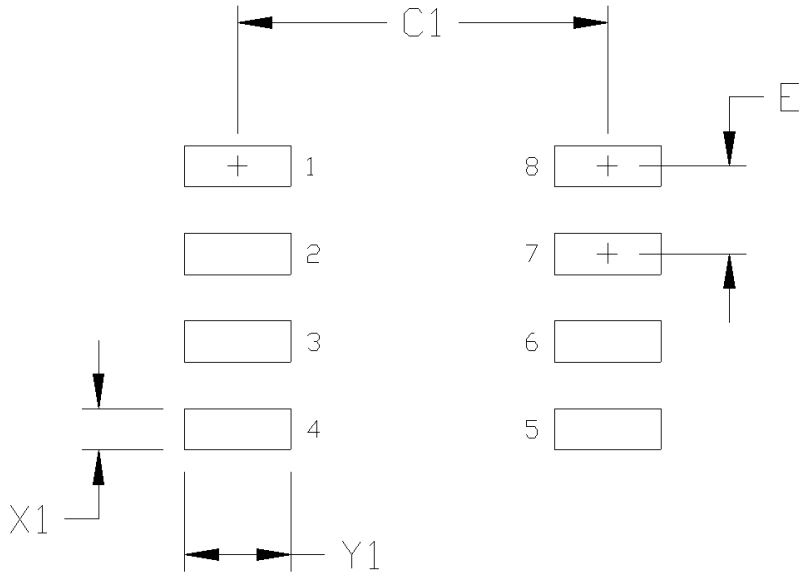


Figure 6.4. 8-Pin Narrow Body SOIC Land Pattern

Table 6.4. 8-Pin Narrow Body SOIC Land Pattern Dimensions

Symbol	mm
C1	5.40
E	1.27
X1	0.60
Y1	1.55

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

6.5 Top Marking: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the top markings for the Si8931/32 in a 8-Pin Wide Body Stretched SOIC package. The table explains the top marks shown in the illustration.

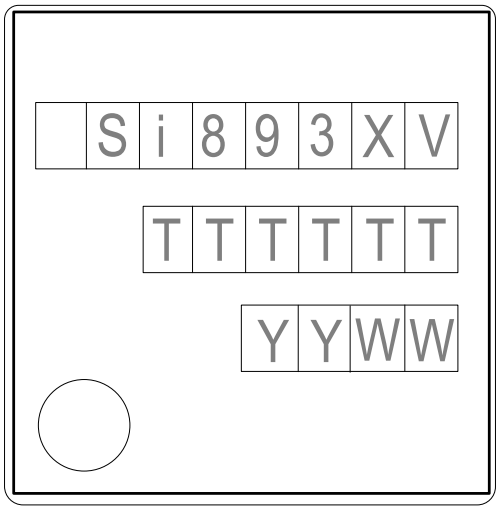


Figure 6.5. 8-Pin Wide Body Stretched SOIC Top Marking

Table 6.5. 8-Pin Wide Body Stretched SOIC Top Mark Explanation

Line 1 Marking:	Customer Part Number	Si893X X = Base part number • 1 = Differential output • 2 = Single-ended output V = Insulation rating: • D = 5.0 kV
Line 2 Marking:	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking:	YY = Year WW = Work Week Circle = 43 mils Diameter Left-Justified	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.

6.6 Top Marking: 8-Pin Narrow Body SOIC

The figure below illustrates the top markings for the Si8931/32 in an 8-Pin Narrow Body SOIC package. The table explains the top marks shown in the illustration.

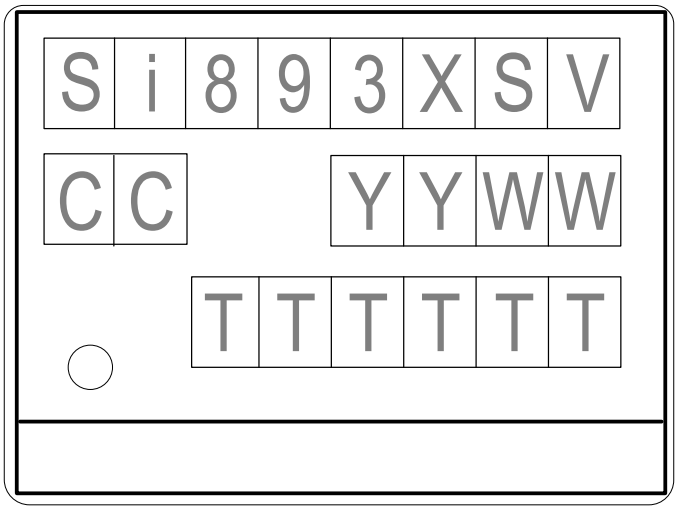


Figure 6.6. 8-Pin Narrow Body SOIC Top Marking

Table 6.6. 8-Pin Narrow Body SOIC Top Marking Explanation

Line 1 Marking:	Customer Part Number	Si893X = Isolator Amplifier Series X = Base part number • 1 = Differential output • 2 = Single-ended output S = Input Range: • A = ±62.5 mV • B = ±250 mV V = Insulation rating: • B = 2.5 kV
Line 2 Marking:	CC = Country of Origin ISO Code Abbreviation	
	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
Line 3 Marking:	TTTTTT = Mfg Code Circle = 19.7 mils Diameter Left-Justified	Manufacturing Code from the Assembly Purchase Order form.

7. Document Revision History

Revision 0.5

March, 2019

- Updated specifications.
- Added narrow body SOIC-8 package.

Revision 0.2

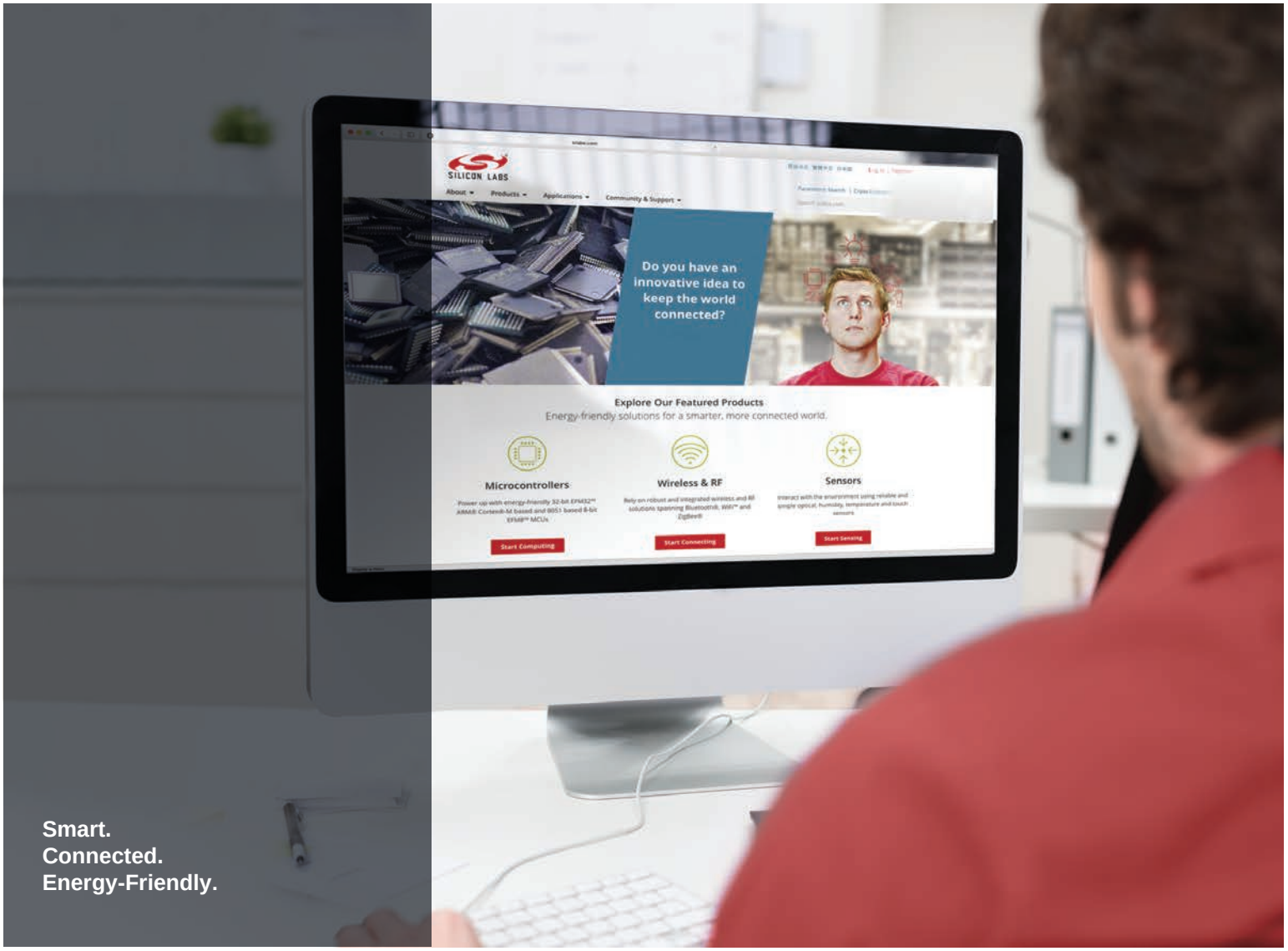
May, 2018

- Corrections and clarifications.

Revision 0.1

January, 2018

- Initial draft.



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