Multi-Mode PWM Power Switch with Primary-Side Feedback

Features

- Built-in 650V Power MOSFET
- Low Start-Up Current (<2uA)
- Primary-Side Feedback Control with Multi-Mode Operation
  CCM @ Heavy Load and Low Line
  QR-Like Operation @ Medium Load
  Green mode with Valley Skip at Light Load
  PFM Mode at No Load
- Built-In Adjustable Load Regulation Compensation
- Constant Voltage/Constant Current Operation
- Output Short Protection
- FB Pin Open/Short Protection
- Soft Driver
- 8ms Soft-start
- OVP (Over Voltage Protection) on Vcc Pin
- On Chip OTP Protection

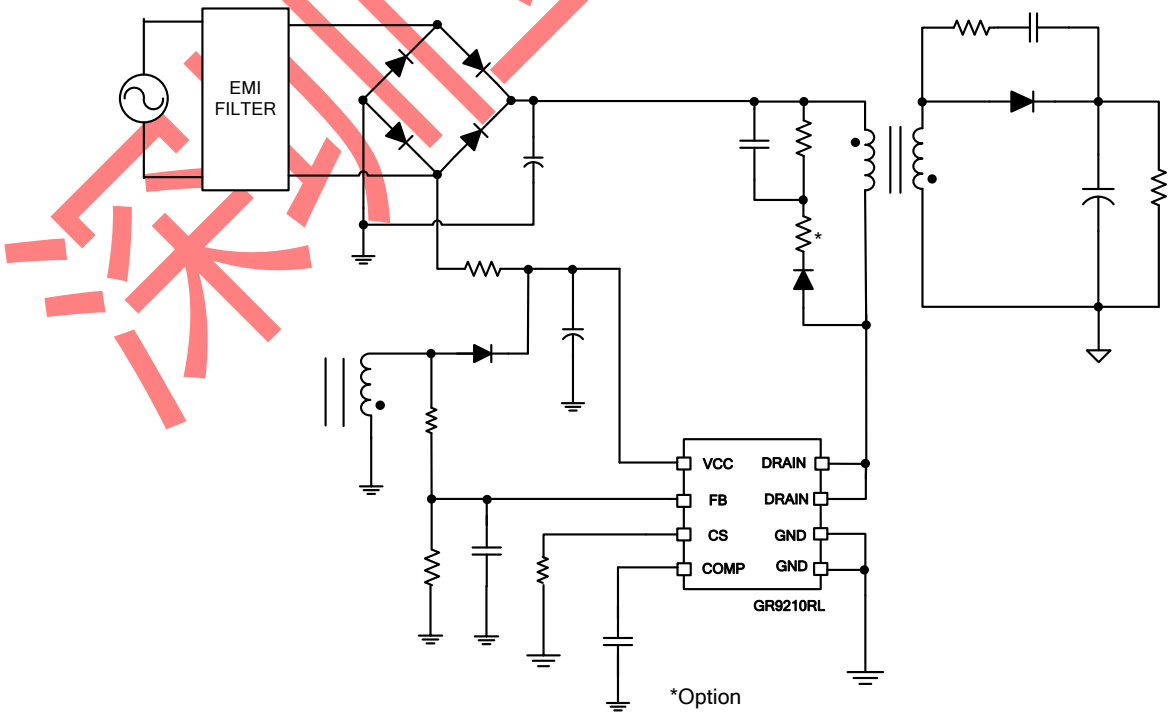
Description

The GR9210RL integrates a high performance primary side feedback PWM controller and a high voltage power MOSFET of 650V. It minimizes the components counts and is available in a tiny DIP-8, SOP-7, SOP-8 package. Those make it an ideal design for low cost application. It provides functions of low startup current, green- mode power-saving operation, VCC over-voltage protection, and FB pin abnormal conditions sensing to prevent the circuit being damaged from the abnormal conditions.

Applications

- Mobile Phone Adapter
- Lower Power AC/DC Adapter

Typical Application Information



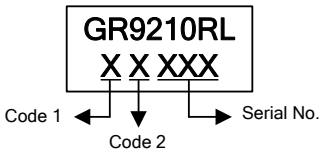
Ordering and Marking Information

GR9210RL

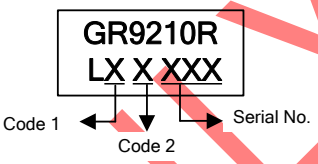
Package Code
J: DIP-8
K: SOP-8
KA: SOP-7

RoHS Code
G: Green (Halogen Free) Device
L : PB Free

DIP-8



SOP-7/8



Code 1	8	9	A	B	...	G	H	I	J
Year	2008	2009	2010	2011		2016	2017	2018	2019
Code 2	1	2	3	4		9	A	B	C
Month	Jan.	Feb.	Mar.	Apr.		Sep.	Oct.	Nov.	Dec.

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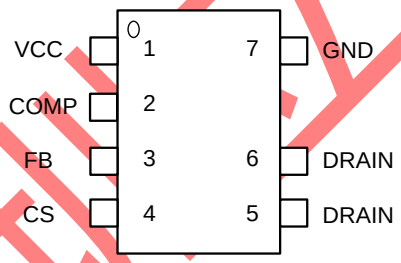
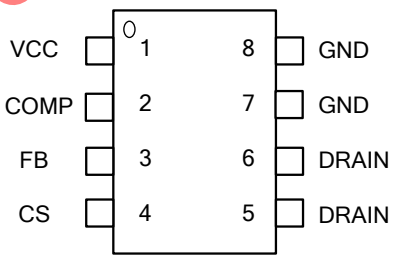
Pin Configuration

TOP VIEW

SOP-7



DIP-8/SOP-8



Pin Description

Pin No.	Name	Function
1	VCC	Power supply pin
2	COMP	Output of the error amplifier for voltage compensation.
3	FB	This pin is for quasi-resonant detection and feedback control.
4	CS	Current sense pin, connected to sense resistor for sensing the MOSFET current signal
5,6	DRAIN	Drain of internal HV MOSFET
7,8	GND	Ground reference pin

Absolute Maximum Ratings

Drain Voltage ---------- -0.3V ~ 650V

Supply voltage VCC ---------- 30V

COMP, CS, FB---------- -0.3~6.0V

Junction temperature ---------- 150℃

Storage temperature range ---------- -65℃ ~ 150 ℃

Lead temperature (DIP-8, SOP-7 & SOP-8, soldering, 10 sec) ---------- 230℃

Lead temperature (All Pb free packages, soldering, 10 sec) ---------- 260℃

ESD, human body model ---------- 2.5KV

ESD, machine model ---------- 250V

Caution: The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed and may cause permanent damage to the IC. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the Electrical Characteristics section of the specification is not implied. The “Electrical Characteristics” table defines the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction temperature	-40	125	℃
Operating ambient temperature	-40	85	℃
Start Up Resistor (AC Half side)	1M	7M	Ω
Supply voltage VCC	8.5	26.5	V
VCC Capacitor	0.68	4.7	μF
COMP pin paralleling capacitor	0.47	2.2	nF
FB Pin paralleling capacitor	4.7	22	pF

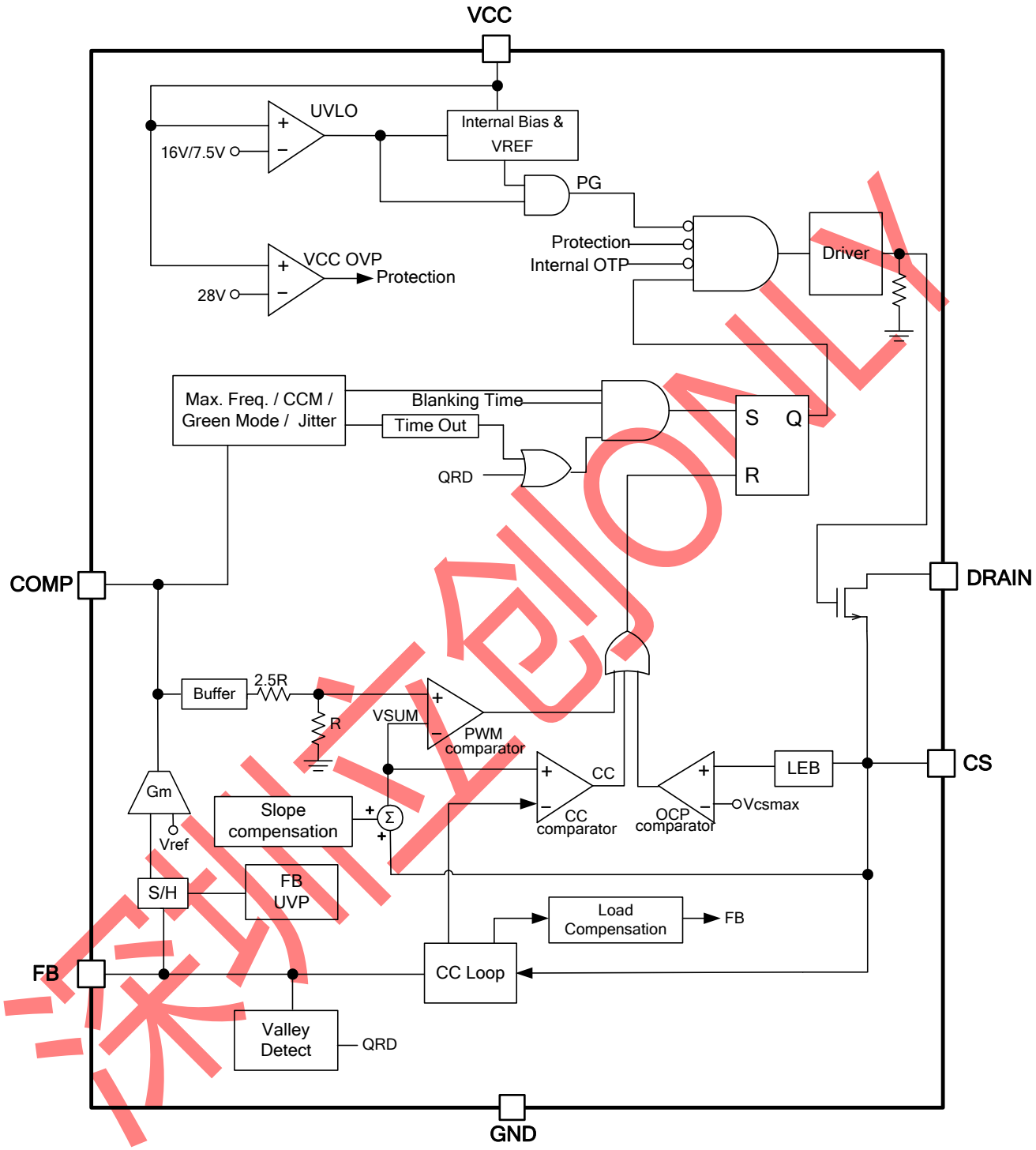
Note:

- Not to exceed the maximum junction temperature of the IC, this relates to the operating power of the IC and the thermal resistance of the IC-package as above.
- The small signal components should be placed to IC pin as possible.
- It’s essential to connect VCC pin with a SMD ceramic capacitor (0.1μF) to filter out the undesired switching noise for stable operation.
- Suggest using electrolytic capacitor or 1206 SMD ceramic capacitor as the VCC capacitor to avoid the acoustic noise from MLCC piezoelectric effect.
- Connecting a capacitor to COMP pin is also essential to filter out the undesired switching noise for stable operation.

Protection Mode

CCM Switching Frequency	FB UVP	VCC OVP
65kHz	Auto recovery	Auto recovery

Block Diagram



Electrical Characteristics (TA = +25℃ unless otherwise stated, VCC = 15.0V)

Parameter		Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE (VCC Pin)					
Startup current VCC=UVLO ON-0.2V	Ivcc_st		1.5	2	uA
Operating current (with 1nF load on OUT pin), Vcomp = 0V	Ivcc0		0.65		mA
Operating current (with 1nF load on OUT pin), Vcomp = 2.5V	Ivcc25		1.4		mA
Operating current (with 1nF load on OUT pin), protection tripped (VCC OVP, FB UVP)	Ivccpro		0.42		mA
UVLO-OFF	$UVLO_{\_off}$	7	7.5	8	V
UVLO-ON	$UVLO_{\_on}$	15	16.0	17	V
OVP level on VCC pin	VCCOVP	27	28	29	V
OVP level on VCC pin Debounce Time*			128		μs
VOLTAGE FEEDBACK (COMP Pin)					
Open loop voltage, COMP pin open	$Vcomp_{open}$		4.1		V
Maximum Frequency Threshold*	V_{SG1}		1.5		V
Green Mode Threshold*	V_{SG2}		1.0		V
PFM Mode Threshold*	V_{SP1}		0.8		V
Minimum Frequency Threshold*	V_{SP2}		0.1		V
CURRENT SENSING (CS Pin)					
Maximum input voltage at Low Line, Vcsmax	V_{csmax}		0.85		V
Maximum input voltage at High Line, VcsmaxL	V_{csmax_L}		0.7		V
Mini Vcs,off, (Vcomp<0.35V)	V_{csmin}		0.16		V
Leading-edge blanking time	TLEB		350		ns
Input impedance*		1			MΩ
FB (FB Pin)					
Upper Clamp Level, IZCD=0.5mA	FB_HC		4.6		V
Lower Clamp Level, IZCD=-0.3mA	FB_LC		-0.3		V
QRD Blanking Time*	T_{BLANK}		3		μs
Mini Sample Delay Time*	T_{sample_min}		1.5		μs
FB UVP Level	V_{FBUVP}	0.9	1	1.1	V
FB UVP De-bounce Time after start-up*			8		ms

Electrical Characteristics (T_A = +25℃ unless otherwise stated, VCC = 15.0V)

Parameter		Min.	Typ.	Max.	Unit
Error Amplifier					
Reference Voltage	Vref	2.465	2.5	2.535	V
Transconductance*	Gm		100		μs
OSCILLATOR					
CCM Frequency	$F_{CCM-Mean}$	60	65	70	kHz
Maximum Frequency Clamp, Vcomp>V_{SG1}*	F_{max}		69		kHz
Green Mode Frequency	F_g		25		kHz
Minimum Frequency	F_{min}		0.4		kHz
Jitter Frequency (CCM, Vcomp>Vs_{G1})*			±6		%
Soft Start Time (CS Pin)					
Soft Start Time*			8		ms
Internal OTP (Guaranteed by design)					
OTP*			145		℃
Hysteresis*			30		℃
MOSFET SECTION					
BVdss Vgs=0		650			V
Rds (on)			5		Ω

*Guaranteed by Design.

Typical Performance Characteristics

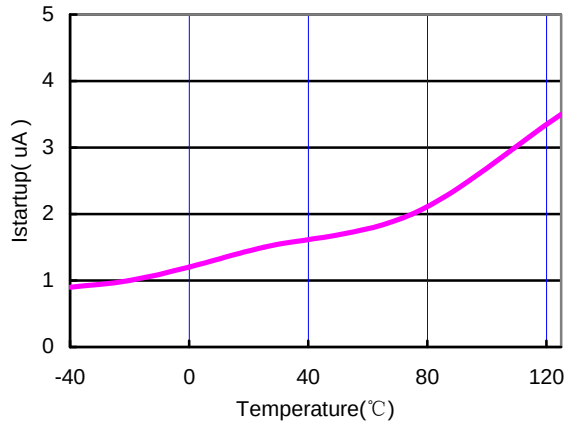


Fig. 1 Istartup current vs. Temperature

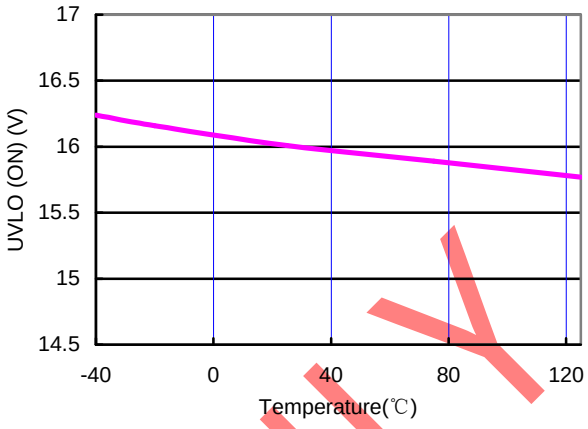


Fig. 2 UVLO (ON) vs. Temperature

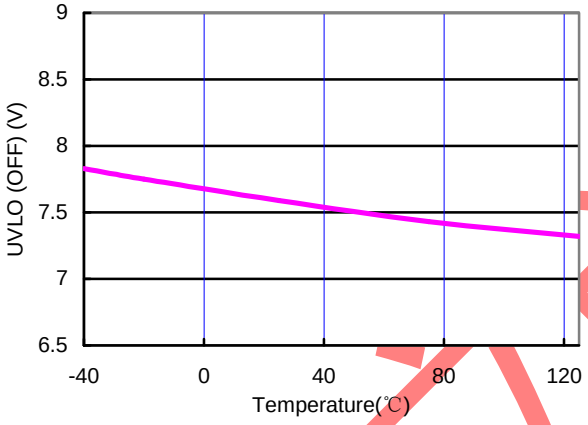


Fig. 3 UVLO (OFF) vs. Temperature

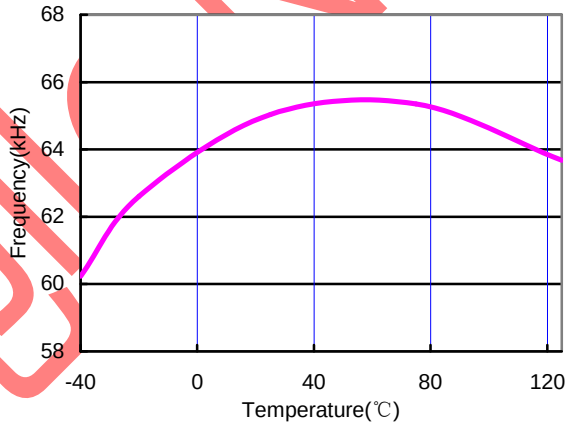


Fig. 4 CCM Frequency vs. Temperature

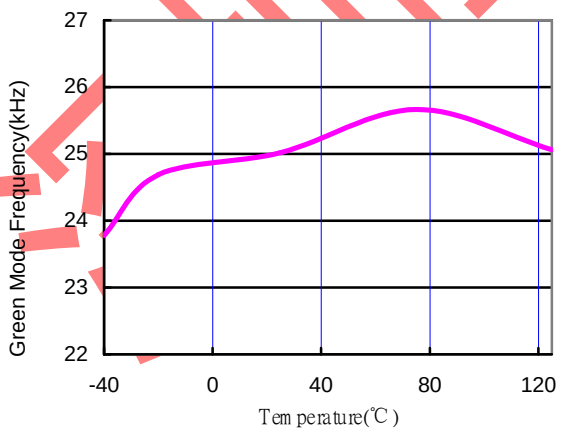


Fig. 5 Green Mode Frequency vs. Temperature

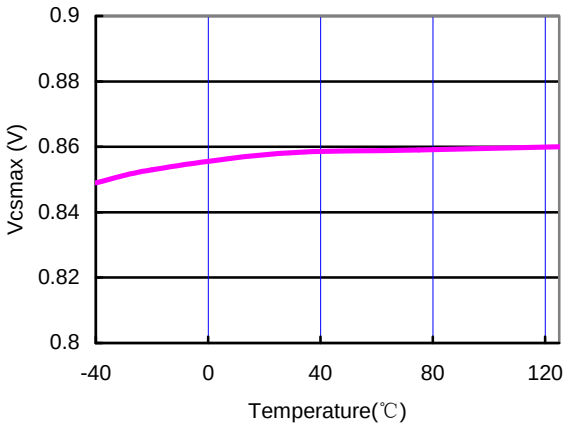


Fig. 6 Vcsmax vs. Temperature

Typical Performance Characteristics

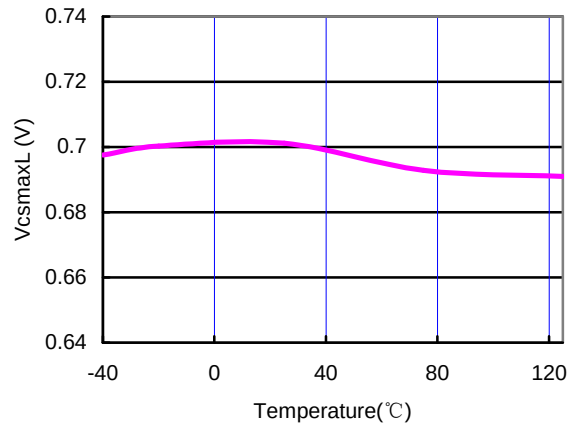


Fig. 7 VcsmaxL vs. Temperature

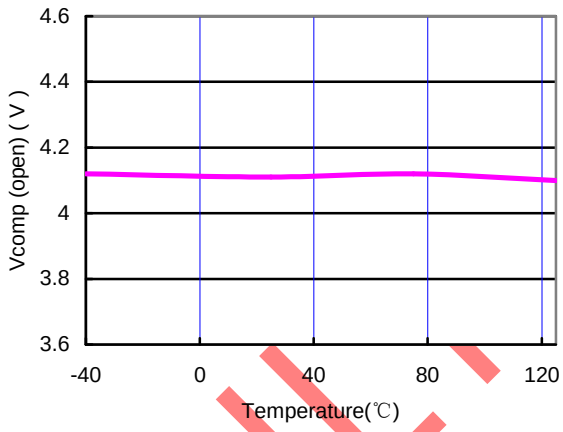


Fig. 8 Vcomp open loop voltage vs. Temperature

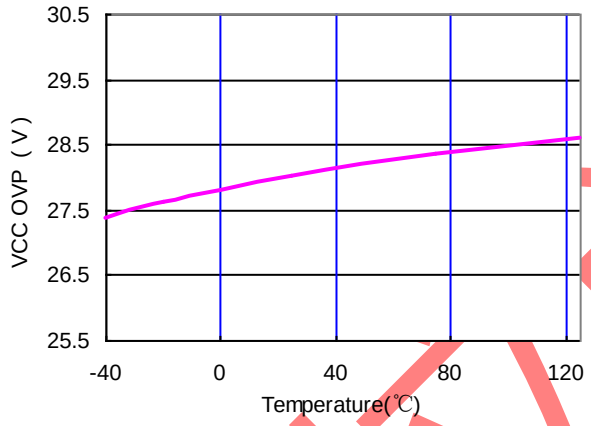


Fig. 9 Vref vs. Temperature

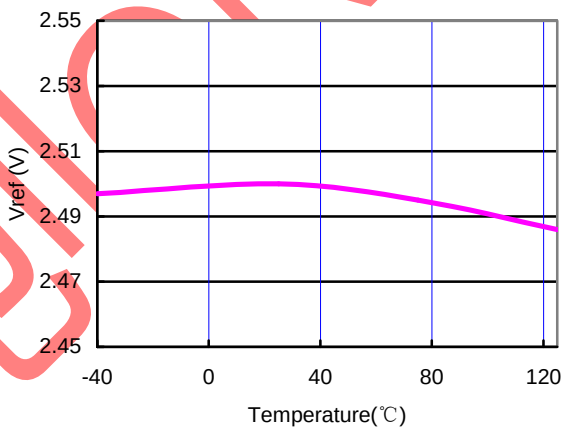


Fig. 10 VCC OVP vs. Temperature

Application Information

Overview

The GR9210RL integrates a high performance multi-mode (QR/CCM) primary side feedback controller and a high voltage power MOSFET of 650V. This results in a low-cost solution for low power AC/DC adapters. It integrated more functions to reduce the external components counts and the size. Its major features are described as below.

Start-up Current

The typical start-up current is 1.5uA. Very low start-up current allows the PWM controller to increase the value of start-up resistor and then reduce the power dissipation on it.

Under-voltage Lockout (UVLO)

A hysteresis UVLO comparator is implemented in GR9210RL, then the turn-on and turn-off thresholds level are fixed at 16V and 7.5V respectively. This hysteresis shown in Fig.13 ensures that the start-up capacitor will be adequate to supply the chip during start-up.

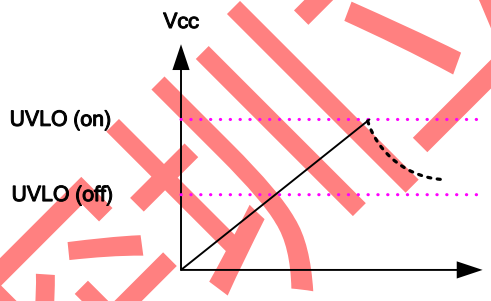


Fig.13

Multi-Mode Operation for High Efficiency

GR9210RL is a multi-mode QR/CCM controller. The controller changes the mode of operation according to switching frequency and comp pin voltage, as shown in the Fig.14. At the normal operating condition, the IC operates in QR mode to reduce the switching loss. In the QR mode, the frequency varies depending on the line voltage and the load conditions. As the output load current is increased, the on-time T_{ON} is increased, and thus the switching frequency decreases. If the switching frequency lowers than 65kHz frequency, the controller adaptively transitions to a CCM mode. Thus, small size transformer can be used with high power conversion efficiency.

As the output load current is decreased, the on-time T_{ON} is decreased, and thus the switching frequency increases. If the switching frequency increases till over the clamp of 69kHz, IC will skip the first valley to turn on in 2nd or 3rd valley.

At light load conditional, the VCOMP is lower than V_{SG1} and the system operates in green mode for high power conversion efficiency. The max switching frequency clamp will start to linearly decrease from 69kHz to 25kHz. The valley switching characteristic is still preserved in green mode. That is, when load decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced.

At zero load or very light load conditions (Vcomp< PFM mode voltage), the max switching frequency clamp will linearly decrease from 25kHz to 0.4kHz, enhancing power saving.

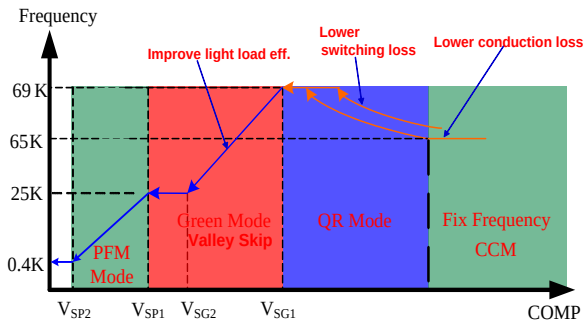


Fig.14

Quasi-Resonant Detection

The QR detection block will detect auxiliary winding voltage to turn on the MOSFET. The time-out generates a MOSFET turn-on signal as the driver output drops to low level for more than 150μs (Time Out) with the falling edge of the driver output.

Leading-edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike will inevitably occur at the sense resistor. To avoid fault trigger, a leading-edge blanking time is built in. During this blanking period, the current-limit comparator is disabled and cannot switch off the gate driver.

Internal Slope Compensation

A built-in slope compensation circuit is constructed in GR9210RL. When the switch is on, a ramp voltage is added to the sensed voltage across the CS pin, which helps to stabilize the system and prevent sub-harmonic oscillations.

Constant Voltage Operation

GR9210RL senses the auxiliary winding on the primary-side to regulate the output voltage, as shown in the Fig. 15. The auxiliary winding voltage is a reflection of the output voltage while the MOSFET is in off state. Via a resistor divider connected between the auxiliary winding and FB pin, the auxiliary voltage is sampled after the sample delay time and will be hold until the next sampling period. The internal error amplifier compares the sampled voltage with an internal reference V_{ref} (2.5V) and the error will be amplified. The error amplifier output COMP controls the duty cycle to regulate the output voltage, thus constant output voltage can be achieved. The output voltage is given as:

$$V_{out} = 2.5\left(1+\frac{Ra}{Rb}\right)\left(\frac{N_s}{N_a}\right) - V_F$$

Where V_F indicates the drop voltage of the output diode, Ra and Rb are top and bottom feedback resistor value, Ns and Na are the turns of transformer secondary and auxiliary. The leakage inductance of transformer will induce ringing to affect output regulation. To optimize the snubber circuit will minimize the high frequency ringing and achieve the best regulation.

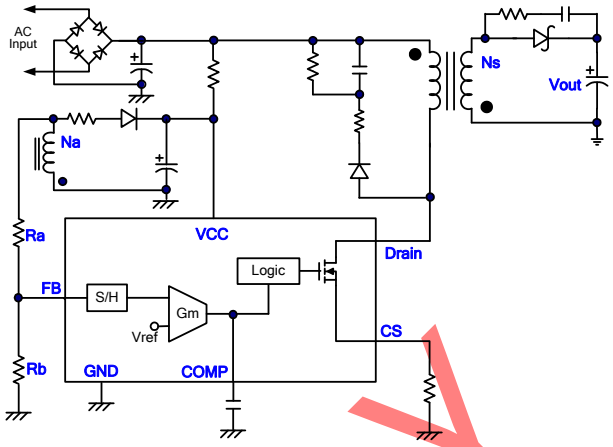


Fig.15

Load Regulation Compensation

In GR9210RL, the load regulation compensation is implemented to achieve good voltage regulation. An offset voltage is generated at FB pin by an internal current flowing into the resister divider. The internal sink current source is proportional to the value of load current. It can also be programmed by adjusting the resistance of the voltage divider to compensate the drop for various cable lines used.

Over-voltage Protection (OVP) on VCC Auto Recovery mode

To prevent power MOSFET from being damaged, the GR9210RL is implemented an OVP function on VCC. When the VCC voltage is higher than the OVP threshold voltage, the output gate driver circuit will be shut down immediately to stop the switching of power MOSFET. The VCC OVP function is an auto-recovery type protection. If OVP happens, the pulses will be stopped and recover at the next UVLO on. The GR9210RL is working in a hiccup mode as shown in Fig. 16.

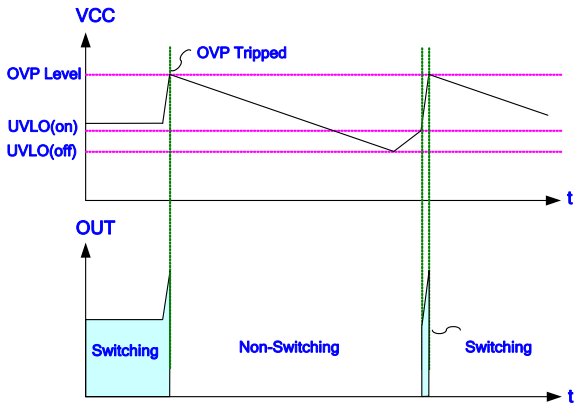


Fig.16

Output Under-voltage Protection (UVP) on FB–

Auto Recovery mode

To protect the circuit from damage due to output short condition, an auto-recovery type of UVP protection is implemented for it. If the FB voltage declines below 1V for over the 8ms, the protection will be activated to turn off the gate until the next UVLO-ON.

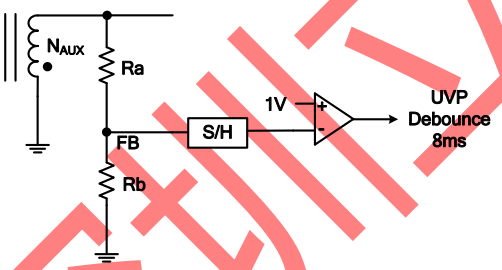


Fig.17

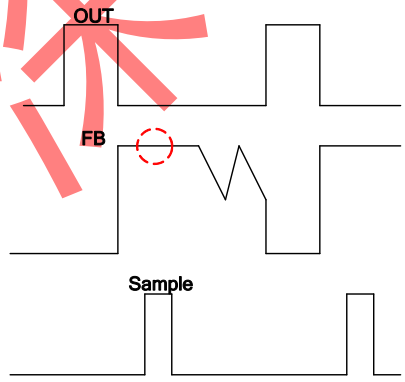


Fig.18

FB Pin Short Protection– Auto Recovery mode

To protect the circuit from damage due to FB short condition, an auto-recovery type of FB short protection is implemented for it. Since the FB pin voltage is clamped at 0 V when the MOSFET is turned on. The FB pin current is used for FB short protection. When the FB is shorted over the 4 switching cycles, FB short protection is triggered.

Gate Clamp/Soft Driving

Driver output is clamped by an internal 13.5V clamping circuit to prevent from undesired over-voltage gate signals. And under the conditions listed below, the gate output will turn off immediately to protect the power circuit. The GR9210RL also has soft driving function to minimize EMI.

Fault Protection

There are several critical protections integrated in the

. CS pin floating

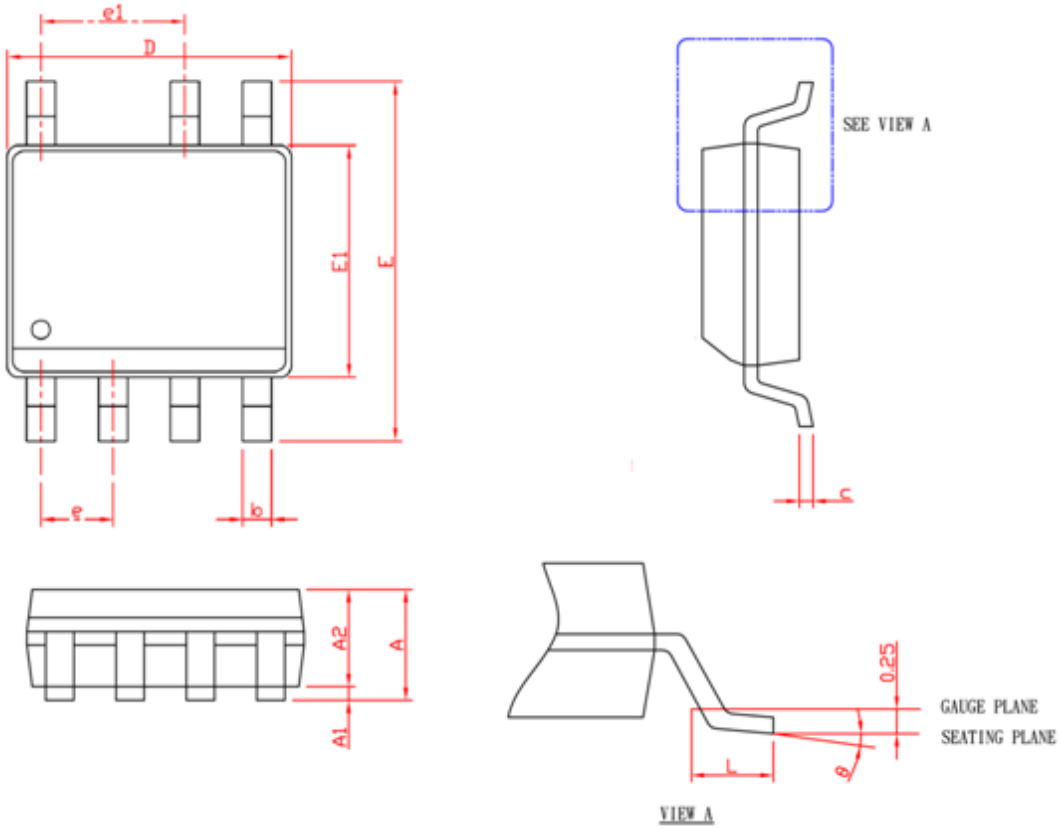
. FB pin shorting (Rb shorting)

. FB pin Open (Ra and Rb Open)

. Ra Open

Package Information

SOP-7



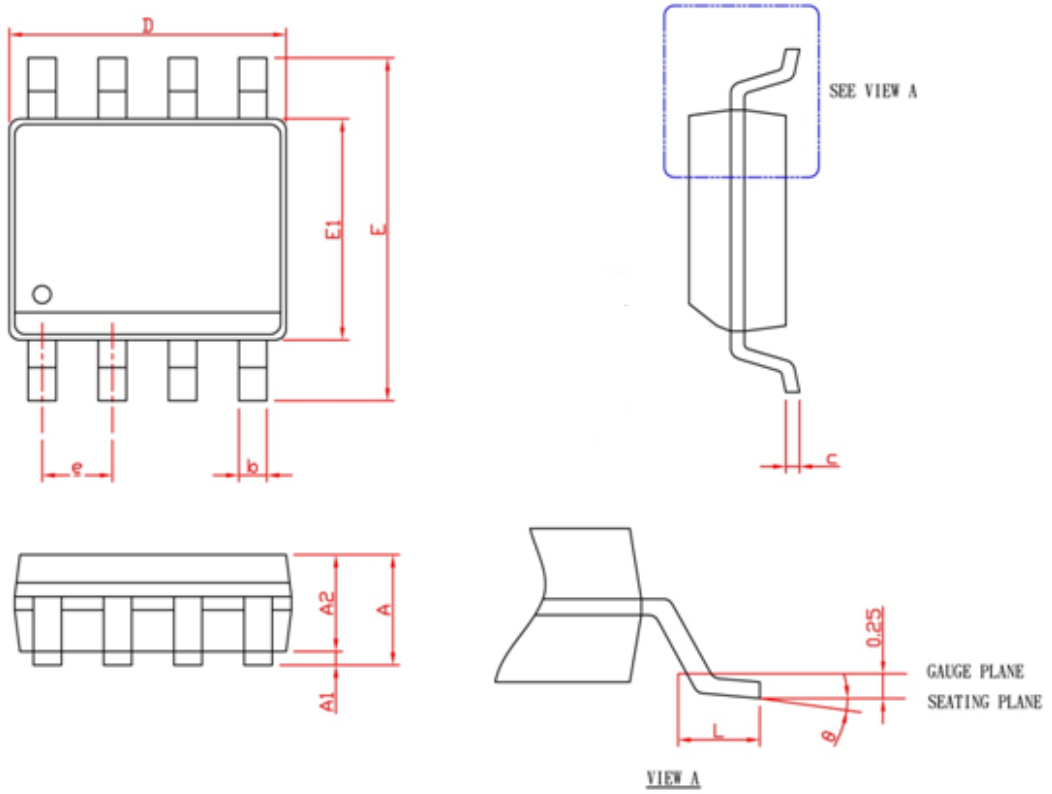
SYMBOL	SOP-7	
	MILLIMETERS	
	MIN.	MAX.
A		1.75
A1	0.10	0.25
A2	1.25	
b	0.31	0.51
c	0.10	0.25
D	4.70	5.10
E	5.80	6.20
E1	3.70	4.10
e	1.27 BSC	
e1	2.54 BSC	
L	0.40	1.27
θ	0^o	8^o

Note: 1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

2. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

SOP-8



SYMBOL	SOP-8	
	MILLIMETERS	
	MIN.	MAX.
A		1.75
A1	0.10	0.25
A2	1.25	
b	0.31	0.51
c	0.10	0.25
D	4.70	5.10
E	5.80	6.20
E1	3.70	4.10
e	1.27 BSC	
L	0.40	1.27
θ	0^o	8^o

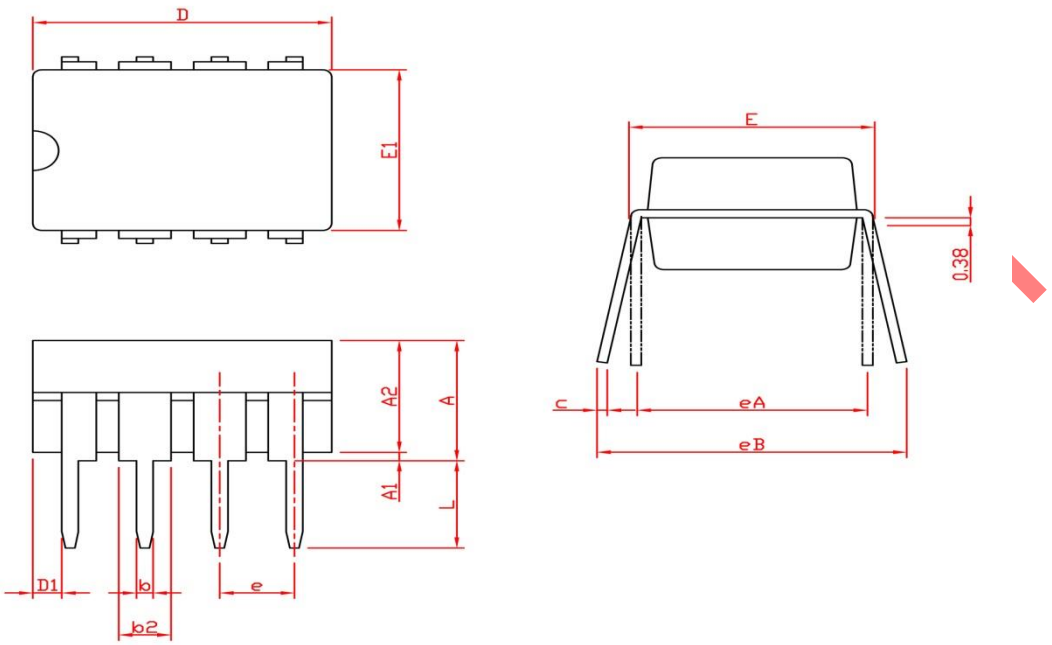
Note: 1. Followed from JEDEC MS-012 AA.

2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

DIP-8



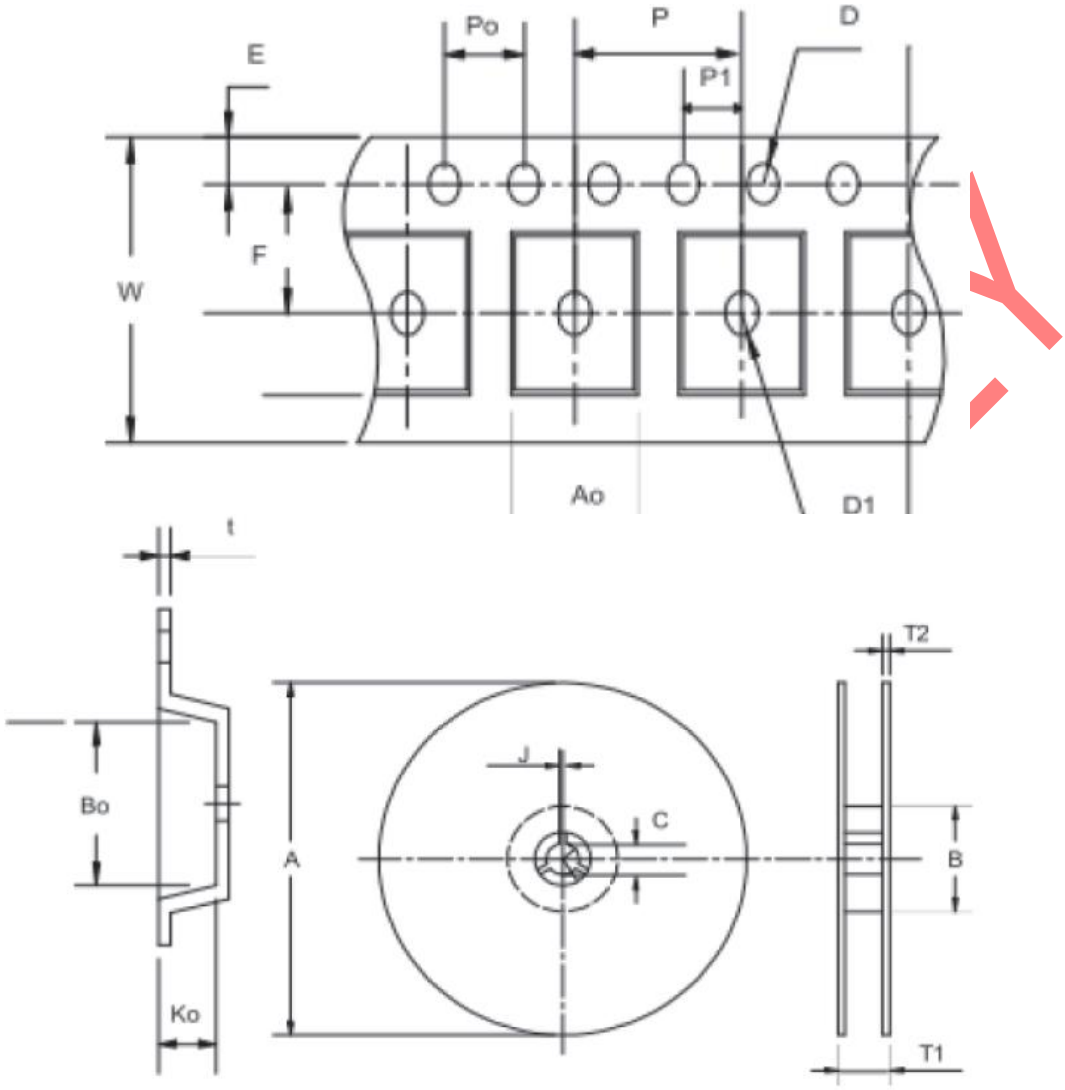
SYMBOL	DIP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
c	0.20	0.35	0.008	0.014
D	9.01	10.16	0.355	0.400
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
Ea	7.62 BSC		0.300 BSC	
Eb		10.92		0.430
L	2.92	3.81	0.115	0.150

Note: 1. Followed from JEDEC MS-001 BA.

2. Dimension D, D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 10 mil.

Carrier Tape & Reel Dimensions

SOP- 7/8



PKG TYPE	W	E	F	P0	A0	P	P1	B0	K0	A	B	T1
SOP-7/8/8P	12±0.3	1.75±0.1	5.5±0.05	4±0.1	6.4±0.2	8±0.1	2±0.2	5.2±0.2	2.1±0.2	330±2	50min	12.4+2/-0

Devices Per Unit

Application	Carrier Width	Devices Per Reel
SOP- 7/8	12	2500

Tape and Specification Reel

SOP-7/8