

CAMERA MOD Optical Image Stabilizer for Mobile Phones

Lens Driver for **Optical Image Stabilizer**

BU63163GWL

General Description

The BU63163GWL is an IC that has a built-in PWM/BTL driver bridge 2.5ch. Low power consumption OIS function is achieved by using DSP method. Furthermore, PWM Frequency adjustment is enabled by built-in PLL, and, small area implementation for Camera Mod for mobile phones is supported by CSP.

Features

- Programmable DSP Control System
- 2wire and 4wire Serial Interface
- PWM/Analog BTL Driver for OIS Actuator X,Y Axis and Focus
- Support for Digital Gyroscope
- Variable Current Source (6bit) for Hall Sensor Drive
- Gain Adjustment for Hall Sensor
- 4 Levels Tunable Slew Rate for PWM Drive
- **Clock Detection**
- Thermal Shut Down (TSD), Under Voltage Locked Out (UVLO) and Over Current Protection (OCP)
- PLL Circuit

Application Circuit

LDO for Digital Voltage Source

Key Specifications

Control Supply Voltage (AVDD): 27 to 261/

_	control capping voltage (/ WBB).	2.7 10 3.00
	Motor Supply Voltage (VM)	
	PWM driven:	2.3 to 4.8V
	BTL driven:	1.75 to 4.8V
	Stand-by Current:	1uA(Max.)
	Operating Frequency:	27MHz(Typ.)
	H-bridge Output Current:	200mA(Max.)
	Output ON Resistance:	1.8Ω(Typ.)

Package UCSP50L2

(Typ.) (Typ.) (Max.) 2.30mm x 2.30mm x 0.55mm

Application

CAMERA MOD for Mobile Phones

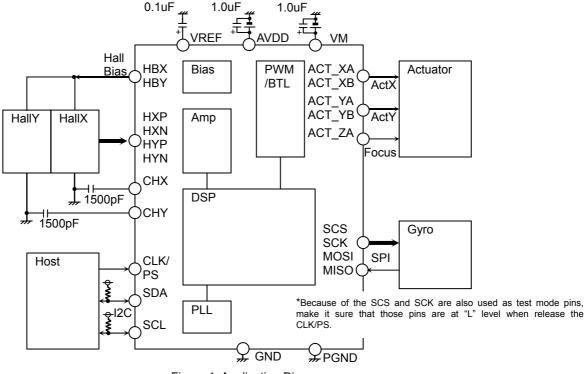


Figure 1. Application Diagram

OProduct Structure : Silicon Monolithic Integrated Circuit OThis product is not designed for protection against radioactive rays.

Terminal Assignment [Bottom View]

	1	2	3	4	5
E	ACT_ YA	ACT_ YB	ACT_ XA	ACT_ XB	PGND
D	SCK	MISO	SCS	MOSI	VM
С	HXP	HXN	HYP	SCL	ACT_ ZA
В	НВХ	HBY	HYN	SDA	CLK/ PS
A	СНХ	СНҮ	VREF	AVDD	GND

Figure 2. Terminal Assignment

Package Outline

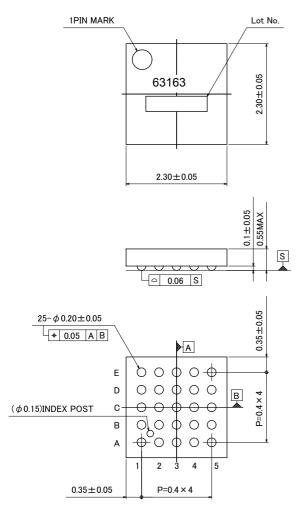
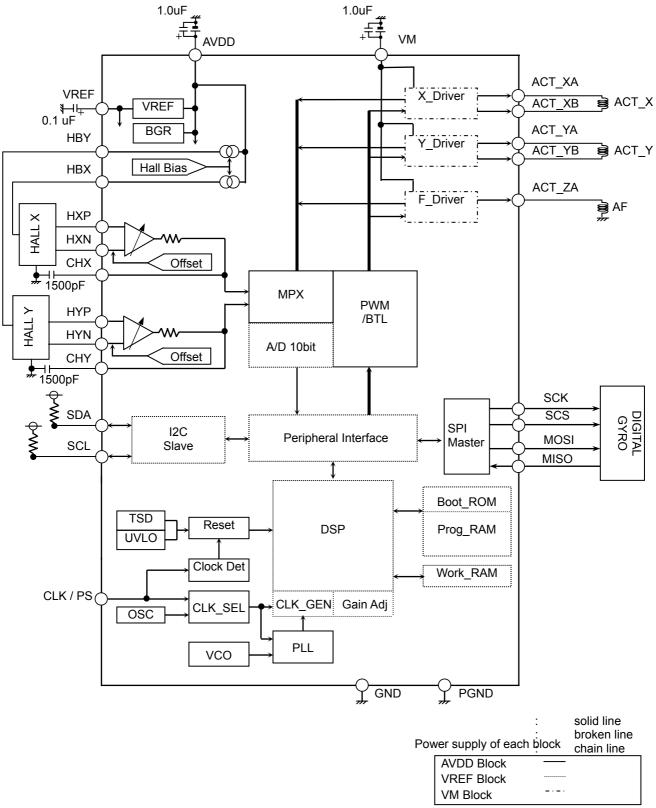


Figure 3. Package Outline (Unit:mm)

erminal No.	& Terminal N	Name
Terminal No.	Terminal Name	Function
A1	СНХ	Capacitor Connection for X Axis Hall Sensor
A2	CHY	Capacitor Connection for Y Axis Hall Sensor
A3	VREF	Capacitor Connection for Internal Reference Voltage
A4	AVDD	Analog Power Supply Input
A5	GND	Ground Terminal
B1	НВХ	Current source Output for X Axis Hall Sensor
B2	HBY	Current Source Output for Y Axis Hall Sensor
B3	HYN	Y Axis Hall Sensor Input -
B4	SDA	2wire Serial Data Input Output Pin
B5	CLK/PS	EXTCLK Terminal / Power Save Input
C1	HXP	X Axis Hall Sensor Input +
C2	HXN	X Axis Hall Sensor Input -
C3	HYP	Y Axis Hall Sensor Input +
C4	SCL	2wire Serial Clock Input Output Pin
C5	ACT_ZA	Current Output for Focus Driver
D1	SCK	4wire Serial Clock Output Pin
D2	MISO	4wire Serial Data Input Pin
D3	SCS	4wire Serial Chip Selection Output Pin
D4	MOSI	4wire Serial Data Output Pin
D5	VM	Motor Power Supply Input
E1	ACT_YA	Output for Y Axis Drive +
E2	ACT_YB	Output for Y Axis Drive -
E3	ACT_XA	Output for X Axis Drive +
E4	ACT_XB	Output for X Axis Drive -
E5	PGND	Motor Ground Terminal

Block Diagram





Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Analog Supply Voltage	AVDD	-0.3 to +7.0	V
Motor Supply Voltage	VM	-0.3 to +7.0	V
Output Voltage	VOUT	-0.3 to +7.0	V
Control Input Voltage 1 (CLK/PS,MISO)	VIN1	-0.3 to +7.0	V
Control Input Voltage 2 (SCL,SDA)	VIN2	-0.3 to +7.0	V
Power Dissipation	Pd	810 *1	mW
Operating Temperature Range	Topr	-30 to +85	°C
Junction Temperature	Tjmax	+125	°C
Storage Temperature	Tstg	-50 to +125	°C
X/Y-axis Driver Output Current	IXY	-200 to +200 *2	mA/ch
Focus Driver Output Current	IFO	-200 to +200 *2	mA/ch
Motor Supply Current	IM	-600 to +600 *2	mA

*1 Reduced by 8.1m W/°C over 25°C, when mounted on a glass epoxy 8-layer board. (50mm×58mm×1.75mm) *2 Do not exceed Pd, ASO, and Tjmax=125°C

Operating Conditions(Ta= -30 to +85°C)

Parameter	Symbol	Limit	Unit
Analog Supply Voltage	AVDD	2.7 to 3.6	V
Motor Supply Voltage	VM	2.3 to 4.8 *3	V
X/Y-axis Driver Output Current (max)	lout1	±200 *4	mA/ch
Focus Driver Output Current (max)	lout2	+100 *4	mA/ch
2wire Serial Interface Frequency	FSCL	0 to 400	kHz
CLK/PS Input Frequency	FCLK	4 to 30	MHz

*3 Operates until minimum of 1.75 V when BTL driven
*4 Do not exceed Pd, ASO, and Tjmax=125°C

Electrical Characteristics (Unless otherwise specified Ta=+25°C, VM=3.0V, AVDD=3.0V)

Parameter	neter Symbol Limit			Conditions		
	Symbol	Min	Тур	Max	Unit	Conditions
Circuit current						
Stand-by Analog Current	IST_A	-	0	1	μA	PS=0V
Stand-by Driver Current	IST_M	-	0	1	μA	PS=0V
Analog Circuit Current	ICC_A	-	5.5	9.0	mA	PS=AVDD
Driver Circuit Current	ICC_M	-	0.2	0.4	mA	PS=AVDD
Control Input 1 (CLK/PS)						
High-level Input Voltage 1	VIH1	1.19	-	AVDD	V	
Low-level Input Voltage 1	VIL1	0	-	0.50	V	
High-level Input Current 1	IIH1	20	30	40	μA	VIN1=3.0V
Low-level Input Current 1	IIL1	-3	0	3	μA	VIN1=0V
Control Input 2 (SCL,SDA)						
High-level Input Voltage 2	VIH2	1.19	-	AVDD	V	
Low-level Input Voltage 2	VIL2	0	-	0.50	V	
Low-level Output Voltage 2	VOL2	0	-	0.40	V	IIN=+3.0mA
High-level Input Current 2	IIH2	-3	0	3	μA	VIN2=1.8V
Low-level Input Current 2	IIL2	-3	0	3	μA	VIN2=0V
Clock Detection						
Frequency of Detection	FIN	4	-	30	MHz	
Input Clock Duty Cycle	DCY	40	-	60	%	
UVLO			·	·		·
UVLO Voltage	UVLO	2.30	-	2.65	V	

Electrical Characteristics (Unless otherwise specified Ta=+25°C, VM=3.0V, AVDD=3.0V)

Parameter	Symbol	Symbol			Unit	Conditions	
Falameter	Symbol	Min	Тур	Max	Unit	Conditions	
Driver of X/Y Axis							
Output ON Resistance	RONXY	-	1.8	-	Ω	Upper & Lower total	
PWM Output Frequency	FPWM XY	-	500	-	kHz	CLK/PS =6.75MHz DIV_N=269d, DIV_M=1279d Ch* FSEL=0d(*=X,Y)	
BTL Voltage 1	VBTL XY1	-	1.5	-	V	VM=1.8V Ch*_DAT= 213d (*=X,Y)	
BTL Voltage 2	VBTL XY2	-	0.3	-	V	VM=1.8V Ch*_DAT= 349d (*=X,Y)	
Focus Driver							
Output ON Resistance	RONFO	-	1.8	-	Ω	Upper & Lower total	
PWM Output Frequency	FPWM FO	-	500	-	kHz	CLK/PS =6.75MHz DIV_N=269d, DIV_M=1279d ChZ FSEL=0d	
BTL Voltage 1	VBTL FO1	-	1.5	-	V	VM=1.8V ChZ_DAT= 213d	
BTL Voltage 2	VBTL FO2	-	0.3	-	V	VM=1.8V ChZ_DAT= 349d	
Output Current	IOFO	92	100	108	mA	when set to 100mA	
SPI terminal (SCK*5, SCS*5, M	ISO, MOSI)						
SCK Output Frequency	FSPI	6.08	6.75	7.43	MHz	When Divided by 4 (SPICK = 3d)	
High-level Input Current	IIHS	20	30	40	μA	*5	
Low-level Input Current	IILS	-3	0	3	μA		
High-level Input Voltage	VIHS	0.7*AVDD	-	AVDD	V		
Low-level Input Voltage	VILS	0	-	0.3*AVDD	V		
High-level Output Voltage	VOHS	0.8*AVDD	-	AVDD	V		
Low-level Output Voltage	VOLS	0	-	0.2*AVDD	V		

*5 SCS and SCK pins are pulled down by 12.5k Ω when CLK/PS=L.

Characteristics of the SDA and SCL Bus Lines for 2- wire Serial Interface (Unless otherwise specified Ta=25°C, VM=3.0V, AVDD=3.0V)

Parameter	Currents al	FAST-MODE*6			STANDARD-MODE*6			1.1
Parameter	Symbol	Min	Тур	Max	Min	Тур	Max	Unit
SCL clock frequency	fSCL	-	-	400	-	-	100	kHz
High Period of the SCL clock	tHIGH	0.6	-	-	4.0	-	-	μs
Low Period of SCL clock	tLOW	1.3	-	-	4.7	-	-	μs
Rise time of SDA / SCL	tR	-	-	0.3	-	-	1.0	μs
Fall time of SDA / SCL	tF	-	-	0.3	-	-	0.3	μs
Hold time (repeated) START condition	tHD:STA	0.6	-	-	4.0	-	-	μs
Setup time (repeated) START condition	tSU:STA	0.6	-	-	4.7	-	-	μs
Data hold time	tHD:DAT	0	-	0.9	0	-	3.45	μs
Data setup time	tSU:DAT	100	-	-	250	-	-	ns
Setup time for STOP condition	tSU:STO	0.6	-	-	4.0	-	-	μs
Bus free time between a STOP and START condition	tBUF	1.3	-	-	4.7	-	-	μs
Pulse width of spikes which must be suppressed by the input filter	tl	0	-	50	0	-	50	ns

*6 STANDARD-MODE and FAST-MODE 2-wire serial interface devices must be able to transmit or receive at that speed

The maximum bit transfer rates of 100 kbit/s for STANDARD-MODE devices and 400 kbit/s for FAST-MODE devices

This transfer rates is provided the maximum transfer rates, for example it is able to drive 100 kbit/s of clocks with FAST-MODE.

Definition of Timing on the 2-wire Serial Interface

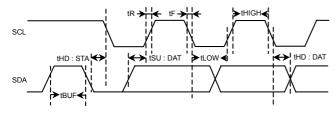


Figure 5. Definition of Timing for Serial Data

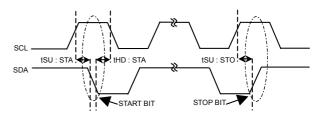


Figure 6. Definition of Timing for START and STOP bit

BU63163GWL have CLK STRETCHING, so I2C master should be corresponding.

Definition of Timing on the 4-wire Serial Interface

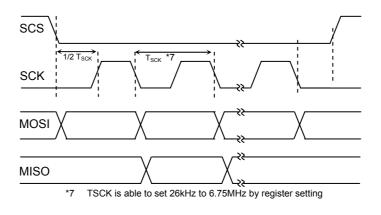


Figure 7. Serial Data Timing

SCK polarity and data lines' rising/falling timing for SCK is configurable

Starting Timing Chart

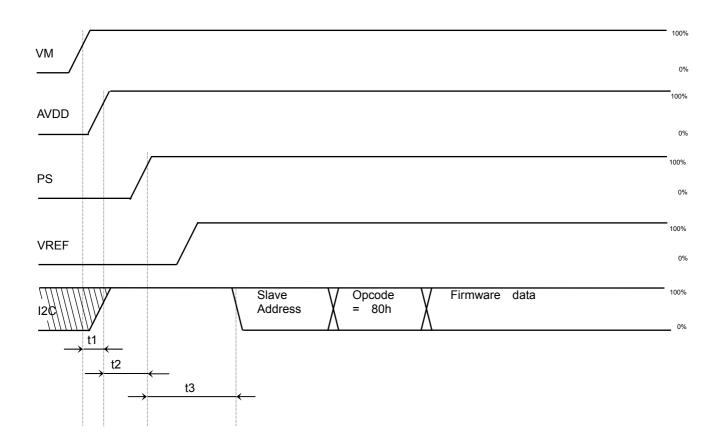


Figure 8. Start Sequence

Parameter	Symbol	MIN.	TYP.	MAX.	UNIT
Time from VM power supply to AVDD power supply	t1	0	-	-	μs
Time from AVDD power supply to PS release	t2	0	-	-	μs
Time from PS release to I2C input	t3	90	-	-	μs

To avoid current flow from the gyroscope to the BU63163GWL, be sure to set or tie the gyroscope power supply equal to AVDD and also start up both the gyroscope and BU63163GWL at the same time.

Memory Map

Peripheral Address Mapping

00h	Clock
07h	
08h	TRIANGLE
0Fh	
10h	I2C slave
17h	
18h	SPI master
1Fh	
20h	Monitor
27h	
28h	PWM
2Fh	
30h	A/D D/A
3Fh	
40h	reserved
5Fh	
60h	PLL
6Fh	
70h	reserved
FFh	

Work Memory of RSP Address Mapping

00h	for X-axis
6Fh	Focus
70h	Work , status
7Fh	
80h	for Y-axis
EFh	
F0h	Work , status
FFh	

Figure 9. Peripheral Memory Map

Figure 10. Work Memory Map

*Please refer to application note for details.

Structure of Download Program

MSB b7 b0 LSB						
+0	00h					
+1	CheckSum[15:8]					
+2	CheckSum[7:0]					
+3	00h					
+4	PRGSIZE[15:8]					
+5	PRGSIZE[7:0]					
+6	00h					
+7	Program+N-1[15:8]					
+8	Program+N-1[7:0]					
+9	Program+N-1[23:16]					
+3*(N-2)+4	Program+2[15:8]					
+3*(N-2)+5	Program+2[7:0]					
+3*(N-2)+6	Program+2[23:16]					
+3*(N-1)+4	Program+1[15:8]					
+3*(N-1)+5	Program+1[7:0]					
+3*(N-1)+6	Program+1[23:16]					
+3*N+4	Program+0[15:8]					
+3*N+5	Program+0[7:0]					
+3*N+6	Program+0[23:16]					



CheckSum>	CheckSum@Initial = 0x535A		
	CheckSum ^= { 8'b0, Program+n[23:16] } ^ Program+n[15:0]		

PRGSIZE --> N-1 (example of above)

Operational Notes

1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

2) Power supply terminals and lines

The VM power supply line for the H-bridge is not internally connected to the AVDD analog power supply line. Therefore, the VM, and AVDD lines can be driven at different voltages. Although these lines can be connected to a common power supply, do not open the power supply pin but connect it to the power supply externally.

Regenerated current may flow as a result of the motor's back electromotive force. Insert capacitors between the power supply and ground terminals to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may lose some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and ground terminals.

For this IC with 2 power supplies and a part consists of the CMOS block, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays, and to the unstable internal logic, respectively. Therefore, give special consideration to power coupling capacitance, width of power and ground wirings, and routing of wiring.

3) Ground terminals and lines

Ensure a minimum GND terminal potential in all operating conditions. Make sure that no terminals are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.

The motor ground PGND and the small signal ground GND are not internally connected to each other. When using both small signal GND and large current PGND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

4) Thermal design

Use a thermal design that allows for a sufficient margin regarding the power dissipation (Pd) in actual operating conditions.

5) Operating in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

6) ASO

When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO.

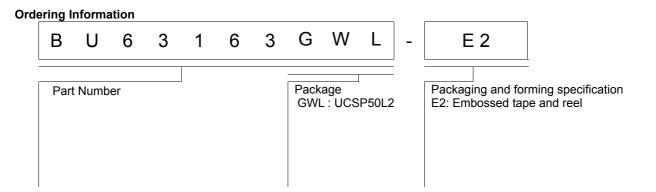
7) Thermal shutdown circuit

This IC incorporates a TSD (thermal shutdown) circuit. If the temperature of the chip reaches the following temperature, the motor output will be opened. The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

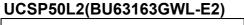
TSD ON temperature °C (Typ.)	Hysteresis temperature °C (Typ.)
150	25

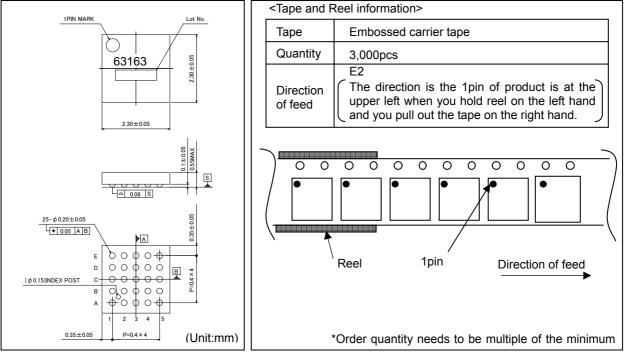
8) Application example

Although the application circuit is recommended for use, make sure to confirm the adequacy of the characteristics. When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.



Physical Dimension Tape and Reel Information





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 - [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
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- 6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- 7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
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- 9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- 2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of lonizer, friction prevention and temperature / humidity control).

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- 1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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 - [d] the Products are exposed to high Electrostatic
- 2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
- 3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
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