TPESD0504P
Low Capacitance TVS Diode Array

www.sot23.com.tw

Features

- Protects four I/O lines and one Vcc line
- Low capacitance
- Working voltages : 5V
- Low leakage current
- Response Time is < 1 ns
- Low capacitance (<1.2pF) for high-speed interfaces
- No insertion loss to 3.0GHz
- Solid-state silicon avalanche technology
- Meets MSL 1 Requirements
- IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- IEC61000-4-4 (EFT) 40A (5/50ns)
- IEC61000-4-5 (Lightning) 5A (8/20μs)

Mechanical Characteristics

- Package: DFN1616-6
- Lead Finish: Lead Free
- UL Flammability Classification Rating 94V-0

RoHS

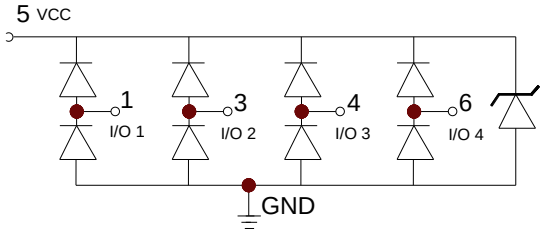
Applications

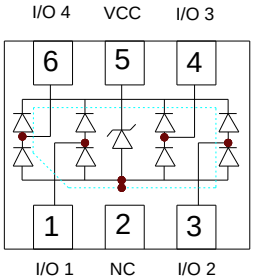
- Digital Visual Interface (DVI)
- 10/100/1000 Ethernet
- USB 1.1/2.0/OTG
- IEEE 1394 Firewire Ports
- Projection TV Monitors and Flat Panel Displays
- Notebook Computers
- Set Top Box
- Projection TV

Ordering Information

Part Number	Qty per Reel	Reel Size
TPESD0504P	3000	7″

Dimensions and Pin Configuration





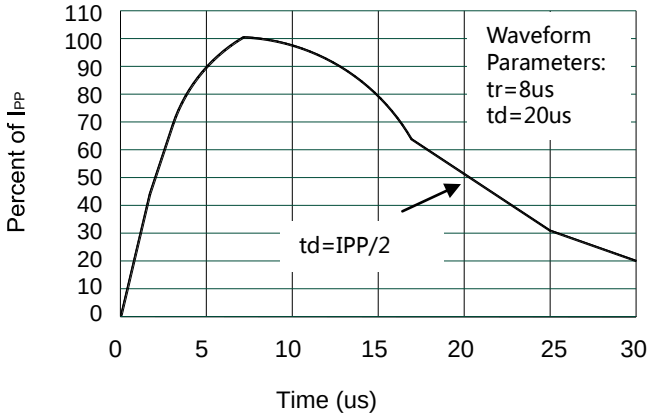
Absolute Maximum Ratings (Tamb=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (tp=8/20μs waveform)	P_{PPP}	150	Watts
Peak Pulse Current(tp=8/20μs waveform)	I_{PP}	5	A
ESD Rating per IEC61000-4-2: Contact Air		8 15	KV
Lead Soldering Temperature	T_L	260 (10 sec.)	℃
Operating Temperature Range	T_J	-55 ~ 150	℃
Storage Temperature Range	T_{STG}	-55 ~ 150	℃

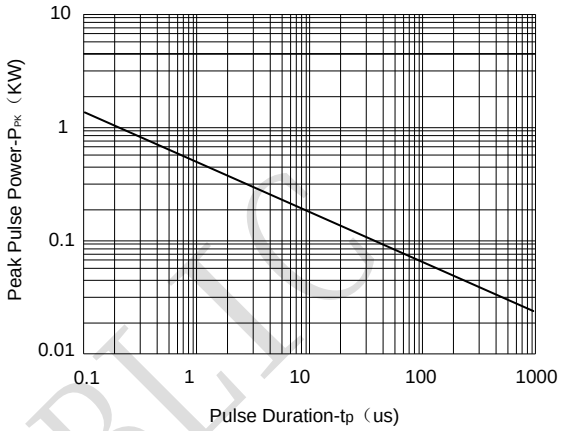
Electrical Characteristics (TA=25°C unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{RWM}	Reverse Working Voltage	Any I/O to Ground			5.0	V
V_{BR}	Reverse Breakdown Voltage	IT = 1mA, Any I/O to Ground	6.0			V
I_R	Reverse Leakage Current	V_{RWM} = 5V, Any I/O to Ground			1	μA
V_F	Diode Forward Voltage	IF = 15mA		0.85	1.2	V
V_C	Clamping Voltage	I_{PP} = 1A, tp =8/20μs, any I/O pin to Ground			15.5	V
		I_{PP} = 5A, tp =8/20μs, any I/O pin to Ground			30	V
I_{PP}	Peak Pulse Current	tp =8/20μs			5	A
C_J	Junction Capacitance	V_R = 0V, f = 1MHz, between I/O pins		0.6	0.8	pF
		V_R = 0V, f = 1MHz, any I/O pin to Ground		1.0	1.2	pF

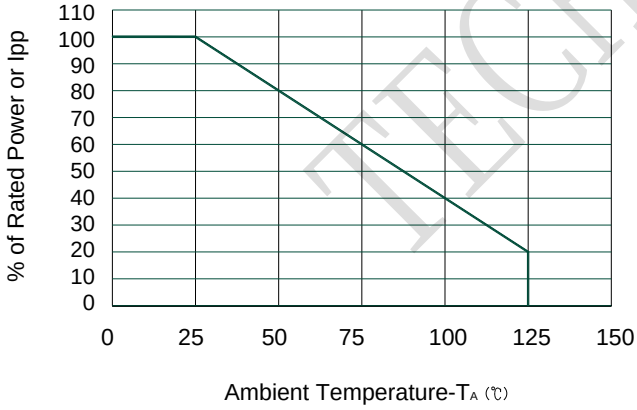
Typical Performance Characteristics (T_A=25°C unless otherwise Specified)



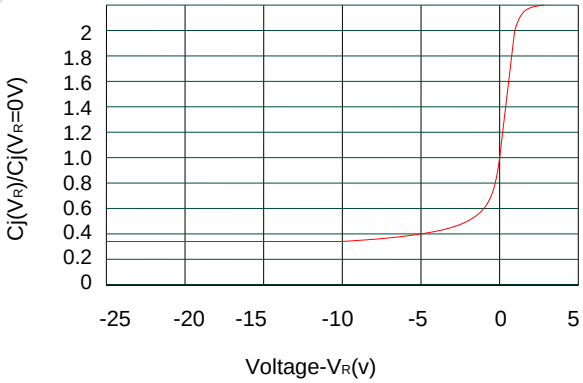
Pulse Waveform



Non-Repetitive Peak Pulse Power vs. Pulse Time

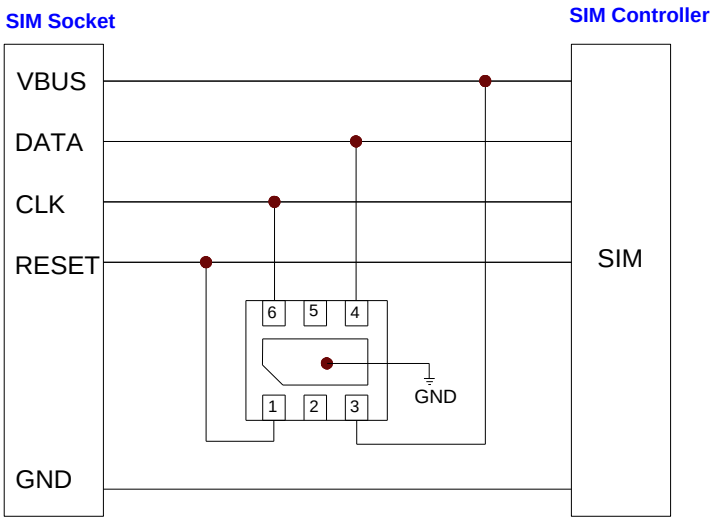


Power Derating Curve



Junction Capacitance vs. Reverse Voltage

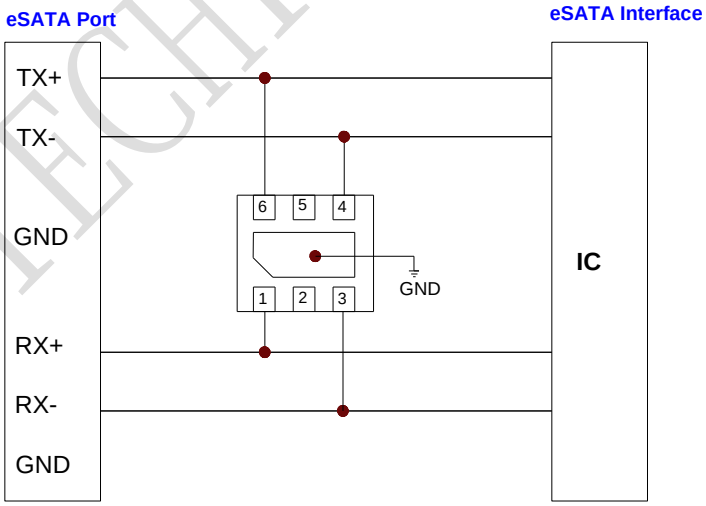
Typical applications



SIM protected solution

Considerations:

- The SIM (Subscriber Identification Module) card has 3 data lines that are low-speed and low-voltage
  - Given the low speed of the signals, the capacitance will not be a concern
- The low-voltage signal lines are best protected by a device which has a low standoff voltage or V_{RWM}
- Protection of the 3 data lines is shown below (i.e. CLK, DATA, and RESET)

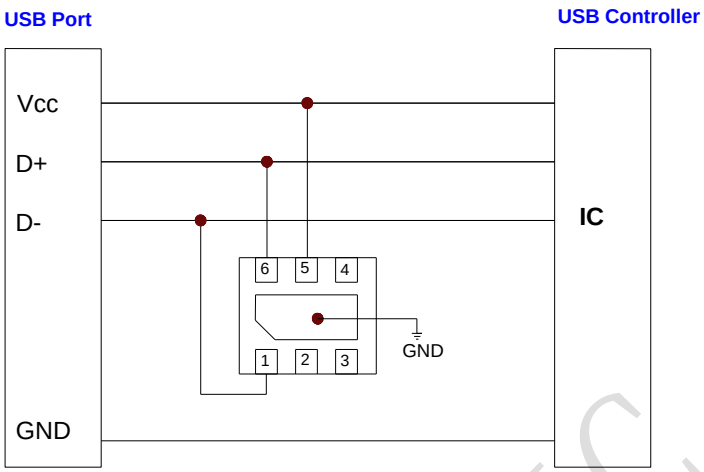


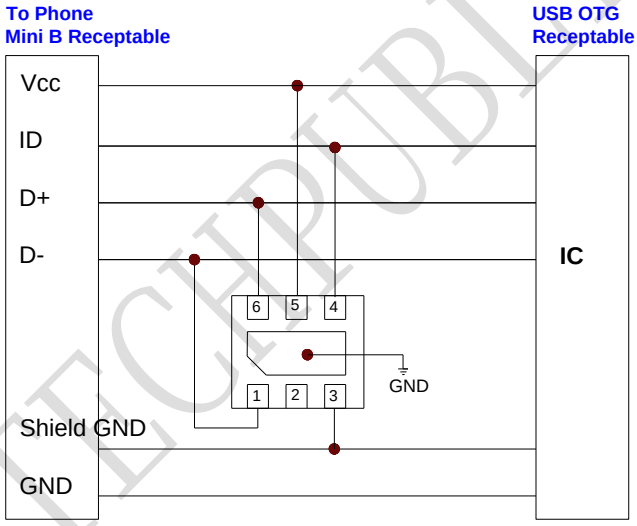
Considerations:

- eSATA is a subset of the SATA protocol that uses 2 differential pairs for communication
  - Four lines need to be protected per port (i.e. TX± and RX±)
  - Currently eSATA is capable of running raw data rates of 1.5Gbps (Gen 1) and 3.0Gbps (Gen 2)
- These high bus speeds require very low capacitance devices to prevent signal degradation
- To maintain the line impedance the designer should avoid using 90º angles and vias

Typical applications

USB2.0 Protection





USB OTG Carkit Protection

Considerations:

● Each port can operate up to 480Mbps

• The high data rate requires a low capacitance device to preserve signal integrity

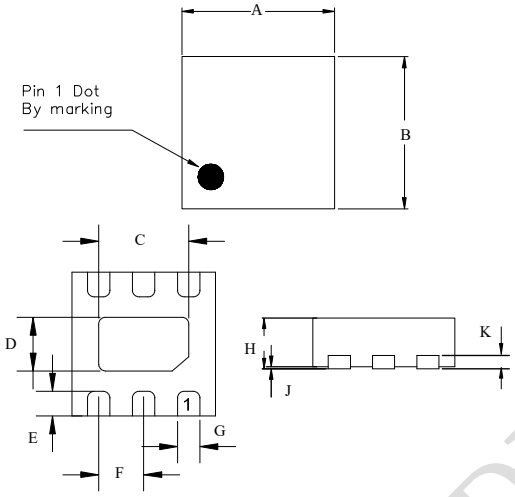
● Requires 2 channels of data line protection per port (i.e. D±)

• A 4 channel device can be useful if protecting a USB stack of 2 ports to make the ESD footprint as small as possible

• VBUS can be protected by connecting it to the VCC pin on the diode array or by using a separate single channel device as previously shown

Outline Drawing - DFN1616-6

DFN1616-6



DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.061	0.065	1.55	1.65	
B	0.061	0.065	1.55	1.65	
C	0.035	0.041	0.90	1.05	
D	0.020	0.026	0.50	0.65	
E	0.008	0.012	0.20	0.30	
F	0.020 REF.		0.50 REF.		
G	0.008	0.026	0.20	0.30	
H	0.020	0.024	0.50	0.60	
J	0.000	0.002	0.00	0.05	
K	0.006 REF.		0.15 REF.		

Suggested Solder
Pad Layout

(mm)