

### Description

The HSP8004 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

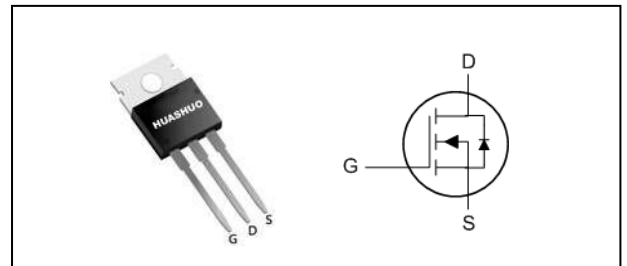
The HSP8004 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

### Product Summary

$V_{DS}$	80	V
$R_{DS(ON),TYP}$	3.1	m $\Omega$
$I_D$	175	A

### TO-220 Pin Configuration



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	80	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	175	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	123	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	440	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	378	mJ
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	192	W
$T_{STG}$	Storage Temperature Range	-55 to 175	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 175	$^\circ C$

### Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	0.65	$^\circ C/W$



**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

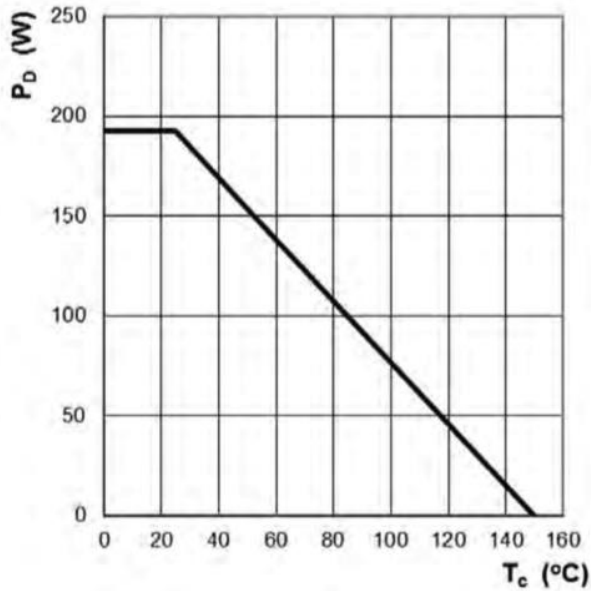
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
B <sub>VDS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	80	---	---	V
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =20A	---	3.1	3.5	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.2	1.8	2.5	V
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =64V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	100	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =5V, I <sub>D</sub> =30A	---	50	---	S
R <sub>g</sub>	Gate Resistance	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	1.2	---	Ω
Q <sub>g</sub>	Total Gate Charge (10V)	V <sub>DD</sub> =40V, V <sub>GS</sub> =10V, I <sub>D</sub> =20A	---	80	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	15	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	16	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =40V, V <sub>GS</sub> =10V, R <sub>G</sub> =6Ω, I <sub>D</sub> =20A	---	17	---	ns
T <sub>r</sub>	Rise Time		---	32	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	50	---	
T <sub>f</sub>	Fall Time		---	18	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V, f=1MHz	---	4450	---	pF
C <sub>oss</sub>	Output Capacitance		---	800	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	50	---	

**Diode Characteristics**

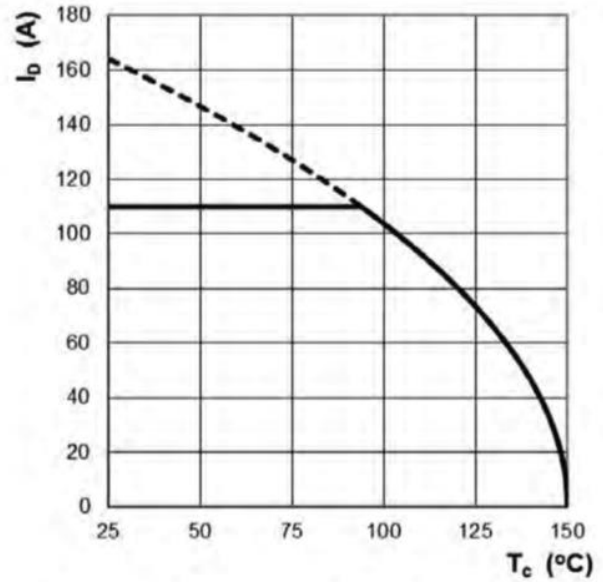
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	175	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V, I <sub>S</sub> =A, T <sub>J</sub> =25°C	---	---	1.5	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> =20A, dI/dt=100A/μs, T <sub>J</sub> =25°C	---	40	---	nS
Q <sub>rr</sub>	Reverse Recovery Charge		---	45	---	nC



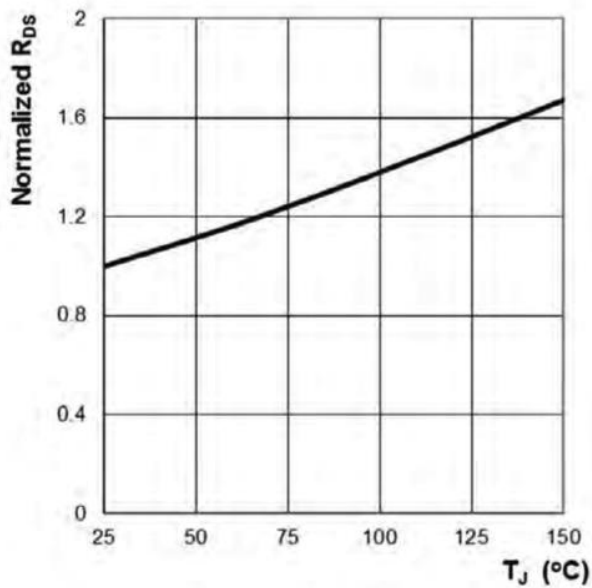
**Electrical Characteristic Diagrams**



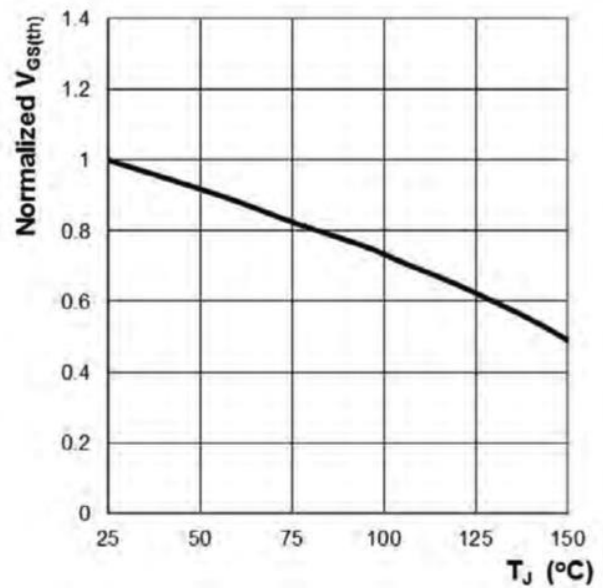
**Figure 1: Power Dissipation**



**Figure 2: Continuous Drain Current vs.  $T_c$**



**Figure 3: Normalized  $R_{DS(ON)}$  vs.  $T_J$**



**Figure 4: Normalized  $BV_{DSS}$  vs.  $T_J$**

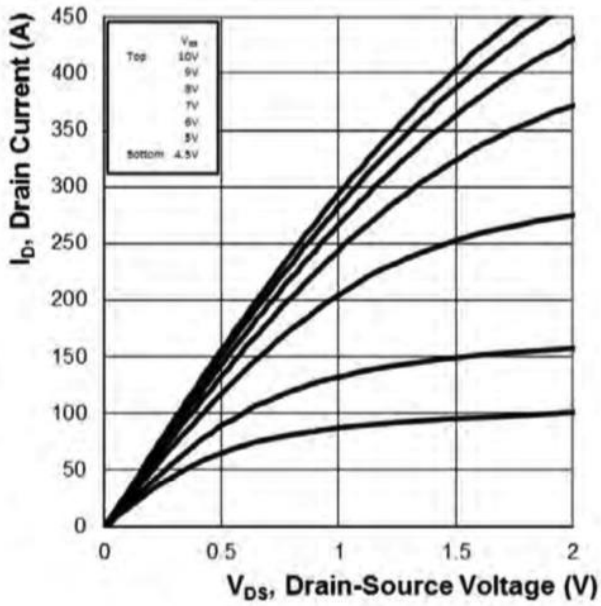


Figure 5: On-Region Characteristics

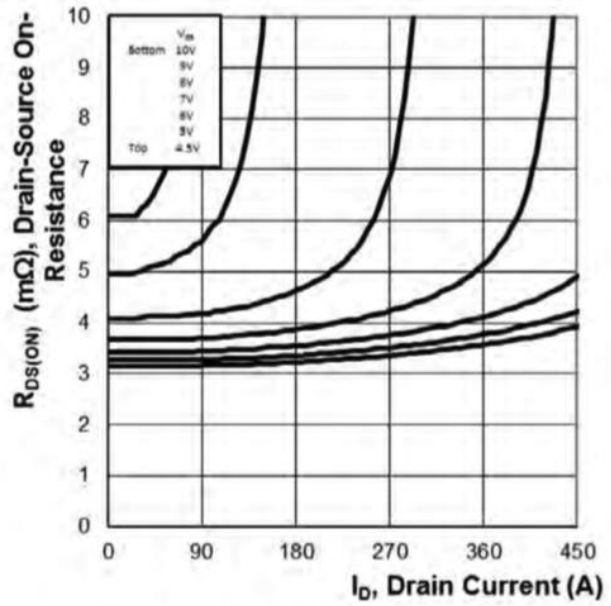


Figure 6: Typ.  $R_{DS}$  Variation vs.  $I_D$  and  $V_{GS}$

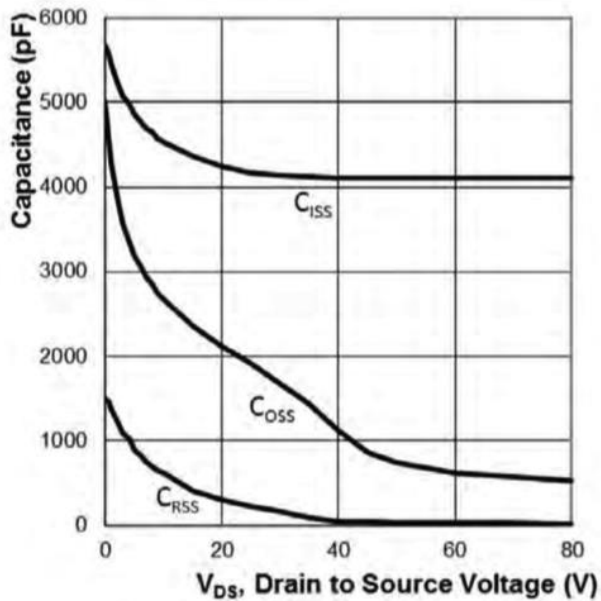


Figure 7: Typ. Capacitance Characteristics

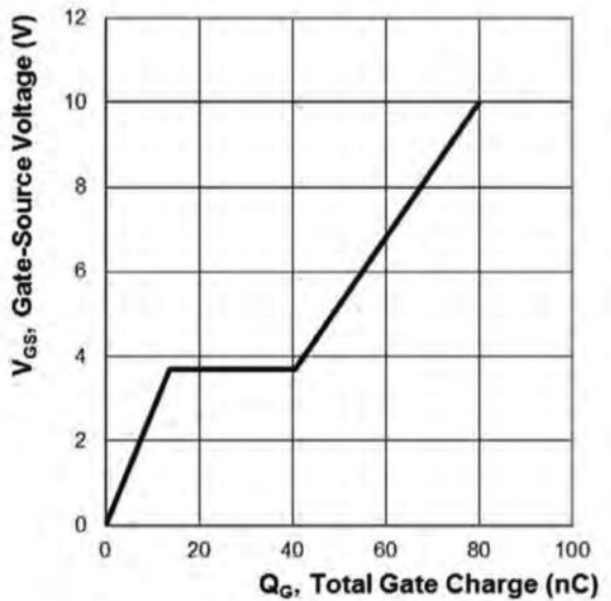


Figure 8: Typ. Gate Charge Characteristics

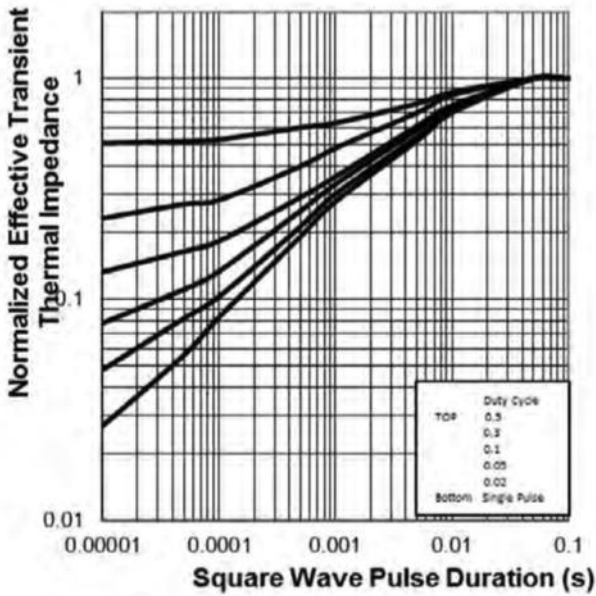


Figure 9: Normalized Thermal Transient Impedance, Junction-to-Case

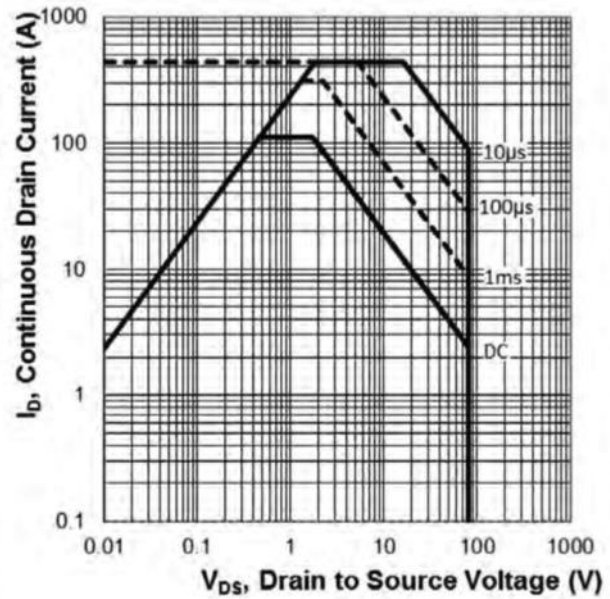


Figure 10: Maximum Safe Operation Area

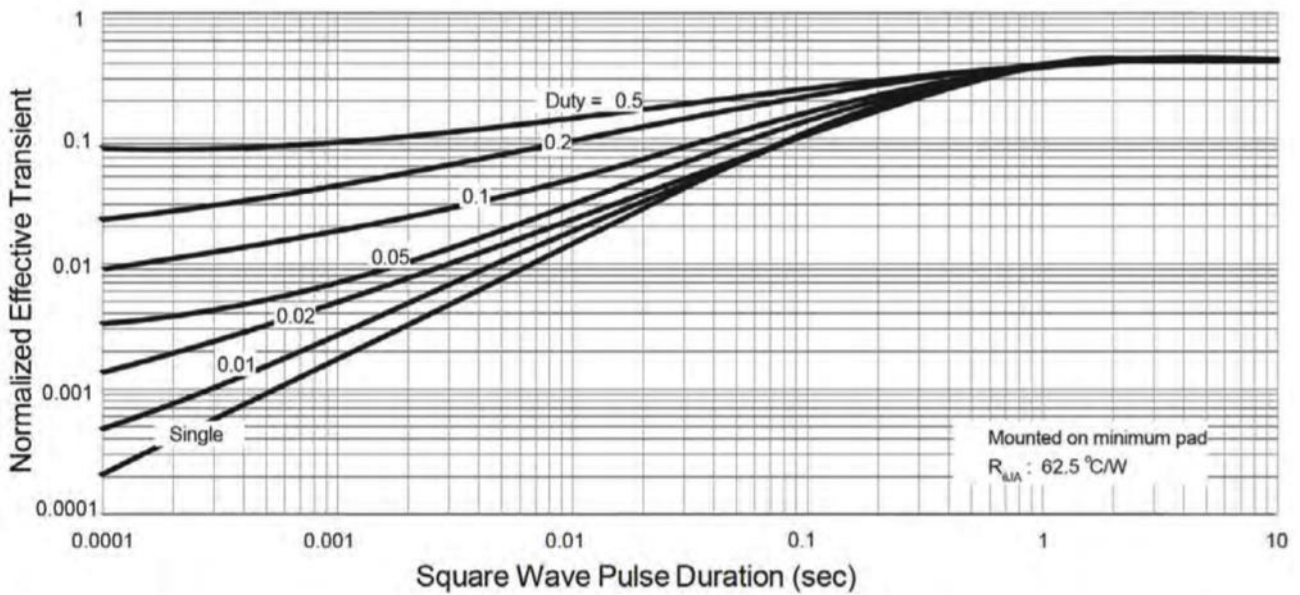


Fig 7 Normalized Maximum Transient Thermal Impedance



Parameter Test Circuits

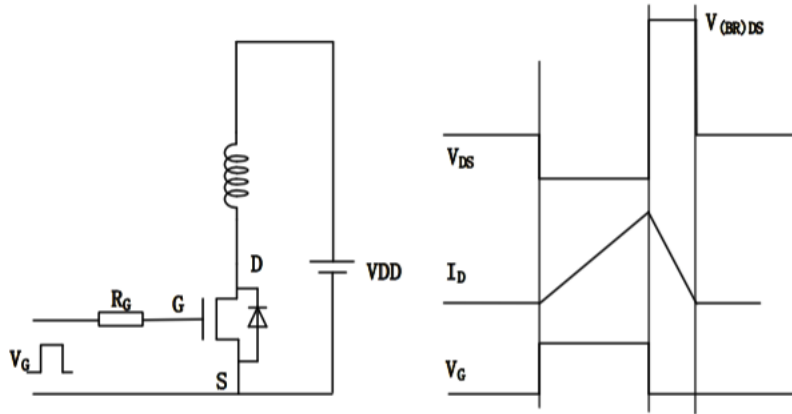


Figure 10 Unclamped Inductive Switching (UIS) Test circuit and waveforms

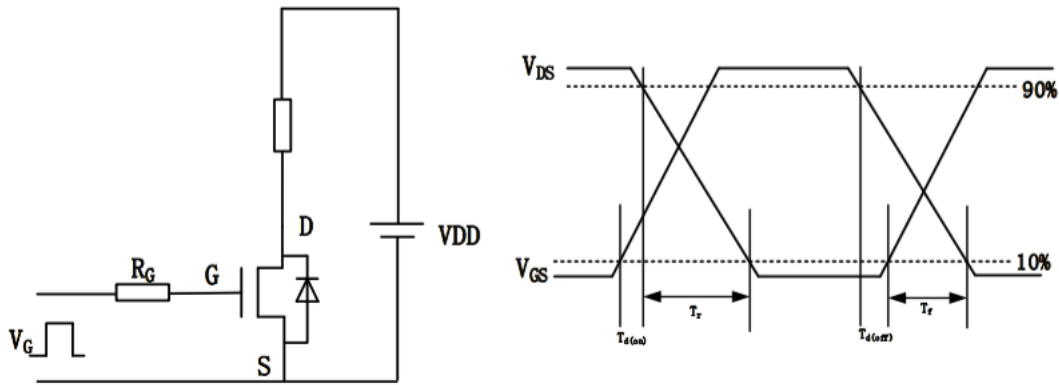


Figure 11 Resistive Switching time Test circuit and waveforms

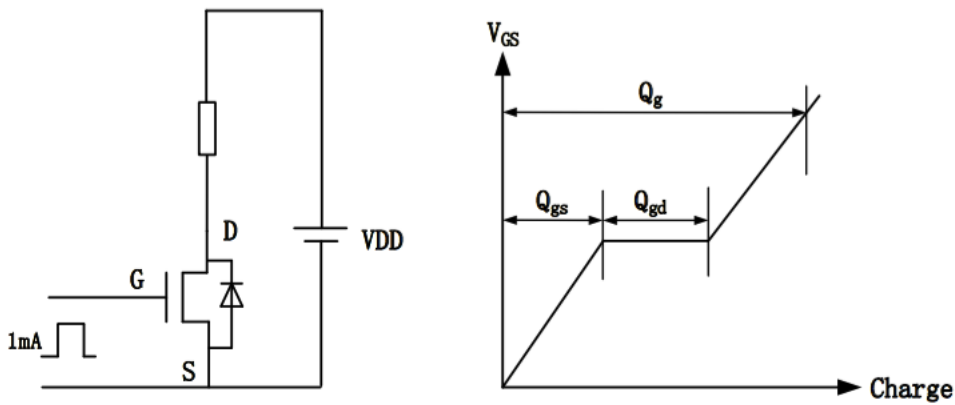


Figure 12 Gate charge Test circuit and waveforms