650V 4A N-Channel Planar MOSFET

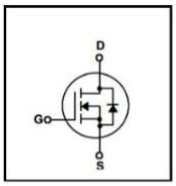
General Description

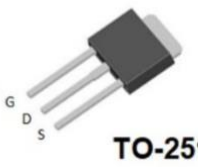
HS4N65 is Fortunatus high voltage MOSFET family based on advanced planar stripe DMOS technology. This advanced MOSFET family has optimized on-state resistance, and also provides superior switching performance and higher avalanche energy strength. This device family is suitable for high efficiency switch mode power supplies.

FEATURES

- RDSON≤3.0Ω @Vgs=10V, Id=2A
- Ultra Low gate Charge(typical 13 nC)
- Low Crss (typical 5pF)
- Fast switching capability
- 100% avalanche tested
- Improved dv/dt capability

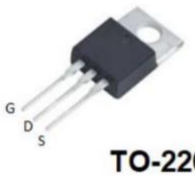
SYMBOL





TO-251

TO-252



TO-220

TO-220F

ASSEMBLY MESSAGE

Product Name	Marking	Package	Halogen Free	Packaging
HSD4N65	4N65UF	TO-251	YES	Tube
HSU4N65	4N65DF	TO-252	YES	Tube/Reel
HSP4N65	4N65CF	TO-220	YES	Tube
HSF4N65	4N65FF	TO-220F	YES	Tube

ABSOLUTE MAXIMUM RATINGS (T_C=25°C unless otherwise noted)

Parameter		Symbol	Rating			Unit
			HSD/U4N65	HSP4N65	HSF4N65	
Drain-Source Voltage		V_{DSS}	650			V
Drain Current	Continuous (T_C = 25°C)	I_D	4			A
	Continuous (T_C = 100°C)		2.7			A
Drain Current	Pulsed (Note1)	I_{DM}	16			A
Gate-Source Voltage		V_{GSS}	±30			V
Avalanche Energy	Single Pulse (Note2)	E_{AS}	232			mJ
	Repetitive (None1)	E_{AR}	15			mJ
Avalanche Current (None1)		I_{AR}	4			A
Peak Diode Recovery dv/dt (Note3)		dv/dt	5			V/ns
Power Dissipation (Note 2)	T_C =25°C	P_D	80	102	38	W
	Derate above 25°C		0.64	0.82	0.3	W/°C
Maximum Junction Temperature		T_J	150			°C
Storage Temperature Range		T_{STG}	-55 to 150			°C

Note: 1. Repetitive Rating: Pulse width limited by maximum junction temperature

2. L=29mH, I_{AS}=4.0A, V_{DD}=50V, RG=25 Ω, Starting TJ = 25°C

3. I_{SD} ≤ 4.0A, di/dt ≤ 300A/μs, V_{DD} ≤ BV_{DSS}, Starting TJ = 25°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Max.			Unit
		HSD/U4N65	HSP4N65	HSF4N65	
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.56	1.23	3.29	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	110	62	120	°C/W

ELECTRICAL CHARACTERISTICS（T =25J ℃,unless otherwise Noted）

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	VGS=0V, ID=250μA	650			V
Zero Gate Voltage Drain Current	I_{DSS}	VDS=650V, VGS=0V			1	uA
		VDS=520V, TC = 125°C			100	uA
Gate-Body Leakage Current, Forward	I_{GSS}	VGS=30V			100	nA
Gate-Body Leakage Current, Reverse		VGS=-30V			-100	nA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	ID = 250 μA		0.62		V/℃
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	VDS=VGS, ID=250μA	2		4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	VGS=10V, ID=2A		2.6	3.0	Ω
Forward Transconductance (Note4)	g_{FS}	VDS = 50V, ID = 2A		2.5		S
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	VDS=25V, VGS=0V, f=1.0MHz		545		pF
Output Capacitance	C_{OSS}			54		pF
Reverse Transfer Capacitance	C_{RSS}			5		pF
SWITCHING PARAMETERS						
Turn-ON Delay Time	$t_{D(ON)}$	VDD=325V, ID=4 A, VGS = 10V ,RG=10Ω (Note4,5)		11		ns
Turn-ON Rise Time	t_R			25		ns
Turn-OFF Delay Time	$t_{D(OFF)}$			32.5		ns
Turn-OFF Fall-Time	t_F			7		ns
Total Gate Charge(Note)	Q_G	VDS =520V, VGS =10V, ID =4A (Note4,5)		13		nC
Gate Source Charge	Q_{GS}			3.4		nC
Gate Drain Charge	Q_{GD}			7		nC
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Drain-Source Diode Forward Voltage	V_{SD}	IS=4A, VGS=0V			1.4	V
Diode Continuous Forward Current	I_S				4	A
Pulsed Drain-Source Current	I_{SM}				16	A
Reverse Recovery Time	t_{RR}	VGS=0V,ISD=4A di/dt=100 A/μs (Note4,5)		510		ns
Reverse Recovery Charge	Q_{RR}			2.5		uC

Note： 4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%

5. Essentially independent of operating temperature

TYPICAL CHARACTERISTICS

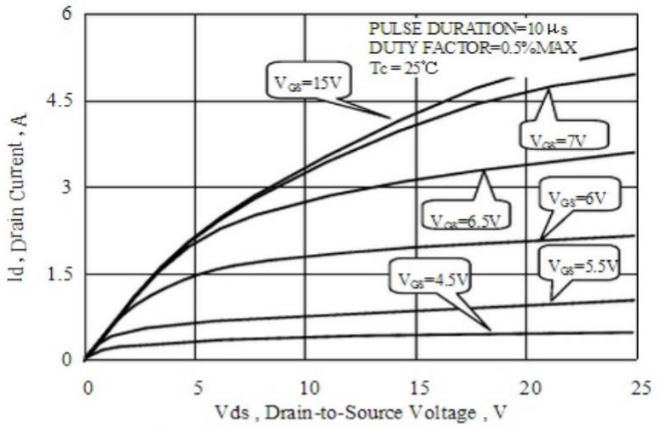


Figure 1. Typical Output Characteristics

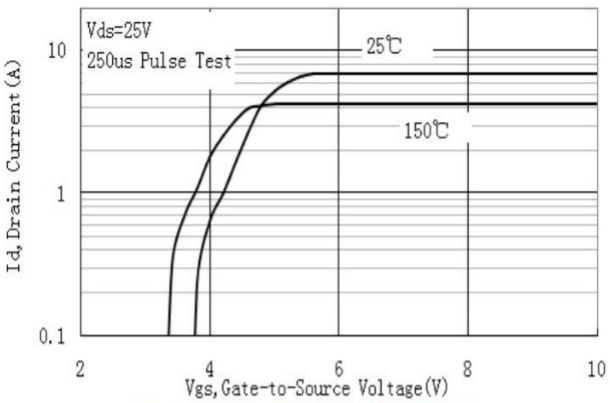


Figure2.Typical Transfer Characteristics

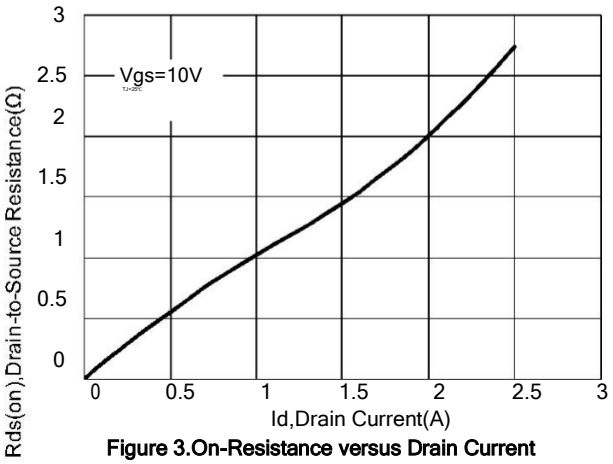


Figure 3.On-Resistance versus Drain Current

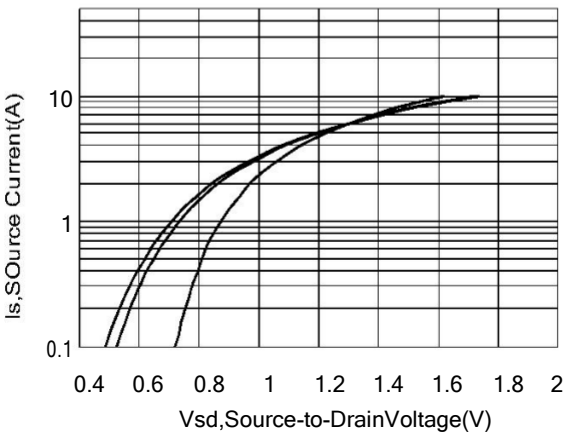


Figure4.Diode ForwardVoltage versus Current

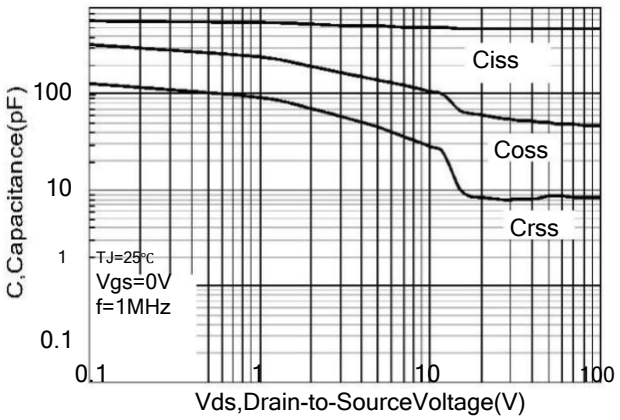


Figure 5.Typical Capacitance vs.Drian-to-Source Voltage

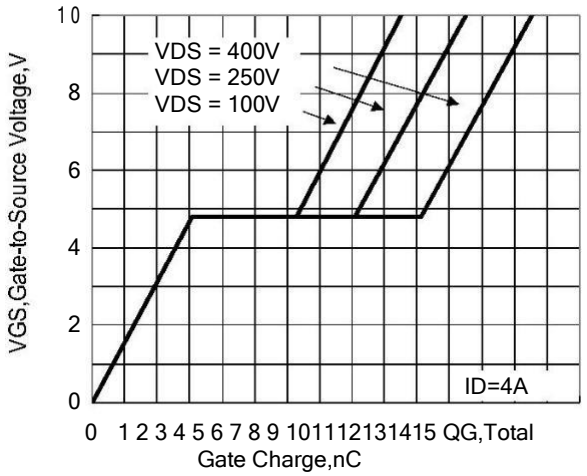


Figure 6.Typical Gate Charge vs.Vgs

TYPICAL CHARACTERISTICS(Cont.)

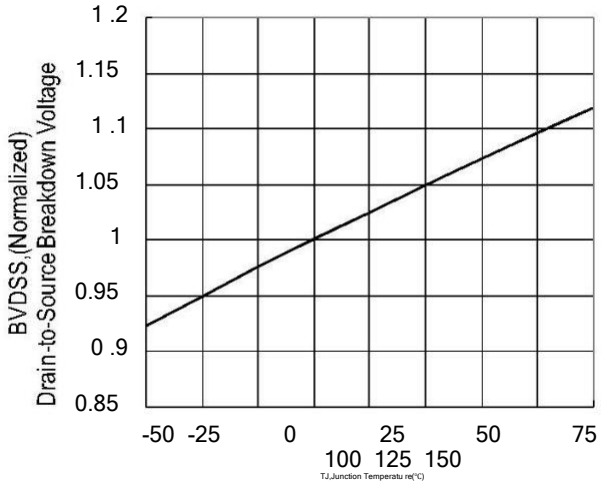


Figure 7.Bvdss Variation with Temperature

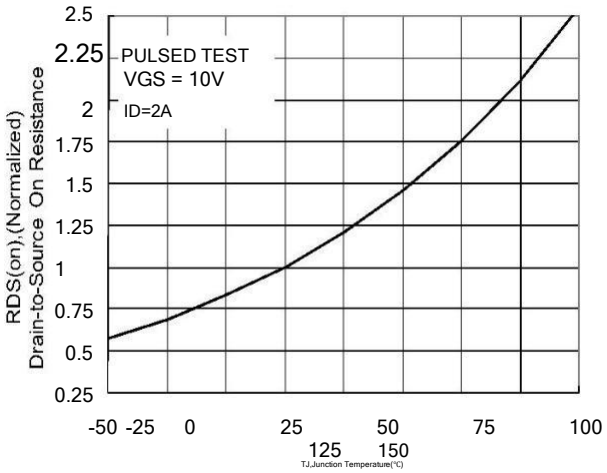


Figure 8.On-Resistance Variation with Temperature

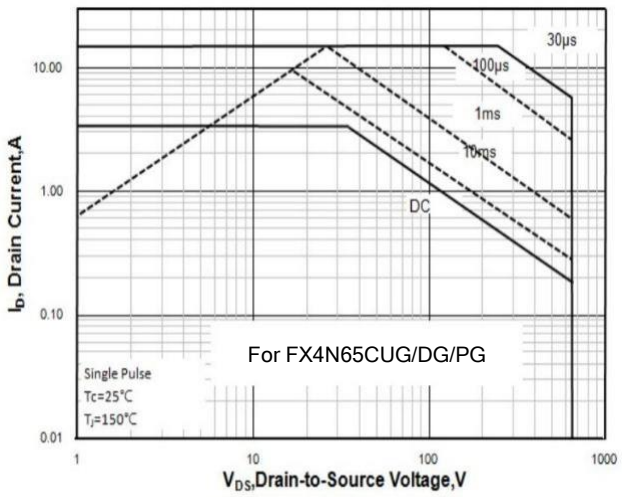


Figure 9. Maximum Safe Operating Area

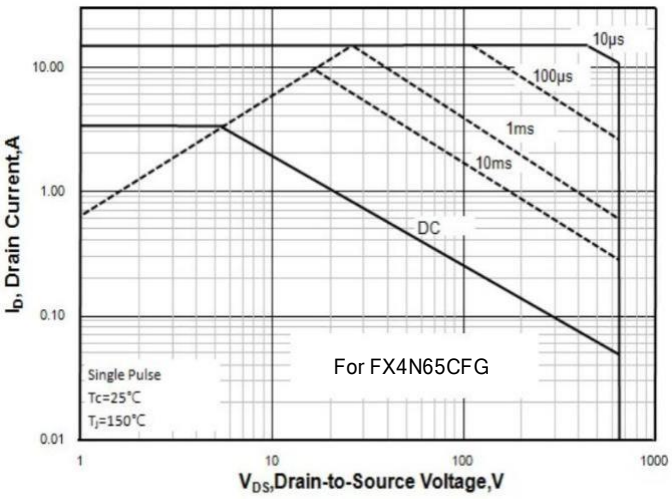


Figure 9. Maximum Safe Operating Area

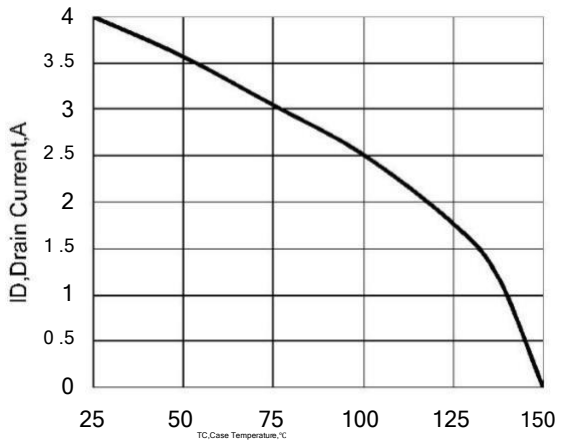
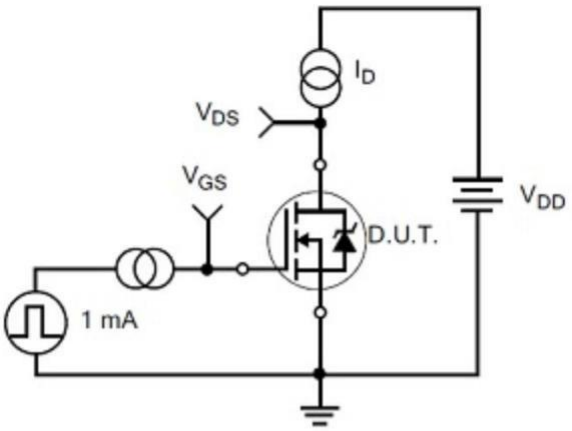
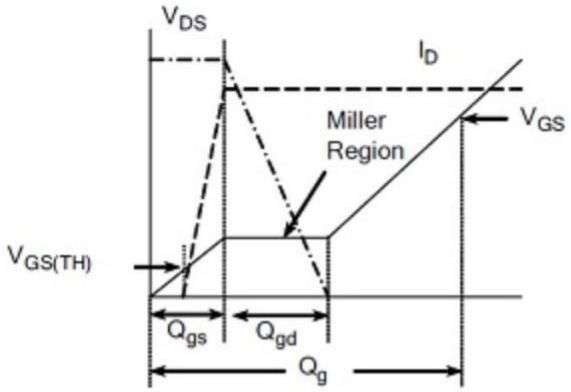


Figure 10. Maximum Continuous Drain Current vs Case Temperature

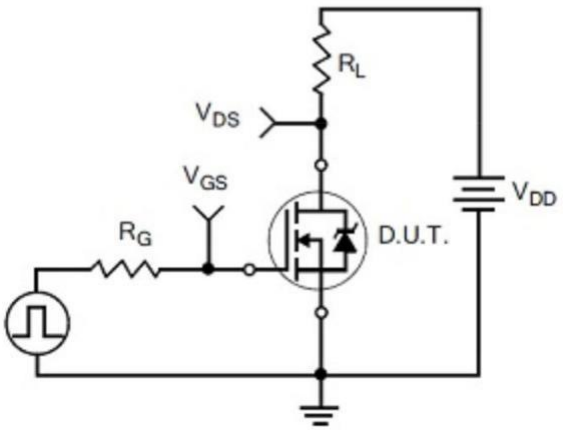
TEST CIRCUITS AND WAVEFORMS



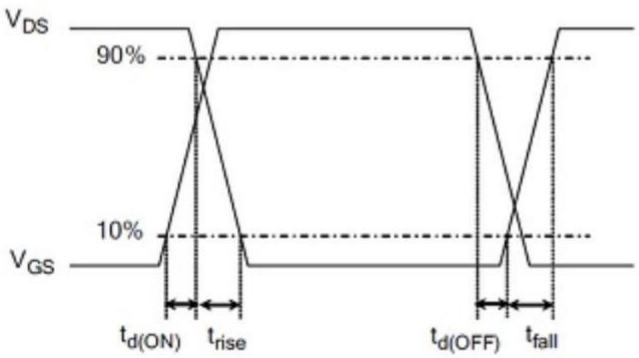
Gate Charge Test Circuit



Gate Charge Waveform

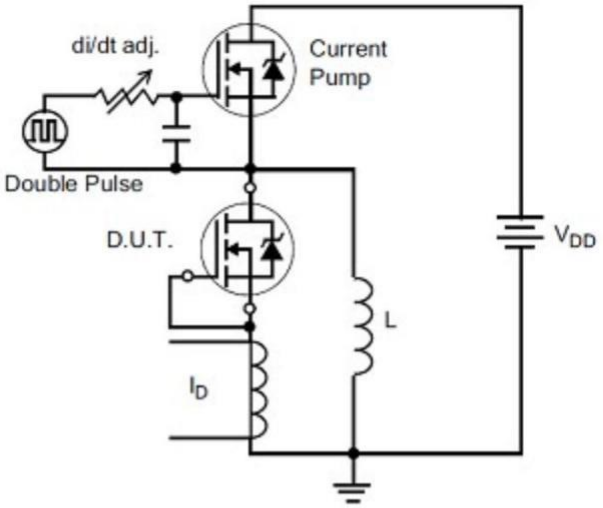


Resistive Switching Test Circuit

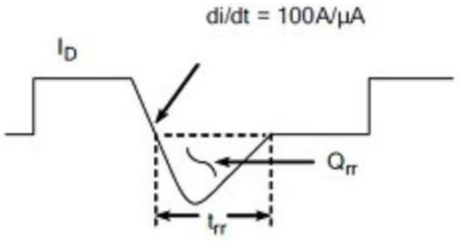


Resistive Switching Waveforms

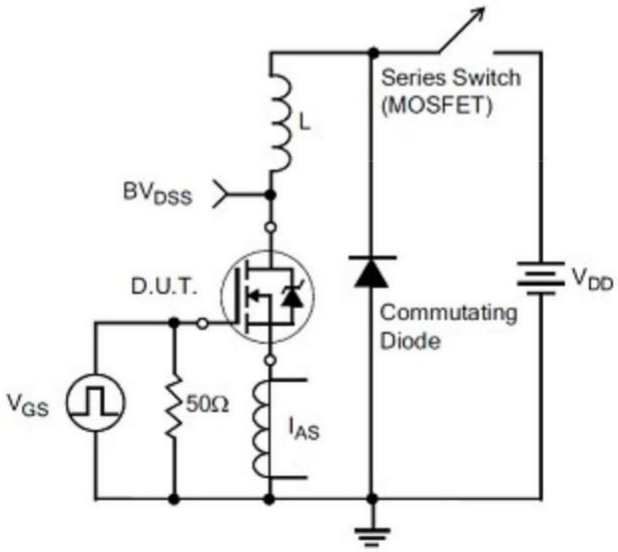
TEST CIRCUITS AND WAVEFORMS(Cont.)



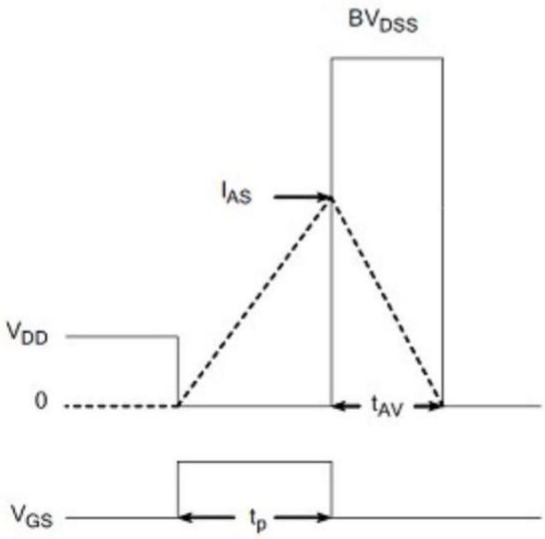
Diode Reverse Recovery Test Circuit



Diode Reverse Recovery Waveform



Unclamped Inductive Switching Test Circuit



$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Unclamped Inductive Switching Waveforms