

## 3-wire Serial EEPROMs 1K/2K/4K

### FEATURES:

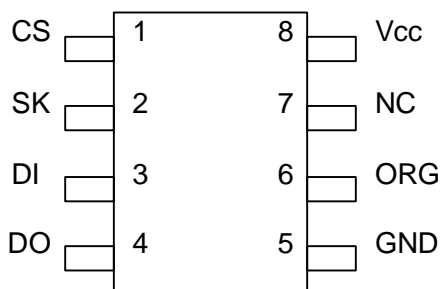
- Internally organized as 128 x 8 or 64 x 16(1K), 256 x 8 or 128 x 16 (2K), 512 x 8 or 256 x 16 (4K)
- Wide-voltage range operation
  - 1.8V-5.5 V
- 3-wire serial interface bus
- Data retention: 100 years
- High endurance: 1,000,000 Write Cycles
- 2 MHz (5V) clock rate
- Sequential read operation
- Self-timed write cycle (10ms max)
- 8-pin PDIP, 8-pin JEDEC SOIC, and 8-pin TSSOP Packages

### DESCRIPTION

FS-RANK Technology's AT93C family provides 1K, 2K and 4K of serial electrically erasable and programmable read-only memory (EEPROM). The wide V<sub>dd</sub> range allows for low-voltage operation down to 1.8V and up to 5.5V. The device, fabricated using traditional CMOS EEPROM technology, is optimized for many industrial and commercial applications where low-voltage and low-power operation is essential. The AT93C46/56/66 is available in 8-pin PDIP, 8-pin JEDEC SOIC, and 8-pin TSSOP packages and is accessed via a 3-wire serial interface.

**Figure 1. Pin Configurations**

8-pin PDIP/TSSOP/SOIC



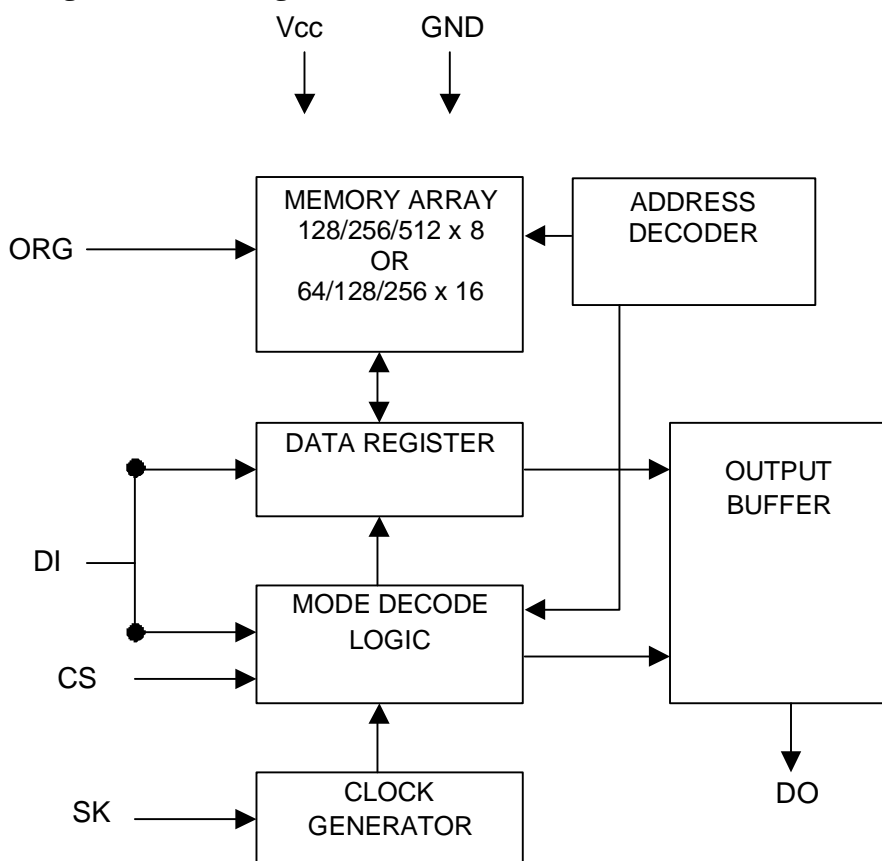
Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
ORG	Internal Organization
NC	No Connect

**ABSOLUTE MAXIMUM RATINGS**

Operating Temperature.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	- 1.0V to Vcc + 7.0V
Maximum Operating Voltage.....	6.25V
DC Output Current.....	5.0 mA

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 2. Block Diagram**



**Notes**

1. The ORG pin is used to select between x8 and x16 mode. When the pin is connected to Vcc, x16 mode is selected. Otherwise, the ORG pin should be grounded in order to select x8 mode.

The interface for the AT93C46/56/66 is accessed through four different signals: Chip Select (CS), Data Input (DI), Data Output (DO), and Serial Data Clock (SK). The Chip Select (CS) signal must be pulled high before issuing a command through the Data Input (DI) pin. The Serial Data Clock (SK) signal is used in conjunction with the Data Input (DI) pin.

**PIN CAPACITANCE**

 Applicable over recommended operating range from  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ ,  $V_{CC} = +5.0\text{V}$ 

Symbol	Test Condition	Max	Units	Condition
$C_{OUT}$	Output Capacitance (DO)	5	pF	$V_{OUT} = 0\text{V}$
$C_{IN}$	Input Capacitance (CK, SK, DI)	5	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and not 100% tested.

**DC CHARACTERISTICS**

Applicable over recommended operating range from:

 $T_{AMB} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = +1.8\text{V}$  to  $+5.5\text{V}$  (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
$V_{CC1}$	Supply Voltage		1.8		5.5	V
$V_{CC2}$	Supply Voltage		2.7		5.5	V
$V_{CC3}$	Supply Voltage		4.5		5.5	V
$I_{CC}$	Supply Current $V_{CC} = 5.0\text{V}$	READ at 1 MHz		0.5	2.0	mA
$I_{CC}$	Supply Current $V_{CC} = 5.0\text{V}$	WRITE at 1 MHz		0.5	2.0	mA
$I_{SB1}$	Standby Current $V_{CC} = 1.8\text{V}$	CS = 0V		0	0.1	$\mu\text{A}$
$I_{SB2}$	Standby Current $V_{CC} = 2.7\text{V}$	CS = 0V		6.0	10.0	$\mu\text{A}$
$I_{SB3}$	Standby Current $V_{CC} = 5.0\text{V}$	CS = 0V		17	30	$\mu\text{A}$
$I_{LI}$	Input Leakage Current	$V_{IN} = 0\text{V}$ to $V_{CC}$		0.1	3.0	$\mu\text{A}$
$I_{LO}$	Output Leakage Current	$V_{IN} = 0\text{V}$ to $V_{CC}$		0.1	3.0	$\mu\text{A}$
$V_{IL1}^{(1)}$	Input Low Level	$2.7\text{V} < V_{CC} < 5.5\text{V}$	-0.6		0.8	V
$V_{IH1}^{(1)}$	Input High Level	$2.7\text{V} < V_{CC} < 5.5\text{V}$	2.0		$V_{CC} + 1$	V
$V_{IL2}^{(1)}$	Input Low Level	$1.8\text{V} < V_{CC} < 2.7\text{V}$	-0.6		$V_{CC} \times 0.3$	V
$V_{IH2}^{(1)}$	Input High Level	$1.8\text{V} < V_{CC} < 2.7\text{V}$	$V_{CC} \times 0.7$		$V_{CC} + 1$	V
$V_{OL1}$	Output Low Level	$2.7\text{V} < V_{CC} < 5.5\text{V}$ ; $I_{OL} = 2.1\text{mA}$			0.4	V
$V_{OH1}$	Output High Level	$2.7\text{V} < V_{CC} < 5.5\text{V}$ ; $I_{OH} = -0.4\text{mA}$	2.4			V
$V_{OL2}$	Output Low Level	$1.8\text{V} < V_{CC} < 2.7\text{V}$ ; $I_{OL} = 0.15\text{mA}$			0.2	V
$V_{OH2}$	Output High Level	$1.8\text{V} < V_{CC} < 2.7\text{V}$ ; $I_{OH} = -100\mu\text{A}$	$V_{CC} - 0.2$			V

 Note: 1.  $V_{IL}$  and  $V_{IH}$  max are reference only and are not tested.

**AC CHARACTERISTICS**

Applicable over recommended operating range from:

 $T_{AMB} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} =$  As specified,  $CL = 1$  TTL Gate & 100pF (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f <sub>SK</sub>	Clock Frequency, SK	4.5V < V <sub>CC</sub> < 5.5V 2.7V < V <sub>CC</sub> < 5.5V 1.8V < V <sub>CC</sub> < 5.5V	0 0 0		2 1 0.25	MHz
t <sub>SKH</sub>	SK High Time	4.5V < V <sub>CC</sub> < 5.5V 2.7V < V <sub>CC</sub> < 5.5V 1.8V < V <sub>CC</sub> < 5.5V	250 250 1000			ns
t <sub>SKL</sub>	SK Low Time	4.5V < V <sub>CC</sub> < 5.5V 2.7V < V <sub>CC</sub> < 5.5V 1.8V < V <sub>CC</sub> < 5.5V	250 250 1000			ns
t <sub>CS</sub>	Minimum CS Low Time	4.5V < V <sub>CC</sub> < 5.5V 2.7V < V <sub>CC</sub> < 5.5V 1.8V < V <sub>CC</sub> < 5.5V	250 250 1000			ns
t <sub>CSS</sub>	CS Setup Time	Relative to SK 4.5V < V <sub>CC</sub> < 5.5V 2.7V < V <sub>CC</sub> < 5.5V 1.8V < V <sub>CC</sub> < 5.5V	50 50 200			ns
t <sub>DIS</sub>	DI Setup Time	Relative to SK 4.5V < V <sub>CC</sub> < 5.5V 2.7V < V <sub>CC</sub> < 5.5V 1.8V < V <sub>CC</sub> < 5.5V	100 100 400			ns
t <sub>CSH</sub>	CS Hold Time	Relative to SK	0			ns
t <sub>DIH</sub>	DI Hold Time	Relative to SK 4.5V < V <sub>CC</sub> < 5.5V 2.7V < V <sub>CC</sub> < 5.5V 1.8V < V <sub>CC</sub> < 5.5V	100 100 400			ns
t <sub>PD1</sub>	Output Delay to "1"	AC Test 4.5V < V <sub>CC</sub> < 5.5V 2.7V < V <sub>CC</sub> < 5.5V 1.8V < V <sub>CC</sub> < 5.5V			250 250 1000	ns
t <sub>PD0</sub>	Output Delay to "0"	AC Test 4.5V < V <sub>CC</sub> < 5.5V 2.7V < V <sub>CC</sub> < 5.5V 1.8V < V <sub>CC</sub> < 5.5V			250 250 1000	ns
t <sub>SV</sub>	CS to Status Valid	AC Test 4.5V < V <sub>CC</sub> < 5.5V 2.7V < V <sub>CC</sub> < 5.5V 1.8V < V <sub>CC</sub> < 5.5V			250 250 1000	ns
t <sub>DF</sub>	CS to DO in High Impedance	AC Test CS = V <sub>IL</sub> 4.5V < V <sub>CC</sub> < 5.5V 2.7V < V <sub>CC</sub> < 5.5V 1.8V < V <sub>CC</sub> < 5.5V			100 100 400	ns
t <sub>WP</sub>	Write Cycle Time	4.5V < V <sub>CC</sub> < 5.5V		3	10	ms
Endurance	5.0V, 25°C		1M			Write Cycles

**INSTRUCTION SET FOR THE AT93C46**

Instruction	SB	Op Code	Address		Data		Comments
			X8	X16	X8	X16	
READ	1	10	A <sub>6</sub> – A <sub>0</sub>	A <sub>5</sub> – A <sub>0</sub>			Reads data stored at specified memory location.
EWEN	1	00	11xxxxx	11xxxx			Write enable command (must be issued before any erase or write operation).
ERASE	1	11	A <sub>6</sub> – A <sub>0</sub>	A <sub>5</sub> – A <sub>0</sub>			Erases memory location A <sub>n</sub> – A <sub>0</sub>
WRITE	1	01	A <sub>6</sub> – A <sub>0</sub>	A <sub>5</sub> – A <sub>0</sub>	D <sub>7</sub> – D <sub>0</sub>	D <sub>15</sub> – D <sub>0</sub>	Writes to memory location A <sub>n</sub> – A <sub>0</sub>
ERAL	1	00	10xxxxx	10xxxx			Erases all memory locations. Valid only at Vcc = 4.5V to 5.5V
WRAL 1		00	01xxxxx	01xxxx	D <sub>7</sub> – D <sub>0</sub>	D <sub>15</sub> – D <sub>0</sub>	Writes all memory locations. Valid only at Vcc = 4.5V to 5.5V
EWDS	1	00	00xxxxx	00xxxx			Disables all erase or write instructions

Note: The X's in the address field represent don't care values and must be clocked.

**INSTRUCTION SET FOR THE AT93C46/56/66**

Instruction	SB	Op Code	Address		Data		Comments
			X8	X16	X8	X16	
READ	1	10	A <sub>8</sub> – A <sub>0</sub>	A <sub>7</sub> – A <sub>0</sub>			Reads data stored at specified memory location.
EWEN	1	00	11xxxxxxxx	11xxxxxxxx			Write enable command (must be issued before any erase or write operation).
ERASE	1	11	A <sub>8</sub> – A <sub>0</sub>	A <sub>7</sub> – A <sub>0</sub>			Erase memory location A <sub>n</sub> – A <sub>0</sub>
WRITE	1	01	A <sub>8</sub> – A <sub>0</sub>	A <sub>7</sub> – A <sub>0</sub>	D <sub>7</sub> – D <sub>0</sub>	D <sub>15</sub> – D <sub>0</sub>	Writes memory location A <sub>n</sub> – A <sub>0</sub>
ERAL	1	00	10xxxxxxxx	10xxxxxxxx			Erases all memory locations. Valid only at Vcc = 4.5V to 5.5V
WRAL 1		00	01xxxxxxxx	01xxxxxxxx	D <sub>7</sub> – D <sub>0</sub>	D <sub>15</sub> – D <sub>0</sub>	Writes all memory locations. Valid only at Vcc = 4.5V to 5.5V.
EWDS	1	00	00xxxxxxxx	00xxxxxxxx			Disables all erase or write instructions

Note: The X's in the address field represent don't care values and must be clocked.

## FUNCTIONAL DESCRIPTION

The AT93C46/56/66 supports 7 different instructions, which must be clocked serially using the CS, SK and DI pins. Before sending each of these instructions, the CS pin must first be pulled high followed by a START bit (logic '1'). The next sequence includes a 2-bit Op Code and usually an 8 or 16-bit address. The next description describes the various functions in the chip.

**READ (READ):** The Read (READ) instruction includes the Op Code ("10") followed by the memory address location to be read. After the instruction and address is sent, the data from the memory location can be clocked out using the serial output pin DO. The data changes on the rising edge of the clock, so the falling edge can be used to strobe the output.

Note that during shifting the last address bit, the DO pin is a dummy bit (logic "0").

**ERASE/WRITE (EWEN):** When the chip is first powered-on, no erase or write instructions can be issued. Only when the Erase/Write Enable (EWEN) instruction is sent will the system be allowed to write to the chip. The EWEN command only needs to be issued once after being powered-on. To disable the chip again, the Erase/Write Disable (EWDS) command can be used.

**ERASE (ERASE):** The Erase (ERASE) instruction clears the designated memory location to a logical '1' state. After the Op Code and address location is inputted, the chip will enter into an erase cycle. When the cycle completes, the chip will automatically enter into standby mode.

**WRITE (WRITE):** The Write (WRITE) instruction is used to write to a specific memory location. If word mode (x16) is selected, then 16 bits of data will be written into the location. If byte mode (x8) is chosen, then 8 bits of data will be written into the location. The write cycle will begin automatically after the 8 or 16 bits are shifted into the chip.

**ERASE ALL (ERAL):** The Erase All (ERAL) instruction is primarily used for testing purposes and only functions when  $V_{cc}=4.5\text{ V}$  to  $5.5\text{ V}$ . This instruction will clear the entire memory array to '1'.

**WRITE ALL (WRAL):** The Write All (WRAL) instruction will program the entire memory array according to the 8 or 16-bit data pattern provided. The instruction will only be valid when  $V_{cc}=4.5\text{ V}$  to  $5.5\text{ V}$ .

**ERASE/WRITE DISABLE (EWDS):** The Erase/Write Disable (EWDS) instruction blocks any kind of erase or program operations from modifying the contents of the memory array. This instruction should be executed after erasing or programming to prevent accidental data loss.

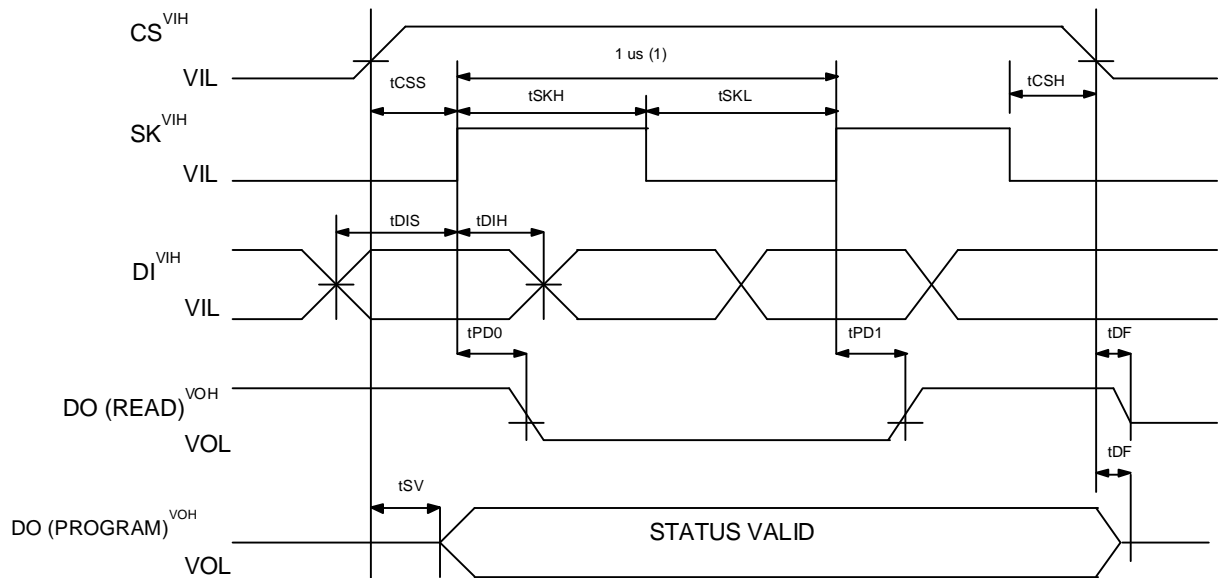
Note also that the READ instruction will operate regardless of whether the chip is disabled from program and write operations.

**Ready/Busy**

To determine whether the chip has completed an erase or write operation, the CS signal can be pulled LOW for a minimum of 250 ns ( $t_{CS}$ ) and then pulled back HIGH to enter Ready/Busy mode. If the chip is currently in the programming cycle,  $t_{WP}$ , then the DO pin will go low (logical "0"). When the write cycle completes, the DO pin is pulled high (logical "1") to indicate that the part can receive another instruction. Note that the Ready/Busy polling cannot be done if the chip has already finished and returned back to standby mode.

**TIMING DIAGRAMS**

**Synchronous Data Timing**



Note (1): This is the minimum SK period.

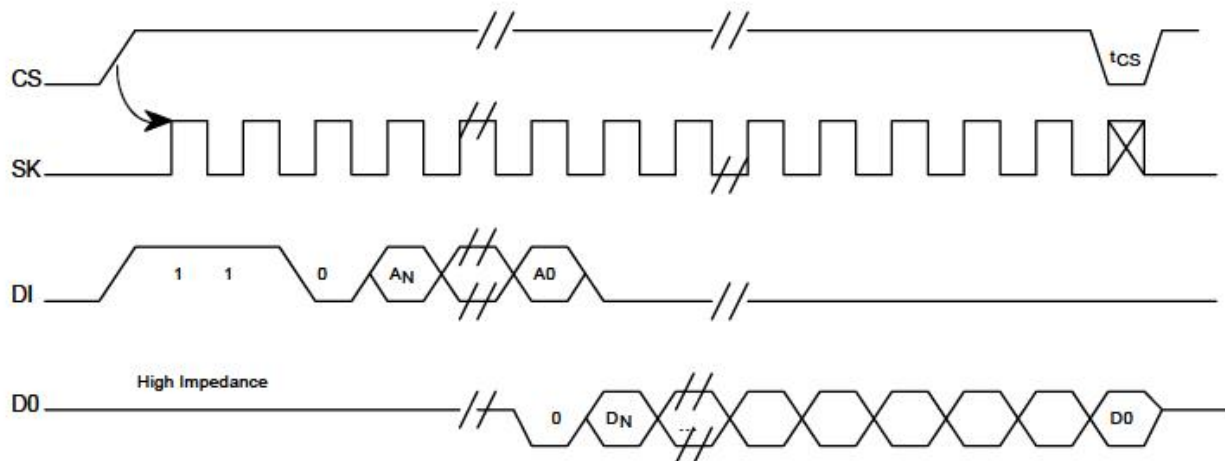
**Organization Key for Timing Diagrams**

I/O	93 C46(1K)	93 C56(2K)	93 C66(4K)
$A_N$	X8	X8	X8
$D_N$	D7	D7	D7

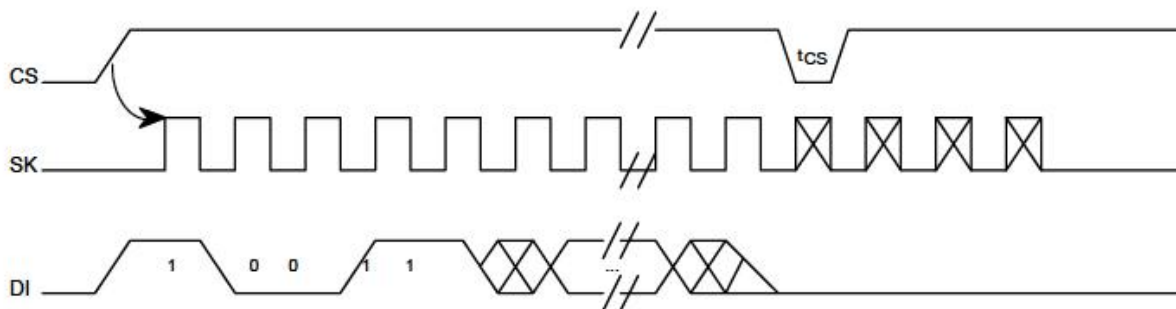
Notes:

1.  $A_8$  is a DON'T CARE value, but the extra clock is required.
2.  $A_7$  is a DON'T CARE value, but the extra clock is required.

**READ TIMING**

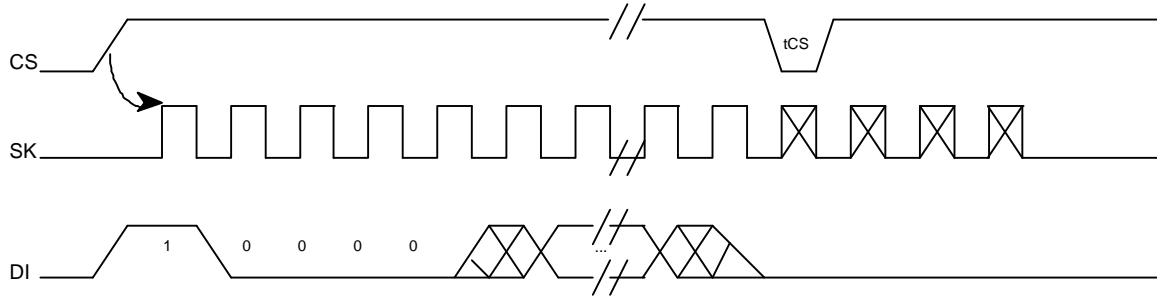


**EWEN TIMING**

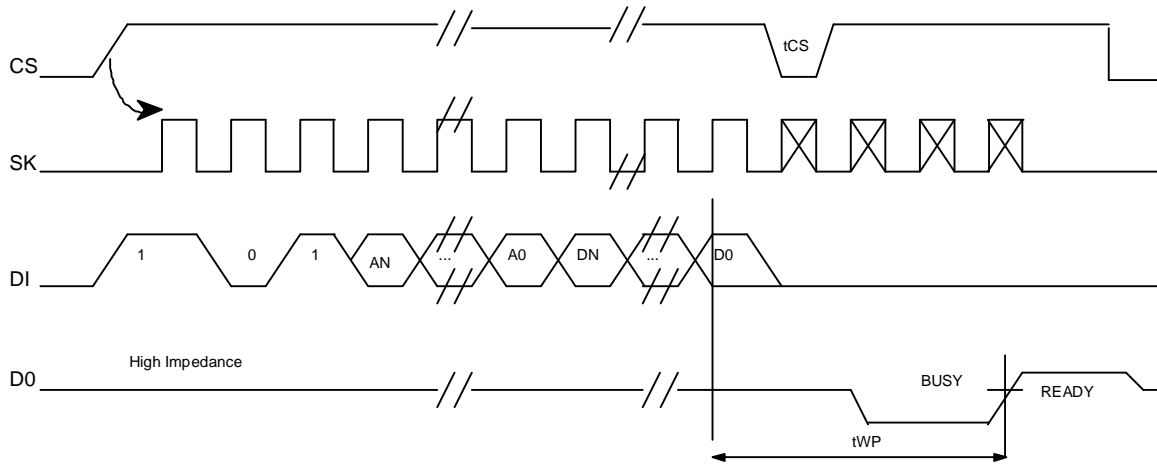




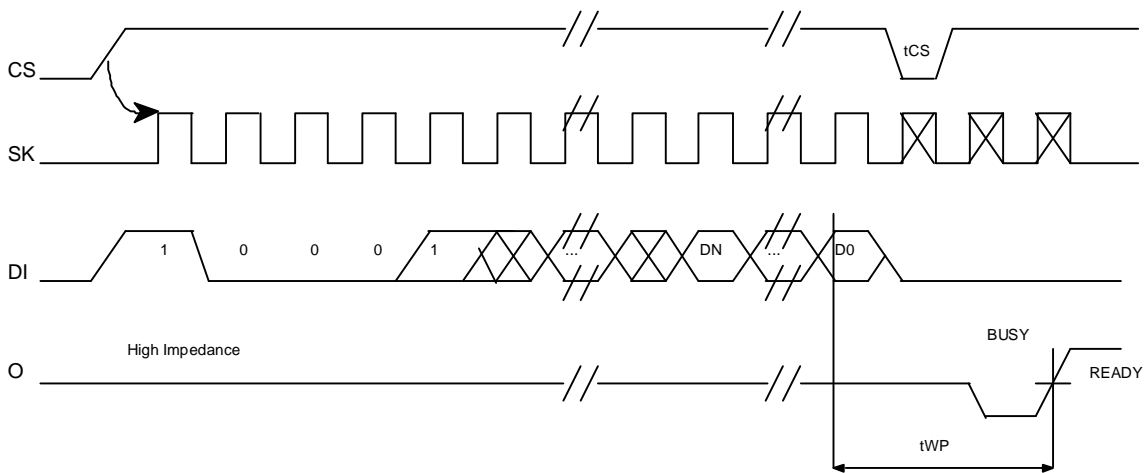
**EWDS TIMING**



**WRITE TIMING**

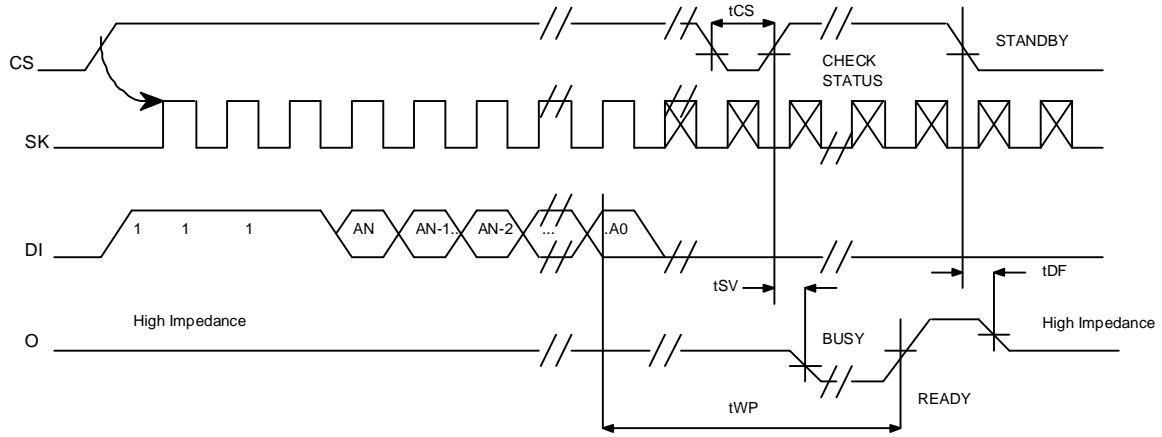


**WRAL TIMING<sup>(1)</sup>**

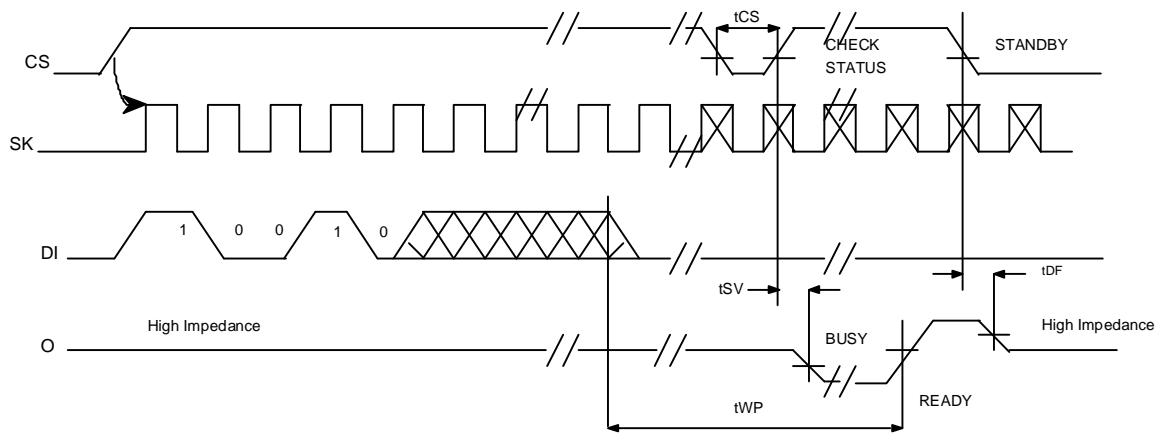


(1) Valid only at Vcc = 4.5V to 5.5V

**ERASE TIMING**



**ERASE TIMING<sup>(1)</sup>**



(1) Valid only at Vcc = 4.5V to 5.5V

### Important statement:

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