TEXAS INSTRUMENTS

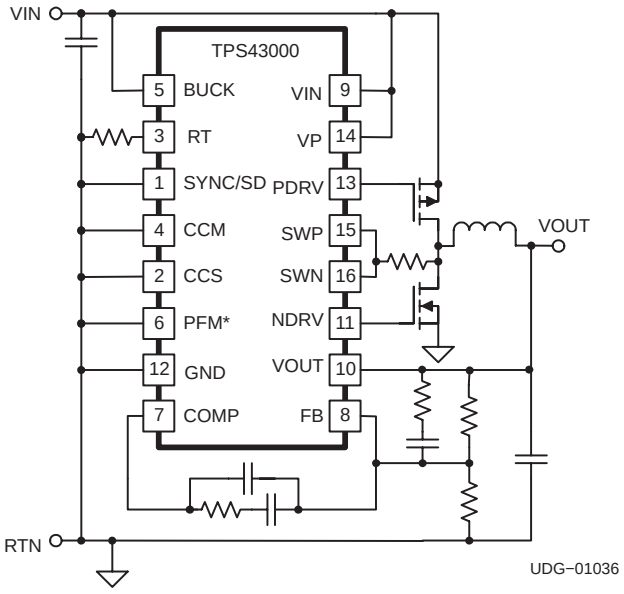
SLUS489 − OCTOBER 2001

MULTI-TOPOLOGY HIGH-FREQUENCY PWM CONTROLLER

FEATURES

- High-Frequency (2-MHz) Voltage Mode PWM Controller
- 1.8-V to 9.0-V Input Voltage Range
- 0.8-V to 8.0-V Output Voltage Range (Higher in Non-Synchronous Boost Topology)
- High-Efficiency Buck, Boost, SEPIC or Flyback (Buck-Boost) Topology
- Synchronous Rectification for High-Efficiency
- Drives External MOSFETs for High-Current Applications
- Synchronizable Fixed-Frequency PWM or Automatic Pulsed Frequency Modulation (PFM) Mode
- Built-In Soft-Start
- User Programmable Discontinuous or Continuous Conduction Mode
- Selectable Pulse-by-Pulse Current Limiting or Hiccup Mode Protection

TYPICAL BUCK APPLICATION



APPLICATIONS

- Networking Equipment
- Servers
- Base Stations
- Cellular Telephones
- Satellite Telephones
- GPS Devices
- Digital Still and Handheld Cameras
- Personal Digital Assistants (PDAs)

DESCRIPTION

The TPS43000 is a high-frequency, voltage-mode, synchronous PWM controller that can be used in buck, boost, SEPIC, or flyback topologies. This highly flexible, full-featured controller is designed to drive a pair of external MOSFETs (one N-channel and one P-channel), enabling it for use with a wide range of output voltages and power levels. With an automatic PFM mode, a shutdown current of less than 1 μA, a sleep-mode current of less than 100 μA and a full operating current of less than 2 mA at 1 MHz, it is ideal for building highly efficient, dc-to-dc converters.

The TPS43000 operates over a wide input voltage range of 1.8 V to 9.0 V. Typical power sources are distributed power systems, two to four nickel or alkaline batteries, or one to two lithium-ion cells. It can be used to generate regulated output voltages from as low as 0.8 V to 8 V or higher. It operates either in a fixed-frequency mode, where the user programs the frequency (up to 2 MHz), or in an automatic PFM mode. In the automatic mode, the controller goes to sleep when the inductor current goes discontinuous, and wakes up when the output voltage has fallen by 2%. In this hysteretic mode of operation, very high efficiency can be maintained over a very wide range of load current. The device can also be synchronized to an external clock source using the dual function SYNC/SD input pin.

description (continued)

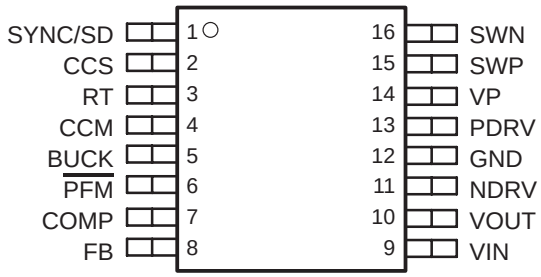
The TPS43000 features a selectable two-level current-limit circuit which senses the voltage drop across the energizing MOSFET. The user can select either pulse-by-pulse current limiting or hiccup mode overcurrent protection. The TPS43000 also features a low-power (LP) mode (which reduces gate charge losses in the N-channel MOSFET at high input/output voltages), undervoltage lockout, and soft-start. The TPS43000 is available in a 16-pin TSSOP (PW) package.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†§

Input voltage (VIN, VP, VOUT) . . . . . −0.3 V to 10 V
(BUCK, CCM, CCS, $\overline{\text{PFM}}$, SYNC/SD) . . . . . −0.3 V to VIN + 0.3 V
(SWN) . . . . . −0.3 V to 17 V
(SWP) . . . . . −0.3 V to VIN + 0.3 V
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Junction temperature range, T_J . . . . . −55°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute- maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to ground. Currents are positive into, negative out of the specified terminals.

PW PACKAGE
(TOP VIEW)



recommended operating conditions

	MIN	MAX	UNIT
Input voltage, VIN, VP		9	V
Input voltage, VOUT		8	
Input voltage, BUCK, CCM, CCS, $\overline{\text{PFM}}$, SYNC/SD, SWP		9	
Input voltage, SWN		17	
Operating junction temperature range, T_J §	−40	85	°C

§ t is not recommended that the device operate for extended periods of time under conditions beyond those specified in this table.

electrical characteristics over recommended operating junction temperature range, T_A = −40°C to 85°C for the TPS43000, RT = 75 kΩ (500 kHz), VIN = VP = 3.5 V, VOUT = 3.1 V, COMP/FB pins shorted, BUCK-configured, $T_A = T_J$ (unless otherwise noted)

VIN

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up voltage	VP = VOUT = 3.5 V, No load	1.45	1.65	1.85	V
Undervoltage lockout (UVLO) hysteresis	No MOSFETs connected	60	150	300	mV
Shutdown current	SYNC/SD = 1.6 V		1	10	µA
	SYNC/SD = VIN		0.5	2	
Operating current	Not in PFM mode, no MOSFETs connected		1.0	1.4	mA
Sleep mode current	PFM mode, COMP/FB=900 mV		75	140	µA
BOOST-configured VIN operating current	Not in PFM mode, no MOSFETs connected, BUCK pin grounded, VIN = 3.1 V, VP = VOUT = 3.5 V		30	75	µA
BOOST-configured VIN sleep mode current	PFM mode, BUCK pin grounded, VP = VOUT = 3.5 V, VIN = 3.1 V, COMP/FB=900 mV		25	60	µA

VOUT

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Shutdown current	SYNC/SD = VIN		0	2	µA
Operating current	Not in PFM mode, no MOSFETs connected		1	5	
Sleep mode current	PFM mode, COMP/FB=900 mV		0	2	
BOOST-configured VOUT operating current	Not in PFM mode, no MOSFETs connected, BUCK pin grounded, VIN = 3.1 V, VP = VOUT = 3.5 V		1.0	1.4	mA
BOOST-configured VOUT sleep mode current	PFM mode, BUCK pin grounded, VP = VOUT = 3.5 V, VIN = 3.1 V, COMP/FB=900 mV		50	120	µA

VP

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Shutdown current	SYNC/SD = VIN		0.5	2	µA
Operating current	Not in PFM mode, no MOSFETs connected		500	800	
Sleep mode current	PFM mode, COMP/FB=900 mV		0	2	

error amplifier

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VREG, regulation voltage (COMP/FB pin)	1.8 V < VIN < 6 V	784	800	816	mV
	VIN = 3.5 V	788	800	812	
FB input current	V_{FB} = 800 mV	−150	−10	150	nA
Sourcing current (out of COMP)	V_{FB} = (VREG − 100 mV), V_{COMP} = 0 V,		−2.0	−0.5	mA
Sinking current (into COMP)	V_{FB} = (VREG + 100 mV), V_{COMP} = 2 V	0.5	1.2		mA
Maximum ouput voltage (COMP pin)	V_{FB} = 0 V, I_{COMP} = −100 µA	1.6	2.0		V
Minimum output voltage (COMP pin)	V_{FB} = 2 V, I_{COMP} = +100 µA		70	120	mV
Unity gain bandwidth	See Note 1		5		MHz

NOTE 1: Ensured by design. Not production tested.

electrical characteristics over recommended operating junction temperature range, T_A = −40°C to 85°C for the TPS43000, RT = 75 kΩ (500 kHz), VIN = VP = 3.5 V, VOUT = 3.1 V, COMP/FB pins shorted, BUCK-configured, $T_A = T_J$ (unless otherwise noted)

soft-start

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Soft-start time	RT = 37.5 kΩ (1 MHz)	1.0	3.0	6.0	ms
	RT = 75 kΩ (500 kHz)	2.0	5.5	12.0	
	RT = 150 kΩ (250 kHz)	4.0	10.5	24.0	

oscillator

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Oscillator frequency	RT = 37.5 kΩ (1 MHz), V_{COMP} = 600 mV	0.90	1.00	1.10	MHz
	RT = 75 kΩ (500 kHz), V_{COMP} = 600 mV	450	500	550	kHz
	RT = 150 kΩ (250 kHz), V_{COMP} = 600 mV	225	250	280	kHz

SYNC/SD

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Synchronization threshold voltage		0.8	1.25	1.6	V
SYNC pulse width	SYNC/SD = 2 V, COMP/FB=600 mV	100	50		ns
SYNC input current	SYNC/SD = 1.6 V		0.5	1	µA
SYNC high to shutdown delay time	Float COMP, V_{FB} = 0 V	10	22	35	µs
Synchronous range	Force COMP/FB to 600 mV	1.1 f_o		1.5 f_o	

current limit

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hiccup overcurrent threshold voltage	Voltage measured from VIN to SWN	175	250	325	mV
Delay to termination of P-channel gate drive time	Measured at PDRV		125	300	ns
BOOST configured hiccup overcurrent threshold voltage	Voltage measured from SWN to GND, BUCK grounded	175	250	325	mV
Delay to termination of N-channel gate drive time	Measured at NDRV, BUCK grounded		150	300	ns
Consecutive overcurrent clock cycles before shutdown		50	63	75	
Clock cycles before restart		800	900	1000	
CCS threshold voltage	Constant current source configured if V_{CCS} > 1 V	0.40	0.70	1.00	V
CCS pull-down current			0.5	1.0	µA
CCS current threshold voltage	Measured from VIN to SWN	85	150	225	mV
BOOST-configured CCS current threshold voltage	Measured from SWN to GND, BUCK grounded	85	150	225	

electrical characteristics over recommended operating junction temperature range, T_A = −40°C to 85°C for the TPS43000, RT = 75 kΩ (500 kHz), VIN = VP = 3.5 V, VOUT = 3.1 V, COMP/FB pins shorted, BUCK-configured, $T_A = T_J$ (unless otherwise noted)

PWM

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK threshold voltage	BUCK configured if V_{BUCK} > 1 V	0.4	0.7	1.0	V
BUCK pull-down current			0.5	1.0	µA
BUCK maximum duty cycle	V_{FB} = 0 V	100%			
BOOST maximum duty cycle	BUCK grounded, V_{FB} = 0 V	70%	90%		
Minimum duty cycle	V_{FB} = 2 V			0%	
CCM threshold voltage	Continuous conduction allowed if V_{CCM} > 1 V	0.4	0.7	1.0	V
CCM pull-down current			0.5	1.0	µA
BUCK rectifier zero current threshold voltage	Measured from SWP to GND	−28	−12	0	mV
BOOST rectifier zero current threshold voltage	Measured from SWP to VOUT, BUCK grounded	0	14	32	mV
Delay to termination of P-channel gate drive time	Measured at PDRV, BUCK grounded		200	300	ns

pulsed frequency modulation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{PFM}$ threshold voltage	PFM mode not allowed if $\overline{PFM}$ > 1 V	0.4	0.7	1.0	V
$\overline{PFM}$ pull-down current			0.5	1.0	µA
FB voltage to awaken (exit sleep mode)		768	784	800	mV
Izero pulses required to enter sleep		5	7	9	
Start-up delay time after sleep			2	5	µs

low power mode

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOUT threshold voltage to enter low power mode	VP = VIN = 5 V	3.45	3.60	3.80	V
VIN threshold voltage to enter low power mode	VP = VOUT = 5 V, BUCK grounded (boost configured)	3.45	3.60	3.80	
Hysteresis voltage to exit low power mode	VOUT < ($V_{THRESHOLD}$−V_{HYST}), VP = VIN = 5 V	225	312	415	mV
	VIN < ($V_{THRESHOLD}$−V_{HYST}), BUCK grounded, VP = VOUT = 5 V	225	312	415	

electrical characteristics over recommended operating junction temperature range, T_A = −40°C to 85°C for the TPS43000, RT = 75 kΩ (500 kHz), VIN = VP = 3.5 V, VOUT = 3.1 V, COMP/FB pins shorted, BUCK-configured, $T_A = T_J$ (unless otherwise noted)

NDRV

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN driven rise time	C_O = 1 nF, VP = VIN = 5 V, VOUT = 3.1 V		25	45	ns
VIN driven fall time			20	40	
VIN driven pull-up resistance	VP = VIN = 5 V, VOUT = 3.1 V		6.5	10.0	Ω
VIN driven pull-down resistance			2.25	4.00	
BUCK P-channel MOSFET off to N-channel MOSFET on anti-x delay time	VP = VIN = 5 V, VOUT = 3.1 V, PDRV and NDRV transitioning HI delta	10	35	75	ns
VOUT driven rise time	C_O = 1 nF, VIN = 3.1 V, VP = VOUT = 5 V, BUCK grounded		25	45	ns
VOUT driven fall time			20	40	
VOUT driven pull-up resistance	VP = VOUT = VIN = 5 V, LP mode activated		6.5	10.0	Ω
VOUT driven pull-down resistance			2.25	4.00	
BOOST P-channel MOSFET off to N-channel MOSFET on anti-x delay time	VP = VOUT = 5 V, VIN = 3.1 V, BUCK grounded	10	35	75	ns

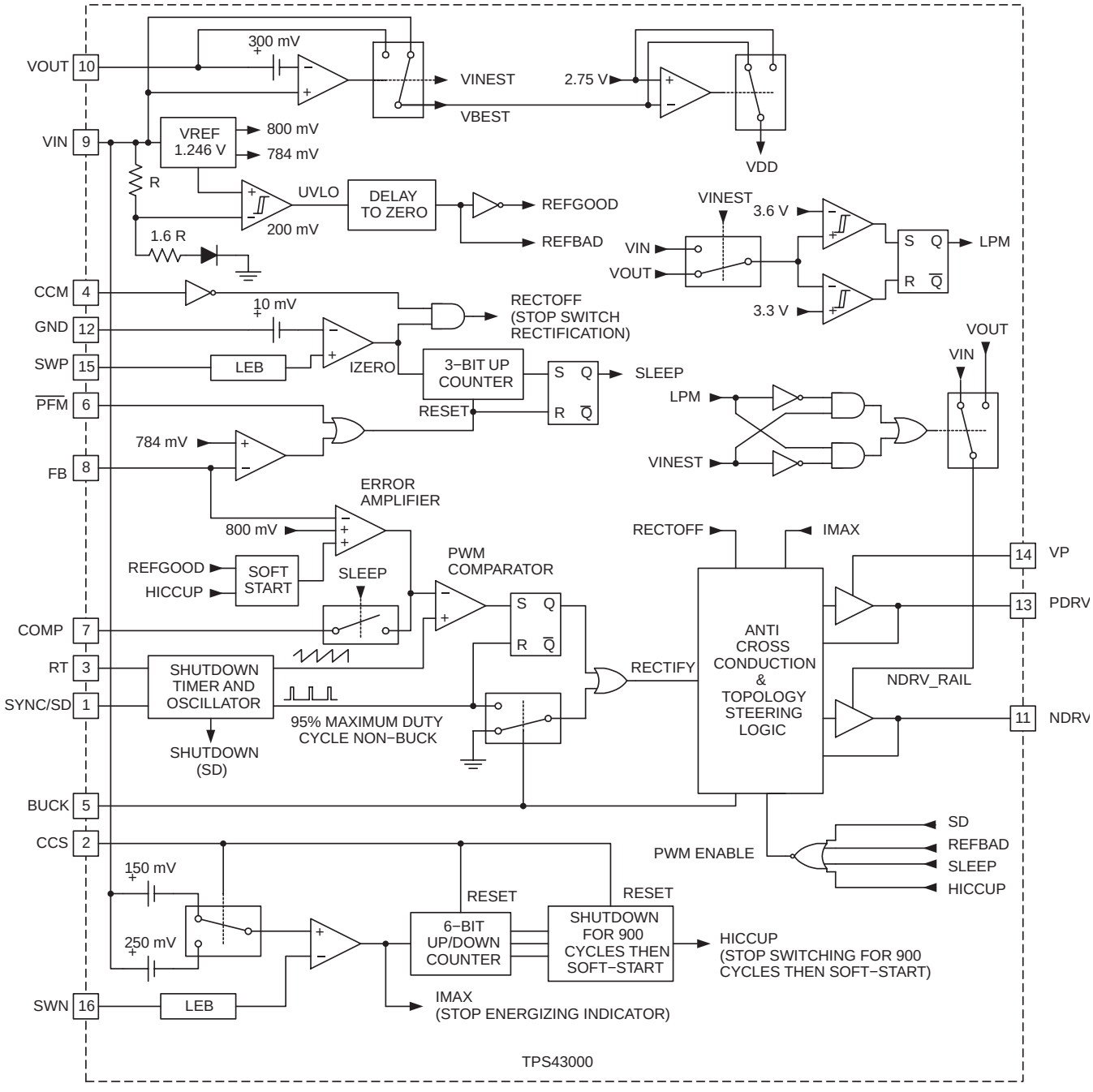
PDRV

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VP driven rise time	VP = VIN = 5 V, VOUT = 3.1 V, C_O = 1 nF		15	40	ns
VP driven fall time			15	40	
VP driven pull-up resistance	VP = VIN = 5 V, VOUT = 3.1 V		2.5	4.0	Ω
VP driven pull-down resistance			3.5	6.0	
BUCK N-channel MOSFET off to P-channel MOSFET on anti-x delay time	VP = VIN = 5 V, VOUT = 3.1 V, NDRV and PDRV transitioning LO delta	10	30	75	ns
BOOST N-channel MOSFET off to P-channel MOSFET on anti-x delay time	VP = VOUT = 5 V, VIN = 3.1 V, BUCK grounded	10	30	75	

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BUCK	5	I	Input pin to select topology. Connect this pin to VIN for a buck converter, ground it for a boost or SEPIC. This configures the logic to the two gate drive outputs, and controls D_{MAX}. This pin has a weak internal pulldown.
CCM	4	I	Input pin determines whether or not the I_{ZERO} comparator allows discontinuous conduction mode operation. Pulling this pin high ignores the Izero comparator's output, forcing continuous conduction mode. Connecting it to ground enables Izero, allowing discontinuous conduction mode (DCM) operation. Note that even when pulled high, seven detected I_{ZERO} pulses still initiate PFM mode. This pin has a weak internal pull-down.
CCS	2	I	Current limit feature allowing selection of either pulse-by-pulse current limiting or hiccup mode overcurrent protection. Connect this pin to VIN to select pulse-by-pulse current limiting, the constant current source mode. Connect this pin to ground to enable hiccup mode overcurrent protection. This pin has a weak internal pulldown.
COMP	7	O	Output of the error amplifier. The compensation components are connected from this pin to the FB pin. During sleep mode, this pin goes to high impedance, and is severed from the internal error amplifier's output so that it may hold its dc potential.
FB	8	I	Inverting input to the error amplifier. It is connected to a resistor divider off of VOUT, and to the compensation network.
GND	12	−	Ground pin for the device.
NDRV	11	O	Gate drive output for the N-channel MOSFET (energizing MOSFET for the boost and SEPIC, rectifier MOSFET for the buck).
PDRV	13	O	Gate drive output for the P-channel MOSFET (energizing MOSFET for the buck, rectifier MOSFET for the boost and SEPIC).
$\overline{\text{PFM}}$	6	I	Input pin that disables/enables PFM operation. Connecting it to VIN disables PFM mode. Grounding this pin enables PFM to occur automatically, based on Izero. This pin has a weak internal pulldown.
RT	3	O	A resistor from this pin to ground sets the PWM frequency.
SWP	15	I	Connect this pin through a 1-kΩ resistor to the drain of the P-channel MOSFET for all topologies. It detects Izero pulses using the synchronous rectifier MOSFET. For the SEPIC topology, a Schottky clamp tied to ground must be connected to this pin.
SWN	16	I	Connect this pin through a 1-kΩ resistor to the drain of the N-channel MOSFET for all topologies. It senses overcurrent conditions using the inductor energizing MOSFET.
SYNC/SD	1	I	This dual-function pin is used to synchronize the oscillator or shutdown the controller, turning both MOSFETs off. A pulse from 0 V to 2 V provides synchronization. Duty cycle is not critical, but it must be at least 100 ns wide. Holding this pin to 2 V or greater for over 35 µs shuts down the device. This pin has a weak internal pulldown.
VP	14	I	Power rail input pin for the P-channel MOSFET gate driver. Connect this pin to VIN for a buck, and to VOUT for a boost or SEPIC. Provide good local decoupling.
VIN	9	I	Input supply for the device. It provides power to the device, and may be used for the N−channel gate drive. Provide good local decoupling
VOUT	10	O	Connect this pin to the power supply output. It may be used for the gate drive to the N−channel MOSFET. Provide good local decoupling.

functional block diagram



UDG−01043

APPLICATION INFORMATION

general information

The TPS43000 is a high-frequency, synchronous PWM controller optimized for distributed power, or battery-powered applications where size and efficiency are of critical importance. It includes high-speed, high-current MOSFET drivers for those applications requiring low $R_{DS(on)}$ external MOSFETs. (See functional block diagram).

optimizing efficiency

The TPS43000 optimizes efficiency and extends battery life with its low quiescent current and its synchronous rectifier topology. The additional features of low-power (LP) mode and PFM mode maintain high efficiency over a wide range of load current.

modes of operation

The TPS43000 has four distinct modes of operation:

- fixed PWM with discontinuous conduction mode (DCM) possible
- fixed PWM with forced continuous conduction mode (CCM)
- automatic pulse frequency modulation (PFM) with DCM possible
- PFM with forced CCM

The device mode is controlled by the CCM and $\overline{\text{PFM}}$ pins. The CCM pin lets the user decide whether to allow DCM by connecting the pin to ground or to force CCM by connecting the pin to VIN. The $\overline{\text{PFM}}$ pin lets the user decide whether to allow automatic PFM by connecting the pin to ground or to force fixed PWM by connecting the pin to VIN.

fixed PWM with DCM possible ($\overline{\text{PFM}}$ tied to VIN; CCM tied to ground)

In this mode, the device behaves like a standard switching regulator with the addition of a synchronous rectifier. Shortly after the energizing MOSFET turns off, the synchronous rectifier turns on. The synchronous rectifier turns off either when the inductor current goes discontinuous (DCM) or just prior to the start of the next clock cycle (CCM) when the energizing MOSFET turns on. During the small time interval when neither the energizing MOSFET nor the synchronous rectifier are turned on, the synchronous rectifier MOSFET body diode (or an optional small external Schottky diode in parallel) carries the current to the output until it goes discontinuous. The efficiency drops off at light loads as the losses become a larger percentage of the delivered load.

APPLICATION INFORMATION

fixed PWM with forced CCM ($\overline{PFM}$ and CCM tied to VIN)

CCM is forced under all operating conditions in this mode. The synchronous rectifier turns on shortly after the energizing MOSFET turns off and remains on until just prior to the start of the next clock cycle when the energizing MOSFET turns on. The user should design the converter to operate in CCM over its entire operating range in order to prevent the inductor current from going negative. If the converter is allowed to run discontinuous, the inductor current goes negative (i.e. the output discharges as the current reverses and goes back through the rectifier to the input or ground.) With fixed PWM, the efficiency drops off at light loads as the losses become a larger percentage of the delivered load.

PFM with DCM possible ($\overline{PFM}$ and CCM tied to ground)

In this mode, the device can operate in either fixed PWM or in PFM mode. When the device is initially powered, it operates in fixed PWM mode until soft-start completion. It remains in this mode until it senses that the converter is on the verge of breaking into discontinuous operation. When this condition is sensed, the converter enters PFM mode, invoking a sleep state until the output voltage falls 2% below nominal (a 16-mV drop measured at the FB pin). At this time, the controller starts up again and operates at its fixed PWM frequency for a short duration (load dependent, typically 10 to 200 PWM cycles), increasing the output voltage. If the controller again senses the converter is on the verge of going discontinuous, the cycle repeats. If discontinuous operation is not sensed, the converter remains in fixed PWM mode. PFM mode results in a very low duty cycle of operation, reducing all losses and greatly improving light load efficiency. During the sleep state, most of the circuitry internal to the TPS43000 is powered down. This reduces quiescent current, which lowers the average dc operating current, enhancing its efficiency.

PFM with forced CCM ($\overline{PFM}$ tied to ground; CCM tied to VIN)

This mode is similar to the PFM with DCM possible mode except that the controller forces the converter to operate in CCM. The converter can be designed to run discontinuous at light loads. The controller senses discontinuous operation and enters the PFM mode. With PFM, the converter can maintain a very high efficiency over a very wide range of load current.

anticross−conduction and adaptive synchronous rectifier commutation logic

When operating in the continuous conduction mode (CCM), the energizing MOSFET and the synchronous rectifier MOSFET are simply driven out of phase, so that when one is on the other is off. There is a built-in time delay of about 40 ns to prevent any cross-conduction.

In the event that the converter is operating in the discontinuous conduction mode (DCM), the synchronous rectifier needs to be turned off quickly, when the rectifier current drops to zero. Otherwise, the output begins to discharge as the current reverses and goes back through the rectifier to the input or ground (this obviously cannot happen when using a conventional diode rectifier). To prevent this, the TPS43000 incorporates a high-speed comparator that senses the voltage on the synchronous rectifier using the SWP input, which is connected to the synchronous rectifier MOSFET's drain through a 1-kΩ resistor. This comparator is used to determine when the inductor current is on the verge of going discontinuous and is referred to as the I_{ZERO} comparator. In the boost and SEPIC (single-ended primary inductance converter) topologies, the synchronous rectifier is turned off when the voltage on the SWP pin decreases to within 12 mV of VOUT. For this reason, it is important to have the VOUT pin well decoupled. In the buck topology, the synchronous rectifier is turned off when the voltage on the SWP pin increases to −12 mV with respect to ground. The I_{ZERO} threshold is defined as follows:

$$I_{ZERO} = \frac{12\ mV}{R_{DS(on)}} \quad (1)$$

APPLICATION INFORMATION

When the $R_{DS(on)}$ of the MOSFET is used as the sense element, several issues arise. Before the I_{ZERO} comparator is enabled, the MOSFET must be fully enhanced, and the drain-to-source voltage must be allowed to settle. The TPS43000 has an internal circuit that enables the I_{ZERO} comparator approximately 40 ns after the rectifier MOSFET is enhanced.

> **NOTE:** For the SEPIC topology, the voltage on the drain of the rectifier MOSFET swings to −VIN when the energizing MOSFET is on. Therefore, in order to prevent the SWP input pin from being damaged, it must connect to a Schottky diode clamp to ground.

PFM mode

For improved efficiency at light loads, the TPS43000 can be programmed to automatically enter PFM (Pulse Frequency Modulation) mode by connecting the $\overline{PFM}$ pin to ground. PFM is initiated by the I_{ZERO} comparator used for synchronous rectifier commutation. An internal digital counter is used to count the number of I_{ZERO} pulses at the output of the I_{ZERO} comparator. When seven I_{ZERO} pulses occur, the controller enters sleep state until the voltage at the FB pin falls to approximately 784 mV (output voltage drops 2% below nominal). At this time, the controller turns back on and operates at its fixed-frequency for a short duration (load dependent, typically 10 to 200 PWM cycles) increasing the output voltage. The cycle repeats when another seven I_{ZERO} pulses occur. This results in a very low duty cycle of operation, reducing all losses and improving light load efficiency. During the sleep state, most of the circuitry internal to the TPS43000 is powered down. This reduces quiescent current, which lowers the average dc operating current, enhancing its efficiency. The error amplifier output is disconnected from the COMP pin during the sleep state. The COMP pin goes to high impedance and maintains approximately the same voltage level it was at when it entered the sleep state. This minimizes error amplifier overshoot/undershoot when coming out of the sleep state. The user can disable PFM by connecting the $\overline{PFM}$ pin to VIN.

low power mode

At relatively high gate drive voltages, gate drive losses can become excessive and begin to dominate under light load conditions. The expression for gate drive power loss is given by equation (2). The power varies as a function of the applied gate voltage squared.

$$P_{GATELOSS} = \frac{Q_G \times \left(V_G\right)^2 \times f}{V_S}, \quad (2)$$

where Q_G is the total gate charge, V_S is the gate voltage specified in the MOSFET manufacturer's data sheet, V_G is the applied gate drive voltage, and f is the switching frequency.

When both VIN and VOUT are above 3.6 V, the TPS43000 automatically enters LP mode and selects the lower voltage of VIN or VOUT to provide the gate drive voltage on the NDRV pin. This minimizes gate drive losses at relatively high input and output voltages and helps maintain high efficiency at light loads. The PDRV pin remains powered by either VIN (buck topology) or VOUT (boost, flyback, and SEPIC topologies) via the VP power input pin.

To help provide a smooth transition in and out of LP mode, its circuitry has 300 mV of hysteresis. When either VIN or VOUT drops below 3.3 V, the TPS43000 transitions back to *normal* mode and the NDRV pin is powered by the higher potential of VIN or VOUT.

APPLICATION INFORMATION

synchronization and shutdown

The TPS43000 incorporates a dual function synchronization and shutdown pin. It may be used to synchronize the TPS43000's switching frequency to an external clock, or to shutdown the device entirely.

To synchronize the internal clock to an external source, the SYNC/SD pin must be driven high, greater than 1.6 V. The circuitry synchronizes to the rising edge of the input. Duty cycle is not critical, but the pulse width must be at least 100 ns wide but less than 10 μs to avoid shutdown. The external SYNC clock should be between 10% and 25% above the free-running switching frequency.

To ensure a shutdown of the converter, the SYNC/SD pin must be held high (above 1.6 V) for a minimum of 35 μs. In shutdown, both the energizing and rectifier MOSFETs are turned off. The quiescent current is reduced to less than 10 μA with 1.6 V applied to SYNC/SD and less than 2 μA with VIN potential applied to SYNC/SD. Bringing this pin low again allows the device to resume operation, starting with a full soft-start cycle.

overcurrent protection

The TPS43000 allows the user to select either pulse-by-pulse current limiting or hiccup mode overcurrent protection using the CCS pin. To minimize external part count and minimize losses, the energizing MOSFET's $R_{DS(on)}$ is used as the current sense element. The TPS43000 incorporates a high-speed comparator, referred to as the I_{MAX} comparator, that senses the voltage across the energizing MOSFET using the SWN input ,which is connected to the energizing MOSFET's drain through a 1-kΩ resistor. The I_{MAX} comparator compares its SWN input to either ground (boost, flyback, and SEPIC topologies) or VIN (buck topology). Before the I_{MAX} comparator is enabled, the energizing MOSFET must be fully enhanced, and the drain-to-source voltage must be allowed to settle. The TPS43000 has an internal circuit that enables the I_{MAX} comparator approximately 60 ns after the energizing MOSFET is enhanced.

pulse-by-pulse current limiting − constant current source mode (CCS tied to VIN)

In the pulse-by-pulse current limiting mode, the energizing MOSFET gate drive is terminated once the overcurrent threshold is reached. An overcurrent, I_{MAX}, is sensed when the voltage drop across the energizing MOSFET reaches 150 mV. The pulse-by-pulse current limiting threshold is defined by the equation:

$$I_{MAX(pp)} = \frac{150\ mV}{R_{DS(on)}} \tag{3}$$

In the boost, flyback, and SEPIC topologies, IMAX(pp) is reached when the voltage on the SWN pin is 150 mV above ground. In the buck topology, IMAX(pp) is reached when the voltage on the SWN pin is 150 mV below VIN. For this reason, it is important to have the VIN pin well decoupled. Pulse-by-pulse current limiting is enabled by connecting the CCS input pin to VIN.

hiccup mode over current protection (CCS tied to ground)

In the hiccup mode overcurrent protection scheme, an internal digital counter is used to count the number of I_{MAX} pulses at the output of the I_{MAX} comparator. An I_{MAX} condition is sensed when the voltage drop across the energizing MOSFET reaches 250 mV. The hiccup mode overcurrent threshold is defined by the equation:

$$I_{MAX(hu)} = \frac{250\ mV}{R_{DS(on)}} \tag{4}$$

In the boost, flyback, and SEPIC topologies, $I_{MAX(hu)}$ condition is reached when the voltage on the SWN pin is 250 mV above ground. In the buck topology, $I_{MAX(hu)}$ condition is reached when the voltage on the SWN pin is 250 mV below VIN. When 63 $I_{MAX(hu)}$ pulses are reached, both the energizing MOSFET and rectifier MOSFET are turned off. The MOSFET switches are held off for 882 clock cycles before a soft-start is initiated. Hiccup mode overcurrent protection is enabled by connecting the CCS input pin to ground.

APPLICATION INFORMATION

start-up and soft-start

The TPS43000 incorporates an UVLO circuit that disables the output drivers when the voltage at the VIN pin is below 1.65 V. In order to prevent the converter from oscillating during low input voltage startup, the UVLO circuit is designed with 200 mV of hysteresis and the converter remains on until VIN drops below 1.45 V.

The TPS43000 has a built-in soft-start that varies as a function of the switching frequency. The soft-start is a closed-loop soft-start, meaning that the reference input to the error amplifier is ramped up over the soft-start interval and the converter control loop is allowed to track the ramping reference signal. The soft-start interval is set to approximately 2000 oscillator clock cycles. This method generally allows for faster soft-start times with minimal output voltage overshoot at startup. During start-up, the synchronous rectifier is held off until the COMP pin reaches 700 mV.

programming the PWM frequency

The oscillator frequency is programmed by a resistor from the RT pin to ground. The approximate operating frequency is determined by the equation:

$$f_{SW}\,(\text{MHz}) = \frac{38}{R_T\,(\text{k}\Omega)} \tag{5}$$

The maximum operating frequency is 2 MHz. Some applications may want to remain in a fixed-frequency mode of operation, even at light load, rather than going into PFM mode. This lowers efficiency at light load. One way to improve the efficiency while maintaining fixed frequency operation is to lower the PWM frequency under light-load conditions. This can be easily done, as shown in Figure 1. By adding a second timing resistor and a small MOSFET switch, the host can switch between two discrete frequencies at any time.

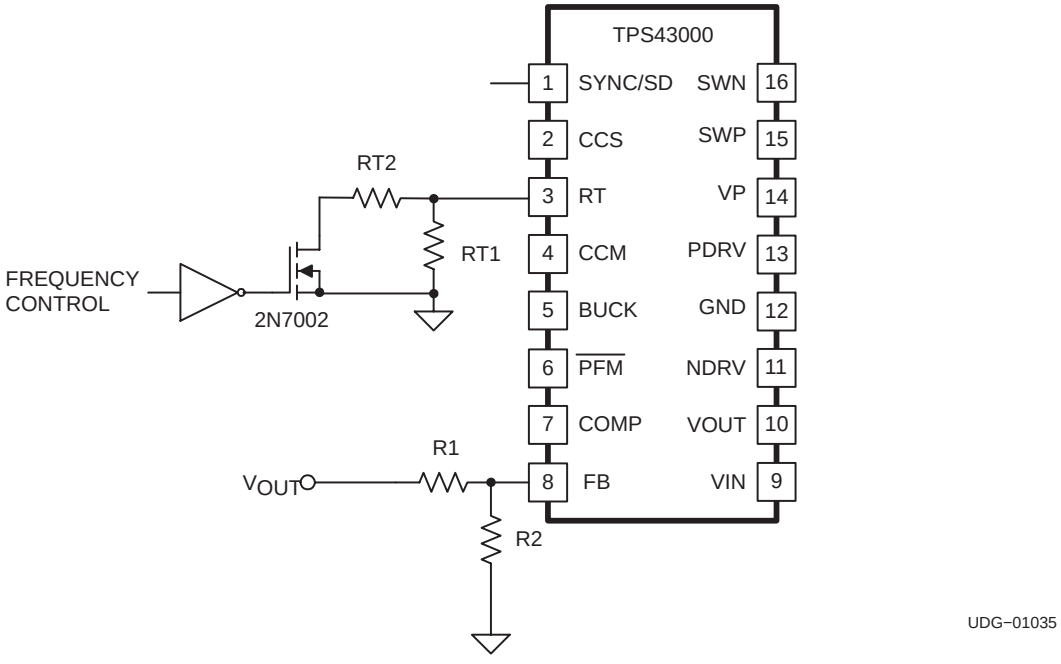


Figure 1. Changing the PWM Frequency

APPLICATION INFORMATION

error amplifier

The TPS43000 uses voltage mode control for each of the topologies. The output voltage is sensed and fed back to the FB pin (inverting input) and compared to an internal 800 mV reference connected to the non-inverting input. The difference (i.e. error voltage), is amplified by the internal error amplifier. The output of the error amplifier (COMP), is then compared to the oscillator sawtooth ramp to control the pulse width used to drive the power switch (energizing MOSFET). The duty cycle is varied to regulate the output voltage. The higher the error voltage, the longer the energizing MOSFET switch is on.

The transient response of a converter is a function of both small signal and large signal responses. The small signal response is determined by the error amplifier's loop compensation (feedback network), whereas the large signal response is a function of the error amplifier's gain bandwidth and slew rate (dv/dt) as well as the slew rate of the inductor current (di/dt). The TPS43000 internal error amplifier has a 5-MHz unity gain bandwidth. This almost assures that the loop bandwidth is limited by external circuit characteristics rather than error amplifier limitations. The internal error amplifier is capable of sourcing and sinking an ensured 500 μA, which assures that even during large signal transients, external components determine circuit behavior. Using low feedback capacitance allows the error amplifier to rapidly slew from one level to another, insuring excellent transient response.

loop compensation

The voltage loop needs to be compensated to provide control loop stability margin, and to minimize the output voltage overshoot/undershoot response to line and load transients. A Type III error amplifier compensation network can be used to optimize the loop response for any of the topologies and operating modes implemented with the TPS43000. The Type III amplifier circuit is shown in Figure 2. This configuration has a pole at the origin and two zero-pole pairs. It can provide up to 180° of phase boost.

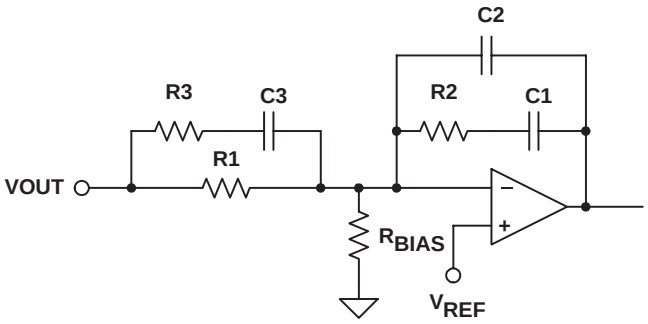


Figure 2. Type III Error Amplifier Compensation Network

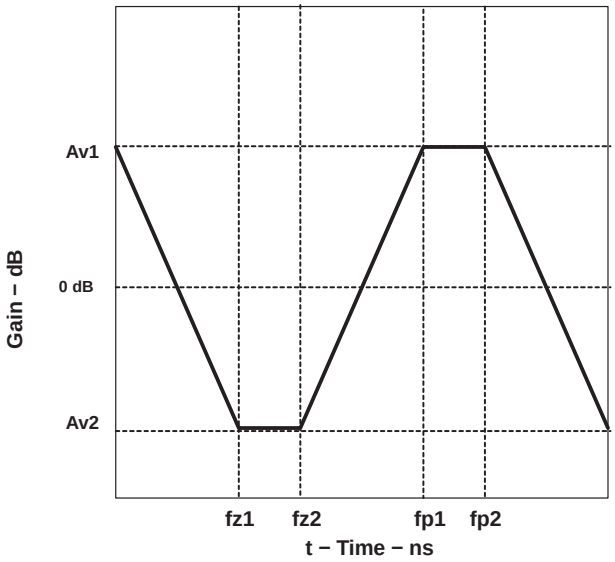


Figure 3. Type III Error Amplifier Compensation Gain Response

APPLICATION INFORMATION

The frequency of the poles and zeros are defined by the following equations:

zeros

$$f_{z1} = \frac{1}{(2\pi \times R2 \times C1)} \quad (6)$$

$$f_{z2} \approx \frac{1}{(2\pi \times R1 \times C3)}, \text{ assuming } R1 \gg R3 \quad (7)$$

poles

$$f_{p1} = \frac{1}{(2\pi \times R3 \times C3)} \quad (8)$$

$$f_{p2} \approx \frac{1}{(2\pi \times R2 \times C2)}, \text{ assuming } C1 \gg C2 \quad (9)$$

In voltage mode control, the buck, boost, flyback, and SEPIC toplogies all have a 2nd order double-pole LC filter characteristic when operated in CCM. In the buck topology, the frequency of the LC double pole is straight forward.

$$f_{LC} = \frac{1}{\left(2\pi(LC)^{1/2}\right)} \text{ buck topology} \quad (10)$$

In the boost, flyback, and SEPIC toplogies, the frequency of the LC double pole varies as a function of the duty cycle.

$$f_{LC} = \frac{(1 - D)}{\left(2\pi(LC)^{1/2}\right)} \text{ boost, flyback, \& SEPIC topologies} \quad (11)$$

In addition, each of the topologies have an ESR zero, which occurs when the output capacitor impedance transitions from capacitive to resistive. The frequency at which this occurs is the ESR zero frequency, f_{ESR}, and is defined by the equation:

$$f_{ESR} = \frac{1}{2\pi \left(R_{ESR}\right) \times C} \quad (12)$$

In the boost, flyback, and SEPIC topologies operated in CCM, there is also a right half-plane (RHP) zero. The RHP zero has the same positive gain slope as the conventional zero, but has a 90° phase lag. This combination, in conjunction with its dependence on line and load, make it nearly impossible to compensate within the control loop. The frequency at which this RHP zero occurs, f_{RHP}, is defined by the equations:

$$f_{RHP} = \frac{R_O \times (1 - D)^2}{(2\,\pi\,L)} \text{ boost topology} \quad (13)$$

$$f_{RHP} = \frac{R_O \times (1 - D)^2}{(2\,\pi\,LD)} \text{ flyback topology} \quad (14)$$

where R_O is the equivalent output load resistance.

APPLICATION INFORMATION

With voltage-mode control, the closed-loop design goal for each of the topologies with the Type III error amplifier compensation is to set the crossover frequency above the resonant frequency of the LC filter (prevents filter oscillations during a transient response), but below the lowest possible RHP zero frequency. This is accomplished by setting the two zeros in the compensation network before the LC double pole frequency. This provides a phase boost. The two poles should be placed a decade above the crossover frequency.

The following is a typical procedure for selecting the loop compensation values for a buck converter operated in CCM:

Step 1. Select the desired crossover frequency a decade above the LC pole frequency.
Step 2. Set the resistor divider formed by R1 and R_{BIAS} to develop the desired regulation voltage. Note that R_{BIAS} sets the dc operating point of the loop, but has no effect on ac operation and does not factor into the loop compensation calculations.
Step 3. Set the zero formed by R1 and C3 to approximately one-half decade above the LC double pole to compensate for the phase loss.
Step 4. Set the zero formed by R2 and C1 to approximately one-half decade below the LC double pole to avoid a conditional instability.
Step 5. Set the pole formed by R3 and C3 to cancel the ESR zero of the output capacitor.
Step 6. Set the pole formed by R2 and C2 to approximately one-half decade above the crossover frequency.

If the converter is operated in DCM, the lead network (R3 and C3 in Figure 2) can be eliminated for all topologies. This configuration is referred to as a Type II error amplifier compensation network and has a pole at the origin and a single zero-pole pair. It can provide up to 90° of phase boost. The frequency of the pole and zero are defined by the following equations:

zero

$$f_{z1} = \frac{1}{(2\pi \times R2 \times C1)} \quad (15)$$

pole

$$f_{p1} \approx \frac{1}{(2\pi \times R2 \times C2)}, \text{ Assuming } C1 \gg C2 \quad (16)$$

The zero-pole pair is used to compensate for the power circuit's ESR zero and the pole formed by the output capacitor and the effective output resistance.

APPLICATION INFORMATION

design examples: buck, boost, non-synchronous boost, flyback, and SEPIC

buck converter

The buck topology is simple and efficient, and should be used whenever the desired output voltage is less than the minimum input voltage. Figure 4 shows the TPS43000 in a typical (750 kHz) buck converter with an input voltage range of 3.0 V to 9.0 V, an output voltage of 2.7 V, and a load current from 0 A to 2 A.

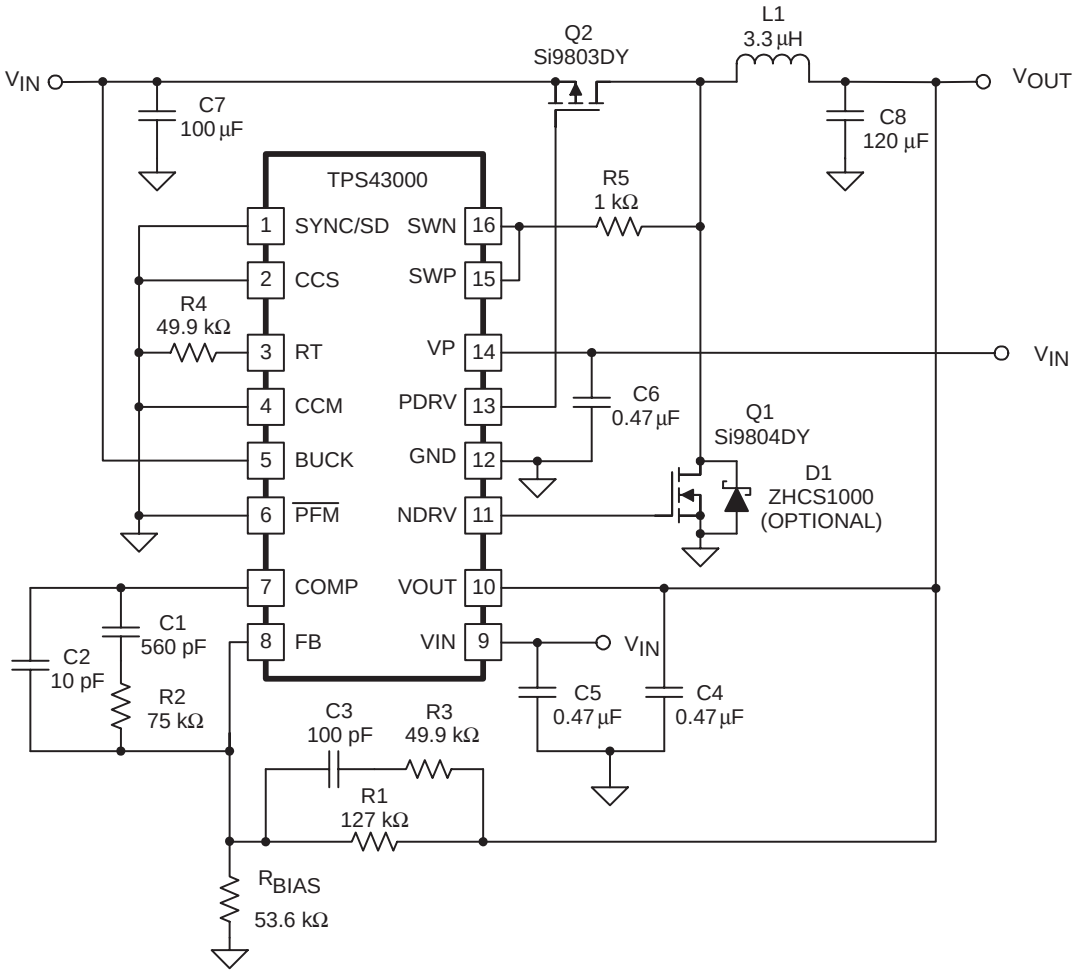


Figure 4. 2.7-V Output Buck Topology

For a buck converter, the average output current is related to the peak inductor current by:

$$I_{pk} = I_{OUT} + \frac{\left(V_{IN} - V_{OUT}\right) \times D}{\left(2 \times f_{SW} \times L\right)} \quad (17)$$

APPLICATION INFORMATION

where f_{SW} is the switching frequency, L is the inductor value, and D is the duty cycle. The duty cycle for a buck converter is defined as:

$$D = \frac{V_{OUT}}{V_{IN}} \tag{18}$$

Note that in these equations the voltage drop across the rectifier has been neglected.

boost converter

The boost topology is simple and efficient, and should be used whenever the desired output voltage is greater than the maximum input voltage. Figure 5 shows the TPS43000 in a typical (750 kHz) boost converter with an input voltage range of 2.5 V to 4.5 V, an output voltage of 5.0 V, and a load current from 0 A to 1 A.

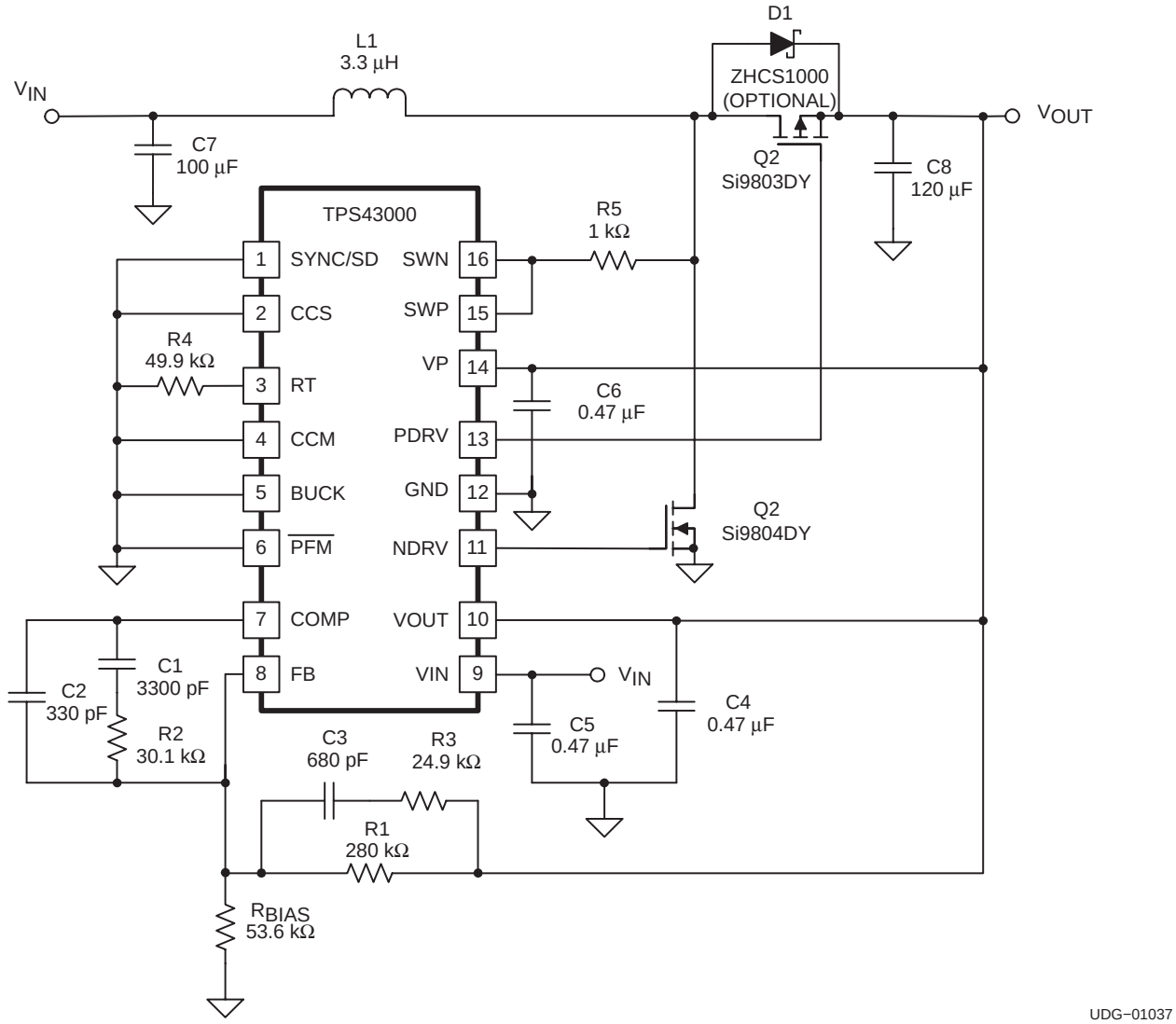


Figure 5. 5-V Output Boost Topology

APPLICATION INFORMATION

For a boost converter, the average output current is related to the peak inductor current by the following equation:

$$I_{pk} = \frac{\left(V_{OUT} \times I_{OUT}\right)}{\left(\eta \times V_{IN}\right)} + \frac{\left(V_{IN} \times D\right)}{\left(2 \times f_{SW} \times L\right)} \quad (19)$$

where f_{SW} is the switching frequency, L is the inductor value, and D is the duty cycle. The duty cycle for a boost converter is defined as:

$$D = \frac{\left(V_{OUT} - V_{IN}\right)}{V_{OUT}} \quad (20)$$

Note that in these equations the voltage drop across the rectifier has been neglected.

non−synchronous boost converter

The TPS43000 can also be used in non-synchronous applications to provide output voltages greater than 8 V from low voltage inputs. Figure 6 shows the TPS43000 in a non-synchronous boost converter (750 kHz) application with an input voltage range of 2.5 V to 9.0 V, an output voltage of 12 V, and a load current from 0 A to 1 A. Since none of the device pins are exposed to the boosted voltage, the output voltage is limited only by the ratings of the external MOSFET, rectifier, and filter capacitor. At these higher output voltages, good efficiency is maintained since the rectifier drop is small compared to the output voltage. Note that the PFM mode can still be used to maintain high efficiency at light load.

Since all the power supply pins (VIN, VOUT, VP) operate off the input voltage, it must be greater than 2.5 V and high enough to assure proper gate drive to the charge MOSFET.

APPLICATION INFORMATION

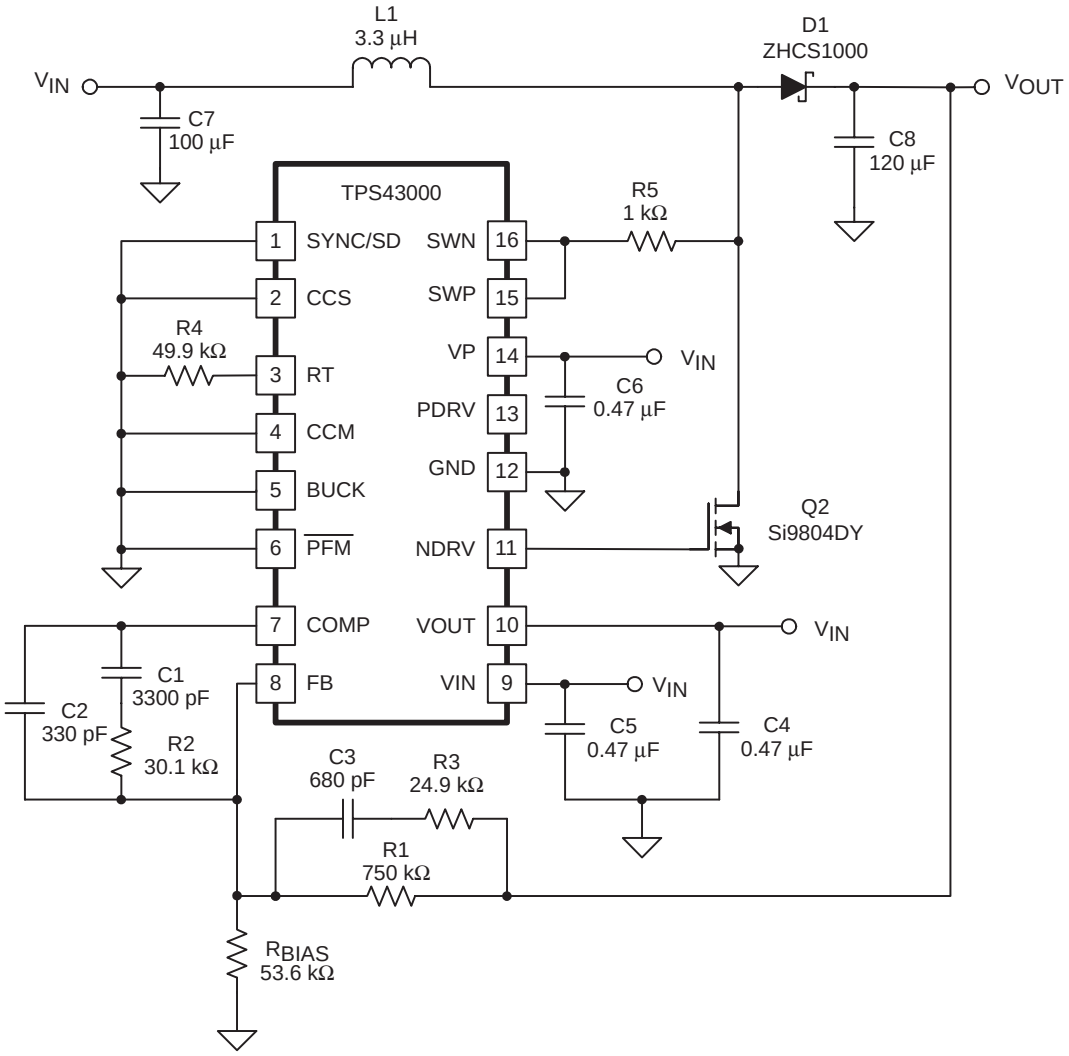


Figure 6. 12-V Output Non-Synchronous Boost Topology

APPLICATION INFORMATION

flyback converter

A flyback converter (750 kHz) using the TPS43000 is shown in Figure 7. It uses a standard two-winding coupled inductor with a 1:1 turns ratio. The advantage of this topology is that the output voltage can be greater or less than the input voltage. For example, this is ideal for generating 3.3 V from a lithium-ion cell.

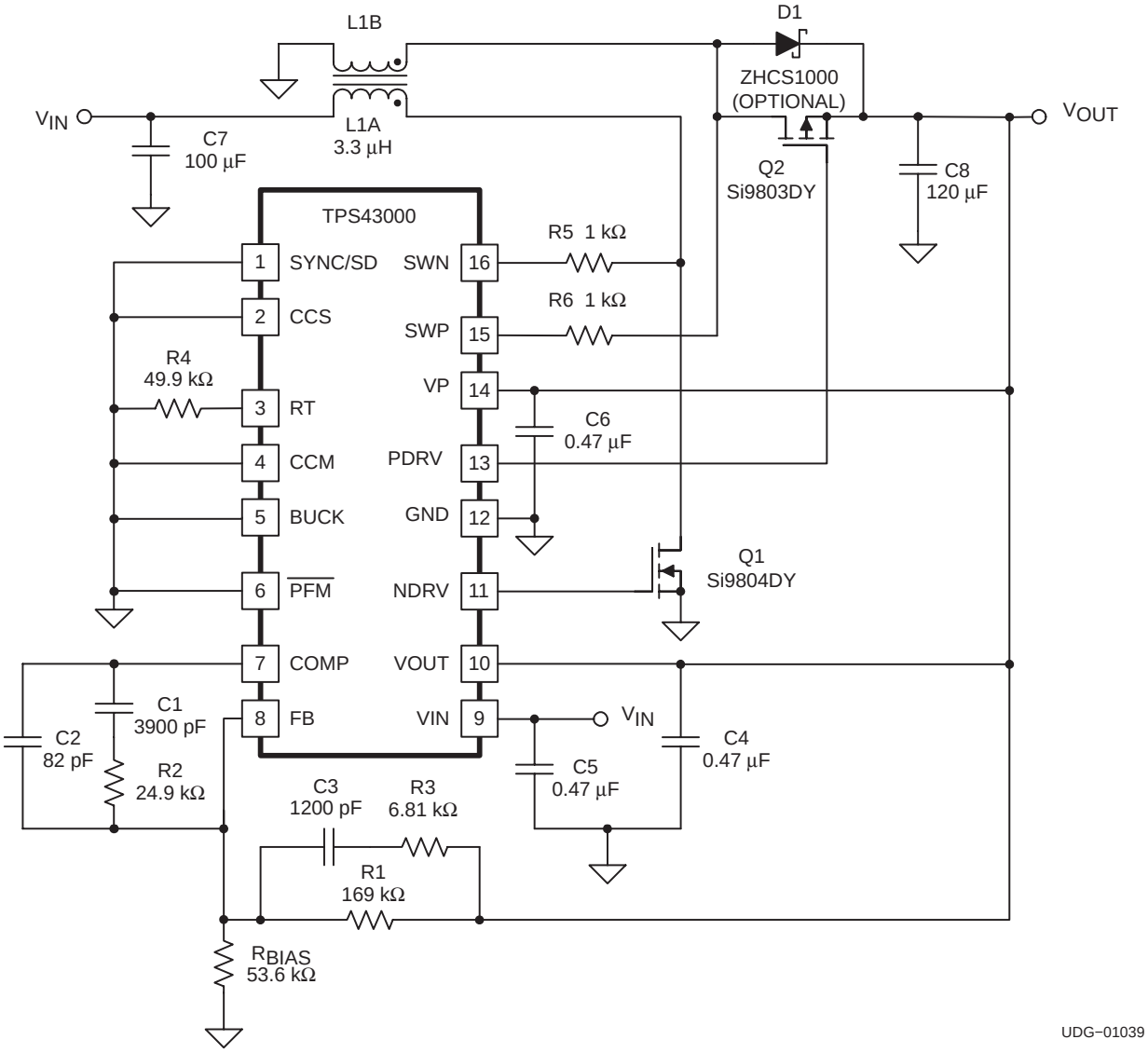


Figure 7. 3.3-V Output Flyback Topology

NOTE: Resistor-capacitor snubbers can be placed across the primary and secondary windings to reduce ringing due to leakage inductance. These are optional, and may not be required in the application.

For a flyback converter, the average output current is related to the peak inductor current by:

$$I_{pk} = \frac{\left(V_{OUT} \times I_{OUT}\right)}{\left(\eta \times V_{IN}\right)} + \frac{\left(V_{IN} \times D\right)}{\left(2 \times f_{SW} \times L\right)} \quad (21)$$

where f_{SW} is the switching frequency, L is the inductor value, and D is the duty cycle. The duty cycle for a flyback converter is defined as:

$$D = \frac{V_{OUT}}{\left(V_{IN} + V_{OUT}\right)} \quad (22)$$

Note that in these equations the voltage drop across the rectifier has been neglected.

SEPIC converter

The TPS43000 may also be used in the SEPIC topology. This topology, which is similar to the flyback, uses a capacitor to aid in energy transfer from input to output. Figure 8 shows the TPS43000 in a SEPIC converter (750 kHz) application with an input voltage range of 2.5 V to 6.0 V, an output voltage of 3.3 V, and a load current from 0 A to 1 A.

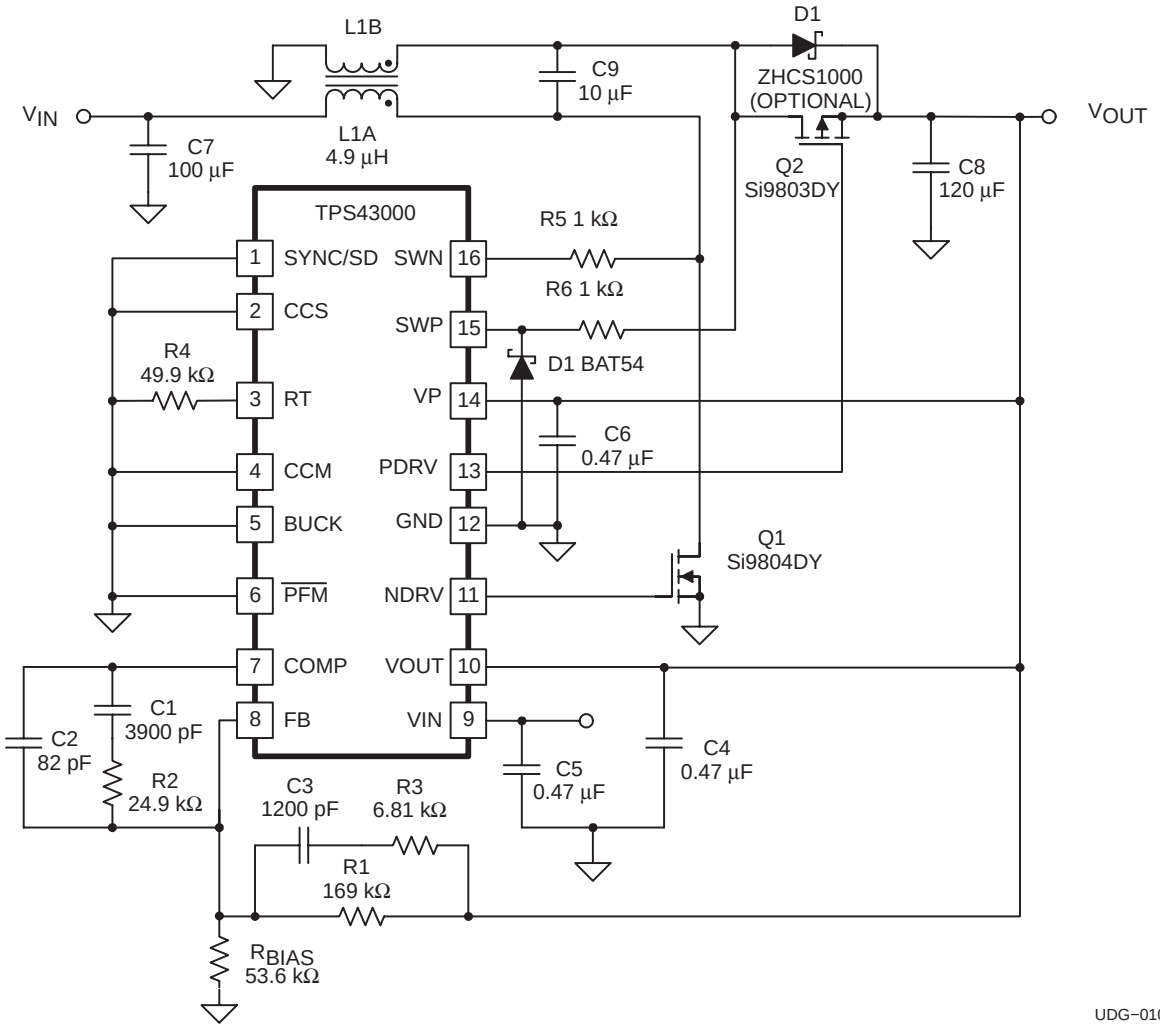


Figure 8. 3.3-V Output SEPIC Topology

APPLICATION INFORMATION

The SEPIC topology offers the same advantage of the flyback in that it can generate an output voltage that is greater or less than the input voltage. However, it also offers improved efficiency. Although it requires an additional capacitor in the power stage, it greatly reduces ripple current in the input capacitor and improves efficiency by transferring the energy in the leakage inductance of the coupled inductor to the output. This also provides snubbing for the primary and secondary windings, eliminating the need for RC snubbers. Note that the capacitor must have low ESR, with sufficient ripple current rating for the application. Another advantage of the SEPIC is that the inductors do not have to be on the same core.

theory of operation

When the energizing MOSFET (Q1) is on, V_{IN} is applied across L1A with the dotted end negative (see Figure 8). At the same time, the voltage across the SEPIC capacitor C9 (equal to V_{IN}) is applied across L1B with its dotted end also negative. Since L1A = L1B and the voltages across the two inductors are equal (V_{IN}), the inductor currents ramp up at the same rate ($di/dt=V_{IN}/L$). The energizing MOSFET current is the sum of the two inductor currents. When the energizing MOSFET turns off, the inductor current wants to continue to flow causing the inductor voltages to reverse until the output rectifer begins to conduct. The voltage across L1B is clamped to V_{OUT} (plus the rectifier drop) and with its dotted end positive. The voltage across the SEPIC capacitor (V_{IN}) cancels with V_{IN} and the voltage across L1A is also V_{OUT} with its dotted end positive. Again, since L1A=L1B and the voltage across the two inductors are equal (V_{OUT}), the inductor current ramps down at the same rate ($di/dt=V_{OUT}/L$). The SEPIC capacitor is charged by L1A when the energizing MOSFET is off and is discharged by L1B when the energizing MOSFET is on. Since the voltages across the inductors are identical at all times throughout the switcing cycle, the inductors can be coupled on a single magnetic core with an equal number of turns. This improves the SEPIC application's dynamic performance and also allows reduction of the input filtering requirements through ripple steering.

selecting the inductor

The inductor must be chosen based on the desired operating frequency and the maximum load current. Higher frequencies allow the use of lower inductor values, reducing component size. Higher load currents require larger inductors with higher current ratings and less winding resistance to minimize losses. The inductor must be rated for operation at the highest anticipated peak current. Refer to equations 17, 19, and 21 to calculate the peak inductor current for a buck, boost, flyback, or SEPIC design, based on VIN, VOUT, duty cycle, maximum load, frequency, and inductor value. Some manufacturers rate their parts for maximum energy storage in microjoules (μJ). This is expressed by:

$$E = 0.5 \times L \times \left(I_{pk}\right)^2 \tag{23}$$

where E is the required energy rating in microjoules, L is the inductor value in microhenries (μH) (with current applied), and I_{pk} is the peak current in amps that the inductor sees in the application. Another way in which inductor ratings are sometimes specified is the maximum volt-seconds applied. This is given simply by:

$$ET = \frac{\left(V_{IN} \times D\right)}{f_{SW}} \tag{24}$$

where ET is the required rating in V-μs, D is the duty cycle for a given V_{IN} and V_{OUT}, and f_{SW} is the switching frequency in MHz. Refer to equations 18, 20, and 22 to calculate the duty cycle for a buck, boost, flyback, or SEPIC converter.

In any case, the inductor must use a low loss core designed for high-frequency operation. High-frequency ferrite cores are recommended. Some manufacturers of off-the-shelf surface-mount designs are listed in Table 1. For flyback and SEPIC topologies, use a two-winding coupled inductor. SEPIC designs can also use two discrete inductors.

APPLICATION INFORMATION

Table 1. SMT Commercial Inductor Manufacturers

Coilcraft Inc.	(800) 322−2645	1102 Silver Lake RD, Cary, IL 60013
Coiltronics Inc.	(407) 241−7876	6000 Park of Commerce Blvd, Boca Raton, FL 33487
Dale Electronics, Inc.	(605) 665−9301	East Highway 50, Yankton, SD 57078
Pulse Engineering Ltd.	(204) 633−432	1300 Keewatin Street, Winnipeg, MB R2X 2R9
Sumida	1−847−545−6700 Fax 1−847−545−6720	1701 Golf Road, Tower 3, Suite 400, Rolling Meadows, IL 60008
BH Electronics	(612) 894−9590	12219 Wood Lake Drive, Burnsville, MN 55337
Tokin America Inc.	(408) 432−8020	155 Nicholson Lane, San Jose CA 95134

selecting the filter capacitor

The input and output filter capacitors must have low ESR and low ESL. Surface-mount tantalum, OSCONs or multilayer ceramics (MLCs) are recommended. The capacitor selected must have the proper ripple current rating for the application. Some recommended capacitor types are listed in Table 2.

Table 2. Recommended SMT Filter Capacitors

Manufacturer	Part Number	Features
AVX	TPS series	Low ESR tantalum
Kemet	T410 series	Low ESR tantalum
Murata	GRM series	Low ESR ceramic
Sanyo	OSCON series	Low ESR organic
Sprague	591D series	Low ESR, low profile tantalum
	594D series	Low ESR tantalum
Tokin	Y5U, Y5V Type	Low ESR ceramic
Taiyo Yuden	X5R Type	Low ESR ceramic

circuit layout and grounding

As with any high-frequency switching power supply, circuit layout, hookup, and grounding are critical for proper operation. Although this may be a relatively low-power, low-voltage design, these issues are still very important. The MOSFET turn-on and turn-off times necessary to maintain high efficiency at high switching frequencies of 1 MHz or more result in high dv/dt and di/dts. This makes stray circuit inductance especially critical. In addition, the high impedances associated with low-power designs, such as in the feedback divider, make them especially susceptible to noise pickup.

layout

The component layout should be as tight as possible to minimize stray inductance. This is especially true of the high-current paths, such as in series with the MOSFETs and the input and output filter capacitors.

The components associated with the feedback, compensation and timing should be kept away from the power components (MOSFETs, inductor). Keep all components as close to the device pins as possible. Nodes that are especially noise sensitive are the FB, RT and COMP pins.

APPLICATION INFORMATION

grounding

A ground plane is highly recommended. The GND pin of the TPS43000 should be close to the source of the N-channel MOSFET, the input filter capacitor, and the output filter capacitor. The grounded end of the RT resistor, the feedback divider resistor, and the SYNC/SD, CCS, CCM, $\overline{\text{PFM}}$, and BUCK pins (when tied to ground based on the application) form the signal ground and should be connected to the quietest location of the ground plane (away from switching elements).

MOSFET gate resistors

The TPS43000 includes low-impedance CMOS output drivers for the two external MOSFET switches. The NDRV output has a nominal pull-up resistance of 6.5 Ω and a nominal pull-down resistance of 2.25 Ω. The PDRV output has a nominal pull-down resistance of 3.5 Ω and a nominal pull-up resistance of 2.5 Ω. For high-frequency operation using low gate charge MOSFETs, no gate resistors are required. To reduce high-frequency ringing at the MOSFET gates, low-value series gate resistors may be added. These should be non-inductive resistors, with a value of 2 Ω to 10 Ω, depending on the frequency of operation. Lower values result in better switching times, improving efficiency.

minimizing output ripple and noise spikes

The amount of output ripple is determined primarily by the type of output filter capacitor and how it is connected in the circuit. In most cases, the ripple is dominated by the ESR (equivalent series resistance) and ESL (equivalent series inductance) of the capacitor, rather than the actual capacitance value. Low ESR and ESL capacitors are mandatory in achieving low output ripple. Surface-mount packages greatly reduce the ESL of the capacitor, minimizing noise spikes. To further minimize high frequency spikes, a surface-mount ceramic capacitor should be placed in parallel with the main filter capacitor. For best results, a capacitor should be chosen whose self-resonant frequency is near the frequency of the noise spike. For high switching frequencies, ceramic capacitors alone may be used, reducing size and cost.

For applications where the output ripple must be extremely low, a small LC filter may be added to the output. The resonant frequency should be below the selected switching frequency, but above that of any dynamic loads. The filter's resonant frequency is given by:

$$f_{RES} = \frac{1}{\left(2\pi \times (L \times C)^{1/2}\right)} \tag{25}$$

where f is the frequency in Hz, L is the filter inductor value in Henries, and C is the filter capacitor value in Farads. It is important to select an inductor rated for the maximum load current and with minimal resistance to reduce losses. The capacitor should be a low-impedance type, such as a tantalum.

If an LC ripple filter is used, the feedback point can be taken before or after the filter, as long as the filter's resonant frequency is well above the loop crossover frequency. Otherwise, the additional phase lag makes the loop unstable. The only advantage to connecting the feedback after the filter is that any small voltage drop across the filter inductor is corrected for in the loop, providing the best possible voltage regulation. However, the resistance of the inductor is usually low enough that the voltage drop is negligible.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS43000PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	43000	Samples
TPS43000PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	43000	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

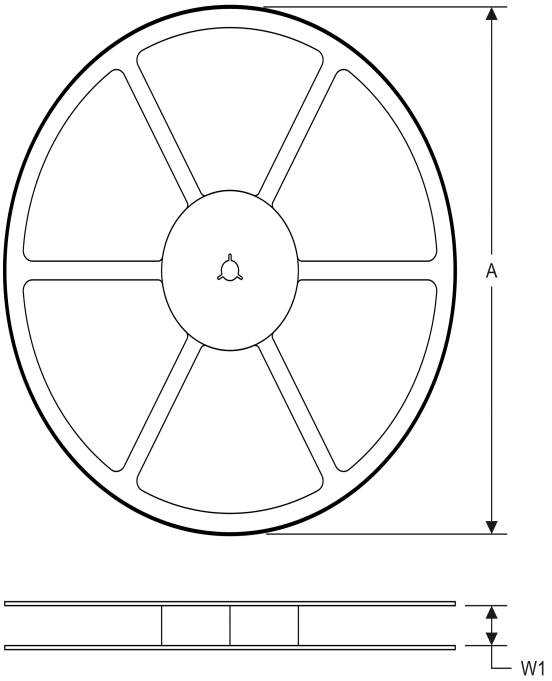
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

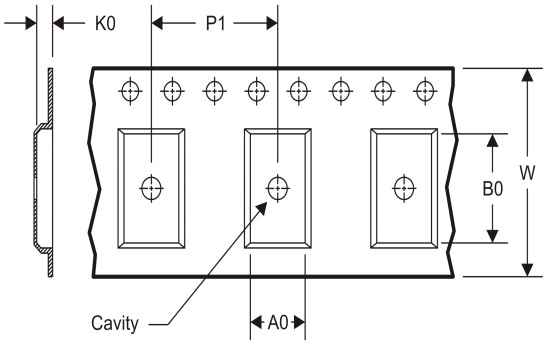
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



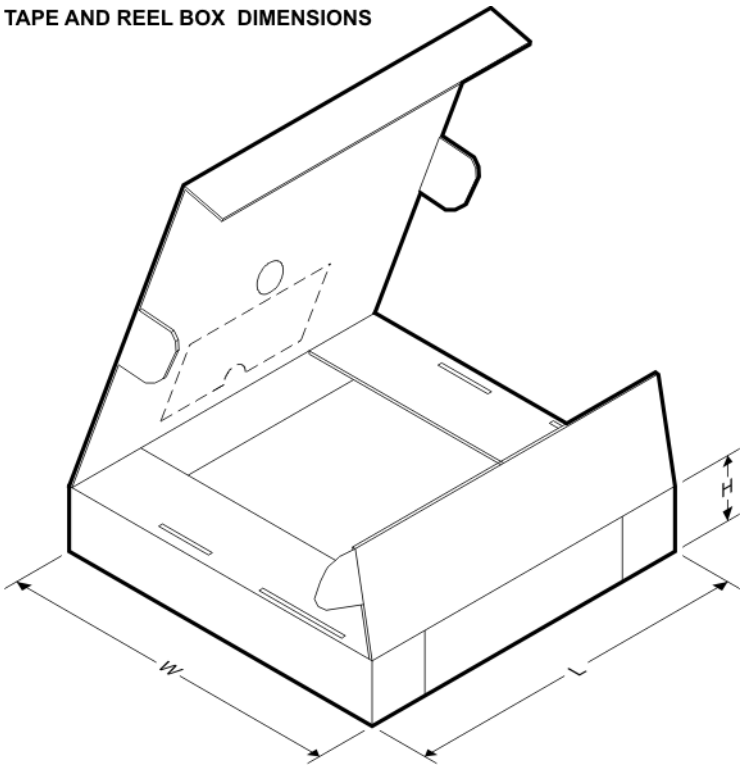
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS43000PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

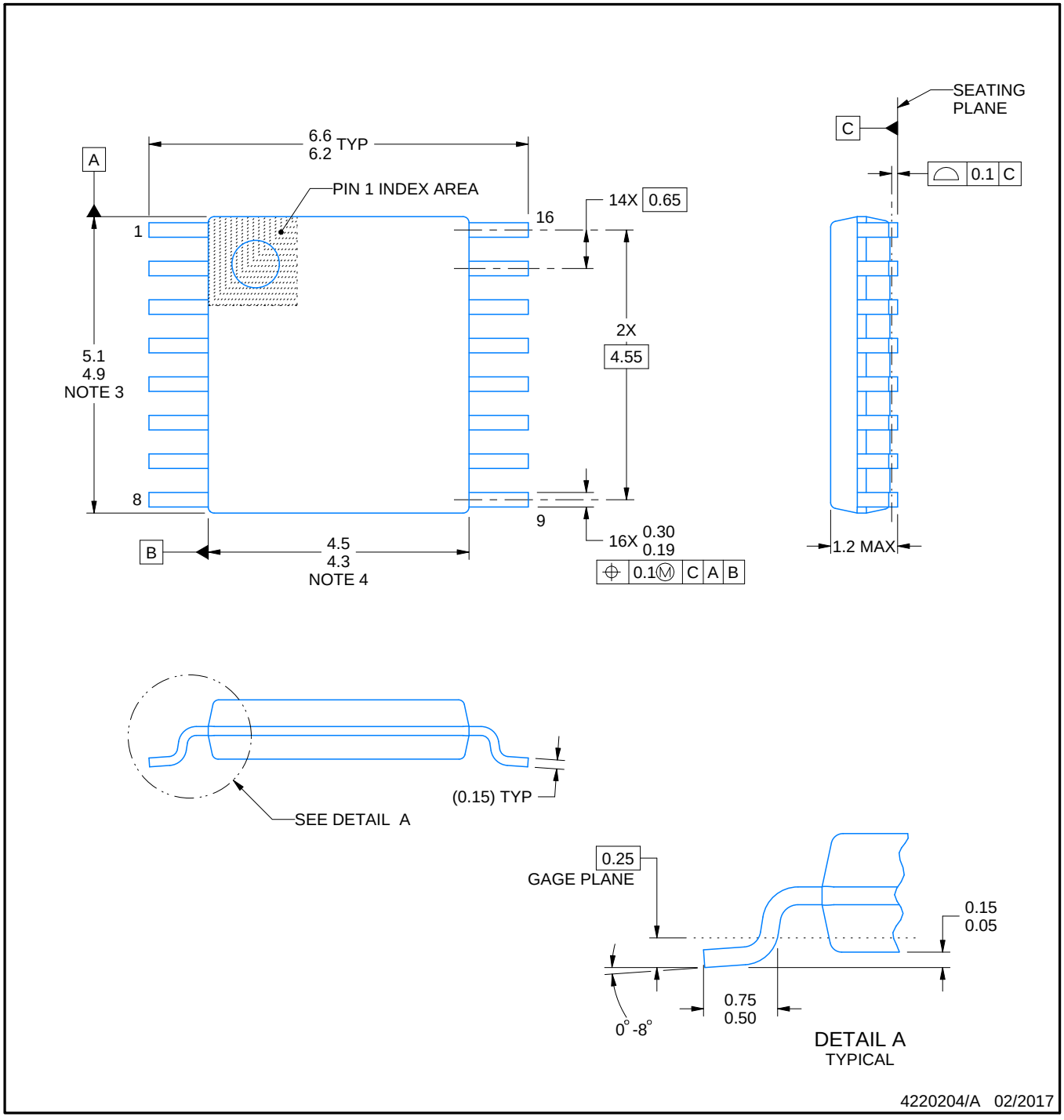
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS43000PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

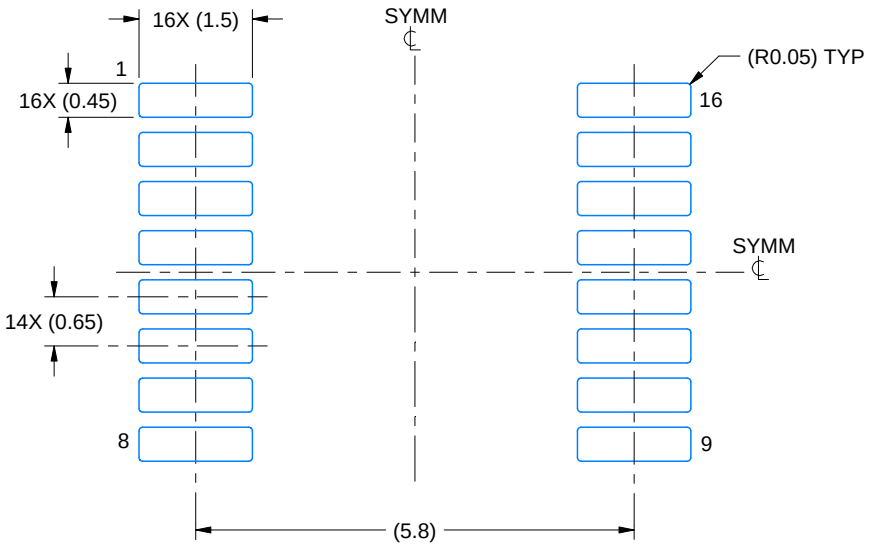
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

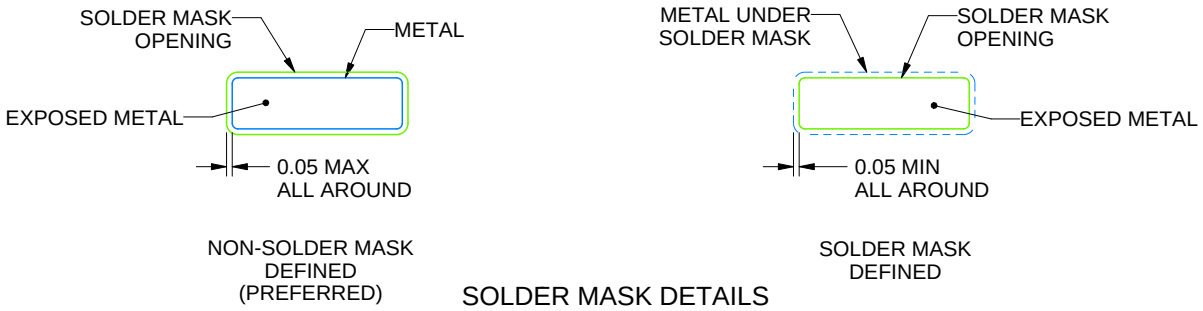


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

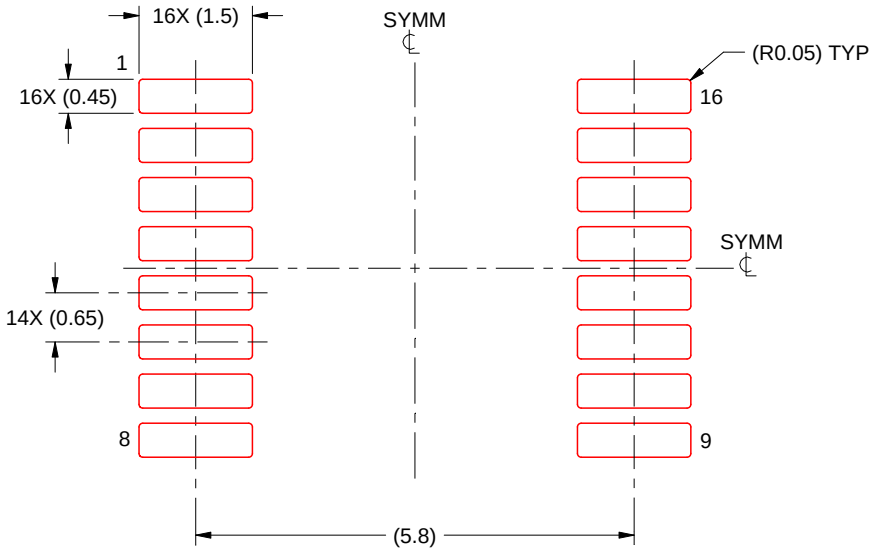


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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