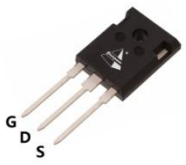
N-channel Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	500	
$R_{DS(on)}$ max. at 25°C (Ω)	V_{GS}=10V	0.2
Q_g max. (nC)	160	
Q_{gs} (nC)	30	
Q_{gd} (nC)	53	
Configuration	single	

Features

- I_D=24A(Vgs=10V)
- Ultra Low Gate Charge
- Improved dv/dt Capability
- 100% Avalanche Tested
- R_OHS compliant



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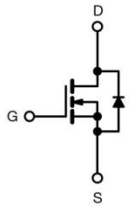


Schematic diagram

Applications

- Switching Mode Power Supplies (SMPS)
- PWM Motor Controls
- DC to DC Converters
- LED Lighting
- Bridge Circuits

ORDERING INFORMATION	
Device	SPA24N50G
Device Package	TO-247
Marking	24N50G

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
		SPA24N50G	
Drain to Source Voltage	V_{DSS}	500	V
Continuous Drain Current (@T_C=25°C)	I_D	24 (1)	A
Continuous Drain Current (@T_C=100°C)		15 (1)	A
Drain current pulsed (2)	I_{DM}	96 (1)	A
Gate to Source Voltage	V_{GS}	±30	V
Single pulsed Avalanche Energy (3)	E_{AS}	2016	mJ
Peak diode Recovery dv/dt (4)	dv/dt	6	V/ns
Total power dissipation (@T_C=25°C)	P_D	280	W
Derating Factor above 25°C		2.2	W/°C
Operating Junction Temperature & Storage Temperature	T_{STG}, T_J	-55 to + 150	°C
Maximum lead temperature for soldering purpose	T_L	260	°C

Notes
1. Drain current is limited by maximum junction temperature.
2. Repetitive rating : pulse width limited by junction temperature.
3. L = 7mH, I_{AS} = 24A, V_{DD} = 50V, R_G=25Ω, Starting at T_J = 25°C
4. I_{SD} ≤ I_D, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Starting at T_J =25°C

THERMAL CHARACTERISTICS			
Parameter	**Symbol**	**Value**	**Unit**
Thermal resistance, Junction to case	R_{thjc}	0.44	°C/W
Thermal resistance, Junction to ambient	R_{thja}	38	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)						
Parameter	**Symbol**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Off Characteristics						
Drain to source breakdown voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	500	--	--	V
Breakdown voltage temperature coefficient	ΔBV_{DSS} / ΔTJ	I_D=250uA, referenced to 25°C	--	0.49	--	V/°C
Drain to source leakage current	I_{DSS}	V_{DS}=500V, V_{GS}=0V	--	--	1	uA
		V_{DS}=500V, T_C=125°C	--	--	50	uA
Gate to source leakage current, forward	I_{GSS}	V_{GS}=30V, V_{DS}=0V	--	--	100	nA
Gate to source leakage current, reverse		V_{GS}=-30V, V_{DS}=0V	--	--	-100	nA
On Characteristics						
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250uA	2	--	4	V
Drain to source on state resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D =12A	--	0.15	0.2	Ω
Forward Transconductance	Gfs	V_{DS} = 30 V, I_D = 12A	--	22	--	S
Dynamic Characteristics						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	--	5240	--	pF
Output capacitance	C_{oss}		--	472	--	
Reverse transfer capacitance	C_{rss}		--	15	--	
Turn on delay time	$t_{d(on)}$	V_{DS}=250V, I_D=24A , R_G=25Ω	--	76	--	ns
Rising time	tr		--	82	--	
Turn off delay time	$t_{d(off)}$		--	198	--	
Fall time	t_f		--	78	--	
Total gate charge	Q_g	V_{DS}=400V, V_{GS}=10V, I_D=24A	--	118	160	nC
Gate-source charge	Q_{gs}		--	30	--	
Gate-drain charge	Q_{gd}		--	53	--	

SOURCE TO DRAIN DIODE RATINGS CHARACTERISTICS						
Parameter	**Symbol**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Continuous source current	I_S	Integral reverse p-n Junction diode in the MOSFET	--	--	24	A
Pulsed source current	I_{SM}		--	--	96	A
Diode forward voltage drop.	V_{SD}	I_S=24A, V_{GS}=0V	--	--	1.4	V
Reverse recovery time	T_{rr}	I_S=24A, V_{GS}=0V, dI_F/dt=100A/us	--	520	--	ns
Reverse recovery Charge	Qrr		--	10	--	uC

Fig1. Output characteristics

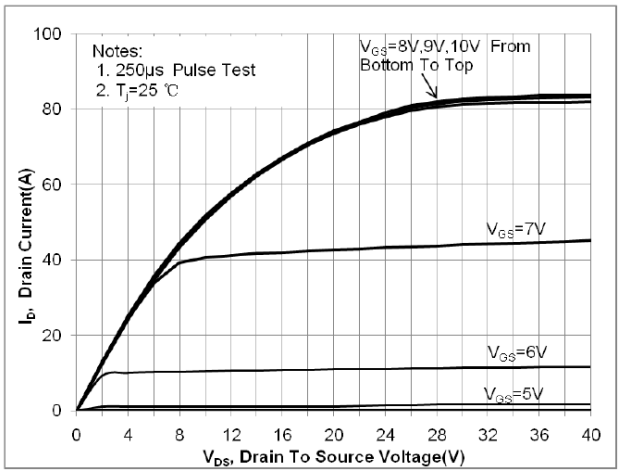


Fig2. Drain-source on-state resistance

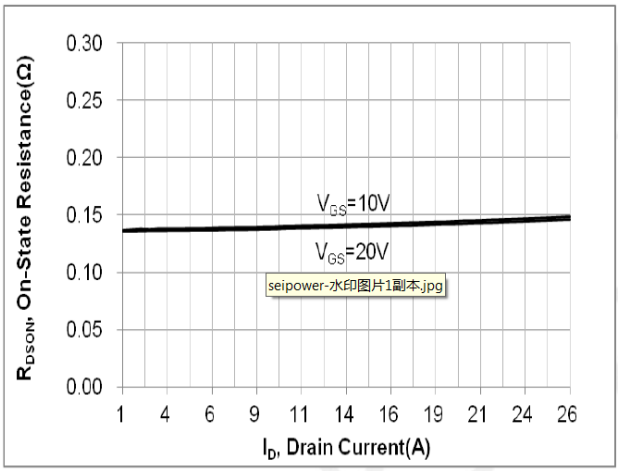


Fig3. Gate charge characteristics

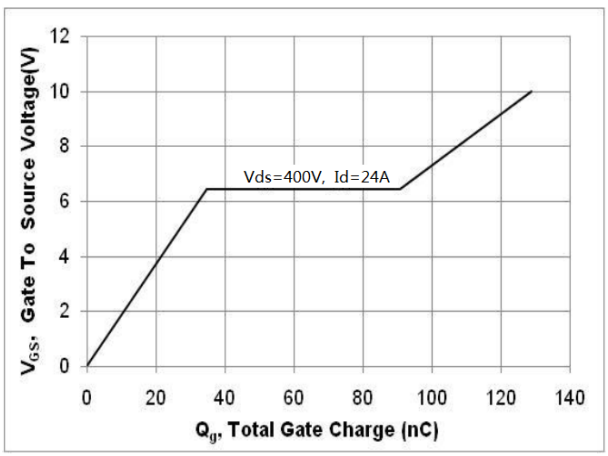


Fig 4. Capacitance Characteristics

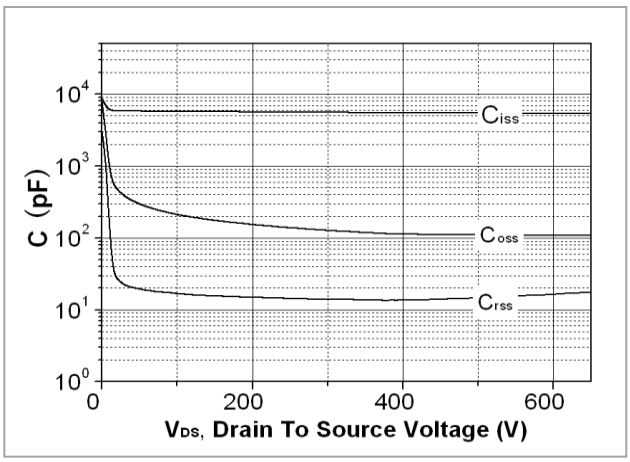


Fig 5. $R_{DS(ON)}$ vs junction temperature

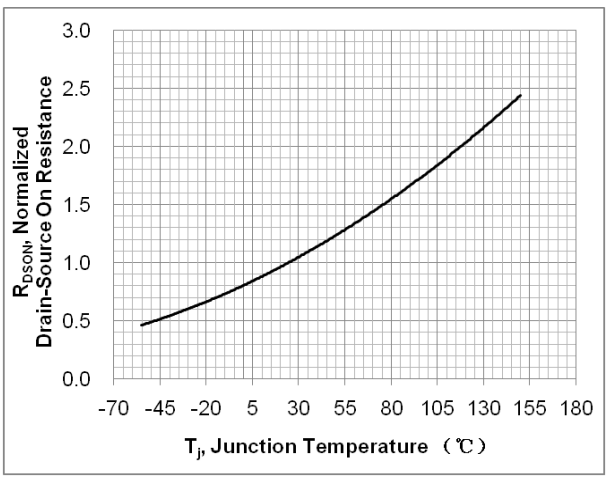


Fig 6. BV_{DSS} vs junction temperature

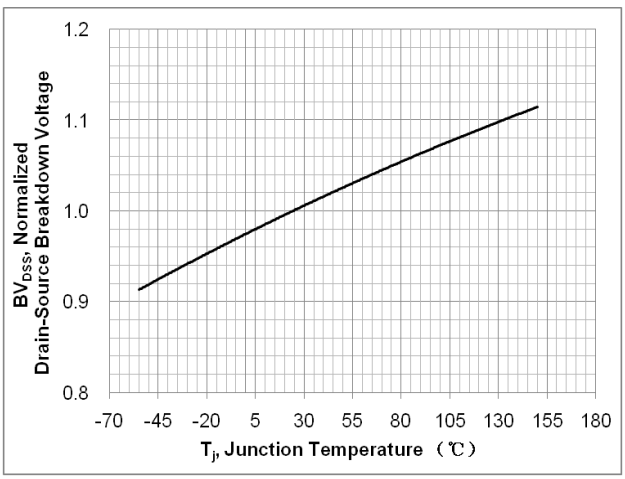


Fig 7 . Safe operating area

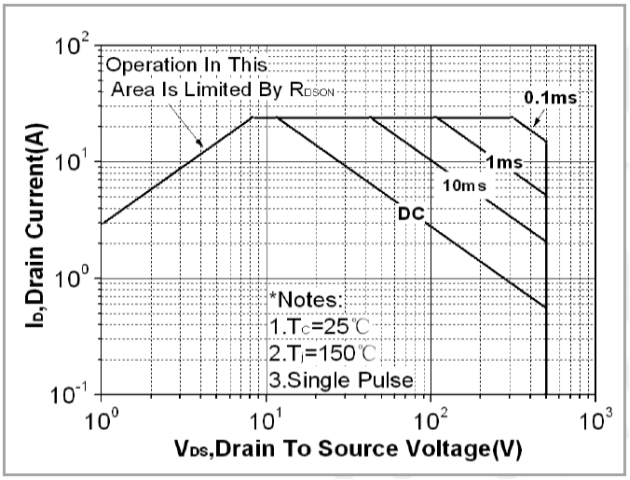


Fig 8 . Transient thermal impedance

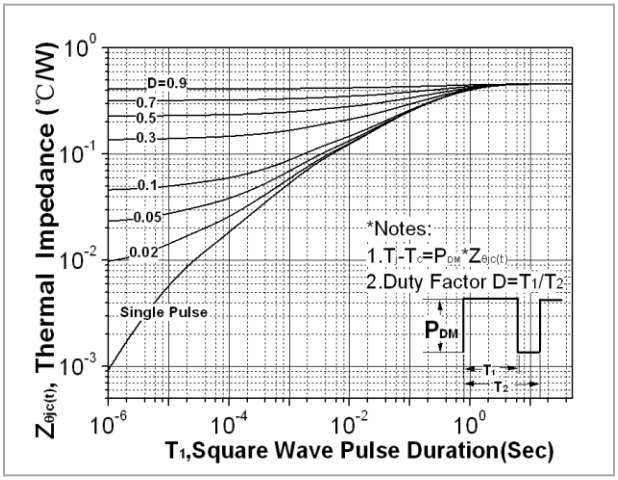


Fig 9. Forward characteristics of reverse diode

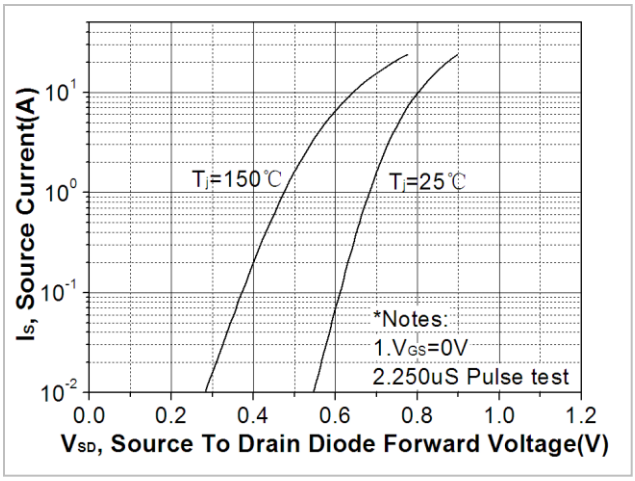
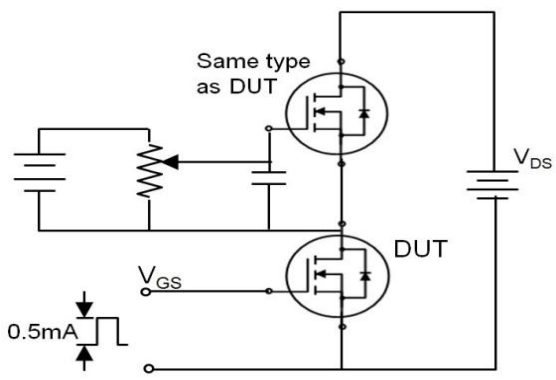


Fig 10. Gate charge test circuit & waveform



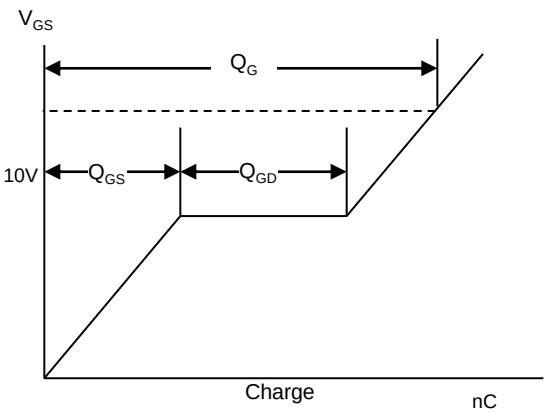


Fig 11. Switching time test circuit & waveform

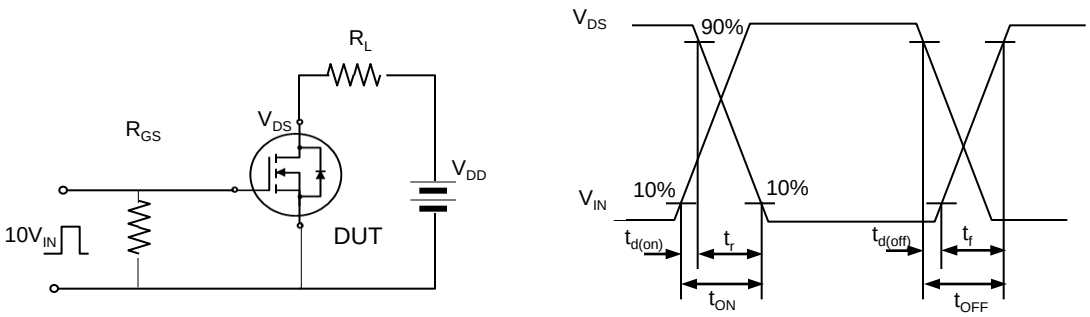


Fig 12. Unclamped Inductive switching test circuit & waveform

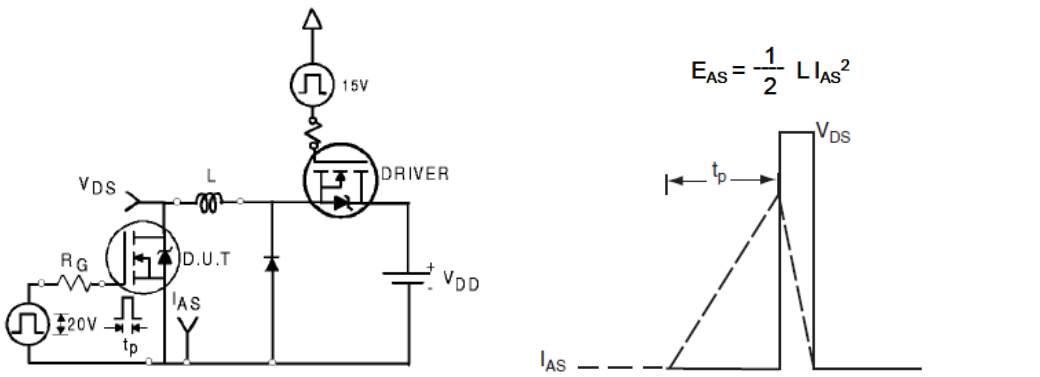
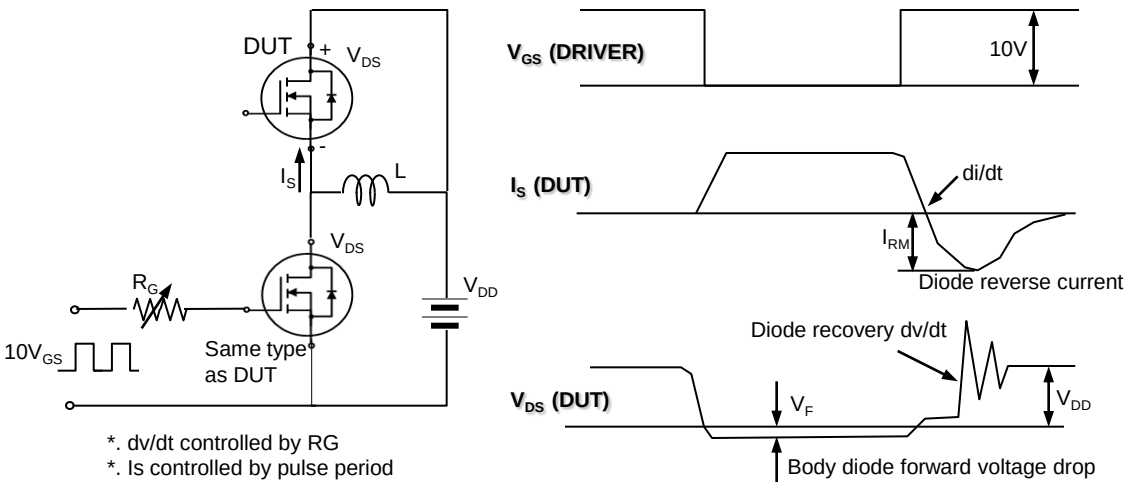


Fig 13. Peak diode recovery dv/dt test circuit & waveform



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