



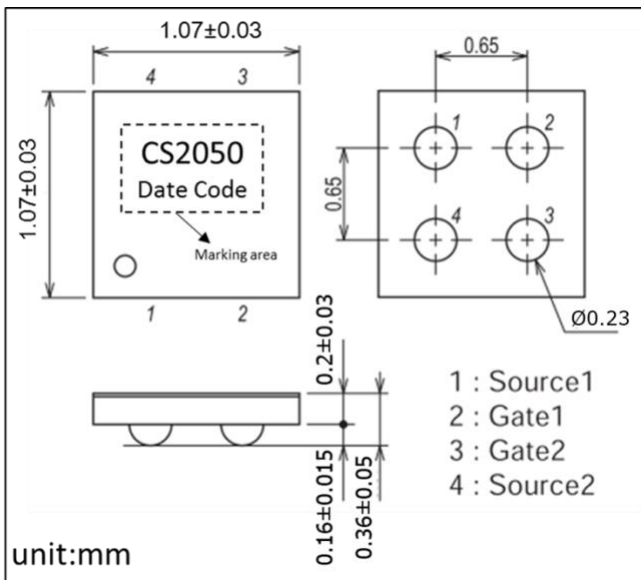
Features

- ★ 2.5V Drive
- ★ Common-drain type
- ★ Typical ESD Protection HBM Class 2

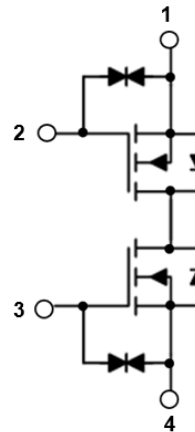
Product Summary

V _{SS}	R _{SS(ON)} Max	I _S Max
20V	36.0mΩ @ 4.5V	6A
	38.0mΩ @ 4.0V	
	48.0mΩ @ 3.1V	
	55.0mΩ @ 2.5V	

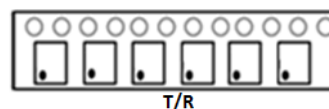
WLCSP Package Dimensions



Electrical Connection



Taping Type: T/R



Absolute Maximum Ratings (T_A=25°C)

- Package :CSP
- JEITA, JEDEC :---
- Minimum Packing Quantity:5000pcs. / reel

Absolute Maximum Ratings (T_A=25°C)

Symbol	Parameter	Rating	Units
V _{SS}	Source to Source Voltage	20	V
V _{GSS}	Gate to Source Voltage	±12	V
I _S	Continuous Source Current ₁	6	A
I _{SP}	Pulsed Source Current ₂	60	A
P _T	Total Power Dissipation ₁	1.6	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C



Electrical Characteristics at T_A=25°C

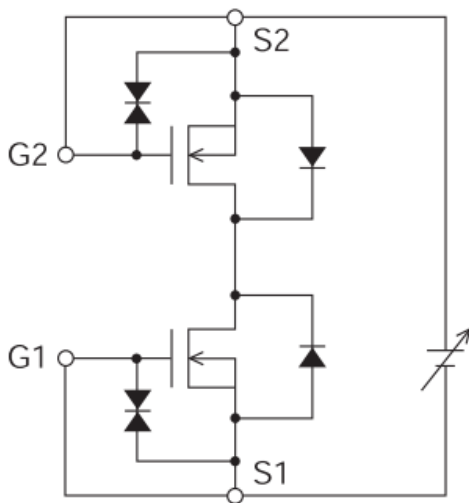
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{SSS}	Source-Source Breakdown Voltage	V _{GS} =0V, I _S =250uA	20	---	---	V
R _{SS(ON)}	Static Source-Source On-State Resistance	V _{GS} =4.5V, I _S =1.5A	23	32	36	mΩ
		V _{GS} =4.0V, I _S =1.5A	25	33	38	
		V _{GS} =3.7V, I _S =1.5A	26	34	41	
		V _{GS} =3.1V, I _S =1.5A	27	36	48	
		V _{GS} =2.5V, I _S =1.5A	31	42	55	
V _{GS(th)}	Gate Threshold Voltage	V _{SS} =V _{GS} , I _S =250uA	0.5	0.65	1.2	V
I _{SSS}	Zero Gate Voltage Source Current	V _{SS} =20V, V _{GS} =0V	---	---	1	uA
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±8V, V _{SS} =0V	---	---	±10	uA
G _{fs}	Forward Transconductance	V _{SS} =10V, I _D =3.0A	---	5.2	---	S
Q _g	Total Gate Charge ₃	V _{SS} =15V, V _{GS} =4.5V, I _S =6A	---	10.4	---	nC
T _{d(on)}	Turn-On Delay Time ₃	V _{DD} =10V, V _{GS} =4.5V, R _G =3.3Ω I _S =3A	---	3.2	---	ns
T _r	Rise Time ₃		---	9.8	---	
T _{d(off)}	Turn-Off Delay Time ₃		---	31	---	
T _f	Fall Time ₃		---	3.6	---	
V _{FSS}	Forward Source-Source Voltage	V _{GS} =0V, I _S =1.5A	---	0.72	1.1	V

Note :

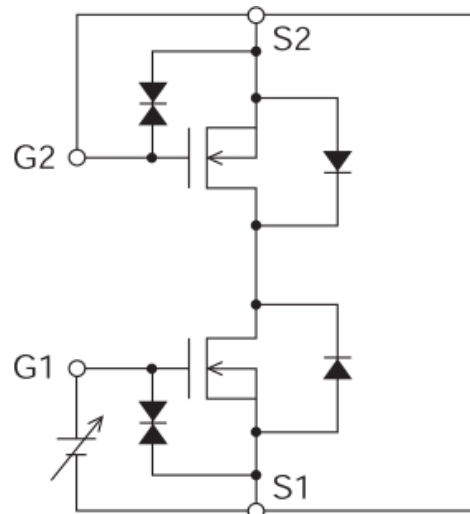
- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≤ 10us , duty cycle ≤ 1%
- 3.Guaranteed by design, not subject to production testing.

Test circuits are example of measuring FET1 sides

Test Circuit 1 V_{SSS} / I_{SSS}



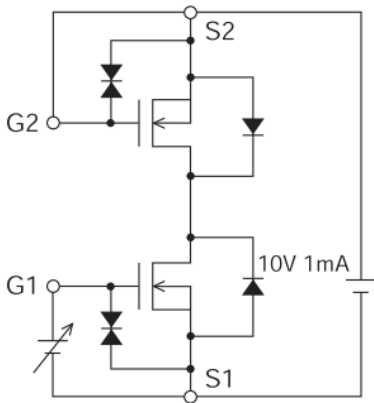
Test Circuit 2 I_{GSS}(+) / (-)



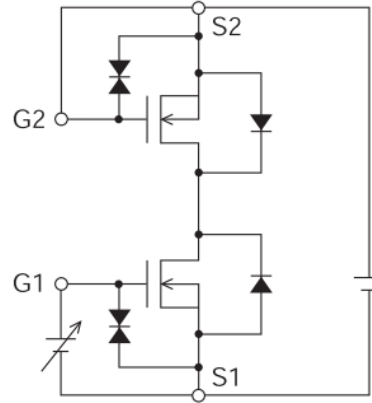


Dual N-Ch Fast Switching MOSFETs

Test Circuit 3 $V_{GS(off)}$

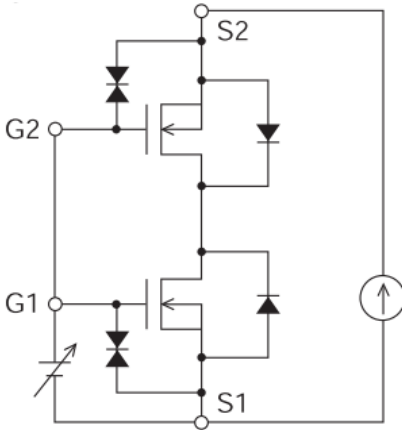


Test Circuit 4 G_{fs}

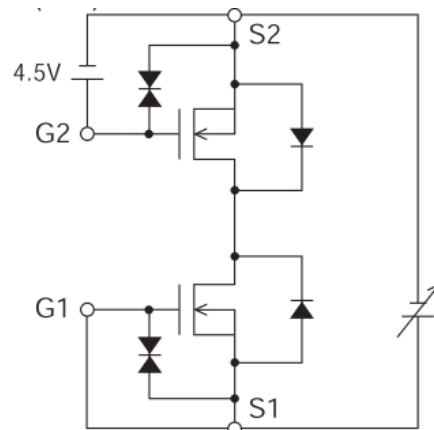


* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.

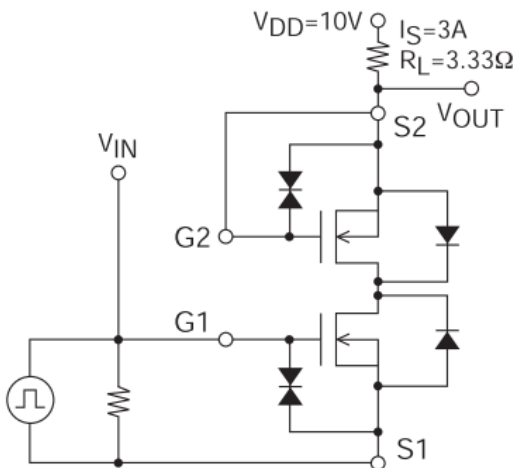
Test Circuit 5 $R_{SS(ON)}$



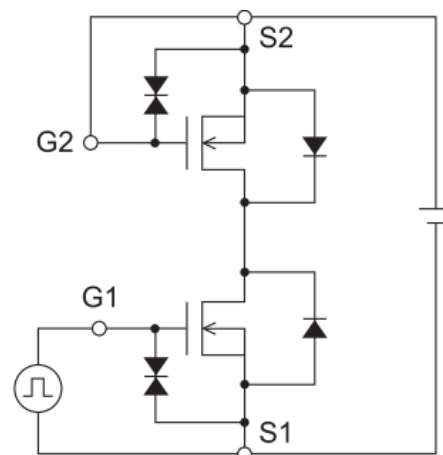
Test Circuit 6 $V_{F(S-S)}$



Test Circuit 7 $T_{d(on)}$, T_r , $T_{d(off)}$, T_f



Test Circuit 8 Q_g



* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.



Dual N-Ch Fast Switching MOSFETs

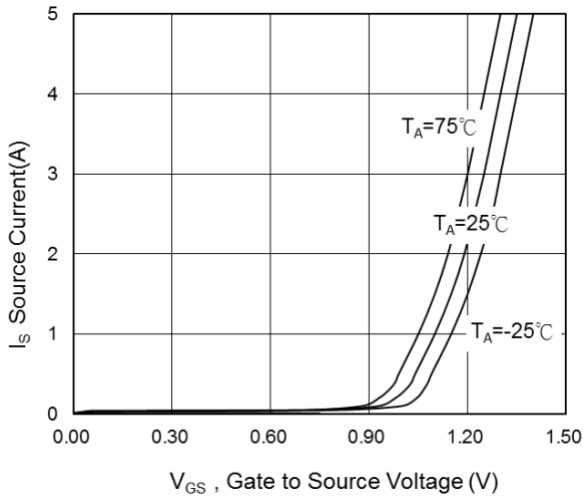


Fig.1 I_S - V_{GS}

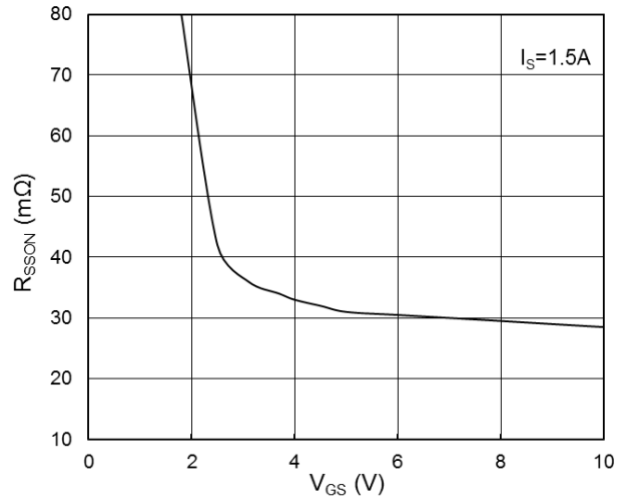


Fig.2 $R_{SS(ON)}$ - V_{GS}

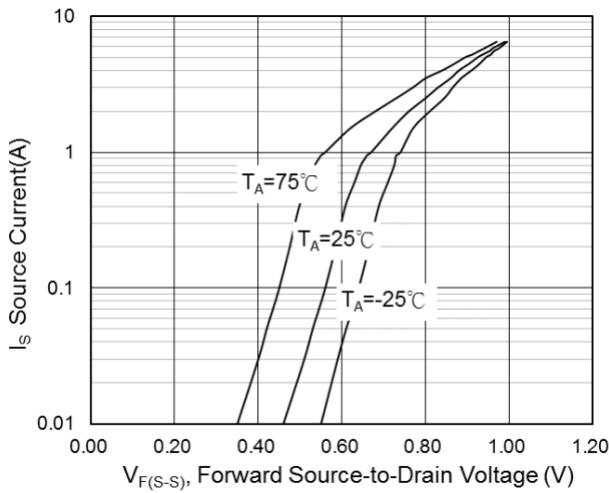


Fig.3 I_S - $V_{F(S-S)}$

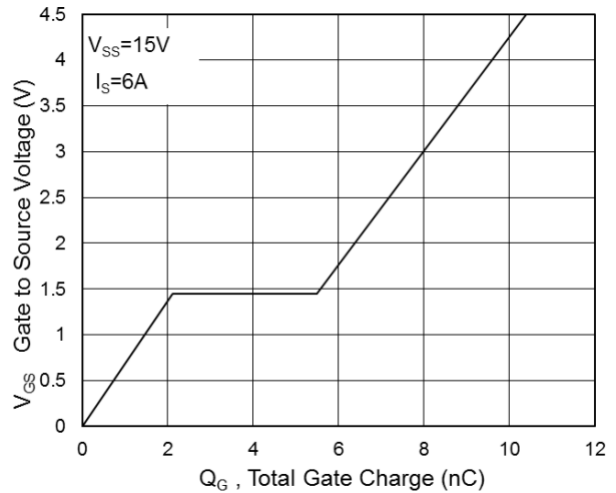


Fig.4 V_{GS} - Q_g

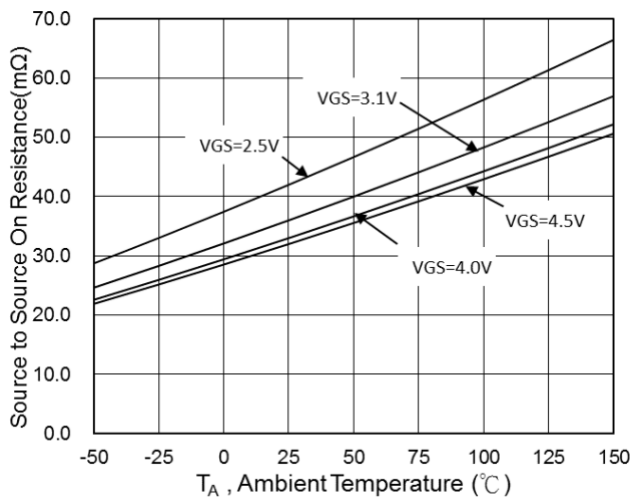


Fig.5 $R_{SS(ON)}$ - T_A

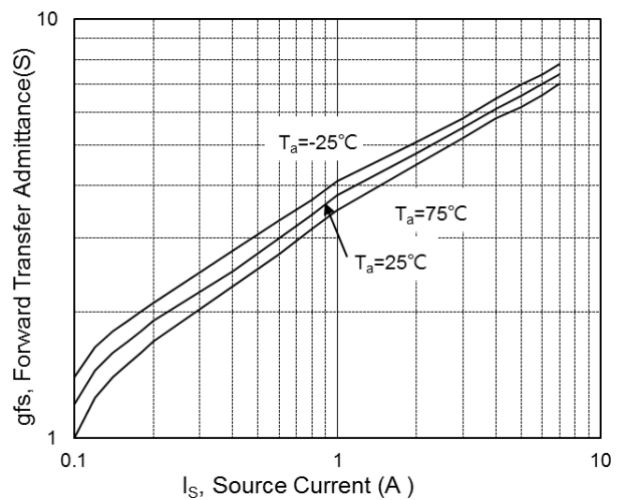


Fig.6 g_{fs} vs I_S



Dual N-Ch Fast Switching MOSFETs

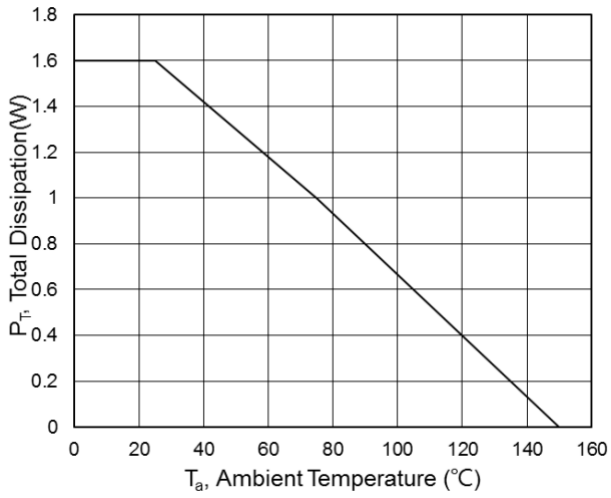


Fig.7 P_T – T_A

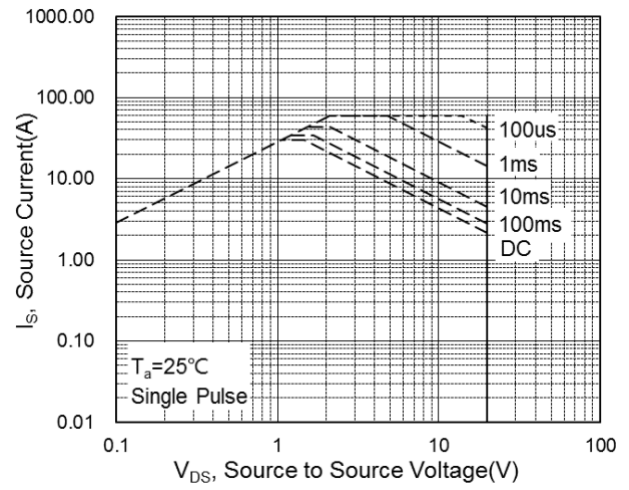


Fig.8 Safe Operating Area