

Description

The HSBA6016 is the high cell density trenched N-ch MOSFETs, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

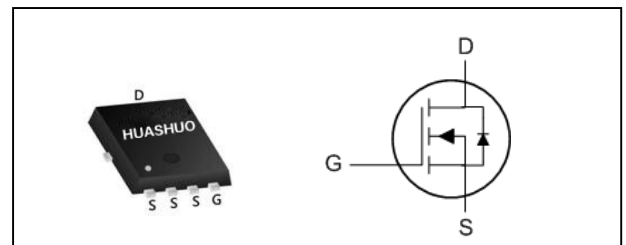
The HSBA6016 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

Product Summary

V_{DS}	60	V
$R_{DS(ON),max}$	12	m Ω
I_D	52	A

PRPAK5X6 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	52	A
$I_D@T_C=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	41	A
I_{DM}	Pulsed Drain Current ²	120	A
EAS	Single Pulse Avalanche Energy ³	72.2	mJ
I_{AS}	Avalanche Current	38	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	62.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	2	$^\circ C/W$



Electrical Characteristics ($T_J=25\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.052	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=30A$	---	---	12	m Ω
		$V_{GS}=4.5V, I_D=15A$	---	---	15	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.2	---	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-5.76	---	$\text{mV}/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=48V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=48V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
gfs	Forward Transconductance	$V_{DS}=5V, I_D=30A$	---	42	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	1.5	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=48V, V_{GS}=4.5V, I_D=15A$	---	53.3	---	nC
Q_{gs}	Gate-Source Charge		---	10.5	---	
Q_{gd}	Gate-Drain Charge		---	9.9	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V, V_{GS}=10V, R_G=3.3\Omega, I_D=15A$	---	10.4	---	ns
T_r	Rise Time		---	9.2	---	
$T_{d(off)}$	Turn-Off Delay Time		---	63	---	
T_f	Fall Time		---	4.8	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	3240	---	pF
C_{oss}	Output Capacitance		---	210	---	
C_{rss}	Reverse Transfer Capacitance		---	146	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V$, Force Current	---	---	52	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	120	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=A, T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=15A, dI/dt=100A/\mu s,$	---	18	---	nS
Q_{rr}	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	14	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1\text{mH}, I_{AS}=38A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

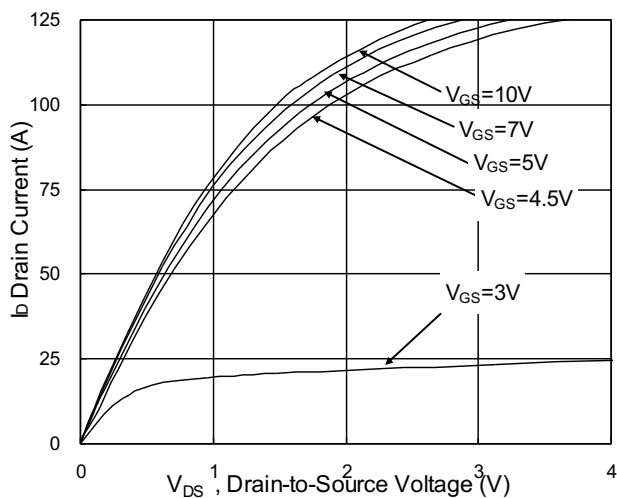


Fig.1 Typical Output Characteristics

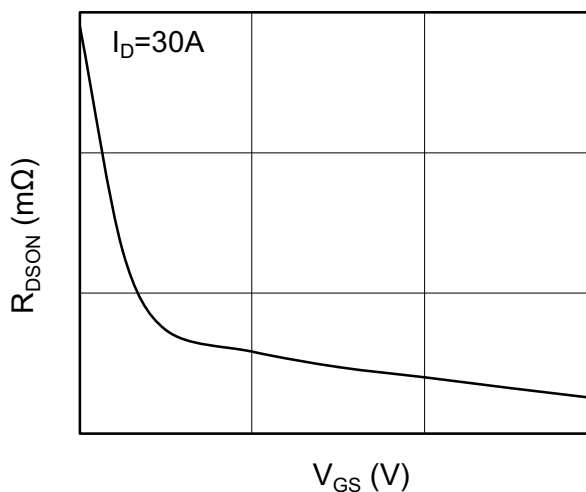


Fig.2 On-Resistance v.s Gate-Source

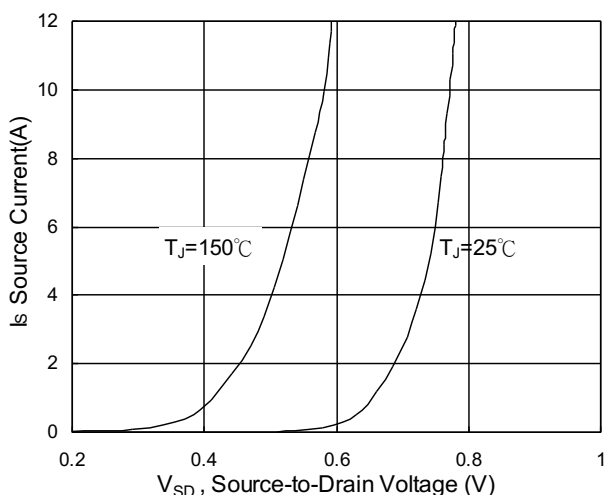


Fig.3 Forward Characteristics of Reverse

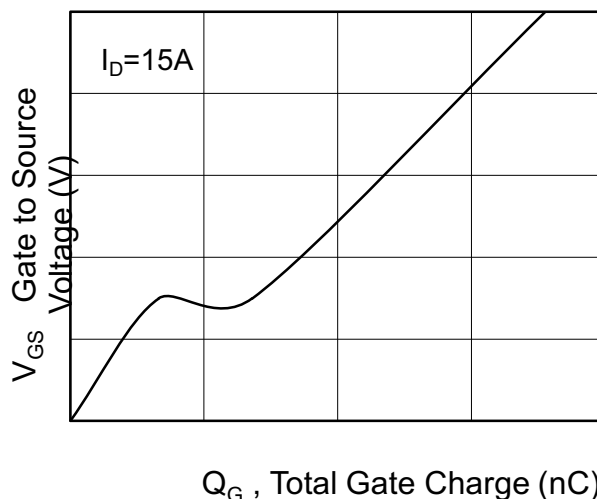


Fig.4 Gate-Charge Characteristics

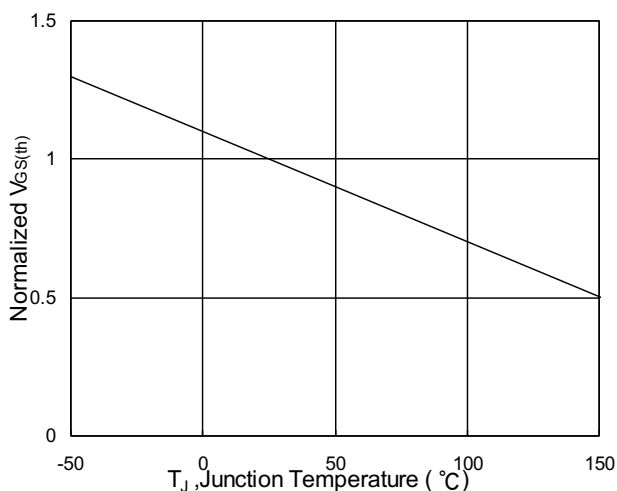


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

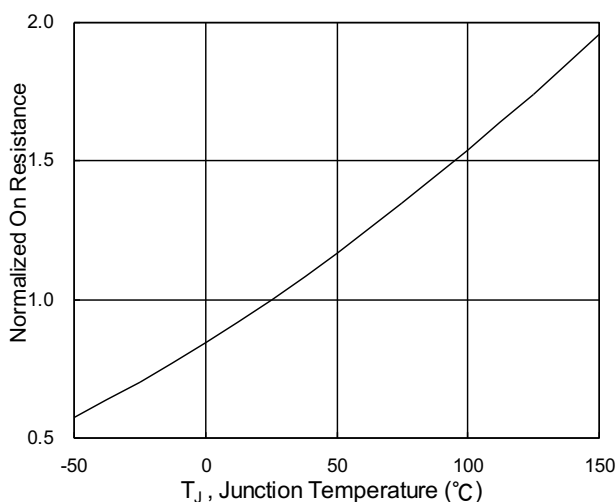


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

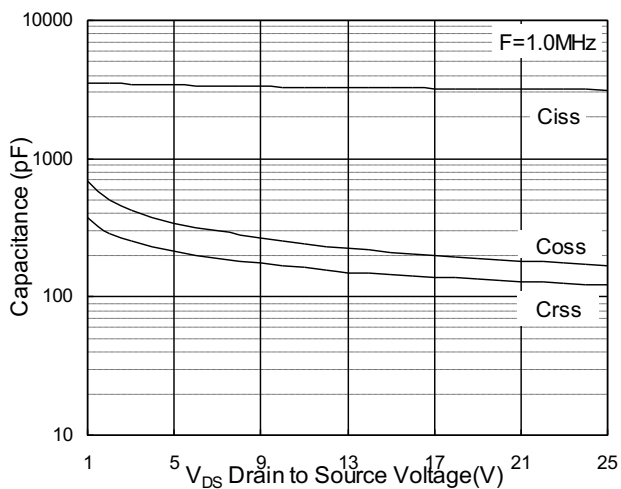


Fig.7 Capacitance

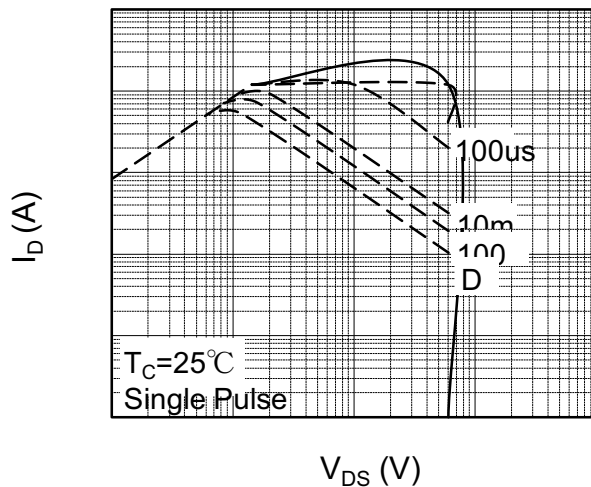


Fig.8 Safe Operating Area

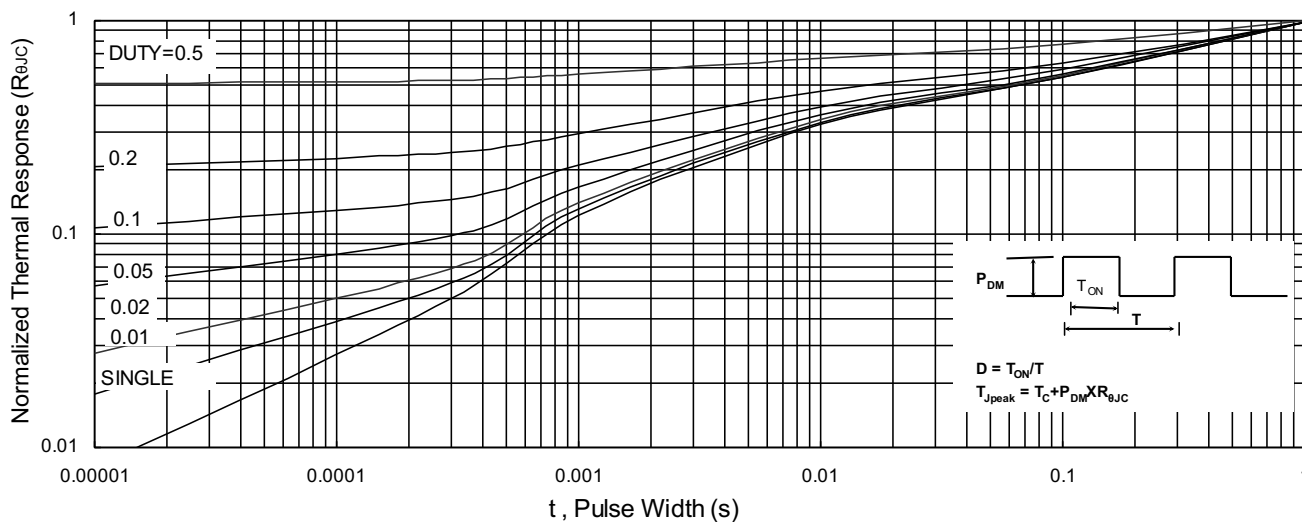


Fig.9 Normalized Maximum Transient Thermal Impedance

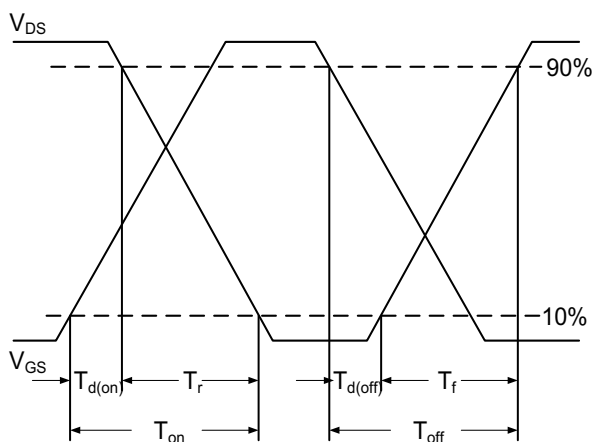


Fig.10 Switching Time Waveform

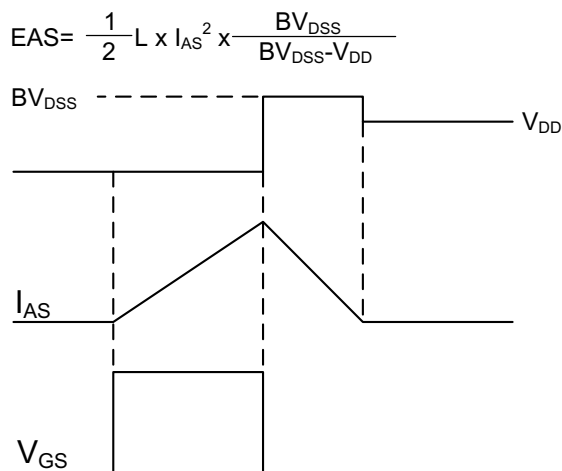


Fig.11 Unclamped Inductive Switching Waveform