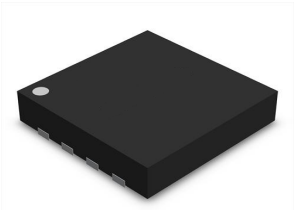
JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD

DFNWB3X3-8L-K Plastic-Encapsulate MOSFETS

CJBE5005 Dual N-Channel MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$TYP	I_D
20V	9.3 mΩ@4.5V	10A
	9.7mΩ@4.0V	
	10.0mΩ@3.8V	
	10.7mΩ@3.1V	
	12.5mΩ@2.5V	

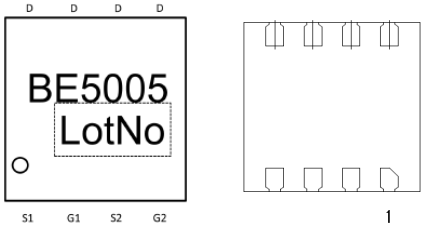
DFNWB3×3-8L-K



DESCRIPTION

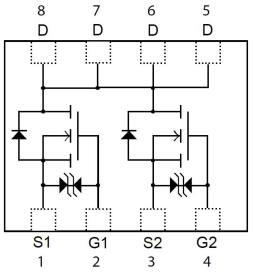
The CJBE5005 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch,facilitated by its common-drain configuration.

MARKING:



Top Back

Equivalent Circuit



MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current	I_D	10	A
Pulsed Drain Current	I_{DM}*	60	A
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$	83.3	℃/W
Junction Temperature	T_j	150	℃
Storage Temperature	T_{stg}	-55~+150	℃
Lead Temperature for Soldering Purposes(1/8'' from case for 10 s)	T_L	260	℃

MOSFET ELECTRICAL CHARACTERISTICS

T_a=25℃ unless otherwise specified

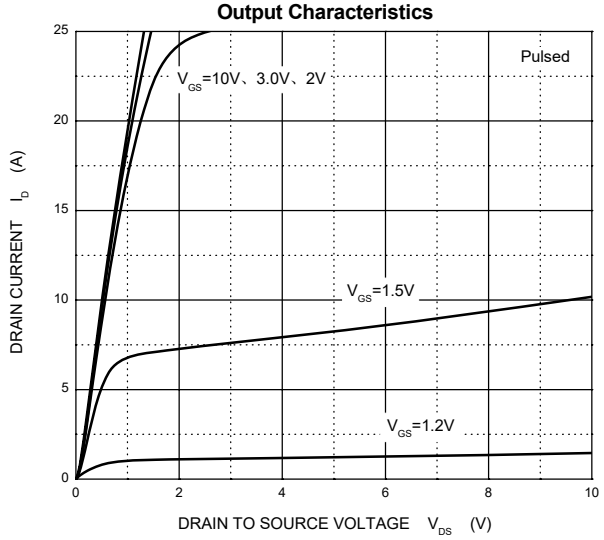
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	20			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =16V,V_{GS} = 0V			1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±4.5V, V_{DS} = 0V			±1	μA
		V_{GS} =±8V, V_{DS} = 0V			±10	μA
Gate threshold voltage (note 1)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	0.4		1	V
Drain-source on-resistance (note 1)	$R_{DS(on)}$	V_{GS} =4.5V, I_D =5A	8	9.3	11.5	mΩ
		V_{GS} =4.0V, I_D =5A	8.2	9.7	12.5	mΩ
		V_{GS} =3.8V, I_D =5A	8.5	10.0	13	mΩ
		V_{GS} =3.1V, I_D =5A	9	10.7	14	mΩ
		V_{GS} =2.5V, I_D =5A	9.5	12.5	17	mΩ
Forward tranconductance (note 1)	g_{FS}	V_{DS} =5V, I_D =7A	9	36		S
Diode forward voltage(note 1)	V_{SD}	I_S=1A, V_{GS} = 0V			1	V
DYNAMIC PARAMETERS (note 2)						
Input Capacitance	C_{iss}	V_{DS} =10V,V_{GS} =0V,f =1MHz		1700		pF
Output Capacitance	C_{oss}			230		pF
Reverse Transfer Capacitance	C_{rss}			200		pF
Total gate charge	Q_g	V_{DS} =10V,V_{GS} =4.5V,I_D =7A		17		nC
Gate-source charge	Q_{gs}			1.5		nC
Gate-drain charge	Q_{gd}			4.7		nC
SWITCHING PARAMETERS(note 2)						
Turn-on delay time	$t_{d(on)}$	V_{GS}=5V,V_{DD}=10V, R_L=1.35Ω,R_{GEN}=3Ω		2.5		ns
Turn-on rise time	t_r			7.2		ns
Turn-off delay time	$t_{d(off)}$			49		ns
Turn-off fall time	t_f			108		ns
Drain-Source Diode Characteristics						
Diode Forward Current	I_S		-	-	8.0	A

Notes :

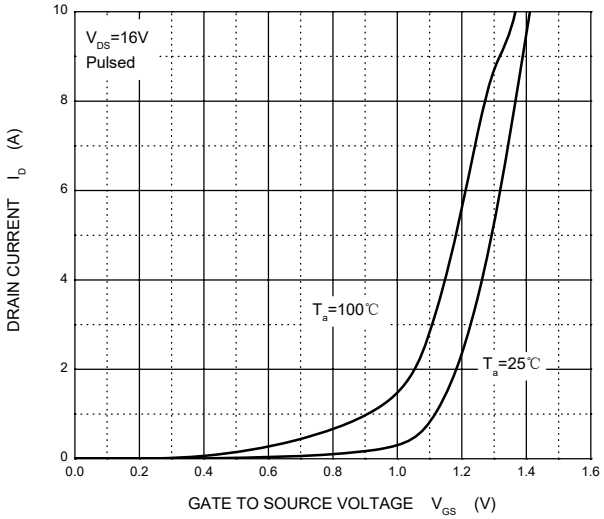
1. Pulse Test : Pulse width≤300μs, duty cycle≤0.5%.
2. Guaranteed by design, not subject to production testing.

Typical Characteristics

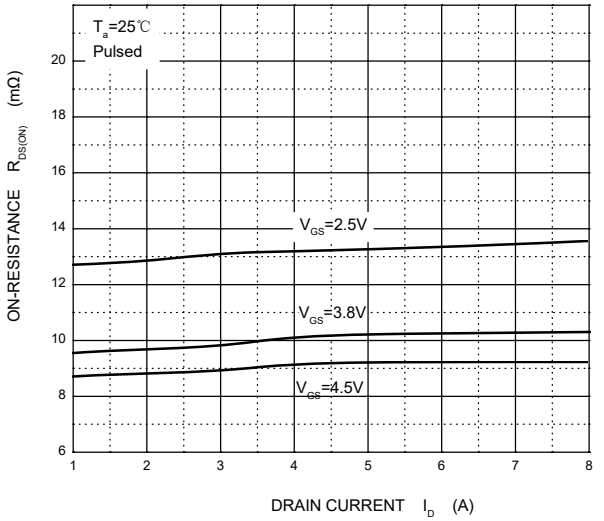
Output Characteristics



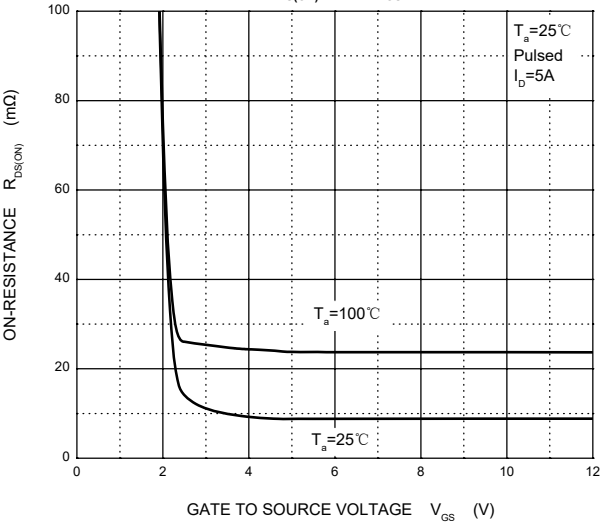
Transfer Characteristics



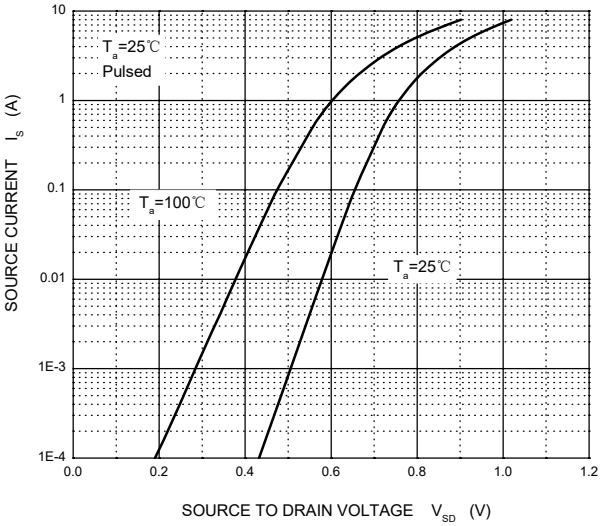
$R_{DS(ON)}$ —— I_D



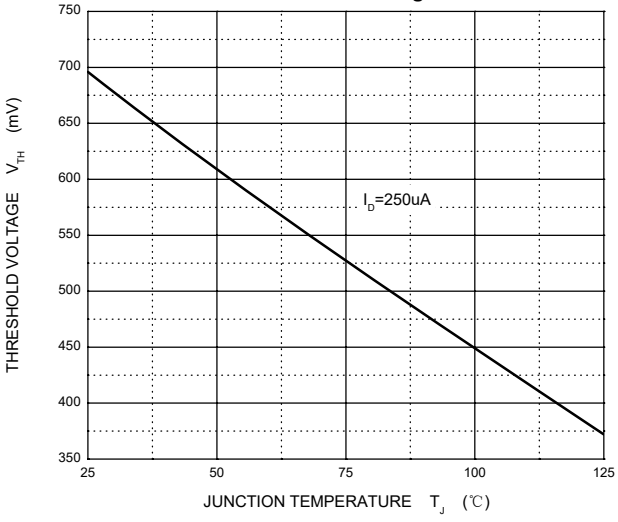
$R_{DS(ON)}$ —— V_{GS}



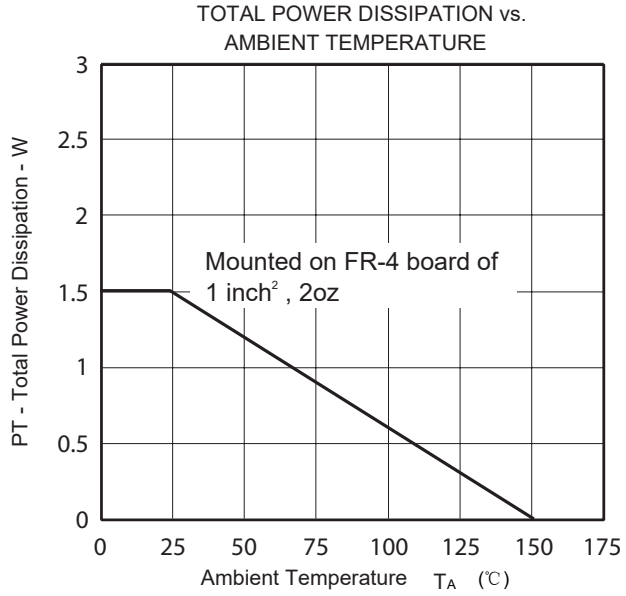
I_S —— V_{SD}

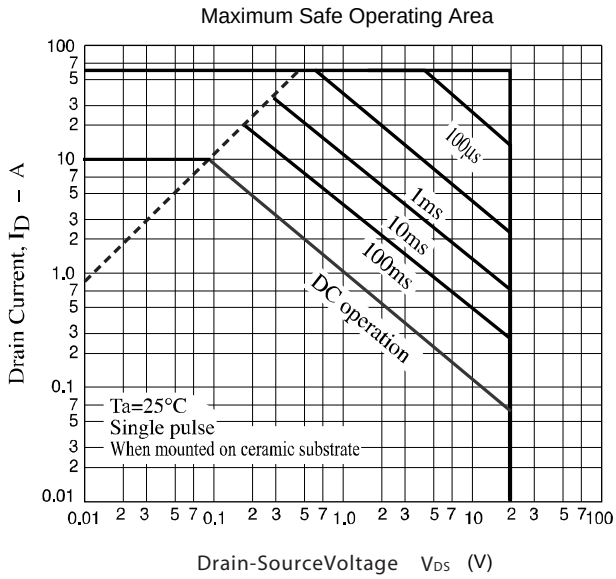


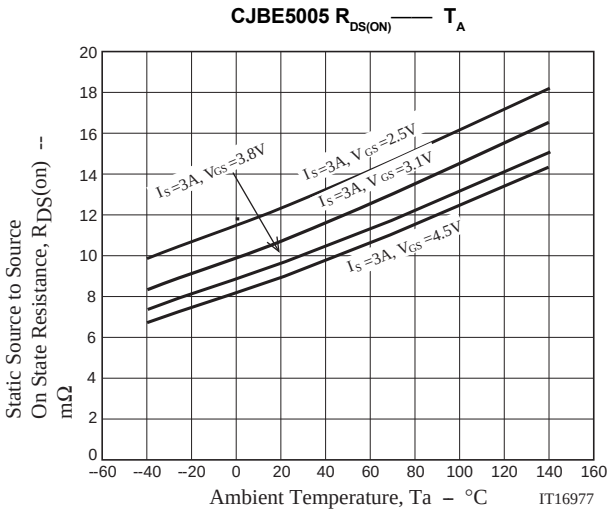
Threshold Voltage



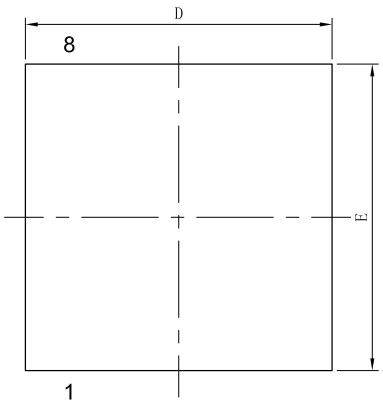
Typical Characteristics



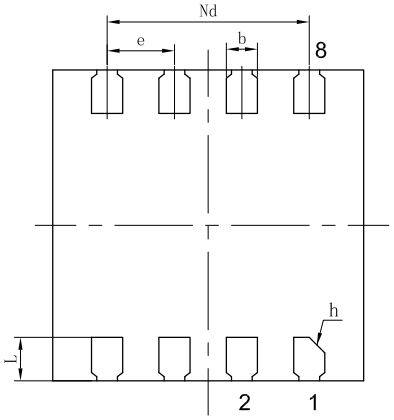




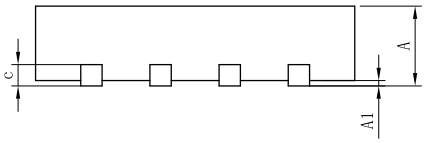
DFNWB3×3-8L-K Package Outline Dimensions(Unit:mm)



TOP VIEW



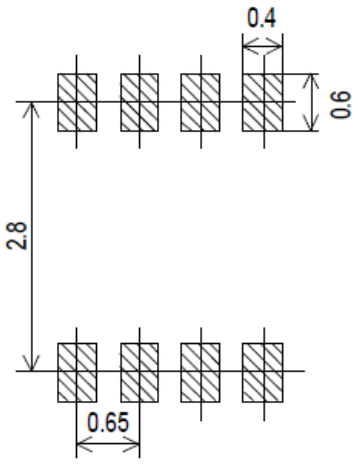
BOTTOM VIEW



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
c	0.19	0.20	0.21
D	2.90	3.00	3.10
Nd	1.90	1.95	2.00
E	2.90	3.00	3.10
e	0.65BSC		
L	0.37	0.42	0.47
h	0.10	0.15	0.20
载体尺寸（mil）	102X84		

DFNWB3×3-8L-K Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.050mm.
3.The pad layout is for reference purposes only.