2×600mA,Dual Channel Ultra-Fast CMOS LDO Regulator

General Description

The LP2206 is a dual channel, low noise, and low dropout regulator sourcing up to 600mA at each channel. The range of output voltage is from 0.81V to Vin by operating from 2.5V to 5.5V input.

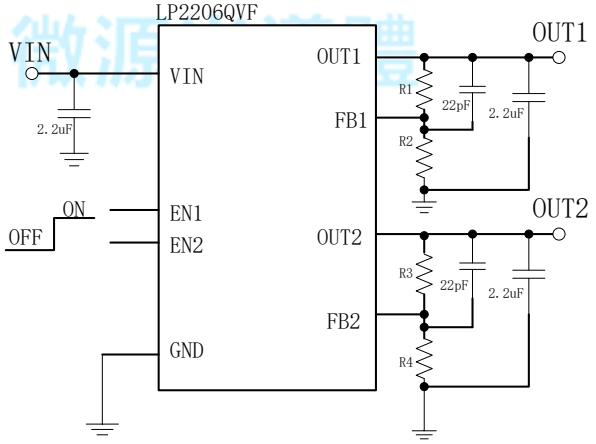
LP2206 offers 2% accuracy, extremely low dropout voltage (280mV @ 400mA), and extremely low ground current, only 75μA per LDO. The shutdown current is near zero current which is suitable for battery-power devices. Other features include current limiting, over temperature, output short circuit protection.

LP2206 can operate stably with very small ceramic output capacitors, reducing required board space and component cost. LP2206 is available in fixed output voltages in the TDFN-8(2*2mm) and ESOP8 package.

Features

- Wide Operating Voltage Ranges : 2.5V to 6.0V
- Low-Noise for RF Applications
- High PSRR: -68dB at 1kHz
- No Noise Bypass Capacitor Required
- Fast Response in Line/Load Transient
- TTL-Logic-Controlled Shutdown Input
- Dual LDO Outputs (280mV/400mA)
- High Output Accuracy 2%
- Ultra-low Quiescent Current 75uA
- Thermal Shutdown Protection
- RoHS Compliant and 100% Lead (Pb)-Free

Typical Application Circuit



Order Information

LP2206 □ □ □

- F: Pb-Free
- Package Type
  - QV: TDFN-8
  - SP: ESOP8

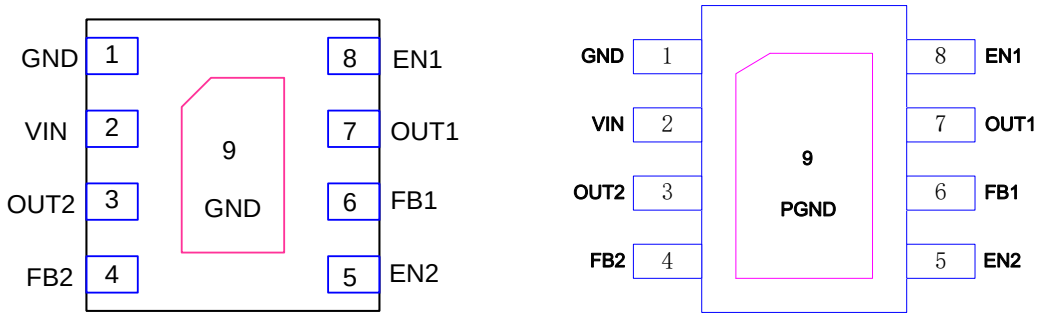
Marking Information

Device	Marking	Package	Shipping
LP2206QVF	2206 YWX	TDFN-8	3K/REEL
LP2206SPF	LPS LP2206 YWX	ESOP-8	2.5K/REEL
Y: Year code. W: Week code. X: Batch numbers.			

Applications

- CDMA/GSM Cellular Handsets
- Smart mobile phone
- Battery-Powered Equipment
- DSC Sensor
- Wireless Card

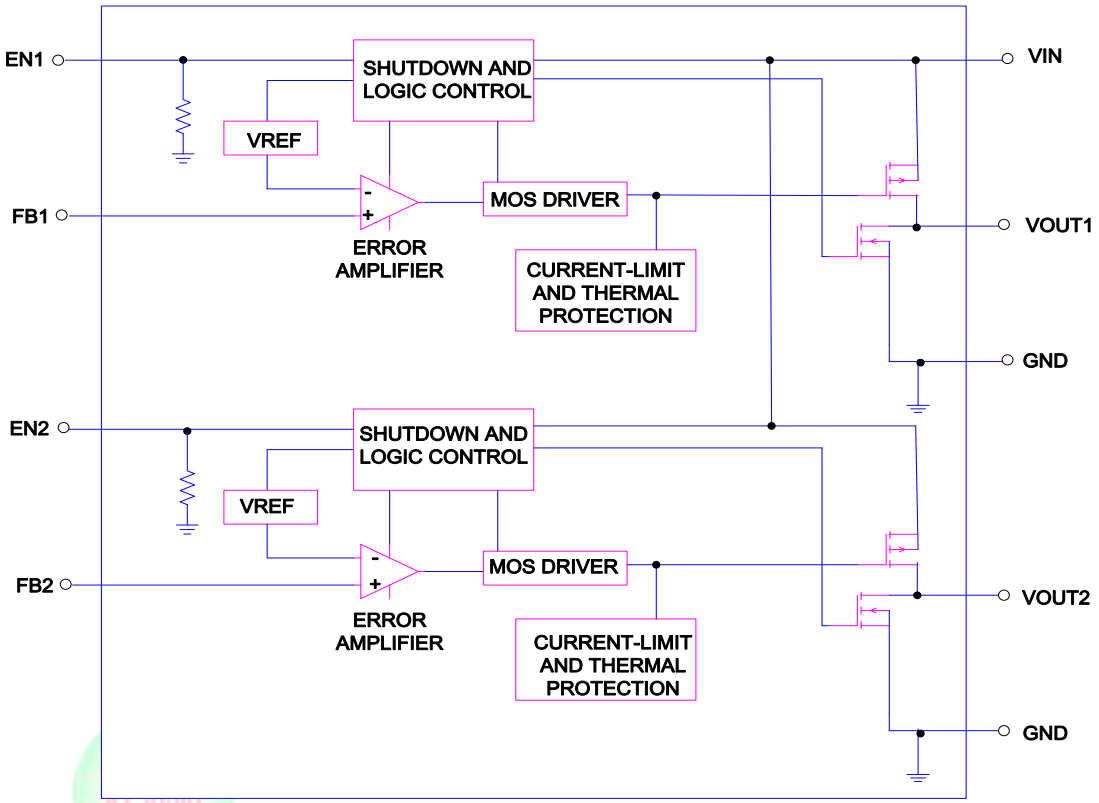
Functional Pin Description

Package Type	Pin Configurations
TDFN-8 / ESOP-8	

Pin Description

Pin	Name	Description
1	GND	Ground pin.
2	VIN	Input pin.
3	OUT2	Output pin of channel 2.
4	FB2	Feedback pin of channel 2.
5	EN2	Enable pin of channel 2.
6	FB1	Feedback pin of channel 2.
7	OUT1	Output pin of channel 1.
8	EN1	Enable pin of channel 2.
9	GND	Ground pin.

Function Diagram



Absolute Maximum Ratings

- ✧ Supply Input Voltage ---------- 7V

Power Dissipation, PD @ TA = 25°C

- ✧ TDFN-8 ---------- 1.2W
- ✧ ESOP-8 ---------- 2.0W

Package Thermal Resistance

- ✧ TDFN-8, θJA ---------- 95°C/W
- ✧ ESOP-8, θJA ---------- 50°C/W
- ✧ Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- ✧ Storage Temperature Range ---------- −65°C to 165°C

ESD Susceptibility

- ✧ HBM (Human Body Mode) ---------- 2kV
- ✧ MM(Machine-Mode) ---------- 200V

Recommended Operating Conditions

- ✧ Operation Junction Temperature Range ---------- −40°C to 125°C
- ✧ Operation Ambient Temperature Range ---------- −40°C to 85°C

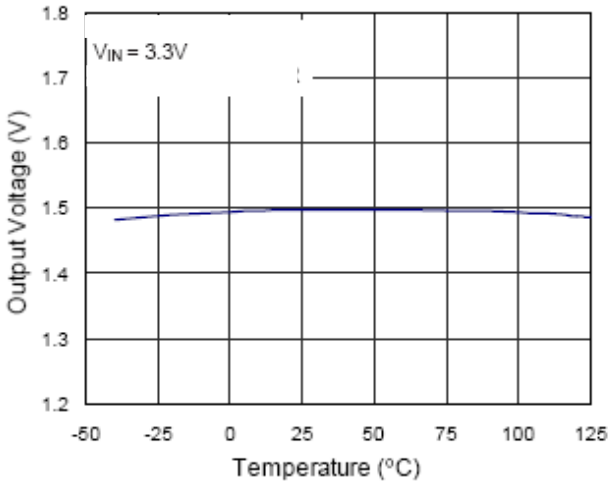
Electrical Characteristics

(V_{IN} = V_{OUT} + 1V, C_{IN} = C_{OUT} = 2.2μF,C_{FB}=22pF, T_A = 25° C, unless otherwise specified)

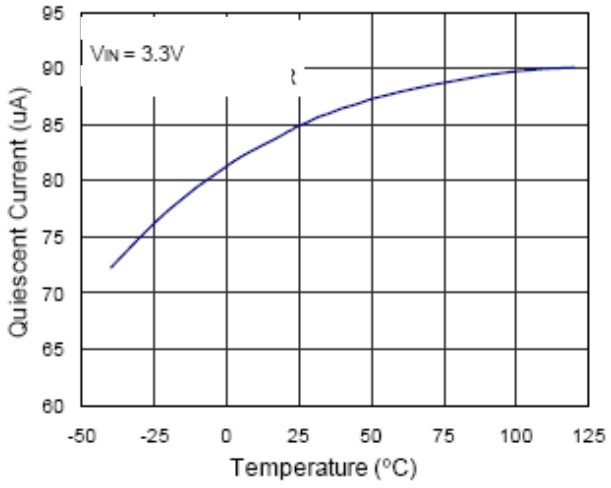
Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Maximum output Current		I_{max}	R_{LOAD} = 1Ω		750		mA
Current Limit		I_{LIM}	I_{OUT}=1mA	0.784	0.8	0.816	mA
Quiescent Current		I_Q	V_{EN} ≥ 1.4V, I_{OUT} = 0mA		90	130	μA
Dropout Voltage		V_{DROP}	I_{OUT} = 200mA, V_{OUT} >2.8V		140	160	mV
			I_{OUT} = 400mA, V_{OUT} >2.8V		280	320	mV
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 1V) to 5.5V, I_{OUT} = 1mA			0.3	%
Load Regulation		ΔV_{LOAD}	1mA < I_{OUT} < 400mA			2	%
Standby Current		I_{STBY}	V_{EN} = GND, Shutdown		0.01	1	μA
EN Input Bias Current		I_{IBSD}	V_{EN} = 1V or 5V	0.8		5.3	uA
EN Threshold	Logic-Low Voltage	V_{IL}	V_{IN} = 3V to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	V_{IH}	V_{IN} = 3V to 5.5V, Start-Up	1.4			V
Output Noise Voltage			10Hz to 100kHz, I_{OUT} = 200mA		100		uVRMS
Power Supply Rejection Rate	f=1kHz	PSRR	I_{OUT} = 10mA		−76		dB
	f=10kHz				−68		dB
Thermal Shutdown Temperature		T_{SD}			150		°C

Typical Operating Characteristics

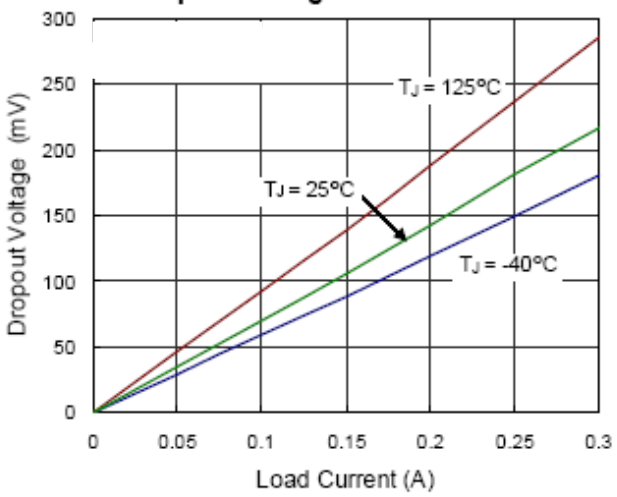
Output Voltage vs. Temperature



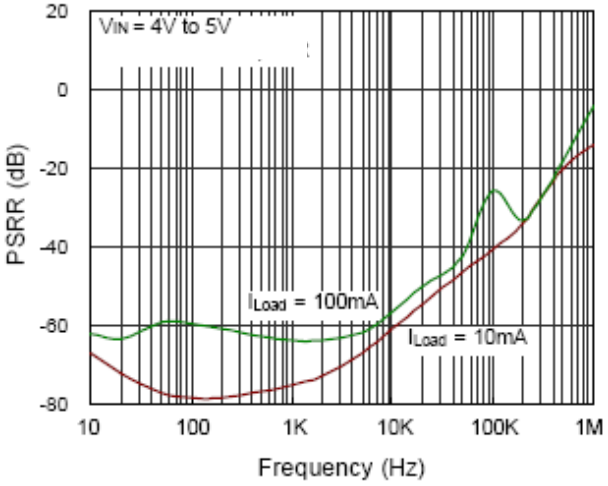
Quiescent Current vs. Temperature



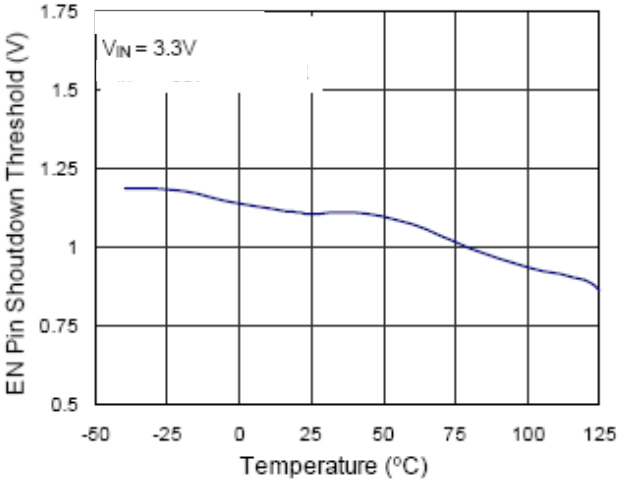
Dropout Voltage vs. Load Current



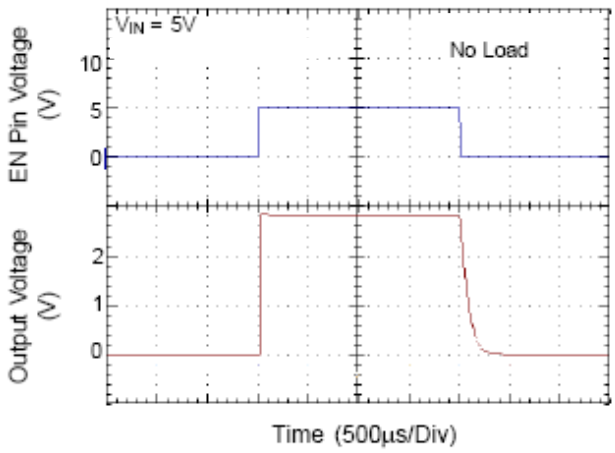
PSRR



EN Pin Shoutdown Threshold vs. Temperature



EN Pin Shutdown Response



Application Information

Like any low-dropout regulator, the external capacitors used with the LP2206 must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 2μF on the LP2206 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP2206 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 25mΩ on theLP2206 output ensures stability. The LP2206 still works well with output capacitor of other types due to the wide stable ESR range. Output capacitor of larger capacitance can reduce noise and improve load transient response. The output capacitor should be located no more than 0.5 inch from the VOUT pin of the LP2206 and returned to a clean analog ground.

Start-up Function Enable Function

The LP2206 features an LDO regulator enable/disable function. To ensure the LDO regulator will switch on, the EN turn on control level must be greater than 1.4 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. To protect the system, the LP2206 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state mode.

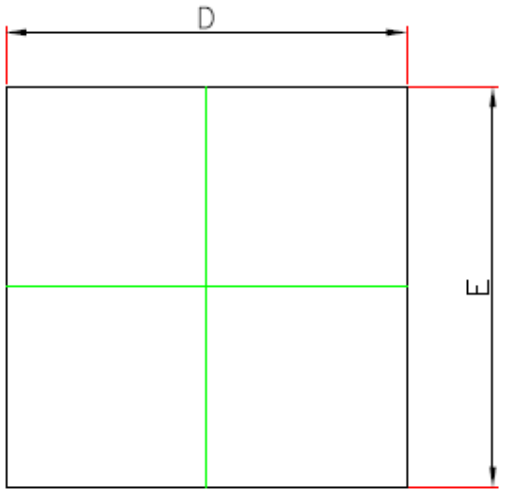
Setting the Output Voltage

Set the output voltage by selecting the resistive voltage divider ratio. The voltage divider drops the output voltage to the 0.8V feedback voltage. Use a 100K resistor for R2 of the voltage divider. Determine the high-side resistor R1 by the equation:

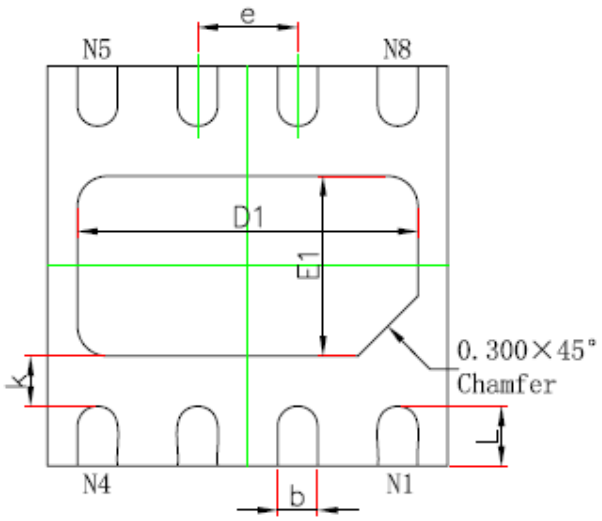
$$Vout=(R1/R2+1) \times V_{FB}$$

Packaging Information

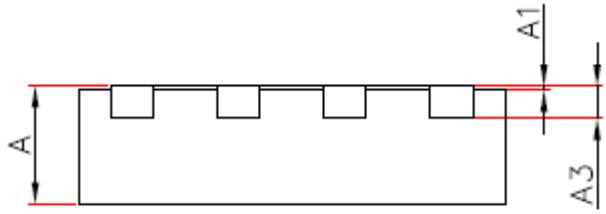
TDFN-8



TOP VIEW



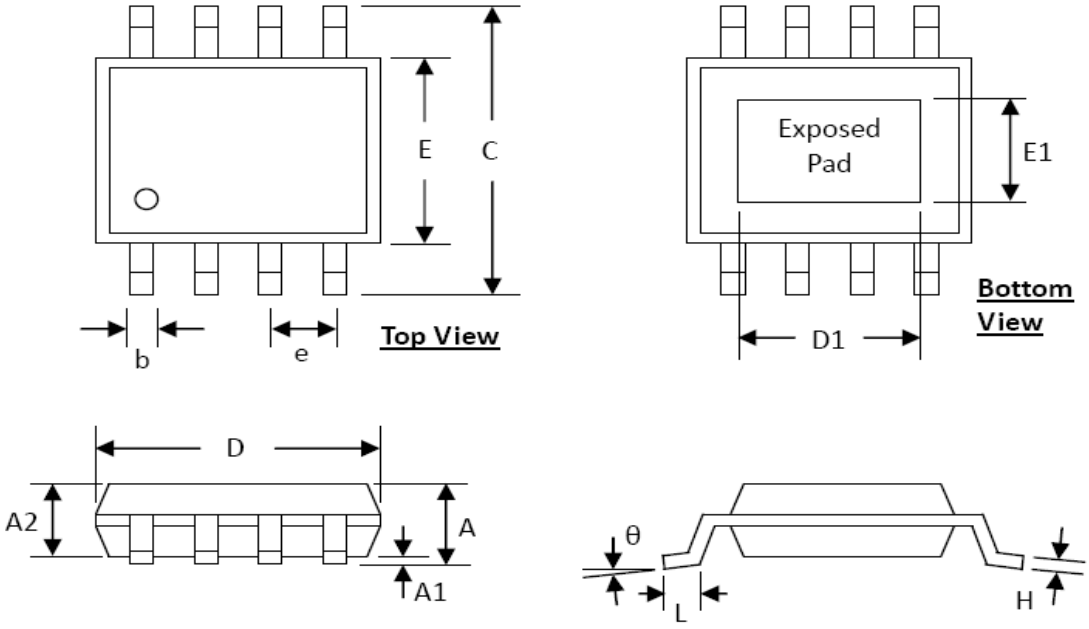
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions In Millimeters	Dimensions In Inches
	Norm.	Norm.
A	0.550+/-0.050	0.022+/-0.002
A1	0.000 | 0.050	0.000 | 0.002
A3	0.152REF.	0.006REF.
D	2.000+/-0.100	0.079+/-0.004
E	2.000+/-0.100	0.079+/-0.004
D1	1.700+/-0.100	0.067+/-0.004
E1	0.900+/-0.100	0.035+/-0.004
k	0.200MIN.	0.008MIN.
b	0.200+/-0.050	0.008+/-0.002
e	0.500TYP.	0.020TYP.
L	0.300+/-0.050	0.012+/-0.002

ESOP-8



SYMBOLS	DIMENSION (MM)		DIMENSION (INCH)	
	MIN	MAX	MIN	MAX
A	1.30	1.70	0.051	0.067
A1	0.00	0.15	0.000	0.006
A2	1.25	1.52	0.049	0.060
b	0.33	0.51	0.013	0.020
C	5.80	6.20	0.228	0.244
D	4.80	5.00	0.189	0.197
D1	3.15	3.45	0.124	0.136
E	3.80	4.00	0.150	0.157
E1	2.26	2.56	0.089	0.101
e	1.27 BSC		0.050 BSC	
H	0.19	0.25	0.0075	0.0098
L	0.41	1.27	0.016	0.050
θ	0°	8°	0°	8°