

## FEATURES

1.8 V analog supply operation

1.8 V to 3.3 V output supply

SNR

71.3 dBFS at 9.7 MHz input

69.0 dBFS at 200 MHz input

SFDR

95 dBc at 9.7 MHz input

83 dBc at 200 MHz input

Low power

45 mW at 20 MSPS

85 mW at 80 MSPS

Differential input with 700 MHz bandwidth

On-chip voltage reference and sample-and-hold circuit

2 V p-p differential analog input

DNL =  $\pm 0.16$  LSB

Serial port control options

Offset binary, gray code, or twos complement data format

Integer 1, 2, or 4 input clock divider

Built-in selectable digital test pattern generation

Energy-saving power-down modes

Data clock out with programmable clock and data alignment

## APPLICATIONS

Communications

Diversity radio systems

Multimode digital receivers

GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, TD-SCDMA

Smart antenna systems

Battery-powered instruments

Hand held scope meters

Portable medical imaging

Ultrasound

Radar/LIDAR

PET/SPECT imaging

## FUNCTIONAL BLOCK DIAGRAM

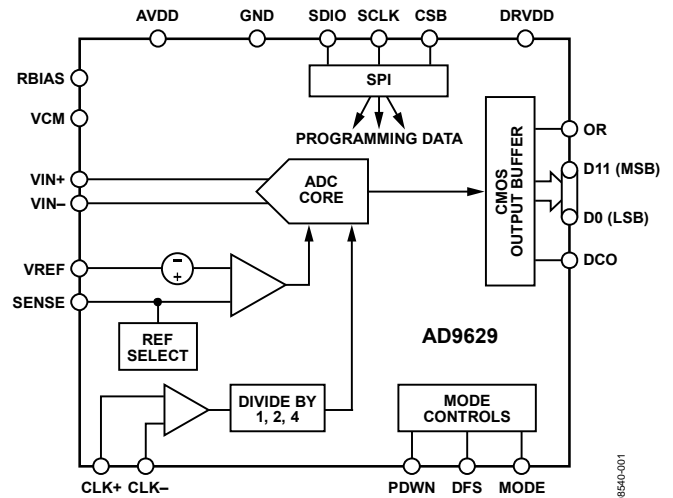


Figure 1.

## PRODUCT HIGHLIGHTS

1. The [AD9629](#) operates from a single 1.8 V analog power supply and features a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
2. The sample-and-hold circuit maintains excellent performance for input frequencies up to 200 MHz and is designed for low cost, low power, and ease of use.
3. A standard serial port interface (SPI) supports various product features and functions, such as data output formatting, internal clock divider, power-down, DCO and data output (D11 to D0) timing and offset adjustments, and voltage reference modes.
4. The [AD9629](#) is packaged in a 32-lead RoHS compliant LFCSP that is pin compatible with the [AD9609](#) 10-bit ADC and the [AD9649](#) 14-bit ADC, enabling a simple migration path between 10-bit and 14-bit converters sampling from 20 MSPS to 80 MSPS.

Rev. B

[Document Feedback](#)

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## REVISION HISTORY

### 2/2017—Rev. A to Rev B

|  |    |
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| Added Endnote 1, Table 16.....                           | 28 |
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| Added Soft Reset Section.....                            | 30 |

### 6/2015—Rev. 0 to Rev. A

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### 10/2009—Revision 0: Initial Version

## GENERAL DESCRIPTION

The [AD9629](#) is a monolithic, single channel 1.8 V supply, 12-bit, 20 MSPS/40 MSPS/65 MSPS/80 MSPS analog-to-digital converter (ADC). It features a high performance sample-and-hold circuit and on-chip voltage reference.

The product uses multistage differential pipeline architecture with output error correction logic to provide 12-bit accuracy at 80 MSPS data rates and to guarantee no missing codes over the full operating temperature range.

The ADC contains several features designed to maximize flexibility and minimize system cost, such as programmable clock and data alignment and programmable digital test pattern generation. The available digital test patterns include built-in

deterministic and pseudorandom patterns, along with custom user-defined test patterns entered via the serial port interface (SPI).

A differential clock input with optional 1, 2, or 4 divide ratios controls all internal conversion cycles.

The digital output data is presented in offset binary, gray code, or twos complement format. A data output clock (DCO) is provided to ensure proper latch timing with receiving logic. Both 1.8 V and 3.3 V CMOS levels are supported.

The [AD9629](#) is available in a 32-lead RoHS compliant LFCSP and is specified over the industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ).

## SPECIFICATIONS

### DC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

Table 1.

| Parameter                                    | Temp | AD9629-20/AD9629-40 |       |           | AD9629-65  |       |       | AD9629-80  |       |       | Unit    |
|--|------|---------------------|-------|-----------|------------|-------|-------|------------|-------|-------|---------|
|  |      | Min                 | Typ   | Max       | Min        | Typ   | Max   | Min        | Typ   | Max   |         |
| RESOLUTION                                   | Full | 12                  |       |           | 12         |       |       | 12         |       |       | Bits    |
| ACCURACY                                     |      | Guaranteed          |       |           | Guaranteed |       |       | Guaranteed |       |       |         |
| No Missing Codes                             | Full | Guaranteed          |       |           | Guaranteed |       |       | Guaranteed |       |       |         |
| Offset Error                                 | Full | -0.40               | +0.05 | +0.50     | -0.40      | +0.05 | +0.50 | -0.40      | +0.05 | +0.50 | % FSR   |
| Gain Error <sup>1</sup>                      | Full | -1.5                |       |           | -1.5       |       |       | -1.5       |       |       | % FSR   |
| Differential Nonlinearity (DNL) <sup>2</sup> | Full | ±0.25               |       |           | ±0.25      |       |       | ±0.30      |       |       | LSB     |
|  | 25°C | ±0.11               |       |           | ±0.11      |       |       | ±0.16      |       |       | LSB     |
| Integral Nonlinearity (INL) <sup>2</sup>     | Full | ±0.40               |       |           | ±0.30      |       |       | ±0.35      |       |       | LSB     |
|  | 25°C | ±0.11               |       |           | ±0.13      |       |       | ±0.16      |       |       | LSB     |
| TEMPERATURE DRIFT                            |      |                     |       |           |            |       |       |            |       |       |         |
| Offset Error                                 | Full | ±2                  |       |           | ±2         |       |       | ±2         |       |       | ppm/°C  |
| INTERNAL VOLTAGE REFERENCE                   |      |                     |       |           |            |       |       |            |       |       |         |
| Output Voltage (1 V Mode)                    | Full | 0.984               | 0.996 | 1.008     | 0.984      | 0.996 | 1.008 | 0.984      | 0.996 | 1.008 | V       |
| Load Regulation Error at 1.0 mA              | Full | 2                   |       |           | 2          |       |       | 2          |       |       | mV      |
| INPUT-REFERRED NOISE                         |      |                     |       |           |            |       |       |            |       |       |         |
| VREF = 1.0 V                                 | 25°C | 0.25                |       |           | 0.25       |       |       | 0.25       |       |       | LSB rms |
| ANALOG INPUT                                 |      |                     |       |           |            |       |       |            |       |       |         |
| Input Span, VREF = 1.0 V                     | Full | 2                   |       |           | 2          |       |       | 2          |       |       | V p-p   |
| Input Capacitance <sup>3</sup>               | Full | 6                   |       |           | 6          |       |       | 6          |       |       | pF      |
| Input Common-Mode Voltage                    | Full | 0.9                 |       |           | 0.9        |       |       | 0.9        |       |       | V       |
| Input Common-Mode Range                      | Full | 0.5                 | 1.3   |           | 0.5        | 1.3   |       | 0.5        | 1.3   |       | V       |
| REFERENCE INPUT RESISTANCE                   | Full | 7.5                 |       |           | 7.5        |       |       | 7.5        |       |       | kΩ      |
| POWER SUPPLIES                               |      |                     |       |           |            |       |       |            |       |       |         |
| Supply Voltage                               |      |                     |       |           |            |       |       |            |       |       |         |
| AVDD   | Full | 1.7                 | 1.8   | 1.9       | 1.7        | 1.8   | 1.9   | 1.7        | 1.8   | 1.9   | V       |
| DRVDD  | Full | 1.7                 | 3.6   |           | 1.7        | 3.6   |       | 1.7        | 3.6   |       | V       |
| Supply Current                               |      |                     |       |           |            |       |       |            |       |       |         |
| IAVDD <sup>2</sup>                           | Full | 24.9/31.1           |       | 26.7/33.2 | 41.2       |       | 46.0  | 46.8       |       | 50.0  | mA      |
| IDRVDD <sup>2</sup> (1.8 V)                  | Full | 1.5/2.5             |       |           | 4.2        |       |       | 5.0        |       |       | mA      |
| IDRVDD <sup>2</sup> (3.3 V)                  | Full | 2.7/4.7             |       |           | 7.5        |       |       | 9.0        |       |       | mA      |
| POWER CONSUMPTION                            |      |                     |       |           |            |       |       |            |       |       |         |
| DC Input                                     | Full | 45.0/56.7           |       |           | 75         |       |       | 85.2       |       |       | mW      |
| Sine Wave Input <sup>2</sup> (DRVDD = 1.8 V) | Full | 47.5/60.5           |       | 50.7/65.0 | 81.7       |       | 86.0  | 93         |       | 100   | mW      |
| Sine Wave Input <sup>2</sup> (DRVDD = 3.3 V) | Full | 53.7/71.7           |       |           | 98.9       |       |       | 114        |       |       | mW      |
| Standby Power <sup>4</sup>                   | Full | 34                  |       |           | 34         |       |       | 34         |       |       | mW      |
| Power-Down Power                             | Full | 0.5                 |       |           | 0.5        |       |       | 0.5        |       |       | mW      |

<sup>1</sup> Measured with 1.0 V external reference.

<sup>2</sup> Measured with a 10 MHz input frequency at rated sample rate, full-scale sine wave, with approximately 5 pF loading on each output bit.

<sup>3</sup> Input capacitance refers to the effective capacitance between one differential input pin and AGND.

<sup>4</sup> Standby power is measured with a dc input and the clock active.

## AC SPECIFICATIONS

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

Table 2.

| Parameter <sup>1</sup>                            | Temp                | AD9629-20/AD9629-40 |           |           | AD9629-65 |      |      | AD9629-80 |     |      | Unit |
|---|---------------------|---------------------|-----------|-----------|-----------|------|------|-----------|-----|------|------|
|   |                     | Min                 | Typ       | Max       | Min       | Typ  | Max  | Min       | Typ | Max  |      |
| SIGNAL-TO-NOISE RATIO (SNR)                       | $f_{IN} = 9.7$ MHz  | 25°C                |           | 71.4      |           | 71.3 |      | 71.3      |     |      | dBFS |
|   | $f_{IN} = 30.5$ MHz | 25°C                |           | 71.2      |           | 71.2 |      | 71.2      |     |      | dBFS |
|   |                     | Full                | 70.5/70.7 |           |           | 70.6 |      |           |     |      | dBFS |
|   | $f_{IN} = 70$ MHz   | 25°C                |           | 70.5/71.0 |           | 71.0 |      | 70.9      |     |      | dBFS |
|   |                     | Full                |           |           |           |      | 70.3 |           |     |      | dBFS |
| $f_{IN} = 200$ MHz                                | 25°C                |                     |           |           |           | 69.0 |      | 69.0      |     | dBFS |      |
| SIGNAL-TO-NOISE-AND-DISTORTION (SINAD)            | $f_{IN} = 9.7$ MHz  | 25°C                |           | 71.4      |           | 71.3 |      | 71.2      |     |      | dBFS |
|   | $f_{IN} = 30.5$ MHz | 25°C                |           | 71.2      |           | 71.2 |      | 71.1      |     |      | dBFS |
|   |                     | Full                | 70.5/70.6 |           |           | 70.5 |      |           |     |      | dBFS |
|   | $f_{IN} = 70$ MHz   | 25°C                |           | 70.4/70.9 |           | 70.9 |      | 70.8      |     |      | dBFS |
|   |                     | Full                |           |           |           |      | 70.2 |           |     |      | dBFS |
| $f_{IN} = 200$ MHz                                | 25°C                |                     | 68        |           | 68        |      | 68   |           |     | dBFS |      |
| EFFECTIVE NUMBER OF BITS (ENOB)                   | $f_{IN} = 9.7$ MHz  | 25°C                |           | 11.4/11.6 |           | 11.6 |      | 11.5      |     |      | Bits |
|   | $f_{IN} = 30.5$ MHz | 25°C                |           | 11.4/11.5 |           | 11.5 |      | 11.5      |     |      | Bits |
|   | $f_{IN} = 70$ MHz   | 25°C                |           | 11.4/11.5 |           | 11.5 |      | 11.5      |     |      | Bits |
|   | $f_{IN} = 200$ MHz  | 25°C                |           | 11.0      |           | 11.0 |      | 11.0      |     |      | Bits |
| WORST SECOND OR THIRD HARMONIC                    | $f_{IN} = 9.7$ MHz  | 25°C                |           | -97       |           | -97  |      | -95       |     |      | dBc  |
|   | $f_{IN} = 30.5$ MHz | 25°C                |           | -95       |           | -95  |      | -94       |     |      | dBc  |
|   |                     | Full                |           |           | -83       |      | -83  |           |     |      | dBc  |
|   | $f_{IN} = 70$ MHz   | 25°C                |           | -96/-94   |           | -95  |      | -95       |     |      | dBc  |
|   |                     | Full                |           |           |           |      |      |           | -81 |      | dBc  |
| $f_{IN} = 200$ MHz                                | 25°C                |                     | -83       |           | -83       |      | -83  |           |     | dBc  |      |
| SPURIOUS-FREE DYNAMIC RANGE (SFDR)                | $f_{IN} = 9.7$ MHz  | 25°C                |           | 97        |           | 97   |      | 95        |     |      | dBc  |
|   | $f_{IN} = 30.5$ MHz | 25°C                |           | 96/95     |           | 95   |      | 93        |     |      | dBc  |
|   |                     | Full                | 83        |           |           | 83   |      |           |     |      | dBc  |
|   | $f_{IN} = 70$ MHz   | 25°C                |           | 96/94     |           | 95   |      | 95        |     |      | dBc  |
|   |                     | Full                |           |           |           |      | 81   |           |     |      | dBc  |
| $f_{IN} = 200$ MHz                                | 25°C                |                     | 83        |           | 83        |      | 83   |           |     | dBc  |      |
| WORST OTHER (HARMONIC OR SPUR)                    | $f_{IN} = 9.7$ MHz  | 25°C                |           | -100      |           | -100 |      | -100      |     |      | dBc  |
|   | $f_{IN} = 30.5$ MHz | 25°C                |           | -100      |           | -100 |      | -100      |     |      | dBc  |
|   |                     | Full                |           |           | -92/-91   |      | -93  |           |     |      | dBc  |
|   | $f_{IN} = 70$ MHz   | 25°C                |           | -97/-100  |           | -100 |      | -100      |     |      | dBc  |
|   |                     | Full                |           |           |           |      |      |           | -89 |      | dBc  |
| $f_{IN} = 200$ MHz                                | 25°C                |                     | -92       |           | -92       |      | -92  |           |     | dBc  |      |
| TWO-TONE SFDR                                     |                     |                     |           |           |           |      |      |           |     |      |      |
| $f_{IN} = 30.5$ MHz (-7 dBFS), 32.5 MHz (-7 dBFS) | 25°C                |                     | 90        |           | 90        |      | 90   |           |     | dBc  |      |
| ANALOG INPUT BANDWIDTH                            | 25°C                |                     | 700       |           | 700       |      | 700  |           |     | MHz  |      |

<sup>1</sup> See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.

**DIGITAL SPECIFICATIONS**

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

**Table 3.**

| Parameter   | Temp | AD9629-20/AD9629-40/AD9629-65/AD9629-80 |                  |             | Unit  |
|---|------|---|------------------|-------------|-------|
|   |      | Min                                     | Typ              | Max         |       |
| <b>DIFFERENTIAL CLOCK INPUTS (CLK+, CLK-)</b>               |      |   |                  |             |       |
| Logic Compliance  |      |   | CMOS/LVDS/LVPECL |             |       |
| Internal Common-Mode Bias                                   | Full |   | 0.9              |             | V     |
| Differential Input Voltage                                  | Full | 0.2                                     |                  | 3.6         | V p-p |
| Input Voltage Range   | Full | GND - 0.3                               |                  | AVDD + 0.2  | V     |
| High Level Input Current                                    | Full | -10                                     |                  | +10         | μA    |
| Low Level Input Current                                     | Full | -10                                     |                  | +10         | μA    |
| Input Resistance  | Full | 8                                       | 10               | 12          | kΩ    |
| Input Capacitance   | Full |   | 4                |             | pF    |
| <b>LOGIC INPUTS (SCLK/DFS, MODE, SDIO/PDWN)<sup>1</sup></b> |      |   |                  |             |       |
| High Level Input Voltage                                    | Full | 1.2                                     |                  | DRVDD + 0.3 | V     |
| Low Level Input Voltage                                     | Full | 0                                       |                  | 0.8         | V     |
| High Level Input Current                                    | Full | -50                                     |                  | -75         | μA    |
| Low Level Input Current                                     | Full | -10                                     |                  | +10         | μA    |
| Input Resistance  | Full |   | 30               |             | kΩ    |
| Input Capacitance   | Full |   | 2                |             | pF    |
| <b>LOGIC INPUTS (CSB)<sup>2</sup></b>                       |      |   |                  |             |       |
| High Level Input Voltage                                    | Full | 1.2                                     |                  | DRVDD + 0.3 | V     |
| Low Level Input Voltage                                     | Full | 0                                       |                  | 0.8         | V     |
| High Level Input Current                                    | Full | -10                                     |                  | +10         | μA    |
| Low Level Input Current                                     | Full | 40                                      |                  | 135         | μA    |
| Input Resistance  | Full |   | 26               |             | kΩ    |
| Input Capacitance   | Full |   | 2                |             | pF    |
| <b>DIGITAL OUTPUTS</b>                                      |      |   |                  |             |       |
| DRVDD = 3.3 V   |      |   |                  |             |       |
| High Level Output Voltage, I <sub>OH</sub> = 50 μA          | Full | 3.29                                    |                  |             | V     |
| High Level Output Voltage, I <sub>OH</sub> = 0.5 mA         | Full | 3.25                                    |                  |             | V     |
| Low Level Output Voltage, I <sub>OL</sub> = 1.6 mA          | Full |   |                  | 0.2         | V     |
| Low Level Output Voltage, I <sub>OL</sub> = 50 μA           | Full |   |                  | 0.05        | V     |
| DRVDD = 1.8 V   |      |   |                  |             |       |
| High Level Output Voltage, I <sub>OH</sub> = 50 μA          | Full | 1.79                                    |                  |             | V     |
| High Level Output Voltage, I <sub>OH</sub> = 0.5 mA         | Full | 1.75                                    |                  |             | V     |
| Low Level Output Voltage, I <sub>OL</sub> = 1.6 mA          | Full |   |                  | 0.2         | V     |
| Low Level Output Voltage, I <sub>OL</sub> = 50 μA           | Full |   |                  | 0.05        | V     |

<sup>1</sup> Internal 30 kΩ pull-down.<sup>2</sup> Internal 30 kΩ pull-up.

**SWITCHING SPECIFICATIONS**

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

Table 4.

| Parameter                                  | Temp | AD9629-20/AD9629-40 |           |        | AD9629-65 |      |     | AD9629-80 |      |     | Unit    |
|--|------|---------------------|-----------|--------|-----------|------|-----|-----------|------|-----|---------|
|  |      | Min                 | Typ       | Max    | Min       | Typ  | Max | Min       | Typ  | Max |         |
| <b>CLOCK INPUT PARAMETERS</b>              |      |                     |           |        |           |      |     |           |      |     |         |
| Input Clock Rate <sup>1</sup>              | Full |                     |           | 80/160 |           |      | 260 |           |      | 320 | MHz     |
| Conversion Rate <sup>2</sup>               | Full | 3                   |           | 20/40  | 3         |      | 65  | 3         |      | 80  | MSPS    |
| CLK Period, Divide-by-1 Mode ( $t_{CLK}$ ) | Full | 50/25               |           |        | 15.38     |      |     | 12.5      |      |     | ns      |
| CLK Pulse Width High ( $t_{CH}$ )          |      |                     | 25.0/12.5 |        |           | 7.69 |     |           | 6.25 |     | ns      |
| Aperture Delay ( $t_A$ )                   | Full |                     | 1.0       |        |           | 1.0  |     |           | 1.0  |     | ns      |
| Aperture Uncertainty (Jitter, $t_j$ )      | Full |                     | 0.1       |        |           | 0.1  |     |           | 0.1  |     | ps rms  |
| <b>DATA OUTPUT PARAMETERS</b>              |      |                     |           |        |           |      |     |           |      |     |         |
| Data Propagation Delay ( $t_{PD}$ )        | Full |                     | 3         |        |           | 3    |     |           | 3    |     | ns      |
| DCO Propagation Delay ( $t_{DCO}$ )        | Full |                     | 3         |        |           | 3    |     |           | 3    |     | ns      |
| DCO to Data Skew ( $t_{SKEW}$ )            | Full |                     | 0.1       |        |           | 0.1  |     |           | 0.1  |     | ns      |
| Pipeline Delay (Latency)                   | Full |                     | 8         |        |           | 8    |     |           | 8    |     | Cycles  |
| Wake-Up Time <sup>3</sup>                  | Full |                     | 350       |        |           | 350  |     |           | 350  |     | $\mu$ s |
| Standby                                    | Full |                     | 600/400   |        |           | 300  |     |           | 260  |     | ns      |
| <b>OUT-OF-RANGE RECOVERY TIME</b>          | Full |                     | 2         |        |           | 2    |     |           | 2    |     | Cycles  |

<sup>1</sup> Input clock rate is the clock rate before the internal CLK divider.

<sup>2</sup> Conversion rate is the clock rate after the CLK divider.

<sup>3</sup> Wake-up time is dependent on the value of the decoupling capacitors.

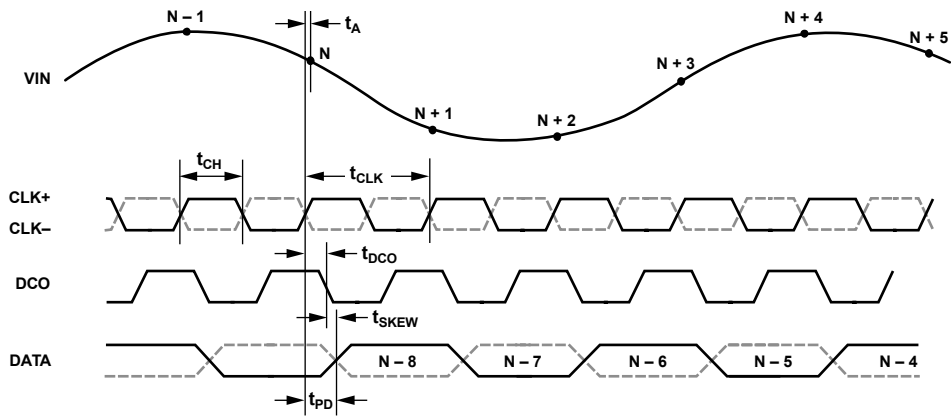


Figure 2. CMOS Output Data Timing

## TIMING SPECIFICATIONS

Table 5.

| Parameter               | Conditions  | Min | Typ | Max | Unit |
|-------------------------|---|-----|-----|-----|------|
| SPI TIMING REQUIREMENTS |   |     |     |     |      |
| $t_{DS}$                | Setup time between the data and the rising edge of SCLK   | 2   |     |     | ns   |
| $t_{DH}$                | Hold time between the data and the rising edge of SCLK  | 2   |     |     | ns   |
| $t_{CLK}$               | Period of the SCLK  | 40  |     |     | ns   |
| $t_S$                   | Setup time between CSB and SCLK   | 2   |     |     | ns   |
| $t_H$                   | Hold time between CSB and SCLK  | 2   |     |     | ns   |
| $t_{HIGH}$              | SCLK pulse width high   | 10  |     |     | ns   |
| $t_{LOW}$               | SCLK pulse width low  | 10  |     |     | ns   |
| $t_{EN\_SDIO}$          | Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge | 10  |     |     | ns   |
| $t_{DIS\_SDIO}$         | Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge  | 10  |     |     | ns   |



## ABSOLUTE MAXIMUM RATINGS

Table 6.

| Parameter                               | Rating                  |
|---|-------------------------|
| AVDD to AGND                            | −0.3 V to +2.0 V        |
| DRVDD to AGND                           | −0.3 V to +3.9 V        |
| VIN+, VIN− to AGND                      | −0.3 V to AVDD + 0.2 V  |
| CLK+, CLK− to AGND                      | −0.3 V to AVDD + 0.2 V  |
| VREF to AGND                            | −0.3 V to AVDD + 0.2 V  |
| SENSE to AGND                           | −0.3 V to AVDD + 0.2 V  |
| VCM to AGND                             | −0.3 V to AVDD + 0.2 V  |
| RBIAS to AGND                           | −0.3 V to AVDD + 0.2 V  |
| CSB to AGND                             | −0.3 V to DRVDD + 0.3 V |
| SCLK/DFS to AGND                        | −0.3 V to DRVDD + 0.3 V |
| SDIO/PDWN to AGND                       | −0.3 V to DRVDD + 0.3 V |
| MODE/OR to AGND                         | −0.3 V to DRVDD + 0.3 V |
| D0 through D11 to AGND                  | −0.3 V to DRVDD + 0.3 V |
| DCO to AGND                             | −0.3 V to DRVDD + 0.3 V |
| Operating Temperature Range (Ambient)   | −40°C to +85°C          |
| Maximum Junction Temperature Under Bias | 150°C                   |
| Storage Temperature Range (Ambient)     | −65°C to +150°C         |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL CHARACTERISTICS

The exposed paddle is the only ground connection for the chip. The exposed paddle must be soldered to the AGND plane of the user's circuit board. Soldering the exposed paddle to the user's board also increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 7. Thermal Resistance

| Package Type  | Airflow Velocity (m/sec) | $\theta_{JA}^{1,2}$ | $\theta_{JC}^{1,3}$ | $\theta_{JB}^{1,4}$ | $\Psi_{JT}^{1,2}$ | Unit |
|---------------|--------------------------|---------------------|---------------------|---------------------|-------------------|------|
| 32-Lead LFCSP | 0                        | 37.1                | 3.1                 | 20.7                | 0.3               | °C/W |
| 5 mm × 5 mm   | 1.0                      | 32.4                |                     |                     | 0.5               | °C/W |
|               | 2.5                      | 29.1                |                     |                     | 0.8               | °C/W |

<sup>1</sup> Per JEDEC 51-7, plus JEDEC 51-5 2S2P test board.

<sup>2</sup> Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).

<sup>3</sup> Per MIL-Std 883, Method 1012.1.

<sup>4</sup> Per JEDEC JESD51-8 (still air).

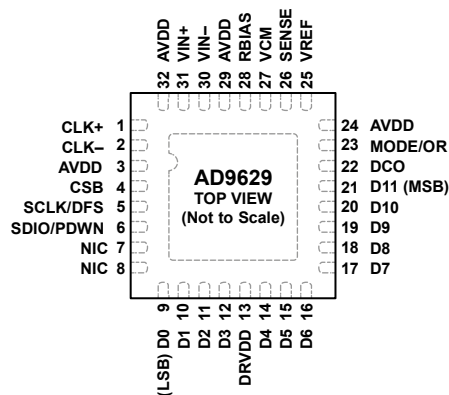
Typical  $\theta_{JA}$  is specified for a 4-layer PCB with a solid ground plane. As shown in Table 7, airflow improves heat dissipation, which reduces  $\theta_{JA}$ . In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the  $\theta_{JA}$ .

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. NIC = NOT INTERNALLY CONNECTED.
2. THE EXPOSED PADDLE IS THE ONLY GROUND CONNECTION. IT MUST BE SOLDERED TO THE ANALOG GROUND OF THE CUSTOMER'S PCB TO ENSURE PROPER FUNCTIONALITY AND MAXIMIZE HEAT DISSIPATION, NOISE, AND MECHANICAL STRENGTH BENEFITS.

08540-003

Figure 3. Pin Configuration

Table 8. Pin Function Description

| Pin No.           | Mnemonic              | Description  |
|-------------------|-----------------------|--|
| 0 (EPAD)          | GND                   | Exposed Paddle. The exposed paddle is the only ground connection. It must be soldered to the analog ground of the customer's PCB to ensure proper functionality and maximize heat dissipation, noise, and mechanical strength benefits.  |
| 1, 2              | CLK+, CLK-            | Differential Encode Clock. PECL, LVDS, or 1.8 V CMOS inputs.   |
| 3, 24, 29, 32     | AVDD                  | 1.8 V Supply Pin for ADC Core Domain.  |
| 4                 | CSB                   | SPI Chip Select. Active low enable. 30 k $\Omega$ internal pull-up.  |
| 5                 | SCLK/DFS              | SPI Clock Input in SPI Mode (SCLK). 30 k $\Omega$ internal pull-down.<br>Data Format Select in Non-SPI Mode (DFS). Static control of data output format. 30 k $\Omega$ internal pull-down. DFS high = twos complement output; DFS low = offset binary output.  |
| 6                 | SDIO/PDWN             | SPI Data Input/Output (SDIO). Bidirectional SPI data I/O in SPI mode. 30 k $\Omega$ internal pull-down.<br>Non-SPI Mode Power-Down (PDWN). Static control of power-down with 30 k $\Omega$ internal pull-down. See Table 14 for details.   |
| 7, 8              | NIC                   | Not Internally Connected.  |
| 9 to 12, 14 to 21 | D0 (LSB) to D11 (MSB) | ADC Digital Outputs.   |
| 13                | DRVDD                 | 1.8 V to 3.3 V Supply Pin for Output Driver Domain.  |
| 22                | DCO                   | Data Clock Digital Output.   |
| 23                | MODE/OR               | Chip Mode Select Input or Out-of-Range (OR) Digital Output in SPI Mode.<br>Default = out-of-range (OR) digital output (SPI Register 0x2A[0] = 1).<br>Option = chip mode select input (SPI Register 0x2A[0] = 0).<br>Chip power down (SPI Register 0x08[7:5] = 100b).<br>Chip standby (SPI Register 0x08[7:5] = 101b).<br>Normal operation, output disabled (SPI Register 0x08[7:5] = 110b).<br>Normal operation, output enabled (SPI Register 0x08[7:5] = 111b).<br>Out-of-Range (OR) digital output only in non-SPI mode. |
| 25                | VREF                  | 1.0 V Voltage Reference Input/Output. See Table 10.  |
| 26                | SENSE                 | Reference Mode Selection. See Table 10.  |
| 27                | VCM                   | Analog Output Voltage at Mid AVDD Supply. Sets common mode of the analog inputs.   |
| 28                | RBIAS                 | Sets Analog Current Bias. Connect to 10 k $\Omega$ (1% tolerance) resistor to ground.  |
| 30, 31            | VIN-, VIN+            | ADC Analog Inputs.   |

# TYPICAL PERFORMANCE CHARACTERISTICS

## AD9629-80

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

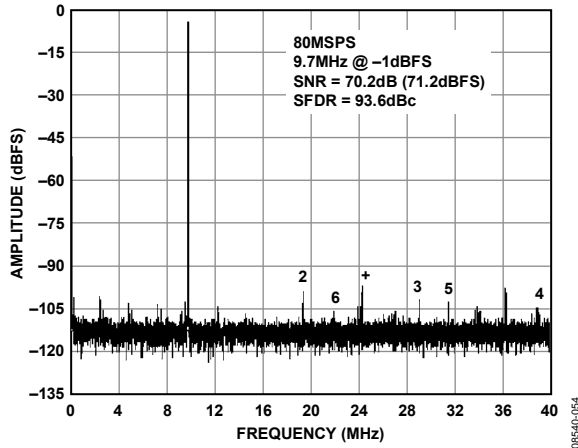


Figure 4. AD9629-80 Single-Tone FFT with  $f_{IN} = 9.7$  MHz

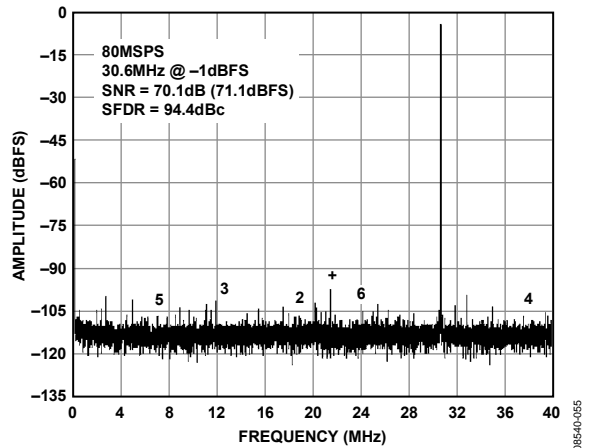


Figure 7. AD9629-80 Single-Tone FFT with  $f_{IN} = 30.6$  MHz

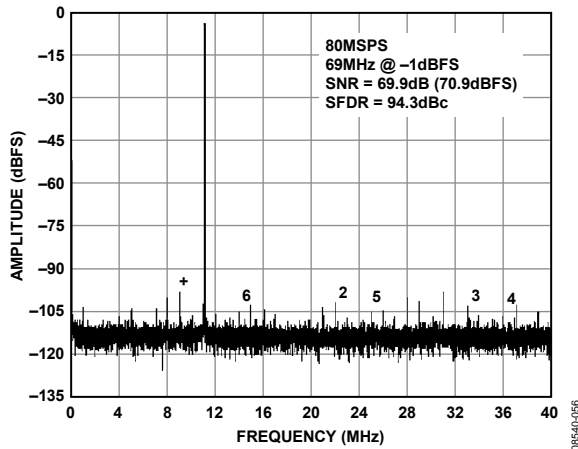


Figure 5. AD9629-80 Single-Tone FFT with  $f_{IN} = 69$  MHz

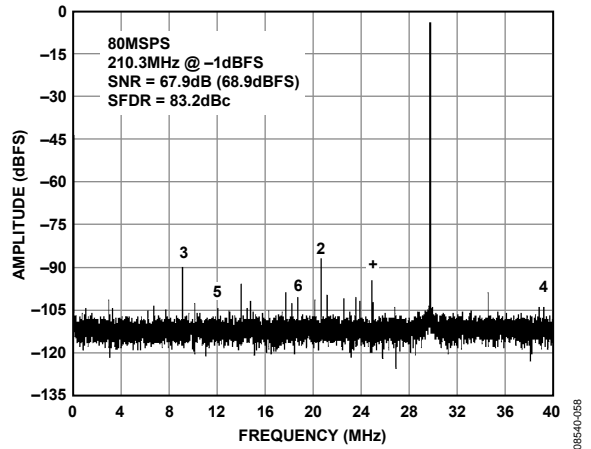


Figure 8. AD9629-80 Single-Tone FFT with  $f_{IN} = 210.3$  MHz

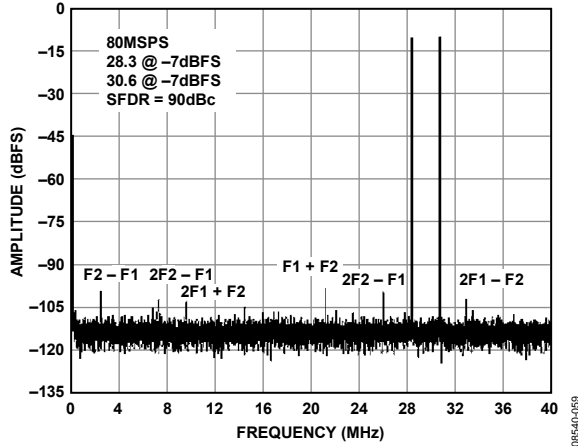


Figure 6. AD9629-80 Two-Tone FFT with  $f_{IN1} = 28.3$  MHz and  $f_{IN2} = 30.6$  MHz

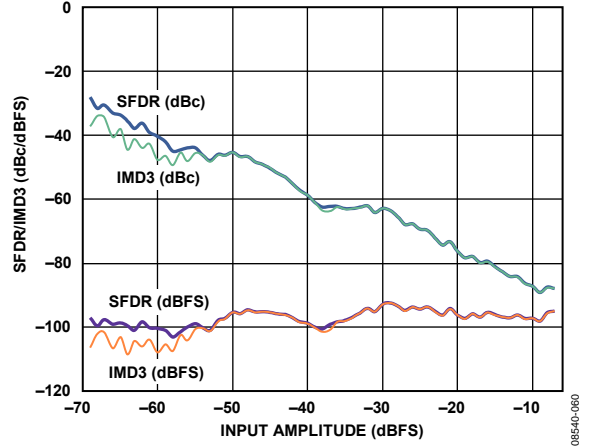


Figure 9. Two-Tone SFDR/IMD3 vs. Input Amplitude (AIN) with  $f_{IN1} = 30.5$  MHz and  $f_{IN2} = 32.5$  MHz

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

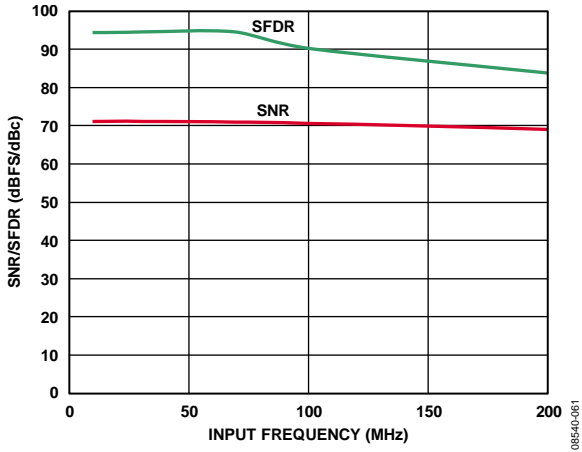


Figure 10. AD9629-80 SNR/SFDR vs. Input Frequency (AIN) with 2 Vp-p Full Scale

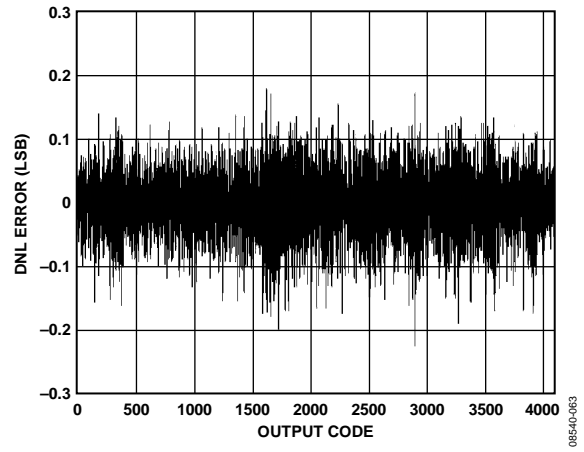


Figure 13. DNL Error with  $f_{IN} = 9.7$  MHz

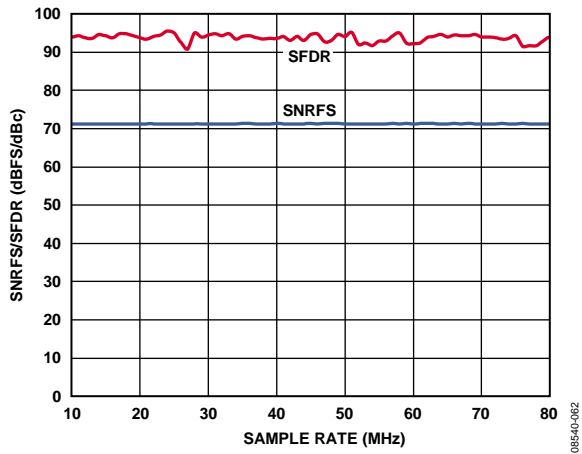


Figure 11. AD9629-80 SNR/SFDR vs. Sample Rate with AIN = 9.7 MHz

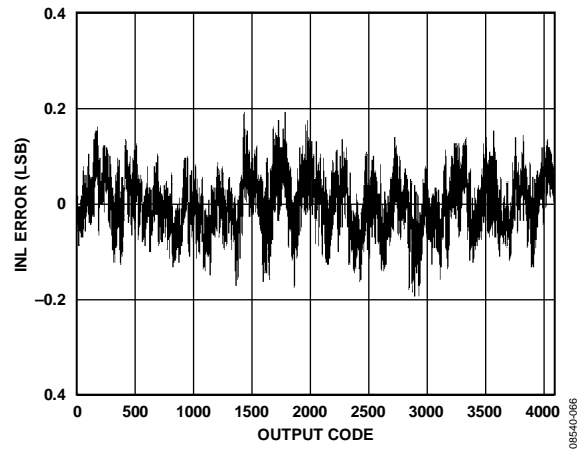


Figure 14. INL with  $f_{IN} = 9.7$  MHz

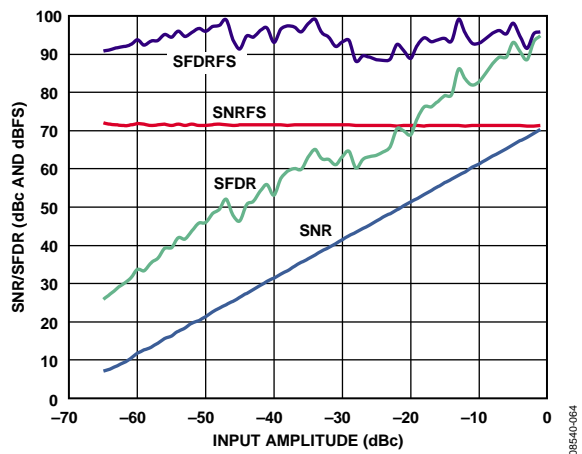


Figure 12. AD9629-80 SNR/SFDR vs. Input Amplitude (AIN) with  $f_{IN} = 9.7$  MHz

**AD9629-65**

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

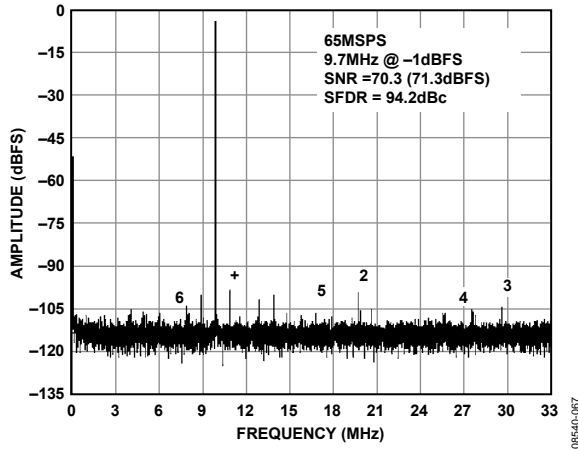


Figure 15. AD9629-65 Single-Tone FFT with  $f_{IN} = 9.7$  MHz

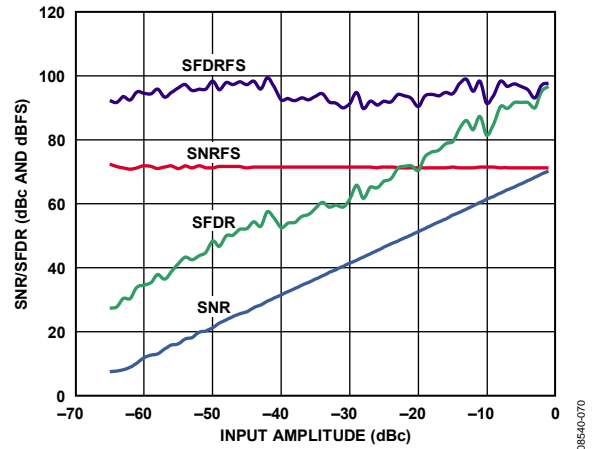


Figure 18. AD9629-65 SNR/SFDR vs. Input Amplitude (AIN) with  $f_{IN} = 9.7$  MHz

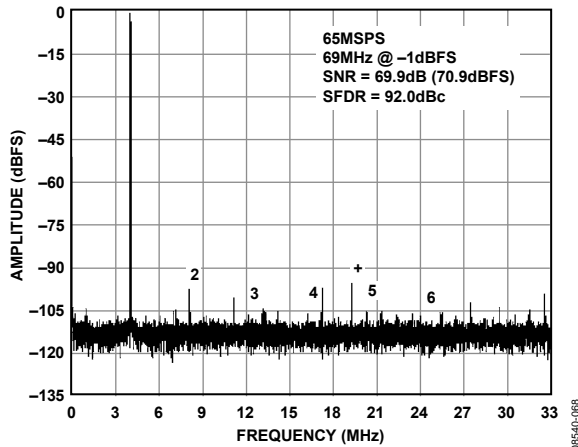


Figure 16. AD9629-65 Single-Tone FFT with  $f_{IN} = 69$  MHz

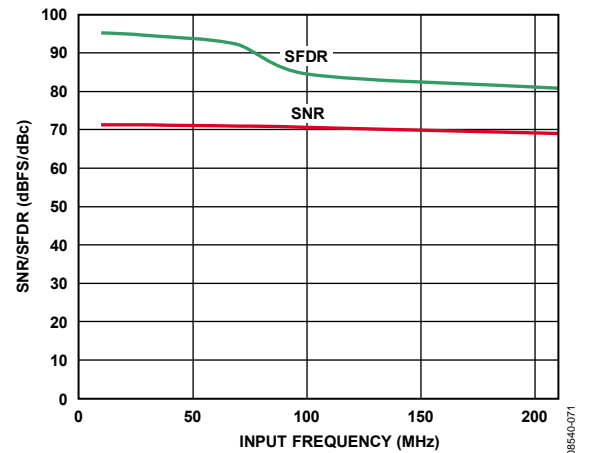


Figure 19. AD9629-65 SNR/SFDR vs. Input Frequency (AIN) with 2 V p-p Full Scale

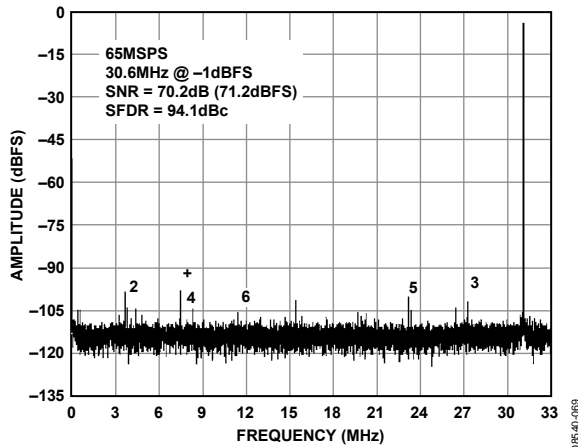


Figure 17. AD9629-65 Single-Tone FFT with  $f_{IN} = 30.6$  MHz

AD9629-40

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

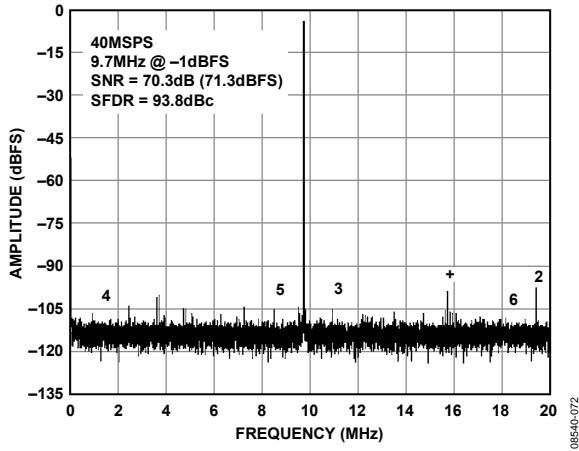


Figure 20. AD9629-40 Single-Tone FFT with  $f_{IN} = 9.7$  MHz

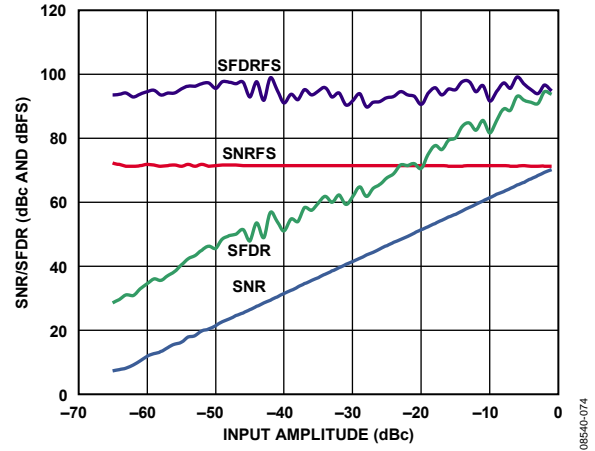


Figure 22. AD9629-40 SNR/SFDR vs. Input Amplitude (AIN) with  $f_{IN} = 9.7$  MHz

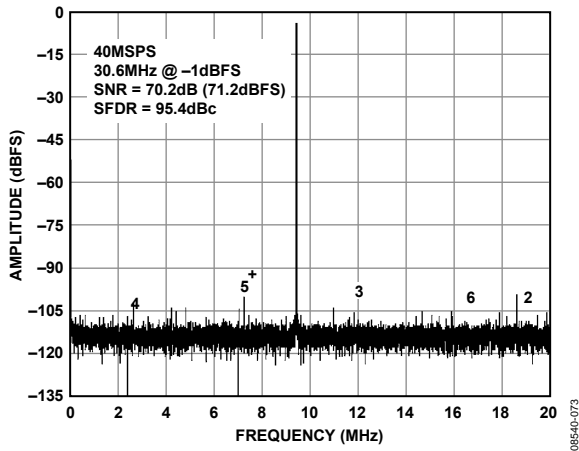


Figure 21. AD9629-40 Single-Tone FFT with  $f_{IN} = 30.6$  MHz

**AD9629-20**

AVDD = 1.8 V; DRVDD = 1.8 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference; AIN = -1.0 dBFS, 50% duty cycle clock, unless otherwise noted.

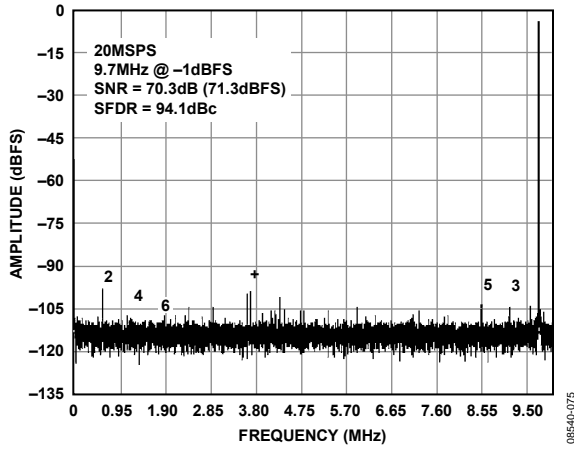


Figure 23. AD9629-20 Single-Tone FFT with  $f_{IN} = 9.7$  MHz

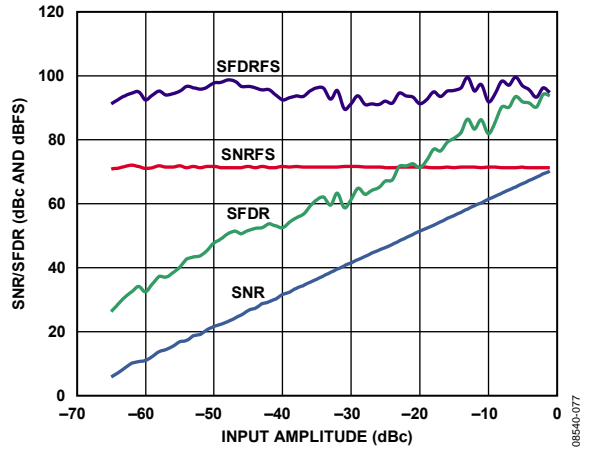


Figure 25. AD9629-20 SNR/SFDR vs. Input Amplitude (AIN) with  $f_{IN} = 9.7$  MHz

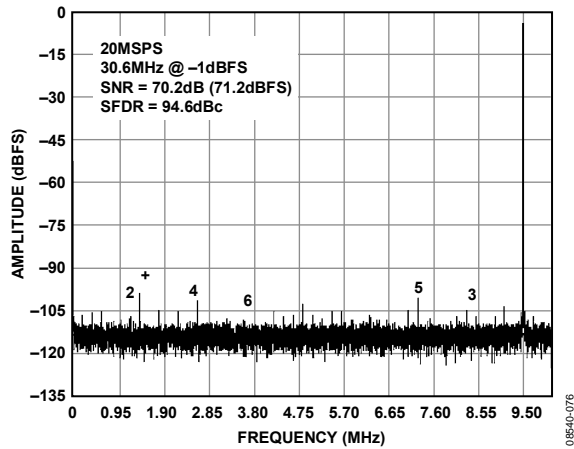


Figure 24. AD9629-20 Single-Tone FFT with  $f_{IN} = 30.6$  MHz

# EQUIVALENT CIRCUITS

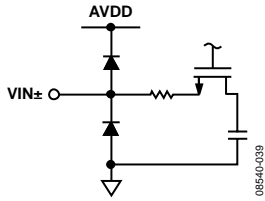


Figure 26. Equivalent Analog Input Circuit

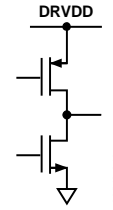


Figure 30. Equivalent D0 to D11 and OR Digital Output Circuit

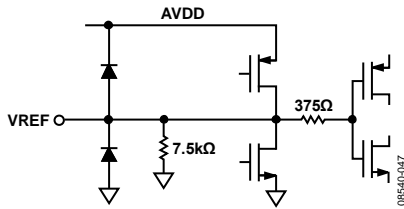


Figure 27. Equivalent VREF Circuit

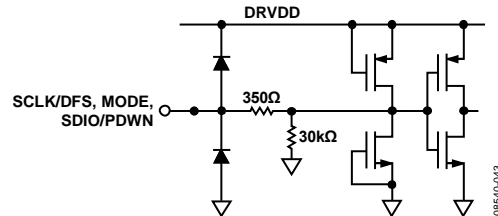


Figure 31. Equivalent SCLK/DFS, MODE, and SDIO/PDWN Input Circuit

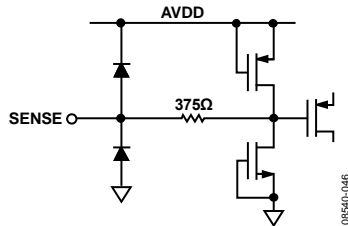


Figure 28. Equivalent SENSE Circuit

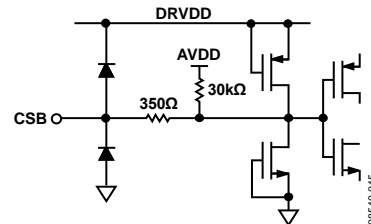


Figure 32. Equivalent CSB Input Circuit

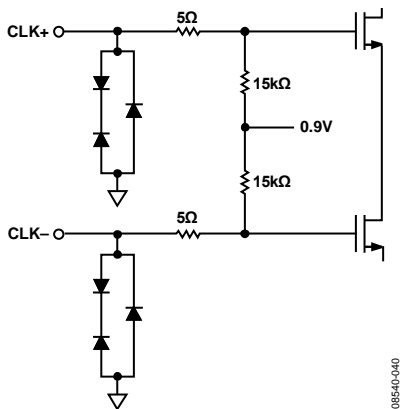


Figure 29. Equivalent Clock Input Circuit

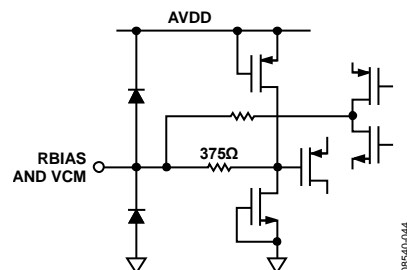


Figure 33. Equivalent RBIAS and VCM Circuit



## THEORY OF OPERATION

The AD9629 architecture consists of a multistage, pipelined ADC. Each stage provides sufficient overlap to correct for flash errors in the preceding stage. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate with a new input sample while the remaining stages operate with preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched-capacitor DAC and an interstage residue amplifier (for example, a multiplying digital-to-analog converter (MDAC)). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage consists of a flash ADC.

The output staging block aligns the data, corrects errors, and passes the data to the CMOS output buffers. The output buffers are powered from a separate (DRVDD) supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

### ANALOG INPUT CONSIDERATIONS

The analog input to the AD9629 is a differential switched-capacitor circuit designed for processing differential input signals. This circuit can support a wide common-mode range while maintaining excellent performance. By using an input common-mode voltage of midsupply, users can minimize signal-dependent errors and achieve optimum performance.

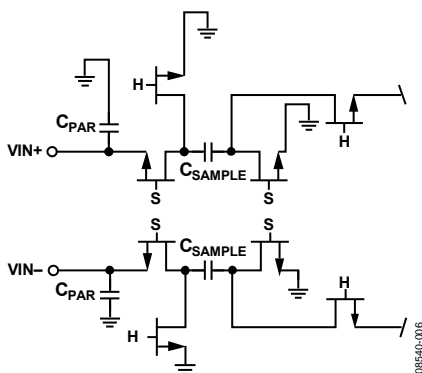


Figure 34. Switched-Capacitor Input Circuit

The clock signal alternately switches the input circuit between sample-and-hold mode (see Figure 34). When the input circuit is switched to sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current injected from the output stage of the driving source. In addition, low Q inductors or ferrite beads can be placed on each leg of the input to reduce high differential capacitance at the analog inputs and, therefore, achieve the maximum bandwidth of the ADC. Such use of low Q inductors or ferrite beads is required when driving the converter front end at

high IF frequencies. Either a shunt capacitor or two single-ended capacitors can be placed on the inputs to provide a matching passive network. This ultimately creates a low-pass filter at the input to limit unwanted broadband noise. See the AN-742 Application Note, the AN-827 Application Note, and the *Analog Dialogue* article “Transformer-Coupled Front-End for Wideband A/D Converters” (Volume 39, April 2005) for more information. In general, the precise values depend on the application.

### Input Common Mode

The analog inputs of the AD9629 are not internally dc-biased. Therefore, in ac-coupled applications, the user must provide a dc bias externally. Setting the device so that  $V_{CM} = AV_{DD}/2$  is recommended for optimum performance, but the device can function over a wider range with reasonable performance, as shown in Figure 35 and Figure 36.

An on-board, common-mode voltage reference is included in the design and is available from the VCM pin. The VCM pin must be decoupled to ground by a 0.1  $\mu\text{F}$  capacitor, as described in the Applications Information section.

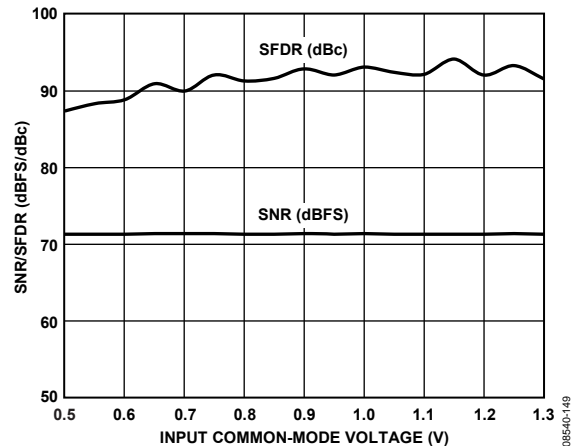


Figure 35. SNR/SFDR vs. Input Common-Mode Voltage,  $f_{IN} = 32.1 \text{ MHz}$ ,  $f_s = 80 \text{ MSPS}$

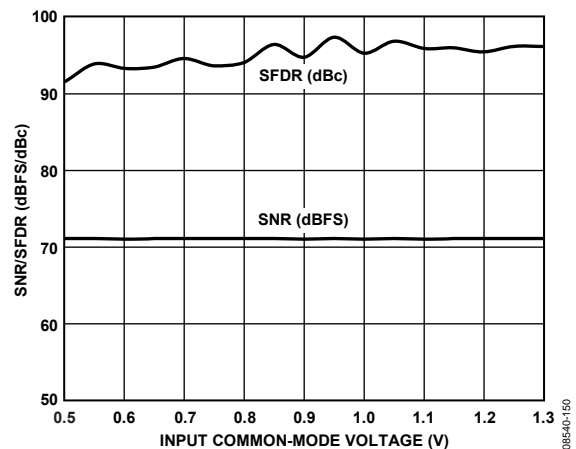


Figure 36. SNR/SFDR vs. Input Common-Mode Voltage,  $f_{IN} = 10.3 \text{ MHz}$ ,  $f_s = 20 \text{ MSPS}$

**Differential Input Configurations**

Optimum performance is achieved while driving the AD9629 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, and ADA4938-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4938-2 is easily set with the VCM pin of the AD9629 (see Figure 37), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

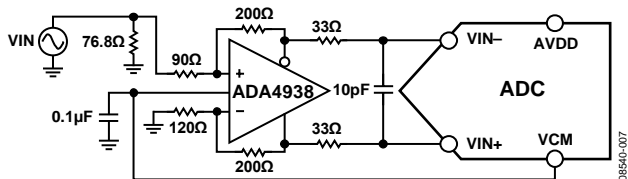


Figure 37. Differential Input Configuration Using the ADA4938-2

For baseband applications below ~10 MHz where SNR is a key parameter, differential transformer-coupling is the recommended input configuration. An example is shown in Figure 38. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

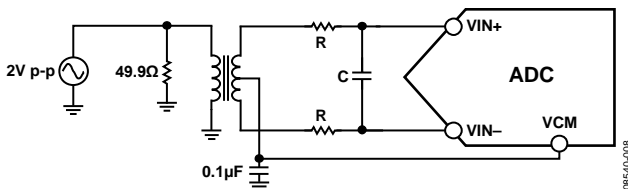


Figure 38. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz (MHz). Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9629. For applications above

~10 MHz where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 40).

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use the AD8352 differential driver. An example is shown in Figure 41. See the AD8352 data sheet for more information.

In any configuration, the value of Shunt Capacitor C is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 9 displays the suggested values to set the RC network. However, these values are dependent on the input signal and should be used only as a starting guide.

Table 9. Example RC Network

| Frequency Range (MHz) | R Series (Ω Each) | C Differential (pF) |
|-----------------------|-------------------|---------------------|
| 0 to 70               | 33                | 22                  |
| 70 to 200             | 125               | Open                |

**Single-Ended Input Configuration**

A single-ended input can provide adequate performance in cost-sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the source impedances on each input are matched, there should be little effect on SNR performance. Figure 39 shows a typical single-ended input configuration.

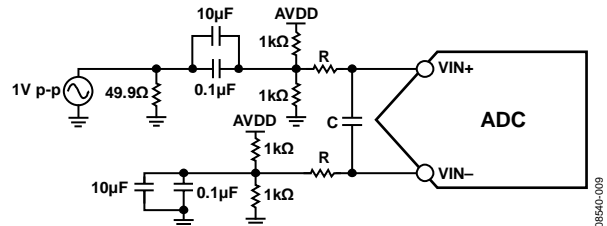


Figure 39. Single-Ended Input Configuration

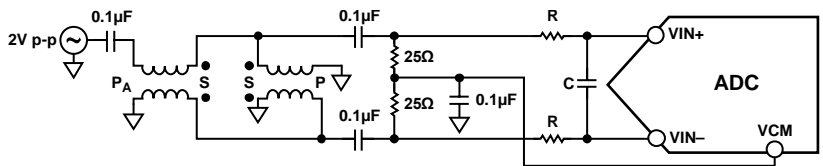


Figure 40. Differential Double Balun Input Configuration

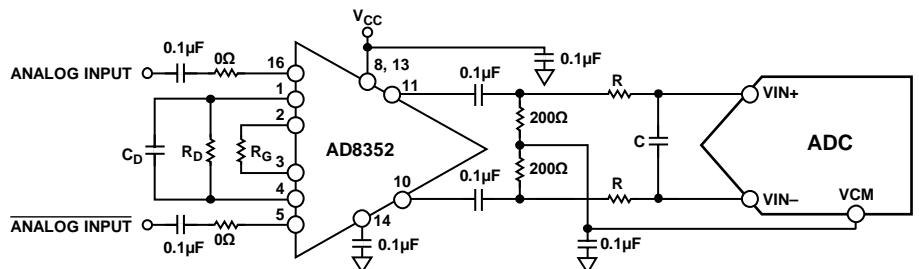


Figure 41. Differential Input Configuration Using the AD8352

**VOLTAGE REFERENCE**

A stable and accurate 1.0 V voltage reference is built into the AD9629. The VREF can be configured using either the internal 1.0 V reference or an externally applied 1.0 V reference voltage. The various reference modes are summarized in the sections that follow. The Reference Decoupling section describes the best practices PCB layout of the reference.

**Internal Reference Connection**

A comparator within the AD9629 detects the potential at the SENSE pin and configures the reference into two possible modes, which are summarized in Table 10. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 42), setting VREF to 1.0 V.

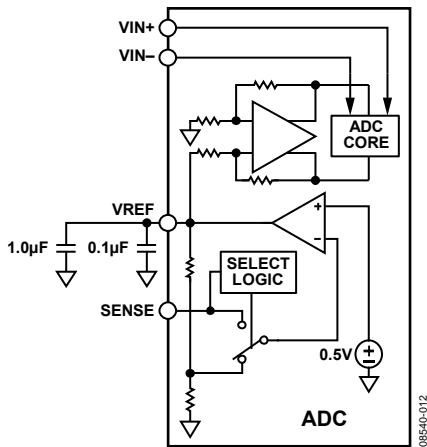


Figure 42. Internal Reference Configuration

If the internal reference of the AD9629 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 43 shows how the internal reference voltage is affected by loading.

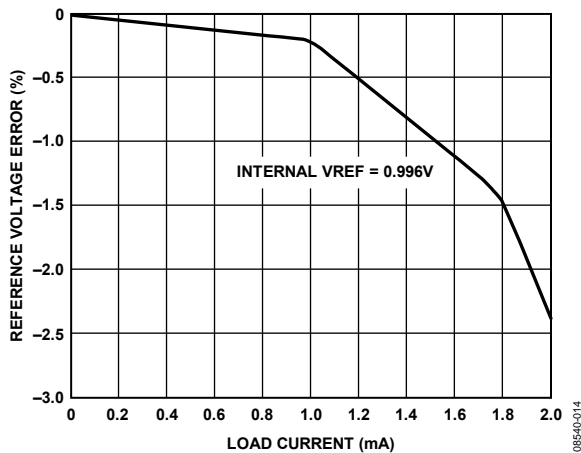


Figure 43. VREF Accuracy vs. Load Current

**External Reference Operation**

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 44 shows the typical drift characteristics of the internal reference in 1.0 V mode.

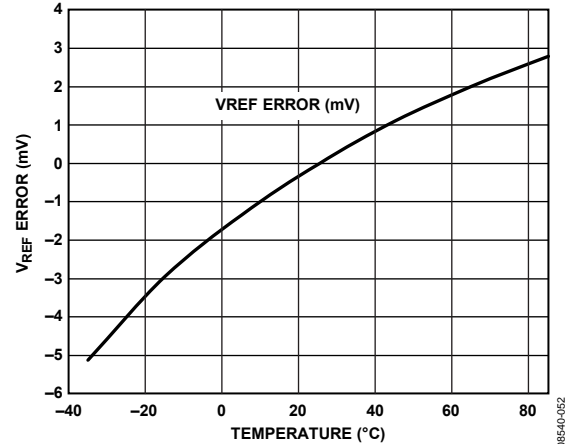


Figure 44. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7.5 kΩ load (see Figure 27). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1.0 V.

Table 10. Reference Configuration Summary

| Selected Mode            | SENSE Voltage (V) | Resulting VREF (V)               | Resulting Differential Span (V p-p) |
|--------------------------|-------------------|----------------------------------|-------------------------------------|
| Fixed Internal Reference | AGND to 0.2       | 1.0 internal                     | 2.0                                 |
| Fixed External Reference | AVDD              | 1.0 applied to external VREF pin | 2.0                                 |

## CLOCK INPUT CONSIDERATIONS

For optimum performance, clock the **AD9629** sample clock inputs, CLK+ and CLK-, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK- pins via a transformer or capacitors. These pins are biased internally (see Figure 45) and require no external bias.

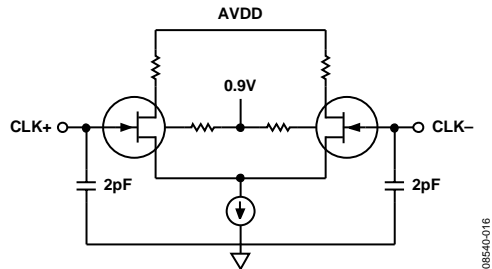


Figure 45. Equivalent Clock Input Circuit

### Clock Input Options

The **AD9629** has a very flexible clock input structure. The clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, clock source jitter is of great concern, as described in the Jitter Considerations section.

Figure 46 and Figure 47 show two preferred methods for clocking the **AD9629**. The CLK inputs support up to 4× the rated sample rate when using the internal clock divider feature. A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

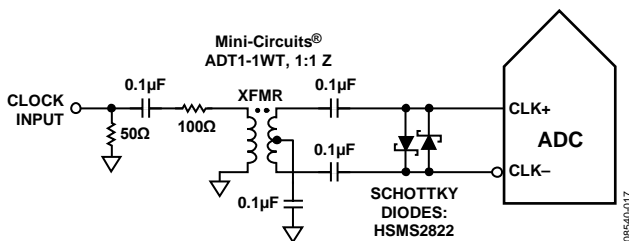


Figure 46. Transformer-Coupled Differential Clock (3 MHz to 200 MHz)

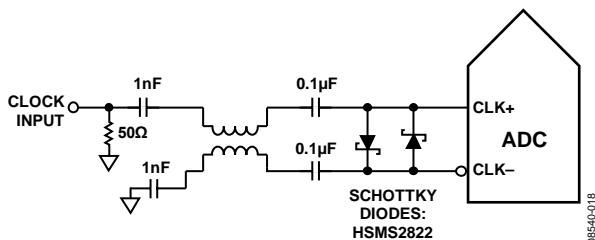


Figure 47. Balun-Coupled Differential Clock (Up to 4× Rated Sample Rate)

The RF balun configuration is recommended for clock frequencies between 80 MHz and 320 MHz, and the RF transformer is recommended for clock frequencies from 3 MHz to 200 MHz. The back-to-back Schottky diodes across the transformer/balun secondary limit clock excursions into the **AD9629** to ~0.8 V p-p differential.

This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the **AD9629** while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 48. The **AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-4/AD9517-4** clock drivers offer excellent jitter performance.

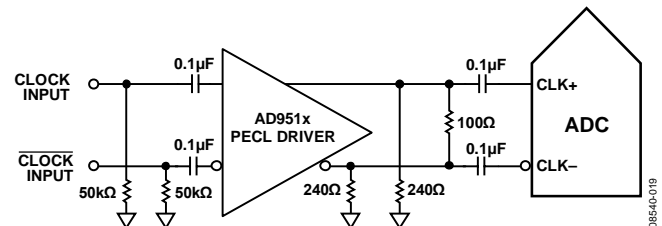


Figure 48. Differential PECL Sample Clock (Up to 4× Rated Sample Rate)

A third option is to ac couple a differential LVDS signal to the sample clock input pins, as shown in Figure 49. The **AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-4/AD9517-4** clock drivers offer excellent jitter performance.

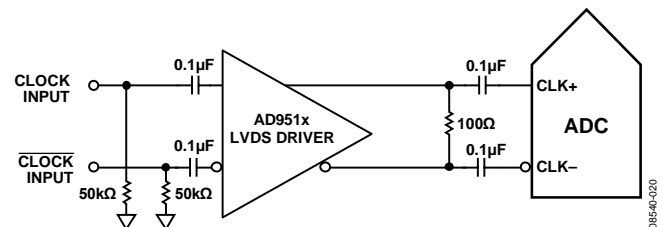
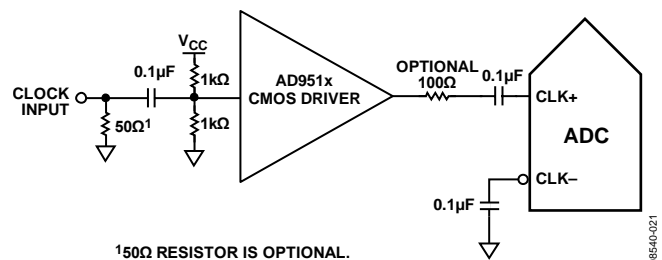


Figure 49. Differential LVDS Sample Clock (Up to 4× Rated Sample Rate)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLK+ pin directly from a CMOS gate, and bypass the CLK- pin to ground with a 0.1 µF capacitor (see Figure 50).



150Ω RESISTOR IS OPTIONAL.

Figure 50. Single-Ended 1.8 V CMOS Input Clock (Up to 200 MHz)

### Input Clock Divider

The **AD9629** contains an input clock divider with the ability to divide the input clock by integer values of 1, 2, or 4.

**Clock Duty Cycle**

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a 50% duty cycle clock with ±5% tolerance is required to maintain optimum dynamic performance as shown in Figure 51.

Jitter on the rising edge of the clock input can also impact dynamic performance and should be minimized as discussed in the Jitter Considerations section.

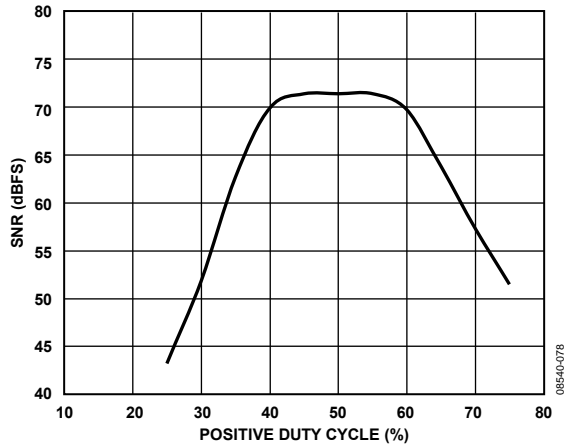


Figure 51. SNR vs. Clock Duty Cycle

**Jitter Considerations**

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR from the low frequency SNR (SNR<sub>LF</sub>) at a given input frequency (f<sub>INPUT</sub>) due to jitter (t<sub>JRMS</sub>) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{INPUT} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the previous equation, the rms aperture jitter represents the clock input jitter specification. IF undersampling applications are particularly sensitive to jitter, as illustrated in Figure 52.

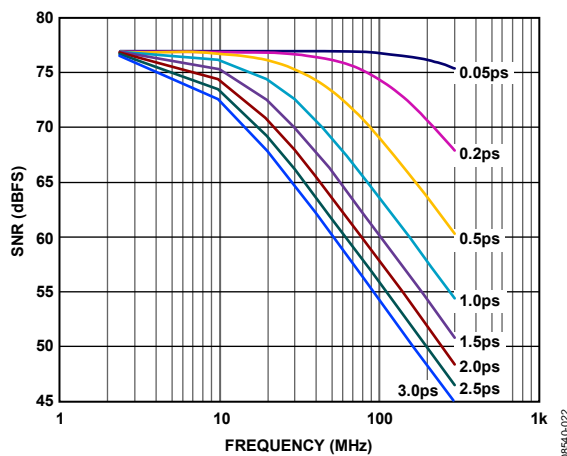


Figure 52. SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases in which aperture jitter may affect the dynamic range of the AD9629. To avoid modulating the clock signal with digital noise, keep power supplies for clock drivers separate from the ADC output driver supplies. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), it should be retimed by the original clock at the last step.

For more information, see the AN-501 Application Note and the AN-756 Application Note available on [www.analog.com](http://www.analog.com).

**POWER DISSIPATION AND STANDBY MODE**

As shown in Figure 53, the analog core power dissipated by the AD9629 is proportional to its sample rate. The digital power dissipation of the CMOS outputs are determined primarily by the strength of the digital drivers and the load on each output bit.

The maximum DRVDD current (IDRVDD) can be calculated as

$$IDRVDD = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where N is the number of output bits (13, in the case of the AD9629).

This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency of f<sub>CLK</sub>/2. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the sample rate and the characteristics of the analog input signal.

Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 53 was taken using the same operating conditions as those used for the Typical Performance Characteristics, with a 5 pF load on each output driver.

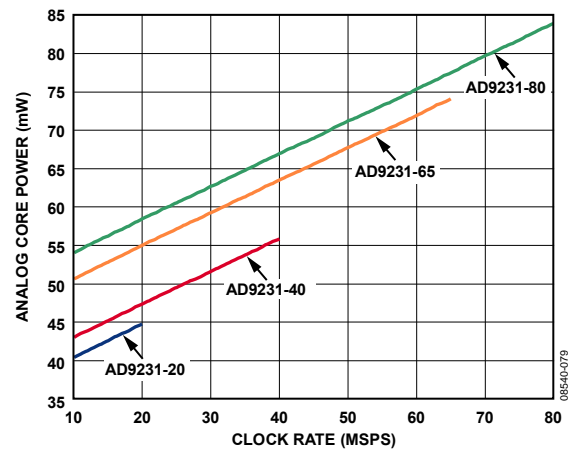


Figure 53. Analog Core Power vs. Clock Rate

In SPI mode, the AD9629 can be placed in power-down mode directly via the SPI port, or by using the programmable external MODE pin. In non-SPI mode, power-down is achieved by asserting the PDWN pin high. In this state, the ADC typically dissipates 500  $\mu$ W. During power-down, the output drivers are placed in a high impedance state. Asserting PDWN low (or the MODE pin in SPI mode) returns the AD9629 to its normal operating mode. Note that PDWN is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map section for more details.

## DIGITAL OUTPUTS

The AD9629 output drivers can be configured to interface with 1.8 V to 3.3 V CMOS logic families. Output data can also be multiplexed onto a single output bus to reduce the total number of traces required.

The CMOS output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies and may affect converter performance.

Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

The output data format can be selected to be either offset binary or twos complement by setting the SCLK/DFS pin when operating in the external pin mode (see Table 11).

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

**Table 11. SCLK/DFS and SDIO/PDWN Mode Selection (External Pin Mode)**

| Voltage at Pin | SCLK/DFS                | SDIO/PDWN                  |
|----------------|-------------------------|----------------------------|
| AGND           | Offset binary (default) | Normal operation (default) |
| DRVDD          | Twos complement         | Outputs disabled           |

## Digital Output Enable Function (OEB)

When using the SPI interface, the data outputs and DCO can be independently three-stated by using the programmable external MODE pin. The MODE pin (OEB) function is enabled via Bits[6:5] of Register 0x08.

If the MODE pin is configured to operate in traditional OEB mode and the OEB pin is low, the output data drivers and DCOs are enabled. If the OEB pin is high, the output data drivers and DCOs are placed in a high impedance state. This OEB function is not intended for rapid access to the data bus. Note that OEB is referenced to the digital output driver supply (DRVDD) and should not exceed that supply voltage.

## TIMING

The AD9629 provides latched data with a pipeline delay of 9 clock cycles. Data outputs are available one propagation delay ( $t_{PD}$ ) after the rising edge of the clock signal.

Minimize the length of the output data lines and loads placed on them to reduce transients within the AD9629. These transients can degrade converter dynamic performance.

The lowest typical conversion rate of the AD9629 is 3 MSPS. At clock rates below 3 MSPS, dynamic performance can degrade.

## Data Clock Output (DCO)

The AD9629 provides a data clock output (DCO) signal intended for capturing the data in an external register. The CMOS data outputs are valid on the rising edge of DCO, unless the DCO clock polarity has been changed via the SPI. See Figure 2 for a graphical timing description.

**Table 12. Output Data Format**

| Input (V)   | Condition (V)     | Offset Binary Output Mode | Twos Complement Mode | OR |
|-------------|-------------------|---------------------------|----------------------|----|
| VIN+ – VIN– | < –VREF – 0.5 LSB | 0000 0000 0000            | 1000 0000 0000       | 1  |
| VIN+ – VIN– | = –VREF           | 0000 0000 0000            | 1000 0000 0000       | 0  |
| VIN+ – VIN– | = 0               | 1000 0000 0000            | 0000 0000 0000       | 0  |
| VIN+ – VIN– | = +VREF – 1.0 LSB | 1111 1111 1111            | 0111 1111 1111       | 0  |
| VIN+ – VIN– | > +VREF – 0.5 LSB | 1111 1111 1111            | 0111 1111 1111       | 1  |

## BUILT-IN SELF-TEST (BIST) AND OUTPUT TEST

The [AD9629](#) includes a built-in self-test feature designed to enable verification of the integrity of each channel as well as to facilitate board level debugging. A built-in self-test (BIST) feature that verifies the integrity of the digital datapath of the [AD9629](#) is included. Various output test options are also provided to place predictable values on the outputs of the [AD9629](#).

### BUILT-IN SELF-TEST (BIST)

The BIST is a thorough test of the digital portion of the selected [AD9629](#) signal path. Perform the BIST test after a reset to ensure the part is in a known state. During BIST, data from an internal pseudorandom noise (PN) source is driven through the digital datapath of both channels, starting at the ADC block output. At the datapath output, CRC logic calculates a signature from the data. The BIST sequence runs for 512 cycles and then stops. Once completed, the BIST compares the signature results with a predetermined value. If the signatures match, the BIST sets Bit 0 of Register 0x24, signifying the test passed. If the BIST test failed, Bit 0 of Register 0x24 is cleared. The outputs are connected during this test, so the PN sequence can be observed as it runs. Writing 0x05 to Register 0x0E runs the BIST. This enables the Bit 0 (BIST enable) of Register 0x0E and resets the PN sequence

generator, Bit 2 (BIST INIT) of Register 0x0E. At the completion of the BIST, Bit 0 of Register 0x24 is automatically cleared. The PN sequence can be continued from its last value by writing a 0 in Bit 2 of Register 0x0E. However, if the PN sequence is not reset, the signature calculation does not equal the predetermined value at the end of the test. At that point, the user needs to rely on verifying the output data.

### OUTPUT TEST MODES

The output test options are described in Table 16 at Address 0x0D. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital back-end blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting, and some are not. The PN generators from the PN sequence tests can be reset by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock. For more information, see the [AN-877](#) Application Note, *Interfacing to High Speed ADCs via SPI*.

## SERIAL PORT INTERFACE (SPI)

The AD9629 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

### CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK, the SDIO, and the CSB (see Table 13). The SCLK (a serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO (serial data input/output) is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) is an active-low control that enables or disables the read and write cycles.

**Table 13. Serial Port Interface Pins**

| Pin  | Function  |
|------|---|
| SCLK | Serial clock. The serial shift clock input, which is used to synchronize serial interface reads and writes.   |
| SDIO | Serial data input/output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame. |
| CSB  | Chip select bar. An active-low control that gates the read and write cycles.  |

The falling edge of CSB, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 54 and Table 5.

Other modes involving the CSB are available. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB can stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits as shown in Figure 54.

All data is composed of 8-bit words. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB-first mode or in LSB-first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

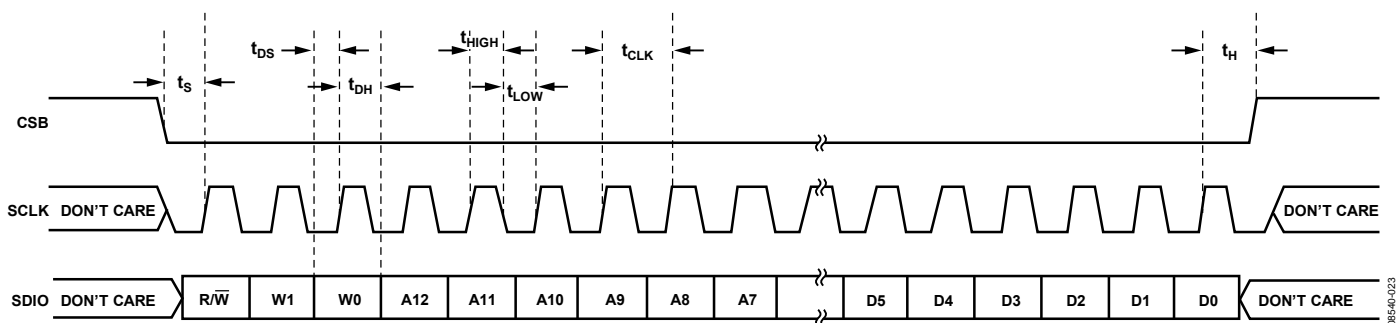


Figure 54. Serial Port Interface Timing Diagram



## HARDWARE INTERFACE

The pins described in Table 13 constitute the physical interface between the programming device of the user and the serial port of the AD9629. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9629 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SDIO/PDWN and SCLK/DFS serve a dual function when the SPI interface is not being used. When the pins are strapped to DRVDD or ground during device power-on, they are associated with a specific function. The Digital Outputs section describes the strappable functions supported on the AD9629.

## CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO/PDWN pin, the SCLK/DFS pin serve as standalone CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the power-down and output data format feature control. In this mode, connect the CSB chip select to DRVDD, which disables the serial port interface.

**Table 14. Mode Selection**

| Pin       | External Voltage | Configuration             |
|-----------|------------------|---------------------------|
| SDIO/PDWN | DRVDD            | Chip power-down mode      |
|           | AGND (default)   | Normal operation(default) |
| SCLK/DFS  | DRVDD            | Twos complement enabled   |
|           | AGND (default)   | Offset binary enabled     |

## SPI ACCESSIBLE FEATURES

Table 15 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9629 part-specific features are described in detail in Table 16.

**Table 15. Features Accessible Using the SPI**

| Feature       | Description   |
|---------------|---|
| Modes         | Allows the user to set either power-down mode or standby mode       |
| Offset Adjust | Allows the user to digitally adjust the converter offset            |
| Test Mode     | Allows the user to set test modes to have known data on output bits |
| Output Mode   | Allows the user to set up outputs                                   |
| Output Phase  | Allows the user to set the output clock polarity                    |
| Output Delay  | Allows the user to vary the DCO delay                               |

## MEMORY MAP

### READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table (see Table 16) contains eight bit locations. The memory map is roughly divided into four sections: the chip configuration registers (Address 0x00 to Address 0x02); the device transfer register (Address 0xFF); the program registers, including setup, control, and test (Address 0x08 to Address 0x2A); and the [AD9629](#) specific customer SPI control register (Address 0x101).

Table 16 documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x2A, the OR/MODE select register, has a hexadecimal default value of 0x01. This means that in Address 0x2A, Bits[7:1] = 0, and Bit 0 = 1. This setting is the default OR/MODE setting. The default value results in the programmable external MODE/OR pin (Pin 23) functioning as an out-of-range digital output. For more information on this function and others, see the [AN-877](#) Application Note, *Interfacing to High Speed ADCs via SPI*. This application note details the functions controlled by Register 0x00 to Register 0xFF. The remaining register, Register 0x101, is documented in the Memory Map section that follows Table 16.

### OPEN LOCATIONS

All address and bit locations that are not included in the SPI map are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x2A). If the entire address location is open, it is omitted from the SPI map (for example, Address 0x13) and should not be written.

### DEFAULT VALUES

After the [AD9629](#) is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table (see Table 16).

#### Logic Levels

An explanation of logic level terminology follows:

- “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.”
- “Clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

#### Transfer Register Map

Address 0x08 to Address 0x18 are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and then the bit autoclears.

**MEMORY MAP REGISTER TABLE**

All address and bit locations that are not included in Table 16 are not currently supported for this device.

**Table 16.**

| Addr (Hex)                         | Register Name          | Bit 7 (MSB)  | Bit 6   | Bit 5                   | Bit 4              | Bit 3  | Bit 2   | Bit 1     | Bit 0 (LSB)   | Default Value (Hex) | Comments   |  |
|------------------------------------|------------------------|--|---|-------------------------|--------------------|--|---|-----------|---|---------------------|--|--|
| Chip Configuration Registers       |                        |  |   |                         |                    |  |   |           |   |                     |  |  |
| 0x00                               | SPI port configuration | 0  | LSB first   | Soft reset <sup>1</sup> | 1                  | 1  | Soft reset <sup>1</sup>   | LSB first | 0   | 0x18                | The nibbles are mirrored so that LSB or MSB first mode registers correctly, regardless of shift mode |  |
| 0x01                               | Chip ID                | 8-bit chip ID, Bits[7:0]<br>AD9629 = 0x70  |   |                         |                    |  |   |           |   | Read only           | Unique chip ID used to differentiate devices; read only  |  |
| 0x02                               | Chip grade             | Open   | Speed grade ID, Bits[6:4] (identify device variants of chip ID)<br>20 MSPS = 000<br>40 MSPS = 001<br>65 MSPS = 010<br>80 MSPS = 011                 |                         |                    |  | Open  |           |   | Read only           | Unique speed grade ID used to differentiate devices; Read only                                       |  |
| Device Index and Transfer Register |                        |  |   |                         |                    |  |   |           |   |                     |  |  |
| 0xFF                               | Transfer               | Open   | Open  | Open                    | Open               | Open   | Open  | Open      | Transfer  | 0x00                | Synchronously transfers data from the master shift register to the slave                             |  |
| Program Registers                  |                        |  |   |                         |                    |  |   |           |   |                     |  |  |
| 0x08                               | Modes                  | External Pin 23 mode input enable  | External Pin 23 function when high<br>00 = full power down<br>01 = standby<br>10 = normal mode: output disabled<br>11 = normal mode: output enabled |                         |                    | Open   | Open  | Open      | 00 = chip run<br>01 = full power down<br>10 = standby<br>11 = chip wide digital reset |                     | 0x00   | Determines various generic modes of chip operation                           |
| 0x0B                               | Clock divide           | Open   |   |                         |                    |  | Clock divider, Bits[2:0]<br>Clock divide ratio<br>000 = divide-by-1<br>001 = divide-by-2<br>011 = divide-by-4 |           |   | 0x00                | The divide ratio is the value plus 1   |  |
| 0x0D                               | Test mode              | User test mode<br>00 = single<br>01 = alternate<br>10 = single once<br>11 = alternate once                       |   | Reset PN long gen       | Reset PN short gen | Output test mode, Bits[3:0] (local)<br>0000 = off (default)<br>0001 = midscale short<br>0010 = positive FS<br>0011 = negative FS<br>0100 = alternating checkerboard<br>0101 = PN 23 sequence<br>0110 = PN 9 sequence<br>0111 = 1/0 word toggle<br>1000 = user input<br>1001 = one/zero bit toggle<br>1010 = 1× sync<br>1011 = one bit high<br>1100 = mixed bit frequency |   |           |   |                     | 0x00   | When set, the test data is placed on the output pins in place of normal data |
| 0x0E                               | BIST enable            | Open   | Open  | Open                    | Open               | Open   | BIST INIT   | Open      | BIST enable   | 0x00                | When Bit 0 is set, the built-in self-test function is initiated                                      |  |
| 0x10                               | Offset adjust          | 8-bit device offset adjustment [7:0] (local)<br>Offset adjust in LSBs from +127 to -128 (twos complement format) |   |                         |                    |  |   |           |   | 0x00                | Device offset trim   |  |

| Addr (Hex)  | Register Name      | Bit 7 (MSB)   | Bit 6 | Bit 5   | Bit 4          | Bit 3  | Bit 2  | Bit 1  | Bit 0 (LSB)                  | Default Value (Hex) | Comments  |
|---|--------------------|---|-------|---|----------------|--|--|--|------------------------------|---------------------|---|
| 0x14  | Output mode        | 00 = 3.3 V CMOS<br>10 = 1.8 V CMOS  |       | Open  | Output disable | Open   | Output invert  | 00 = offset binary<br>01 = twos complement<br>10 = gray code<br>11 = offset binary                         |                              | 0x00                | Configures the outputs and the format of the data   |
| 0x15  | Output adjust      | 3.3 V DCO drive strength<br>00 = 1 stripe (default)<br>01 = 2 stripes<br>10 = 3 stripes<br>11 = 4 stripes |       | 1.8 V DCO drive strength<br>00 = 1 stripe<br>01 = 2 stripes<br>10 = 3 stripes (default)<br>11 = 4 stripes |                | 3.3 V data drive strength<br>00 = 1 stripe (default)<br>01 = 2 stripes<br>10 = 3 stripes<br>11 = 4 stripes |  | 1.8 V data drive strength<br>00 = 1 stripe<br>01 = 2 stripes<br>10 = 3 stripes (default)<br>11 = 4 stripes |                              | 0x22                | Determines CMOS output drive strength properties  |
| 0x16  | Output phase       | DCO Output polarity<br>0 = normal<br>1 = inverted   | Open  | Open  | Open           | Open   | Input clock phase adjust, Bits[2:0]<br>(Value is number of input clock cycles of phase delay)<br>000 = no delay<br>001 = 1 input clock cycle<br>010 = 2 input clock cycles<br>011 = 3 input clock cycles<br>100 = 4 input clock cycles<br>101 = 5 input clock cycles<br>110 = 6 input clock cycles<br>111 = 7 input clock cycles |  |                              | 0x00                | On devices that utilize global clock divide, determines which phase of the divider output is used to supply the output clock; internal latching is unaffected |
| 0x17  | Output delay       | Enable DCO delay  | Open  | Enable data delay   | Open           |  | DCO/data delay, Bits[2:0]<br>000 = 0.56 ns<br>001 = 1.12 ns<br>010 = 1.68 ns<br>011 = 2.24 ns<br>100 = 2.80 ns<br>101 = 3.36 ns<br>110 = 3.92 ns<br>111 = 4.48 ns  |  |                              | 0x00                | Sets the fine output delay of the output clock, but does not change internal timing   |
| 0x19  | USER_PATT1_LSB     | B7  | B6    | B5  | B4             | B3   | B2   | B1   | B0                           | 0x00                | User-defined pattern, 1 LSB   |
| 0x1A  | USER_PATT1_MSB     | B15   | B14   | B13   | B12            | B11  | B10  | B9   | B8                           | 0x00                | User-defined pattern, 1 MSB   |
| 0x1B  | USER_PATT2_LSB     | B7  | B6    | B5  | B4             | B3   | B2   | B1   | B0                           | 0x00                | User-defined pattern, 2 LSB   |
| 0x1C  | USER_PATT2_MSB     | B15   | B14   | B13   | B12            | B11  | B10  | B9   | B8                           | 0x00                | User-defined pattern, 2 MSB   |
| 0x24  | BIST signature LSB | BIST signature, Bits[7:0]   |       |   |                |  |  |  |                              | 0x00                | Least significant byte of BIST signature, read only   |
| 0x2A  | OR/MODE select     | Open  | Open  | Open  | Open           | Open   | Open   | Open   | 0 = MODE<br>1 = OR (default) | 0x01                | Selects I/O functionality in conjunction w/ Address 0x08 for MODE (input) or OR (output) on external Pin 23   |
| 1.1. <a href="#">AD9629</a> Specific Customer SPI Control |                    |   |       |   |                |  |  |  |                              |                     |   |
| 0x101   | USR2               | 1   | Open  | Open  | Open           | Enable GCLK detect   | Run GCLK   | Open   | Disable SDIO pull-down       | 0x88                | Enables internal oscillator for clock rates of <5 MHz   |

<sup>1</sup> See the Soft Reset section for limitations on the use of soft reset.

**MEMORY MAP REGISTER DESCRIPTIONS**

For additional information about functions controlled in Register 0x00 to Register 0xFF, see the [AN-877](#) Application Note, *Interfacing to High Speed ADCs via SPI*.

**USR2 (Register 0x101)****Bit 3—Enable GCLK Detect**

Normally set high, this bit enables a circuit that detects encode rates below about 5 MSPS. When a low encode rate is detected, an internal oscillator, GCLK, is enabled ensuring the proper operation of several circuits. If set low the detector is disabled.

**Bit 2—Run GCLK**

This bit enables the GCLK oscillator. For some applications with encode rates below 10 MSPS, it may be preferable to set this bit high to supersede the GCLK detector.

**Bit 0—Disable SDIO Pull-Down**

This bit can be set high to disable the internal 30 k $\Omega$  pull-down on the SDIO pin, which can be used to limit the loading when many devices are connected to the SPI bus.

## APPLICATIONS INFORMATION

### DESIGN GUIDELINES

Before starting design and layout of the [AD9629](#) as a system, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements needed for certain pins.

#### **Power and Ground Recommendations**

When connecting power to the [AD9629](#), it is strongly recommended that two separate supplies be used. Use one 1.8 V supply for analog (AVDD); use a separate 1.8 V to 3.3 V supply for the digital output supply (DRVDD). If a common 1.8 V AVDD and DRVDD supply must be used, the AVDD and DRVDD domains must be isolated with a ferrite bead or filter choke and separate decoupling capacitors. Several different decoupling capacitors can be used to cover both high and low frequencies. Locate these capacitors close to the point of entry at the PCB level and close to the pins of the part, with minimal trace length.

A single PCB ground plane should be sufficient when using the [AD9629](#). With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

When powering down the [AD9629](#), power off AVDD and DRVDD simultaneously, or DRVDD must be removed before AVDD.

#### **Exposed Paddle Thermal Heat Sink Recommendations**

The exposed paddle (Pin 0) is the only ground connection for the [AD9629](#); therefore, it must be connected to analog ground (AGND) on the customer's PCB. To achieve the best electrical and thermal performance, mate an exposed (no solder mask) continuous copper plane on the PCB to the [AD9629](#) exposed paddle, Pin 0.

The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. Fill or plug these vias with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and the PCB, a silkscreen should be overlaid to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. For detailed information about packaging and PCB layout of chip scale packages, see the [AN-772](#) Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, at [www.analog.com](http://www.analog.com).

#### **Encode Clock**

For optimum dynamic performance a low jitter encode clock source with a 50% duty cycle  $\pm 5\%$  should be used to clock the [AD9629](#).

#### **VCM**

The VCM pin should be decoupled to ground with a 0.1  $\mu\text{F}$  capacitor, as shown in Figure 38.

#### **RBIAS**

The [AD9629](#) requires that a 10 k $\Omega$  resistor be placed between the RBIAS pin and ground. This resistor sets the master current reference of the ADC core and should have at least a 1% tolerance.

#### **Reference Decoupling**

Externally decouple the VREF pin to ground with a low ESR, 1.0  $\mu\text{F}$  capacitor in parallel with a low ESR, 0.1  $\mu\text{F}$  ceramic capacitor.

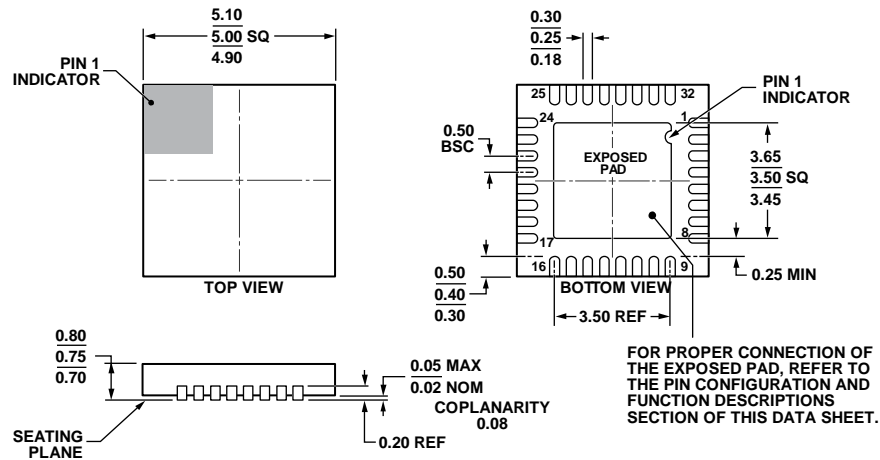
#### **SPI Port**

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the [AD9629](#) to keep these signals from transitioning at the converter inputs during critical sampling periods.

#### **Soft Reset**

In applications where  $\text{DRVDD} \geq 2.75 \text{ V}$ , do not perform soft reset (Register 0x00 Bit 2 and Bit 5 = 1). Soft reset restores [AD9629](#) defaults already available at power-up and is not needed.

# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 55. 32-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
 5 mm x 5 mm Body, Very Very Thin Quad (CP-32-11)  
 Dimensions shown in millimeters

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## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                              | Package Option |
|--------------------|-------------------|--|----------------|
| AD9629BCPZ-80      | -40°C to +85°C    | 32-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-32-11       |
| AD9629BCPZRL7-80   | -40°C to +85°C    | 32-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-32-11       |
| AD9629BCPZ-65      | -40°C to +85°C    | 32-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-32-11       |
| AD9629BCPZRL7-65   | -40°C to +85°C    | 32-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-32-11       |
| AD9629BCPZ-40      | -40°C to +85°C    | 32-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-32-11       |
| AD9629BCPZRL7-40   | -40°C to +85°C    | 32-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-32-11       |
| AD9629BCPZ-20      | -40°C to +85°C    | 32-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-32-11       |
| AD9629BCPZRL7-20   | -40°C to +85°C    | 32-Lead Lead Frame Chip Scale Package (LFCSP_WQ) | CP-32-11       |
| AD9629-80EBZ       |                   | Evaluation Board                                 |                |
| AD9629-65EBZ       |                   | Evaluation Board                                 |                |
| AD9629-40EBZ       |                   | Evaluation Board                                 |                |
| AD9629-20EBZ       |                   | Evaluation Board                                 |                |

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**