High-Efficiency Dual-String with up to 10-WLED White LED Driver

Description

The SM5306 is a current mode boost converter which supplies the power and controls current in up to two strings of 10 LEDs per string. Programming is done over an I^2C-compatible interface. The maximum LED current is adjustable from 5mA to 28.5mA. At any given maximum LED current the LED brightness is further adjusted with exponential or linear dimming steps. Additionally, pulsed width modulation (PWM) brightness control can be enabled allowing for LED current adjustment by a logic level PWM signal.

The boost switching frequency is programmable at 500kHz for low switching loss performance or 1MHz to allow the use of tiny low profile inductors. A setting for a 10% offset of these frequencies is available. Over Voltage Protection is programmable at 16V, 24V, 32V, or 40V to accommodate a wide variety of LED configurations and schottky diode/output capacitor combinations.

The SM5306 is available in a 12-bump, 1.65mm x 1.43mm WLCSP package.

Applications

- Mobile and Smart Phones LCD Backlight
- Tablet LCD Backlight
- Portable Devices LCD Backlight

Ordering Information

Part	Temp. Range	Pb-Free	Package
SM5306	-40°C to +85°C	Yes	12 WLCSP 0.4mm pitch

Features

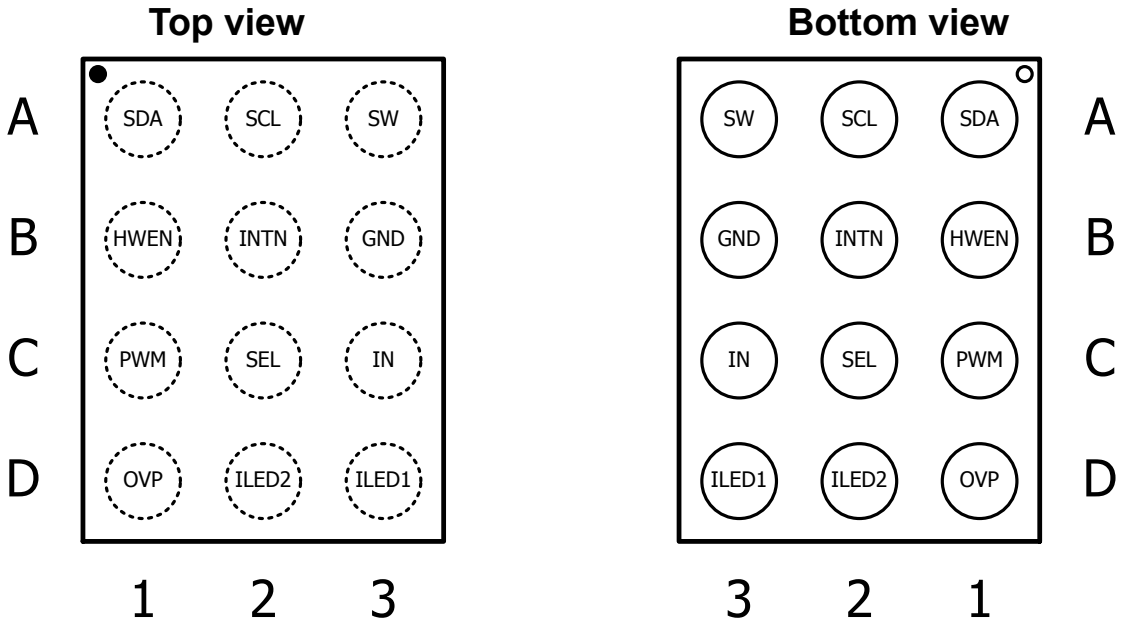
- Drives up to Two String of 10 Series LEDs
- 11-bit Programmable Dimming Resolution
- Exponential or Linear Brightness Control
- PWM Brightness Control for CABC Operation
- Independent Current Control per String
- Internal Soft-Start Limits Inrush Current
- Wide 2.5V to 5.5V Input Voltage Range
- Adaptive Headroom Control
- Selectable Boost Frequency of 500kHz or 1MHz with Optionally Additional Offset
- 12-Bump 1.65mm x 1.43mm WLCSP Package
- Protections
  . Programmable 16V/24V/32V/40V Over-Voltage Protection
  . LED Open/Short Circuit Protection
  . Thermal Shutdown
  . Current Limit

Evaluation Board Request

Will be available

CONFIDENTIAL - Target Datasheet

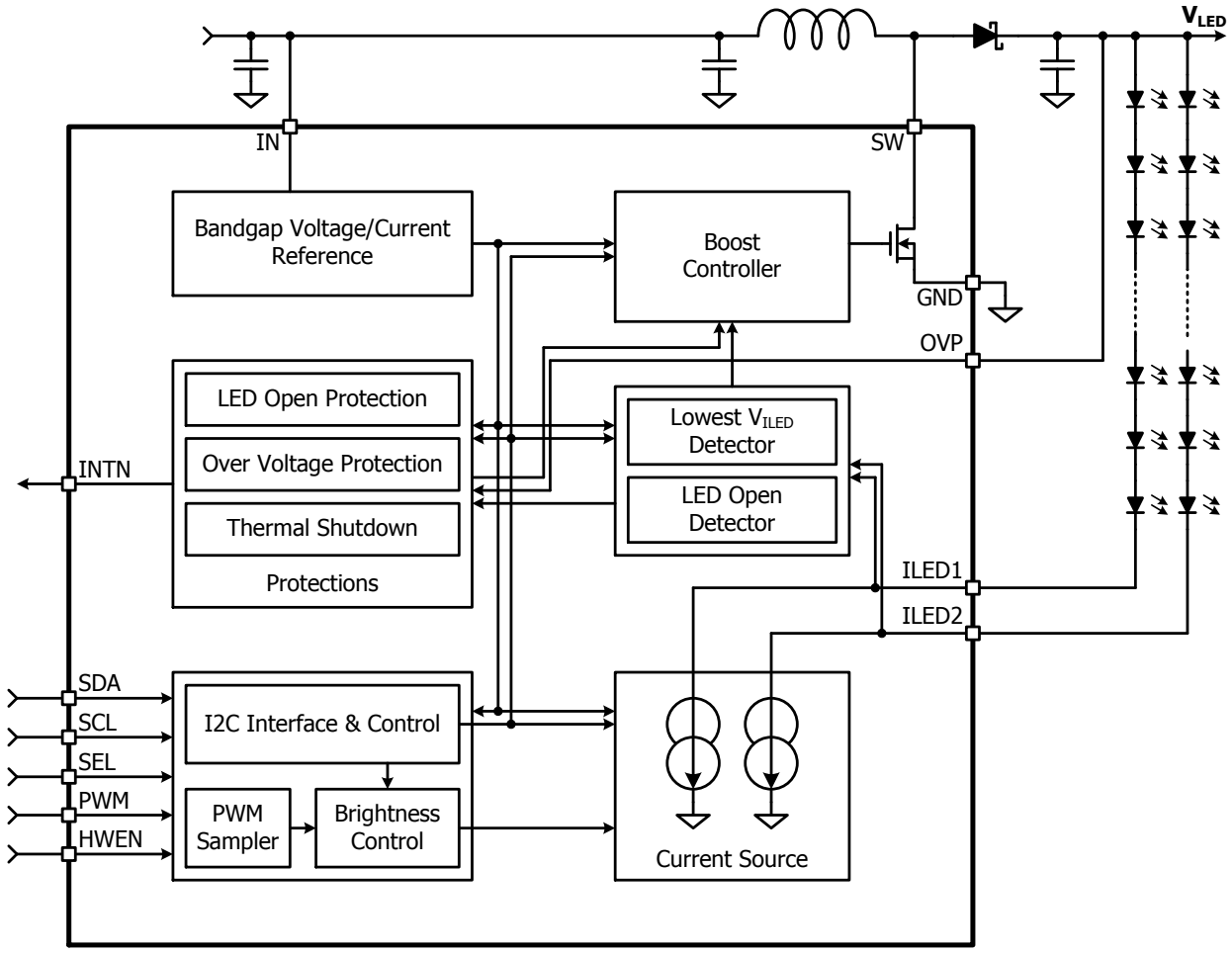
Pin Assignments



Pin Description

Pin	Name	Description
A1	SDA	**Data I/O** pin for the I^2C serial interface.
A2	SCL	**Clock Input** pin for the I^2C serial interface.
A3	SW	**Switching Node** of boost converter. SW pin is the drain of power N-MOSFET. Long traces of inductor to this pin and this pin to rectifying diode should be avoided.
B1	HWEN	**IC Enable Input.** Drive this pin high to enable the device. Drive this pin low to force the device into a low power shutdown. HWEN is a high-impedance input and cannot be left floating.
B2	INTN	**Interrupt Output** for fault status change. Open drain active low signal.
B3	GND	**Ground.**
C1	PWM	**External PWM Input** for brightness control.
C2	SEL	**I2C Address Select.** Ground selects address 0x36h and VIN selects address 0x38h.
C3	IN	**IC Supply Input.** In addition to using bulk capacitors of sufficient capacity, it is highly recommended to use the shunt capacitor of low ESR/ESL to bypass high frequency noise. Place shunt capacitor as close as possible to this pin.
D1	OVP	**Over Voltage Protection Pin.** This pin is sensing the output voltage of the boost converter. The boost converter output is connected to this pin directly.
D2	ILED2	**LED Current Sink Regulation Input 2.**
D3	ILED1	**LED Current Sink Regulation Input 1.**

Operational Diagram



Absolute Maximum Ratings

Stress(es) beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the following operational sections of the specifications is not implied. Exposure to absolute maximum rating condition(s) for extended periods may affect device reliability.

Parameter	Lower Limit	Upper Limit	Unit
IN, HWEN, PWM, SCL, SDA, INTN, SEL to GND[1)]	-0.3	6	V
SW, OVP, ILED1, ILED2 to GND[1)]	-0.3	45	V
ESD Human Body Model [2)]		2000	V
ESD Machine Model [2)]		200	V
Continuous Power Dissipation ($T_A \leq 25$ °C)[3)]		TBD	W
Continuous Power Dissipation ($T_A = 70$ °C)[3)]		TBD	W
Continuous Power Dissipation ($T_A = 80$ °C)[3)]		TBD	W
Operating Ambient Temperature	-40	85	°C
Recommended Operation Junction Temperature	-40	125	°C
Maximum Junction Temperature	-	150	°C
Storage Ambient Temperature	-65	150	°C
Lead Soldering Temperature (within 10s)		300	°C

Notes

1) GND: all of the PGNDx, PGNDHx, CGND, MGND and AGND should be within the limit.
2) Human Body Model (HBM) per JESD22-A114 for all pins.
3) Highly depends on the PCB heat dissipation. Tested with the following Thermal Characteristics test conditions.

Electrical Characteristics

V_{IN} = 3.6V, T_A = - 40°C ~ 85°C*). Typical values are at T_A = +25 °C, unless otherwise specified.

*) Specifications over the T_A range are assured by design, characterized and correlated with process control.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
GENERAL						
Input Voltage Range	V_{S_IN}		2.5	-	5.5	V
Input Supply Current when Disabled	I_{SD_IN1}	2.5V<V_{IN}<5.5V, I_2C shutdown		1	4	µA
	I_{SD_IN2}	2.5V<V_{IN}<5.5V, HWEN=GND		1	4	µA
Input Supply Current	I_{S_IN1}	Not switching		350		µA
	I_{S_IN2}	Switching, Address<02h>[1:0]="00b"		1.52	2.5	mA
VIN Start Threshold Voltage	V_{START}	V_{IN} rising	TBD	TBD	2.5	V
UVLO Hysteresis	HY_{UVLO}	V_{STOP}=V_{START}-HY_{UVLO}		TBD		mV
Initialization Timing	t_{WAIT}		1			ms
LOGIC INPUT/OUTPUT (PWM, HWEN, SEL, INTN)						
Logic Input Low Voltage (PWM, HWEN, SEL)	V_{IL}	2.3V ≤ V_{IN} ≤5.5V	0		0.4	V
Logic Input High Voltage (PWM, HWEN, SEL)	V_{IH}	2.3V ≤ V_{IN} ≤5.5V	1.2		V_{IN}	V
Output Low Voltage (INTN)	V_{OL}	I_{SINK}=1mA			0.4	V
PWM Input Frequency	f_{PWM}	2.3V ≤ V_{IN} ≤5.5V	10		80	kHz
PROTECTIONS						
Thermal Shutdown Temperature[1)]	T_{SD}	Temperature rising		140		°C
Thermal Shutdown Hysteresis[1)]	HY_{TSD}			TBD		°C
Over Voltage Protection Threshold High	V_{OVP_H1}	2.5V<V_{IN}<5.5V, V_{OVP} rising, Address<02h>[6:5]="01b"	23	24	25	V
	V_{OVP_H2}	2.5V<V_{IN}<5.5V, V_{OVP} rising, Address<02h>[6:5]="11b"	39	41	44	V
Over Voltage Protection Hysteresis	HY_{OVP}	V_{OVP_L} (OVP Threshold Low)=V_{OVP_H}-HY_{OVP}		1		V
Switch Current Limit Threshold	I_{LIM1}	2.5V<V_{IN}<5.5V, Address<02h>[4:3]="00b"	TBD	600	TBD	mA
	I_{LIM2}	2.5V<V_{IN}<5.5V, Address<02h>[4:3]="01b"	TBD	800	TBD	mA
	I_{LIM3}	2.5V<V_{IN}<5.5V, Address<02h>[4:3]="10b"	TBD	1000	TBD	mA
	I_{LIM4}	2.5V<V_{IN}<5.5V, Address<02h>[4:3]="11b"	TBD	1200	TBD	mA
BOOST CONVERTER						
Switching Frequency	f_{SW1}	Address<02h>[1:0]="00b"	TBD	500	TBD	kHz
	f_{SW2}	Address<02h>[1:0]="10b"	TBD	560	TBD	kHz
	f_{SW3}	Address<02h>[1:0]="01b"	TBD	1000	TBD	kHz
	f_{SW4}	Address<02h>[1:0]="11b"	TBD	1120	TBD	kHz
Maximum Duty Cycle	D_{MAX}			94		%
SW On-Resistance	R_{DS_ON}	I_{SW}=100mA		250		mΩ
SW Leakage Current	I_{LK_SW}	V_{SW}=45V			10	µA

Electrical Characteristics (Continued)

V_{IN} = 3.6V, T_A = - 40°C ~ 85°C*). Typical values are at T_A = +25 °C, unless otherwise specified.

*) Specifications over the T_A range are assured by design, characterized and correlated with process control.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CURRENT SOURCES						
LED Current Range[1)]	I_{S_LED}				28.25	mA
LED Current Regulation	I_{LED}	2.5V<V_{IN}<5.5V, Full Scale current set to 20mA	19	20	21	mA
Current Matching Between Channels		2.5V ≤ V_{IN} ≤5.5V, T_A=+25°C, Full Scale current set to 10mA	-1		1	%
		2.5V ≤ V_{IN} ≤5.5V, 0°C≤ T_A≤+70°C, Full Scale current set to 10mA	-2.5		2.5	%
Current Source Leakage Current (ILED1, ILED2)	I_{B_LED}			10		µA
Regulated Current Sink headroom Voltage	V_{REG_CS}	ILED=5mA		200		mV
I2C INTERFACE[1), 2)]						
I^2C Logic Input High Threshold Voltage	V_{IH_I2C}	SDA, SCL	1.2			V
I^2C Logic Input Low Threshold Voltage	V_{IL_I2C}	SDA, SCL			0.4	V
I^2C Logic Output Low Voltage	V_{OL_I2C}	SDA, SCL @3mA sink current			0.4	V
SCL Clock Frequency	f_{SCL}		0		400	kHz
SCL Clock High Period	t_{SCL_H}		0.6			µs
SCL Clock Low Period	t_{SCL_L}		1.3			µs
I^2C Spike Rejection Filter Pulse Width	t_{SP}		0		50	ns
I^2C Data Setup Time	t_{SU_DAT}		100			ns
I^2C Data Hold Time	t_{HD_DAT}		0		900	ns
SDA, SCL Rise Time	t_{R_I2C}			20+0.1 xC_B	300	ns
SDA, SCL Fall Time	t_{F_I2C}			20+0.1 xC_B	300	ns
I^2C Bus Free Time between Stop and Start	t_{BUF}		1.3			µs
I^2C Repeated Start Condition Setup Time	t_{SU_STA}		0.6			µs
I^2C Repeated Start Condition Hold Time	t_{HD_STA}		0.6			µs
I^2C Stop Condition Setup Time	t_{SU_STO}		0.6			µs
I^2C Bus Capacitive Load	C_B				400	pF
SDA Input Capacitance	C_{SDA}				10	pF
SCL Input Capacitance	C_{SCL}				10	pF

Notes

1) Guaranteed by design, characterization and correlation with statistical controls. Not fully tested in production.
2) Designed and simulated according to I^2C specifications except general call support

I²C Programming

Device Address

SEL	Device Address								Write	Read
	B7	B6	B5	B4	B3	B2	B1	B0		
Low	0	1	1	0	1	1	0	R/W	0x6Ch	0x6Dh
High	0	1	1	1	0	0	0	R/W	0x70h	0x71h

Register Map

Register Name	Address	Type	Default Reset Values
Control	0x00h	R/W	0xC0h
Configuration	0x01h	R/W	0x18h
Boost Control	0x02h	R/W	0x38h
Brightness MSB	0x03h	R/W	0x00h
Brightness LSB	0x04h	R/W	0x00h
Current	0x05h	R/W	0x1Fh
Reserved[1)]	0x06h		
On/Off Ramp	0x07h	R/W	0x00h
Run Ramp	0x08h	R/W	0x00h
Interrupt Status	0x09h	R/W	0x00h
Interrupt Enable	0x0Ah	R/W	0x00h
Fault Status	0x0Bh	R/W	0x00h
Software Reset	0x0Fh	R/W	0x00h
PWM Out LOW	0x12h	R/W	0x00h
PWM Out High	0x13h	R/W	0x00h
Revision	0x1Fh	R/W	0x02h

Notes

1) No data can be written into this register and only a data of 00h can be read. But an acknowledge bit takes place when this register is selected.

Control Register (Address 0x00h)

Bit	Register Name	Access	Default	Description
7	SLEEP_CMD	R/W	1	The device is put into sleep mode when set to '1'.
6	SLEEP_STATUS	Read	1	Reflects the sleep mode status. A '1' indicates the part is in sleep mode. Used to determine when part has entered or excited sleep mode after writing the SLEEP_CMD bit.
5	Reserved			
4	LINEAR	R/W	0	Enables the linear output mode when set '1'.
3	Reserved			
2	LED_EN_1	R/W	0	Enables the LED 1 output.
1	LED_EN_2	R/W	0	Enables the LED 2 output.
0	Reserved			

Configulation Register (Address 0x01h)

Bit	Register Name	Access	Default	Description
7:5	Reserved			
4	FB_EN_LED2	R/W	1	Enable LED2 feedback
3	FB_EN_LED1	R/W	1	Enable LED1 feedback
2	PWM_LOW	R/W	0	Sets the PWM to active low
1	Reserved			
0	PWM_EN	R/W	0	Enables the PWM

Boost Control Register (Address 0x02h)

Bit	Register Name	Access	Default	Description
7	Reserved			
6:5	BOOST_OVP	R/W	01	Selects the voltage limit for over-voltage protection: 00: 16V 01: 24V 10: 32V 11: 40V
4:3	BOOST_OCP	R/W	11	Selects the current limit for over-current protection: 00: 600mA 01: 800mA 10: 1.0A 11: 1.2A
2	SLOW_START	R/W	0	Slows the boost output transition.
1	SHIFT	R/W	0	Enables the alternate oscillator frequencies: For FMODE=0: SHIFT=0F=500kHz, 1F=560kHz For FMODE=1: SHIFT=0F=1MHz, 1F=1120kHz
0	FMODE	R/W	0	Selects the boost frequency: 0: 500kHz 1: 1MHz

Brightness MSB Register (Address 0x03h) [1)]

Bit	Register Name	Access	Default	Description
7:0	BRT_MSB	R/W	00000000	Sets the MSB of the 11-bit brightness value.

Notes

1) These registers will not update if the device is in Sleep Mode (Control: SLEEP_STATUS = 1)

Brightness LSB Register (Address 0x04h) [1)]

Bit	Register Name	Access	Default	Description
7:3	Reserved			
2:0	BRT_LSB	R/W	000	Sets the LSB of the 11-bit brightness value.

Notes

1) These registers will not update if the device is in Sleep Mode (Control: SLEEP_STATUS = 1)

Current Register (Address 0x05h)

Bit	Register Name	Access	Default	Description
7	Hysteresis	R/W	0	Determine the hysteresis of the PWM sampler. Clearing this bit, the PWM sampler changes its output upon detecting at least 3 equivalent code changes on the PWM input. Setting this bit, the PWM sampler changes its output upon detecting 2 equivalent code changes on the PWM input.
6	Lower Bound	R/W	0	Determines the lower bound of the PWM Sampler. Cleaning this bit, the PWM sampler outputs code 6 when it detects equivalent codes 2 thru 6: and code 0 when it detects equivalent codes 0 thru 1. Setting this bit, the PWM sampler can output codes below 6, based upon the Hysteresis setting and equivalent code sampled from the PWM input.
5	Reserved			
4:0	Current	R/W	11111	Sets the 5-bit full scale current.

On/Off Ramp Register (Address 0x07h)

Bit	Register Name	Access	Default	Description
7	Reserved			
6	Reserved			
5:3	T_START	R/W	000	Ramp time for startup events.
2:0	T_SHUT	R/W	000	Ramp time for shutdown events.

Code	Start-up Time	Shutdown Time
000	4ms	0[1)]
001	261ms	261ms
010	522ms	522ms
011	1.045s	1.045s
100	2.091s	2.091s
101	4.182s	4.182s
110	8.364s	8.364s
111	16.73s	16.73s

Notes
1) Code 0 results in approximately 0.5ms ramp time.

Run Ramp Register (Address 0x08h)

Bit	Register Name	Access	Default	Description
7	Reserved			
6	Reserved			
5:3	T_UP	R/W	000	Time for ramp-up events.
2:0	T_DOWN	R/W	000	Time for ramp-down events.

Code	Ramp-up Time	Ramp-down Time
000	0[1)]	0[1)]
001	261ms	261ms
010	522ms	522ms
011	1.045s	1.045s
100	2.091s	2.091s
101	4.182s	4.182s
110	8.364s	8.364s
111	16.73s	16.73s

Notes
1) Code 0 results in approximately 0.5ms ramp time.

Interrupt Status Register (Address 0x09h)

Bit	Register Name	Access	Default	Description
7	Reserved			
6	Reserved			
5	Reserved			
4	Reserved			
3	Reserved			
2	2	R/W	0	An Over-current condition occurred.
1	1	R/W	0	An Over-voltage condition occurred.
0	0	R/W	0	A thermal shutdown event occurred.

The interrupt status register is cleared upon a read of the register. If the condition that caused the interrupt is still present, then the bit will be set to one again and another interrupt is signaled on the INTN output pin. The interrupt status register is not cleared if the device is in the sleep mode (Control: SLEEP_STATUS=1). To disconnect the interrupt condition from the INTN pin during sleep mode, disable the fault connection in the interrupt Enable register. An interrupt condition will set the status bit and cause an event on the INTN pin only if the corresponding bit in the Interrupt Enable register is one and the Global Enable bit is also one.

Interrupt Enable Register (Address 0x0Ah)

Bit	Register Name	Access	Default	Description
7	GLOBAL	R/W	0	Set to '1' to enable interrupts to drive the INTN pin.
6:3	Reserved			
2	2	R/W	0	Set to '1' to enable the over-current condition interrupt.
1	1	R/W	0	Set to '1' to enable the over-voltage condition interrupt.
0	0	R/W	0	Set to '1' to enable the thermal shutdown condition interrupt.

Fault Status Register (Address 0x0Bh)

Bit	Register Name	Access	Default	Description
7	Reserved			
6	Reserved			
5	OPEN	R/W	0	An open circuit was detected on one of the LED strings.
4	LED2_SHORT	R/W	0	A short was detected on LED string 2.
3	LED1_SHORT	R/W	0	A short was detected on LED string 1.
2	SHORT_EN	R/W	0	Set to '1' to enable short test.
1	OVP_FAULT	R/W	0	An OVP occurred in manufacturing test.
0	OVP_F_EN	R/W	0	Set to '1' to enable OVP manufacturing test.

Software Reset Register (Address 0x0Fh)

Bit	Register Name	Access	Default	Description
7:1	Reserved			
0	SW_RESET	R/W	0	Set to '1' to reset the device. This is a full reset which clears the registers, executers a power-on reset, and reads the EEPROM configuration.

PWM Out Low Register (Address 0x12h)

Bit	Register Name	Access	Default	Description
7	PWM_OUT[7]	Read	0	
6	PWM_OUT[6]	Read	0	
5	PWM_OUT[5]	Read	0	
4	PWM_OUT[4]	Read	0	
3	PWM_OUT[3]	Read	0	
2	PWM_OUT[2]	Read	0	
1	PWM_OUT[1]	Read	0	
0	PWM_OUT[0]	Read	0	

PWM Out High Register (Address 0x13h)

Bit	Register Name	Access	Default	Description
7:0	PWM_OUT	R/W	00000000	The value of the PWM detector. Maximum value is 256 or 100h. if PWM_OUT[7:0] is non-zero PWM_OUT[8] will be zero.
0	PWM_OUT[8]	R/W	0	

Revision Register (Address 0x1Fh)

Bit	Register Name	Access	Default	Description
7:0	PWM_OUT[7]	R/W	00000000	Revision value

Device Functional Description

Operation

The SM5306 provides the power for two high-voltage LED strings (up to 40V at 28.5 mA each). The two high-voltage LED strings are powered from an integrated asynchronous boost converter. The device is programmable over an I^2C-compatible interface.

PWM Input Polarity

The PWM input can be set for active high (default) or active low polarity. With active low polarity the LED current is a function of the negative duty cycle at PWM.

HWEN Input

HWEN is the global hardware enable to the SM5306. HWEN must be pulled high to enable the device. HWEN is a high-impedance input so it cannot be left floating. When HWEN is pulled low the SM5306 is placed in shutdown and all the registers are reset to their default state.

SEL Input

SEL is the select pin for the serial bus device address. When this pin is connected to ground, the seven-bit device address is 36h. When this pin is tied to the IN power rail, the device address is 38h.

INTN Output

The INTN pin is an open drain active low output signal which will indicate detected faults. The signal will assert low when either OCP, OVP, or TSD is detected by the LED driver. The Interrupt Enable register must be set to connect these faults to the INTN pin.

Boost Converter

The high-voltage boost converter provides power for the two current sinks (ILED1 and ILED2). The boost circuit operates using a 10µH to 22µH inductor and a 1µF output capacitor. The selectable 500kHz or 1MHz switching frequency allows for the use of small external components and provides for high boost converter efficiency. Both LED1 and LED2 feature an adaptive voltage regulation scheme where the feedback point (LED1 or LED2) is regulated to a minimum of 300mV. When there are different voltage requirements in both high-voltage LED strings, because of different programmed voltages or string mismatch, the device will regulate the feedback point of the highest voltage string to 300mV and drop the excess voltage of the lower voltage string across the lower strings current sink.

Boost Switching Frequency Select

The SM5306's boost converter can have a 1MHz or 500kHz switching frequency. For a 500kHz switching frequency the inductor must be between 10µH and 22µH. For the 1MHz switching frequency the inductor can be between 10µH and 22µH. Additionally there is a Frequency Shift bit which will offset the frequency approximately 10%. For the 500kHz setting, Shift=0. The boost frequency is shifted to 560kHz when Shift=1. For the 1MHz setting, Shift=0. The boost frequency is shifted to 1120kHz when Shift=1.

Adaptive Headroom

The adaptive headroom circuit controls the boost output voltage to provide the minimal headroom voltage necessary for the current sinks to provide the specified LED current. The headroom voltage is fed back to the error amplifier to dynamically adjust the boost output voltage. The error amplifier's reference voltage is adjusted as the brightness level is changed, since the currents sinks require less headroom at lower LED currents than at higher LED currents. Note that the Lowest V_{ILED} Detector block dynamically selects the LED string that requires the higher boost voltage to maintain the LED current; this string will have the lower headroom voltage. In a single string LED configuration the feedback enable must be enabled for only that string (LED1 or LED2). The adaptive headroom circuit is control by that single string. In a two string LED configuration the feedback enable must be enabled for both strings (LED1 and LED2). The Lowest V_{ILED} Detector block then dynamically selects the LED string to control the adaptive headroom circuit.

Current Sinks

LED1 and LED2 control the current up to a 40V LED string voltage. Current sinks have 5-bit full-scale current programmability and 11-bit brightness control. Current sinks have the same current set through a dedicated brightness register and can additionally be controlled via the PWM input.

Current String Biasing

Each current string can be powered from the SM5306's boost or from an external source. When powered from an external source the feedback input for either current sink can be disabled in the Configuration register so it no longer controls the boost output voltage.

Full-Scale LED Current

The SM5306's full-scale current is programmable with 32 different full scale levels. The full-scale current is the LED current when the brightness code is at max code (0xFF). The 5-bit full-scale current vs code is given by the following equation:

$$I_{LED,\ Full\ Scale} = 5 + Code \times 0.75[mA]$$

Brightness Register Current Control

The SM5306 features Brightness Register Current Control for simple user-adjustable current control set by writing directly to Brightness Registers. The current is a function of the full-scale LED current, the 11-bit code in the respective brightness register, and the PWM input duty cycle (if PWM is enabled). The Brightness Registers should always be written with LSB's first and MSB's. In this mode the SM5306 will use the full 11-bit brightness code while ramping the LED brightness.

Exponential Mapping

In exponential mapping mode the brightness code to backlight current transfer function is given by the equation:

$$I_{LED} = I_{LED,\ Full\ Scale} \times 0.85^{\left[44-\left(\frac{Code+1}{5.81818}\right)\right]} \times D_{PWM}$$

Where $I_{LED,Full\ Scale}$ is the full-scale LED current setting, Code is the backlight code in the brightness register, and D_{PWM} is the PWM input duty cycle. Figure 1 and Figure 2 show the approximate backlight code to LED current response using exponential mapping mode. Figure 1 shows the response with a linear Y axis, and Figure 2 shows the response with a logarithmic Y axis. In exponential mapping mode the current ramp (either up or down) appears to the human eye as a more uniform transition then the linear ramp. This is due to the logarithmic response of the eye.

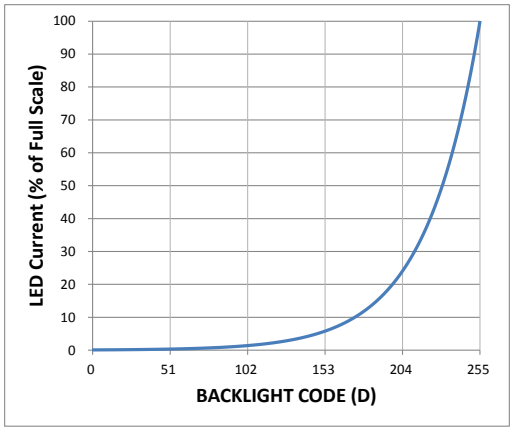


Figure 1. Exponential Mapping Mode (Linear Scale)

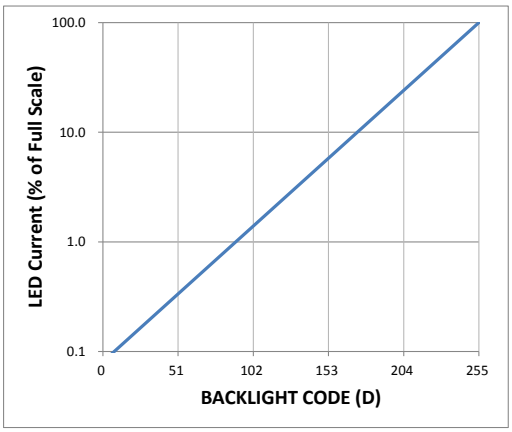


Figure 2. Exponential Mapping Mode (Log Scale)

Linear Mapping

In linear mapping mode the brightness code to backlight current has a linear relationship and follows the equation:

$$I_{LED} = I_{LED,\ Full\ Scale} \times \frac{1}{255} \times Code \times D_{PWM}$$

Where $I_{LED,Full\ Scale}$ is the full-scale LED current setting, Code is the backlight code in the brightness register, and D_{PWM} is the PWM input duty cycle. Figure 3 shows the backlight code to LED current response using linear mapping mode. The Configuration register must be set to enable linear mapping.

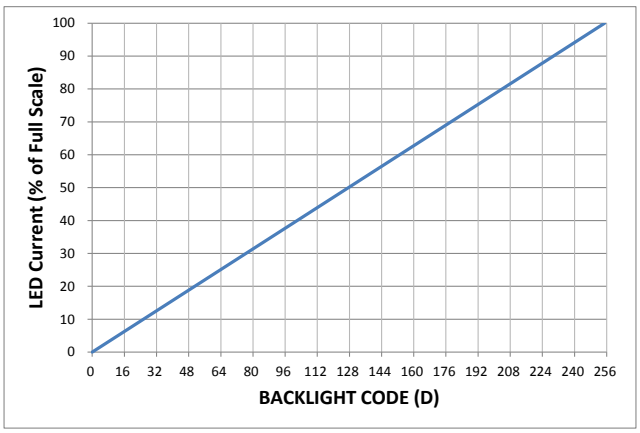


Figure 3. Linear Mapping Mode

LED Current Ramping

Startup/Shutdown Ramp

The LED current turn on time from 0 to the initial LED current set-point is programmable. Similarly, the LED current shutdown time to 0 is programmable. Both the startup and shutdown times are independently programmable with 8 different levels. The startup times are independently programmable from the shutdown times. The startup time is used when the device is first enabled to

a non-zero brightness value. The shutdown time is used when the brightness value is programmed to zero. If HWEN is used to disable the device, the action is immediate and the Shutdown time is not used. The zero code does take a small amount of time which is approximately 0.5ms.

Run-Time Ramp

Current ramping from one brightness level to the next is programmable. There are 8 different ramp up times and 8 different ramp down times. The ramp up time is independently programmable from the ramp down time. The run time ramps are used whenever the device is enabled with a non-zero brightness value and a new non-zero brightness value is written.

Test Features

The SM5306 contains an LED open, an LED short, and Over Voltage manufacturing fault detection. This fault detection is designed to be used during the manufacturing process only and not normal operation. These faults do not set the INTN pin.

Open LED String (LED1 and LED2)

An open LED string is detected when the voltage at the input to either LED1 or LED2 has fallen below 150 mV and the boost output voltage has hit the OVP threshold. This test assumes that the LED string that is being detected for an open is being powered from the boost output (Feedback Enabled). For an LED string not connected to the boost output, and connected to another voltage source, the boost output would not trigger the OVP flag. In this case an open LED string would not be detected.

Shorted LED String

The SM5306 features an LED short fault flag indicating if either of the LED strings has experienced a short. There are two methods that can trigger a short in the LED strings

1. An LED current sink with feedback enabled and the difference between OVP input and the LED current sink input voltage goes below 1V.
2. An LED current sink is configured with feedback disabled (not powered from the boost output) and the difference between VIN and the LED current sink input voltage goes below 1V.

Over-Voltage Protection (Manufacturing Fault Detection and Shutdown)

The SM5306 provides an Over-Voltage Protection (OVP) mechanism specifically for manufacturing test where a display may not be connected to the device. The over voltage protection threshold (OVP) on the SM5306 has 4 different programmable options (16V, 24V, 32V, and 40V). The manufacturing protection is enabled in the Fault Status register bit 0. When enabled, this feature will cause the boost converter to shutdown anytime the selected OVP threshold is exceeded. The OVP_fault bit in the Fault Status register will be set to one. The boost converter will not resume operation until the SM5306 is reset with either a write to the Software Reset bit in the Software Reset register or a cycling of the HWEN pin. The reset will clear the fault.

Fault Flags/Protection Features

The Interrupt Status register contains the status of the protection circuits of the SM5306. The corresponding bits will be set to one if an OVP, OCP, or TSD event occurs. These faults do set the INTN pin when the corresponding bit is set in the Interrupt Enable register.

Over-Voltage Protection (Inductive Boost Operation)

The over-voltage protection (OVP) threshold high voltage on the SM5306 has 4 different programmable options (16V, 24V, 32V, and 40V). Over-voltage protection protects the device and associated circuitry from high voltages in the event the feedback enabled LED string becomes open. During normal operation, the SM5306's inductive boost converter will boost the output up so as to maintain at least 300 mV at the active current sink inputs. When a high-voltage LED string becomes open the feedback mechanism is broken, and the boost converter will inadvertently over boost the output. When the output voltage reaches the over-voltage protection (OVP) threshold the boost converter will stop switching, thus allowing the output node to discharge. When the output discharges to OVP threshold low voltage the boost converter will begin switching again. The OVP sense is at the OVP pin, so this pin must be connected directly to the inductive boost output capacitor's positive terminal. For current sinks that have feedback disabled the over voltage sense mechanism is not in place to protect from potential over-voltage conditions. In this situation the application must ensure that the voltage at LED1 or LED2 doesn't exceed 40V. The default setting for OVP is set at 24V. For applications that require higher than 24V at the boost output the OVP threshold will have to be programmed to a higher level at power up.

Current Limit

The switch current limit for the SM5306's inductive boost is set at 1A. When the current through the NFET switch hits

this over-current protection (OCP) threshold the device turns the NFET off and the inductor's energy is discharged into the output capacitor. Switching is then resumed at the next cycle. The current limit protection circuitry can operate continuously each switch cycle. The result is that during high output power conditions the device can continuously run in current limit. Under these conditions the SM5306's inductive boost converter stops regulating the headroom voltage across the high voltage current sinks. This results in a drop in the LED current.

Thermal Shutdown

The SM5306 contains thermal shutdown protection. In the event the die temperature reaches 150°C, the boost power supply and current sinks will shut down until the die temperature drops to typically 125°C.

Initialization Timing

Initialization Timing with HWEN tied to VIN

If the HWEN input is tied to VIN, then the t_{WAIT} time starts when VIN crosses 2.5V as shown below. The initial I^2C transaction can occur after the t_{WAIT} time expires. Any I^2C transaction during the t_{WAIT} period will be NAK'ed.

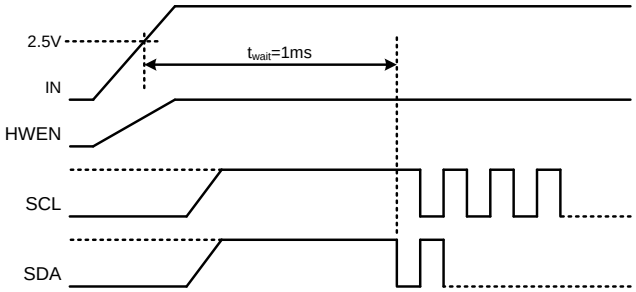


Figure 4. Initialization Timing with HWEN Tied to VIN

Initialization Timing with HWEN driven by GPIO

If the HWEN input is driven by a GPIO then the t_{WAIT} time starts when HWEW crosses 1.2V as shown below. The initial I2C transaction can occur after the t_{WAIT} time expires. Any I2C transaction during the t_{WAIT} period will be NAK'ed

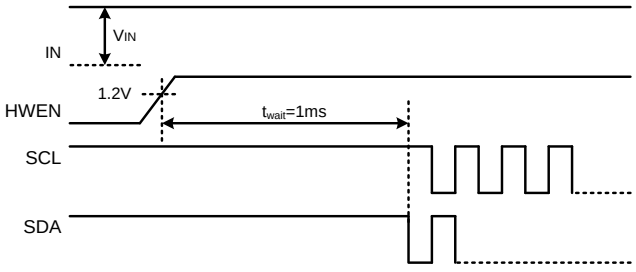


Figure 5. Initialization Timing with HWEN Driven by GPIO

Initialization after Software Reset

The time between the I^2C transaction that issues the software reset, and the subsequent I^2C transaction (ie to configure the SM5306) must be at greater or equal to the t_{WAIT} period of 1ms. Any I^2C transaction during the t_{WAIT} period will be NAK'ed.

I^2C-COMPATIBLE INTERFACE

The SM5306 supports I^2C serial interface, which consists of two lines, a bi-directional data signal (SDA) and a clock signal (SCL). These two lines should be connected to a positive supply voltage via pull-up resistors. A pull-up resistor between the controller's VIO line, and SDA must be greater than $[(V_{IO}-V_{OL})/3mA]$ to meet the V_{OL} requirement on SDA. A larger pull-up resistor results in lower switching current with slower edges, while a smaller pull-up resistor results in higher switching currents with faster edges. The SM5306 always plays a role of the slave. The SM5306 conforms to standard I^2C serial interface (Rev. 03 - 19 June 2007), but doesn't support the general call. The definition of I^2C-bus terminology is shown in the table below.

Table 1. Definition of I^2C Bus Terminology

Term	Description
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus

The standard I^2C interface protocol is briefly described in the following subsections. For more information, refer to the I^2C-bus specification and user manual by Philips.

Protocol Conventions

1. Bus Not Busy

The bus is not busy when both SDA and SCL remain high state.

2. START Data Transfer (S)

A START condition is when the SDA changes from high to low, while the SCL is high.

3. STOP Data Transfer (P)

A STOP condition is when the SDA changes from low to high, while the SCL is high.

4. Data Validity

The data on the SDA line must be high or low state during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low. One clock pulse is generated for each data bit transferred.

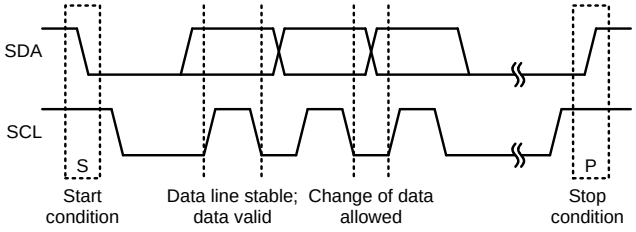


Figure 6. Data Validity

5. Acknowledge and Not Acknowledge

The acknowledge bit takes place after every bytes. The receiver transmits the acknowledge bit to the master as a meaning of successful reception. For the acknowledge bit, the master must generate an extra 9th clock pulse following after the 8th clock pulse. The acknowledge signal is defined when SDA is low during the 9th clock pulse. If SDA remains high during this 9th clock pulse, this is defined as the "Not Acknowledge" signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

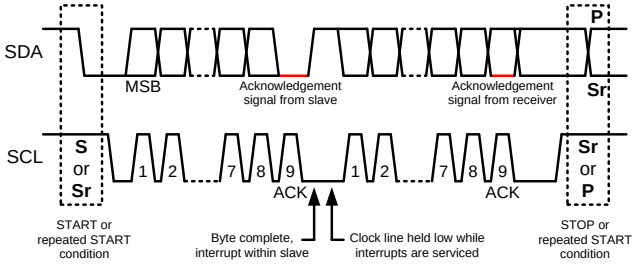


Figure 7. Example of Data Transfer on I²C Bus

6. Formats with 7-bit Addresses

Data transfers follow the format shown in Figure 8. Afterr the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/$\overline{W}$) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition. Various combinations of read/write formats are then possible within such a transfer.

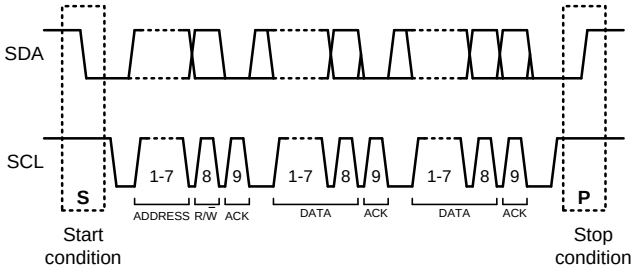


Figure 8. A Complete Data Transfer

Internal Control Register Operations

1. Slave Address

The register of SM5306 has a 7-bit long slave address (0110110b or 0111000b). The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command.

2. Write Operation

In write mode, the master transmits to the SM5306 slave receiver. The Master generates the start condition and sends the slave address (7bit) with the R/$\overline{W}$ bit set to zero. The first byte of information is the register address byte. The register address byte determines which register is to be written by the next byte, if received. If a STOP condition is detected after the register address byte is received, the SM5306 takes no further action (Figure 9) beyond storing the register address byte. Any byte received after the register address byte is data bytes. The first data byte goes into the register of the SM5306 selected by the register address byte. (Figure 10) If multiple data bytes are transmitted before a STOP condition is detected, these bytes are generally stored in subsequent SM5306 internal registers, because the register address byte generally autoincrements. (Figure 11)

3. Read Operation

The SM5306 is read using the internally stored register address byte as an address pointer, the same way the stored register address byte is used as an address pointer for a write. The pointer generally autoincrements after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the SM5306's register address byte by performing a write (Figure 9). The master can now read consecutive N-bytes from the SM5306, with the first data byte being read from the register addressed by the initialized register address byte. When performing read-after-write verification, remember to reset the register address byte's address, because the stored register

address byte address is generally autoincremented after the write (Figure 11).

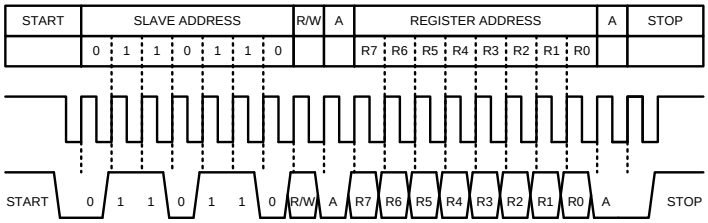


Figure 9. Example of Register Address Transfer on I2C Bus (SEL=0)

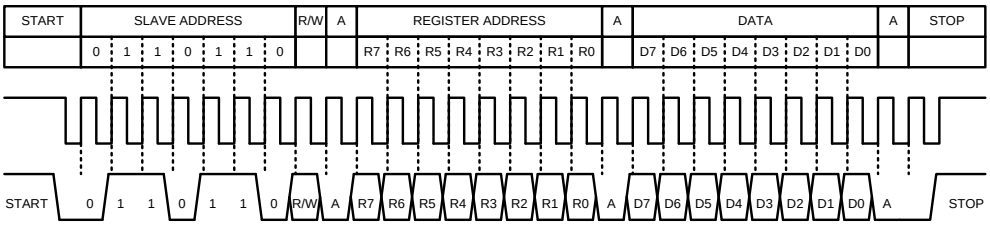


Figure 10. Example of Register Address and 1-byte Data Transfer on I2C Bus (SEL=0)

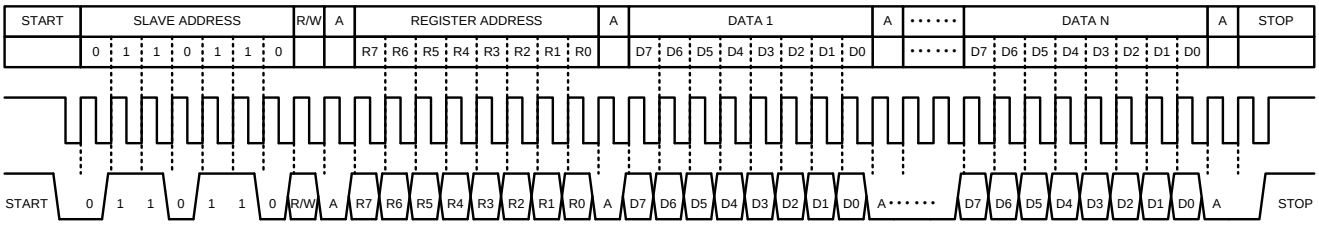


Figure 11. Example of Register Address and N-byte Data Transfer on I2C Bus (SEL=0)

Application Information

Recommended Initialization Sequence

The recommended initialization sequence for the device registers is listed below.

1. Set Configuration register (Address=01h) to enable the PWM and the feedback. For example, writing 09h to the Configuration register enables PWM and feedback of LED1.
2. Configure the Boost Control register (Address =02h) to select the OVP, OCP and FMODE. For example, writing 78h to the Boost Control register sets OVP to 40V, OCP to 1.2A and FMODE to 500 kHz.
3. Set the full scale LED current by writing to the Current register (Address=05h). For example, writing 14h to the Current register selects a full scale LED current of 20mA.
4. Set the PWM Sampler Hysteresis to 2 codes by setting Bit 7 of the Current register. Set the PWM Sampler Lower Bound code to 6 by clearing Bit 6 of the Current register.
5. Select the current control and enable or disable the LED 1 output and/or the LED 2 output by writing to Control register (Address=00h). For example, writing 14h to the Control register select linear current control and enables LED 1.
6. Set the LED brightness by writing to Brightness MSB register (Address=03h) and LSB register (Address=04h). For example, writing FFh to Brightness MSB and 07h to Brightness LSB will set the LED current to 20 mA, with the Current register set to 14h and the PWM input is high.

PWM Operation

PWM Input

The PWM input is sampled by a digital circuit which outputs a brightness code that is equivalent to the PWM input duty cycle. The resultant brightness value is a combination of the maximum current setting, the

brightness registers, and the equivalent PWM brightness code.

PWM input Frequency

The specified input frequency of the PWM signal is 10 kHz to 80 kHz. The recommended frequency is 30 kHz or greater. The PWM input sampler will operate beyond those frequency limits. Performance will change based on the input frequency used. It is not recommended to use frequencies outside the specified range. Lower PWM input frequency increases the likelihood that the output of the sampler may change and that a single brightness step may be visible on the screen. This may be visible at low brightness because the step change is large relative to the output level.

Recommended Settings

For best performance of the PWM sampler it is recommended to have a PWM input frequency of at least 30 kHz. The Hysteresis 1 bit should be set in register 05h to 1 when setting the maximum current. For example, if max current is 20 mA, register 05h is set to 14h, change that to 94h for 1 bit hysteresis and a smooth min-to-max brightness transition.

Adjustments to PWM sampler

The digital sampler has controls for hysteresis and minimum output brightness which allow the optimization of sampler output. The default hysteresis mode of the PWM sampler requires detecting a two code change in the input to increase brightness. Reducing the hysteresis to change on 1 code will allow a smoother brightness transition when the brightness control is swept across the screen in a system. A lower bound to the brightness is enabled by default which will limit the minimum output of the PWM sampler to an equivalent code of 6 when the LEDs are turned on. A detected code of 1 will be forced to off. A minimum 2% PWM input duty cycle is recommended. Input duty cycles of 1% or less will cause delayed off to on transitions.

1. Hysteresis 1 bit, Register 05h, Bit 7

The default setting for the SM5306 has Bit 7 of register 05h is 0b. This requires the detection of a PWM input change that is at least 3 equivalent codes higher than the present code. If this bit is set to 1b, the hysteresis is turned off and the PWM sampler output is allowed to change by 2 code.

Setting this bit to 1b will turn off the 2 code requirement for the PWM sampler output to change. The benefit is the output change will be smoother. The negative is that there may be some PWM input value where the output could change by one code and it might appear as flicker.

2. Lower Bound Disable, Register 05h, Bit 6

The default setting for the SM5306 has Bit 6 of register 05h is 0b. This turns on the lower bound where the minimum output value of the PWM sampler is an equivalent code of 6. If the PWM sampler detects an equivalent code of 0 or 1, the output will be 0 and the LEDs will be off. If the PWM sampler detects an equivalent code of 2 through 6, a current equal to code 6 will be output. Detection of any higher code will output that code conforming to the rules of Hysteresis above.

Setting Bit 6 of register 05h to 1b can be used to allow the output to be below an equivalent code 6. The output of the PWM sampler will match the input pulse width conforming to the rules of Hysteresis and equivalent codes 1, 2, 3, 4, and 5 are also allowed. The benefit is the output is allowed to go dimmer than in the default mode. The negative is at the low codes of 1 and 2, the LEDs may not turn on or the LEDs may appear to flicker.

Disabling the Lower Bound (05h Bit 6 = 1b) allows the minimum duty cycle to be detected at 0.35% PWM input duty cycle. At 30kHz PWM input frequency, the minimum pulse width required to turn on the LEDs is 0.39% x 33µs = 129ns. There is no specified tolerance to this value.

Minimum T_{ON} Pulse Width

The minimum T_{ON} pulse width required to produce a non-zero output is dependent upon the SM5306 settings. The default setting of the SM5306 requires a minimum of 0.78% duty cycle for the output to be turned on. Because the lower bound feature is enabled, a value of 0.78% (equivalent brightness code 2) up to 2.35% (equivalent brightness code 6) will all produce an output equivalent to brightness code 6. At 30 kHz PWM input frequency, the minimum pulse width required to turn on the LEDs is 0.78% x 33µs = 260ns. Because of the hysteresis on the PWM input, this pulse width may not be sufficient to turn on the LEDs. It is recommended that a minimum pulse width of 2% be used. 2% x 33 µs = 660 ns at 30 kHz input frequency. Disabling the Lower Bound as described will allow a smaller minimum pulse width.

Boost Regulator

Inductor Selection

The inductor is a key part of a boost regulator. Its value must be designed by considering the output voltage ripple, transient response, and efficiency. Physical size and cost are also key factors. The maximum output current, input voltage, output voltage and switching frequency determine the inductor value. In general, an inductor with a lower inductance value has higher saturation current and lower series resistance for a given physical size, but higher peak current. This higher peak current can reduce efficiency and increase input and/or output ripple and noise. However an inductor with a higher inductance value reduces the inductor current ripple and the peak current. As a result, conduction losses in the power path decrease. But, at some point the inductor resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. The inductor size increases to get larger inductance in the same DC resistance of the inductor. Therefore the inductor value should be designed by considering circuit efficiency, physical size and cost.

The following equations are related with continuous conduction mode (CCM).

The duty cycle (D) is determined by the input (V_{IN}) and output (V_{OUT}) voltages relationship.

$$D = 1 - \frac{V_{IN}}{V_{OUT}}\eta$$

where, η is the efficiency of boost regulator.

During on-time, the energy is charged in inductor. This on-time (t_{ON}) is calculated by the duty cycle and switching frequency, f_{SW}.

$$t_{ON} = D \cdot T_S$$

The inductor current ripple is

$$\Delta i_L = \frac{V_{IN} \cdot D}{L \cdot f_{SW}}$$

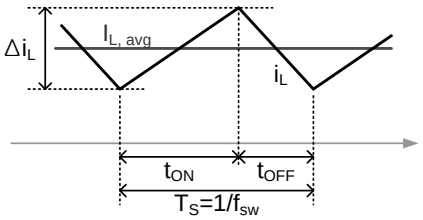


Figure 12. Inductor Current

If the inductor current ripple ratio A is defined by

$$A = \frac{\Delta i_L}{I_{L,avg}}$$

the inductor value can be calculated as

$$L = \frac{V_{IN} \cdot D}{\Delta i_L \cdot f_{SW}} = \frac{V_{IN} \cdot D}{A \cdot I_{L,avg} \cdot f_{SW}}$$

$$I_{L,avg} = \frac{I_{load} \cdot V_{OUT}}{\eta \cdot V_{IN}}$$

$$\therefore L = \left(\frac{\eta}{A}\right) \cdot \left(\frac{V_{OUT} - V_{IN} \cdot \eta}{I_{load} \cdot f_{SW}}\right) \cdot \left(\frac{V_{IN}}{V_{OUT}}\right)^2$$

First, determine inductor current ripple to average ratio (0.3~0.5 by rule of thumb). Then with estimated efficiency η, adequate inductor value L can be calculated.

The saturation current ($I_{L,sat}$) of the inductor should be satisfied with the following equation.

$$I_{L,sat} > I_{L,avg,\max} + \Delta i_L / 2$$
$$= \frac{I_{load,\max} \cdot V_{OUT}}{\eta \cdot V_{IN}} + \frac{V_{IN} \cdot D}{2L \cdot f_{SW}}$$

Input Capacitor Selection

The input capacitor is required to maintain a stable input voltage. For the uniform and low output load, a minimum value of 10uF can be used; larger capacitor(s) may need for dynamic or high output load. To reduce noise and ripple at VIN supply, a low ESR(0.1uF or more) bypass capacitor should be placed as close to VIN pin as possible.

Output Capacitor Selection

The output capacitor maintains the output voltage and supplies current to the load. There are two factors that cause ripples in the output voltage. One is by the ESR of output capacitor; the other is by the capacitance.

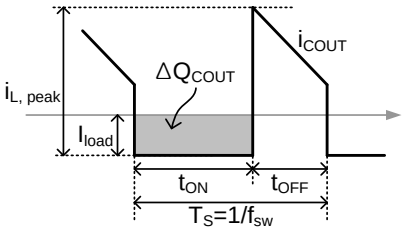


Figure 13. Output Capacitor Current

The output voltage ripple can be described as following equations.

$$\Delta v_{OUT} = \Delta v_{OUT(\mathrm{ESR})} + \Delta v_{OUT(\mathrm{Capacitance})}$$

$$\Delta v_{OUT(\mathrm{ESR})} = I_{L,peak} \cdot R_{ESR}$$

$$\Delta v_{OUT(\mathrm{Capacitance})} = \frac{\Delta Q_{COUT}}{C_{OUT}} = \frac{I_{load} \cdot (V_{OUT} - V_{IN})}{C_{OUT} \cdot V_{OUT} \cdot f_{SW}}$$

Where, ΔQ_{COUT} is the charge extracted from the output capacitor (C_{OUT}) during on-time.

To minimize the output voltage ripple, low ESR capacitors such as multilayer ceramic capacitors with large capacity should be used. If the output voltage ripple by capacitance is dominant at total output voltage ripple, the output capacitor value can be selected as following equation.

$$\Delta v_{OUT} \approx \Delta v_{OUT(\text{Capacitance})}$$

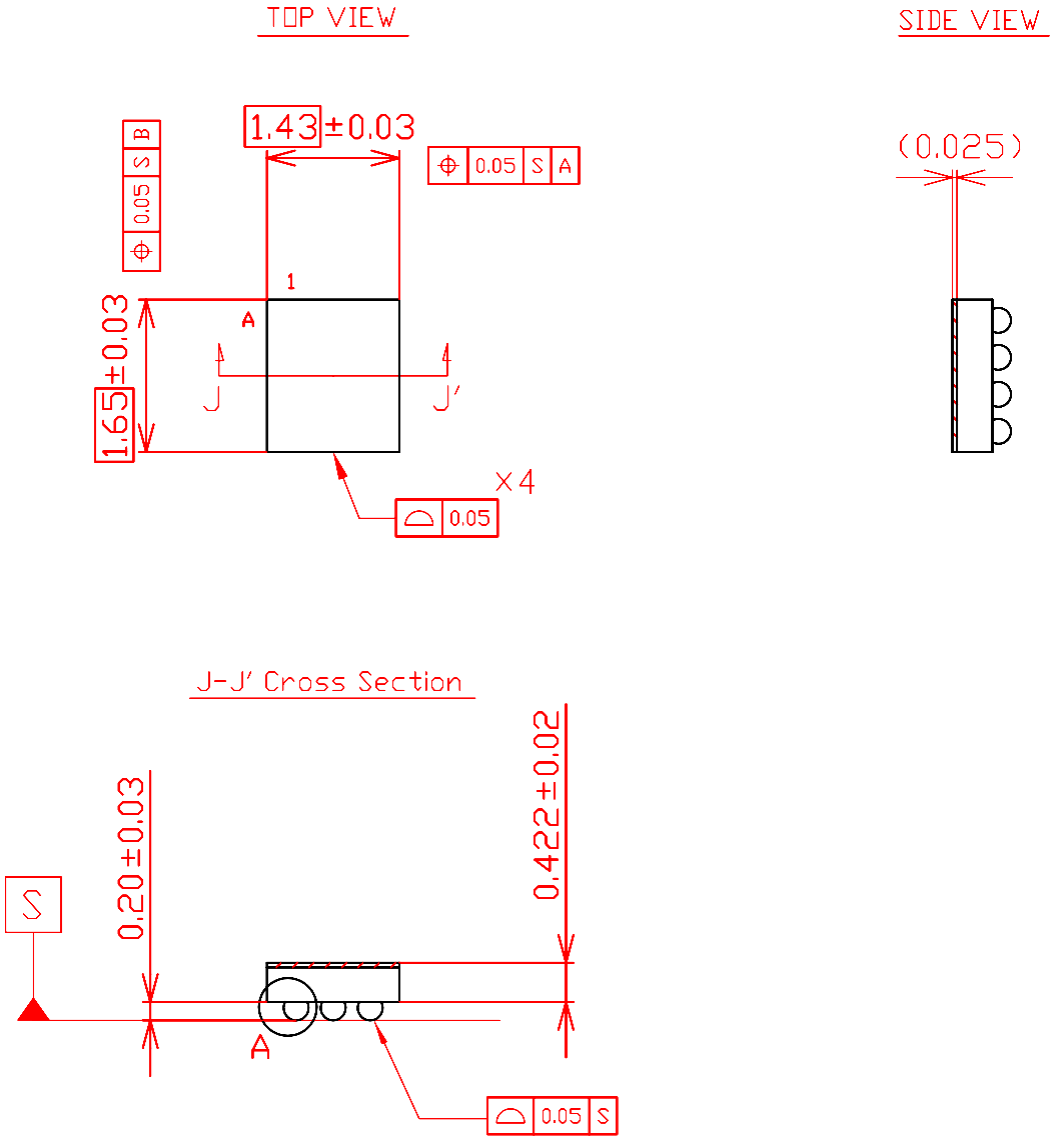
$$C_{OUT} \geq \frac{I_{load} \cdot (V_{OUT} - V_{IN})}{\Delta v_{OUT} \cdot V_{OUT} \cdot f_{SW}}$$

Diode Selection

A high-speed diode is necessary due to the high switching frequency operation of the boost converter. For high efficiency, it is important to minimize the forward voltage drop and recovery time of the diode. Schottky diodes are recommended because of their characteristics of fast recovery and low forward voltage drop.

Package Information

Dimensions are in millimeters unless otherwise noted.



Note :
1.Terminal pitch is defined by terminal center to center value.
2.Dimensions do not include resin burrs.
3.Outer dimension is defined by diced dimension.
4.UBM height is before terminal mount.

Package Information (Continued)

Dimensions are in millimeters unless otherwise noted.